FPGA Mini Project

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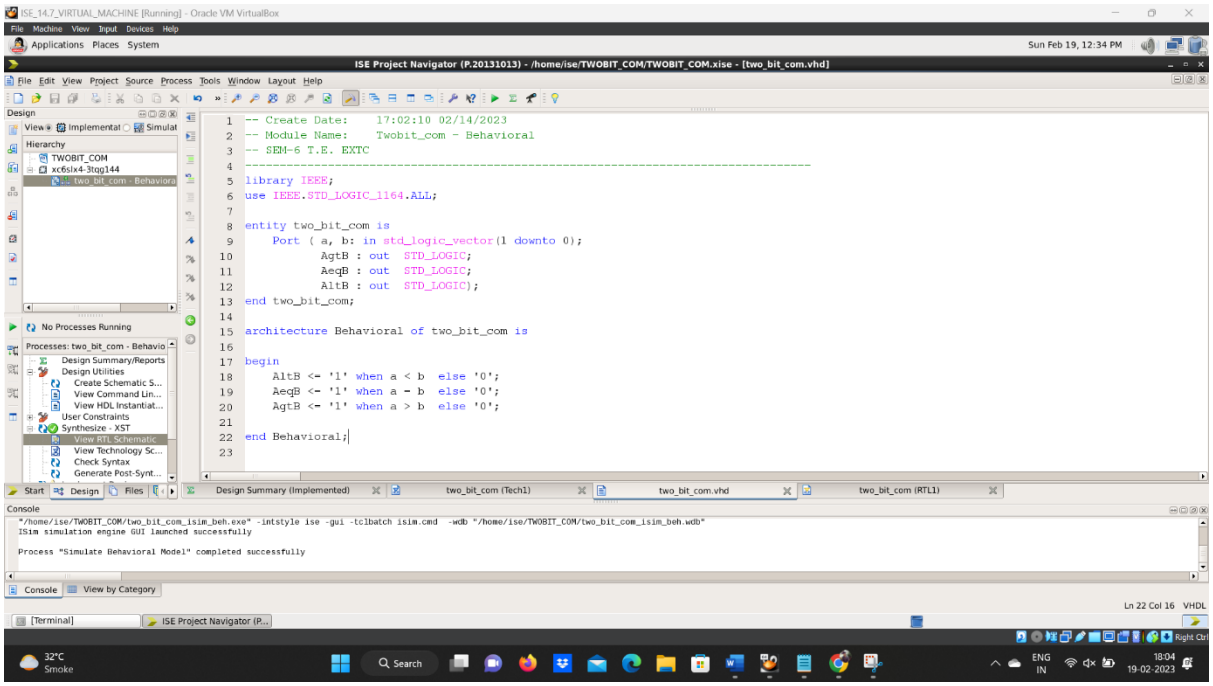
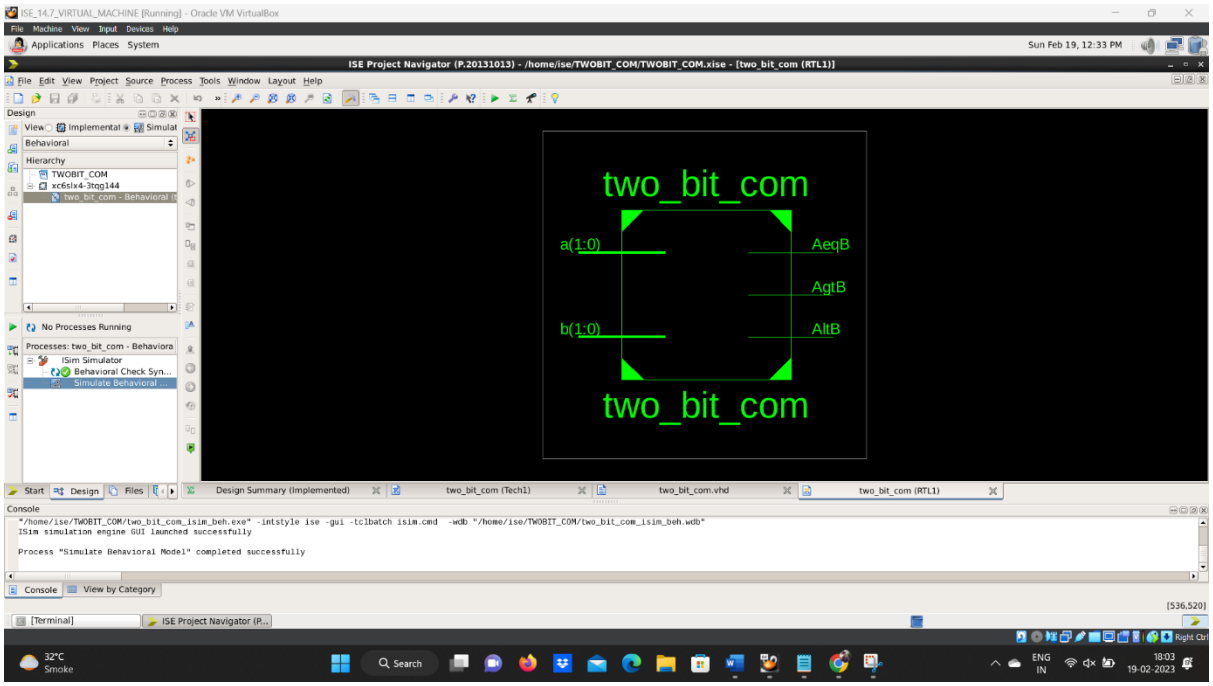
Branch : EXTC SEM-6

Topic : **2 Bit Comparator**

VHDL Code on Xiling ISE software :

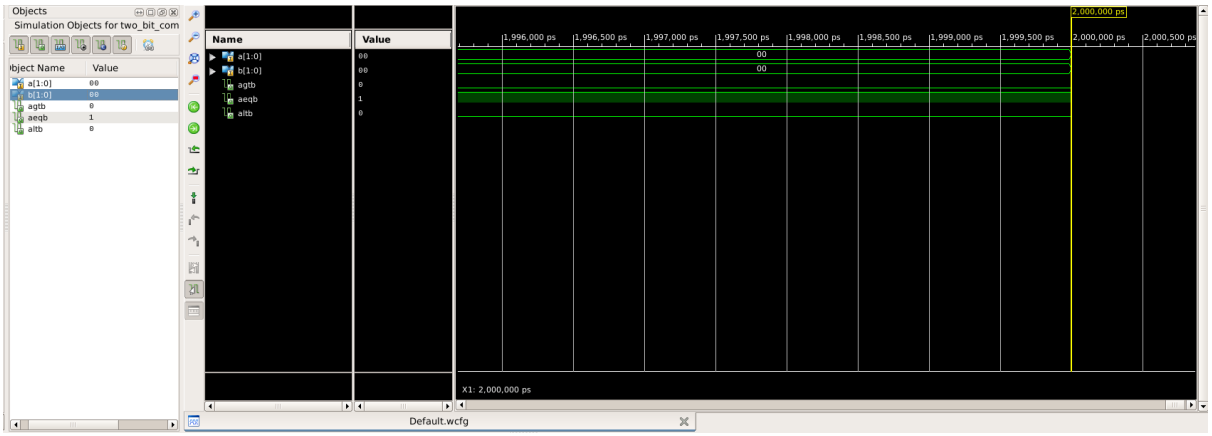


RTL schematic of 2 Bit Comparator :

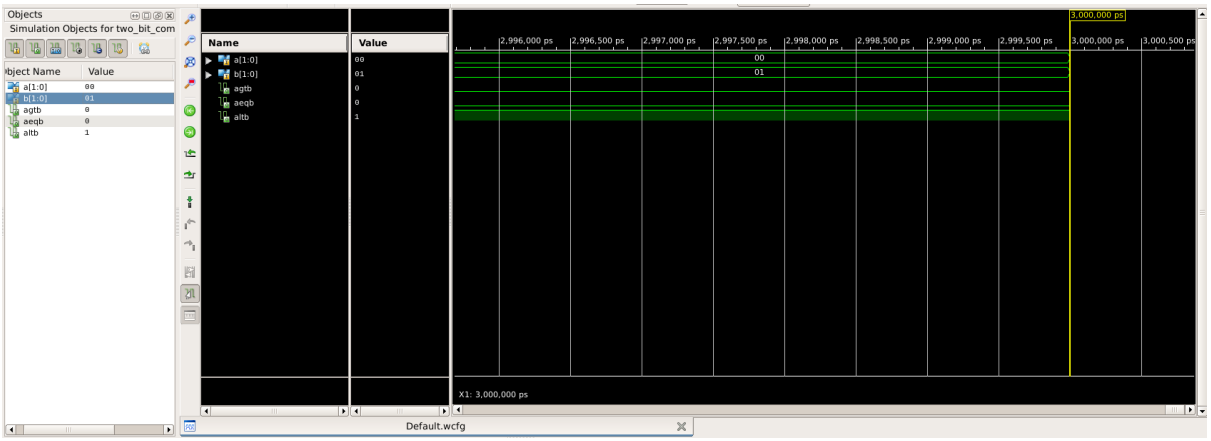


Stimulation output :

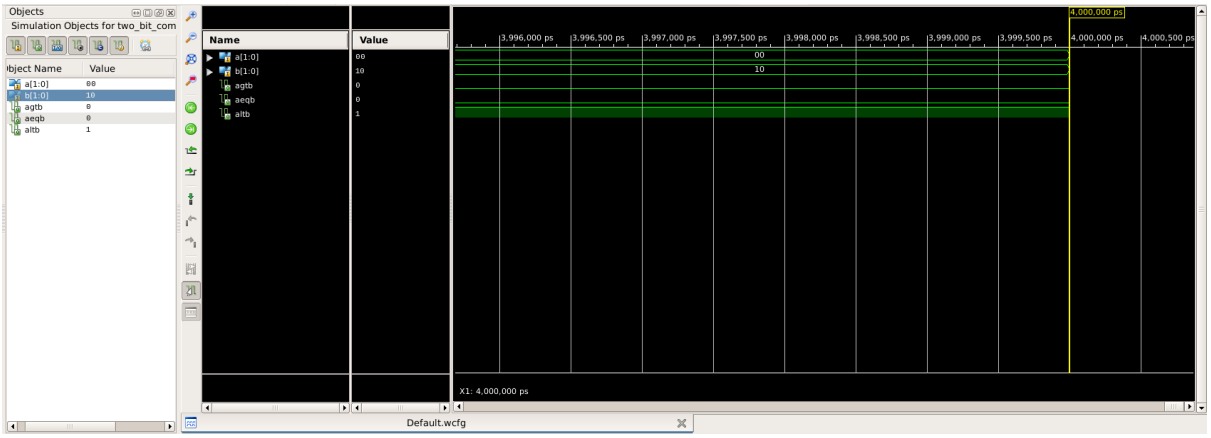
A [0 , 0] and B [0 , 0]:



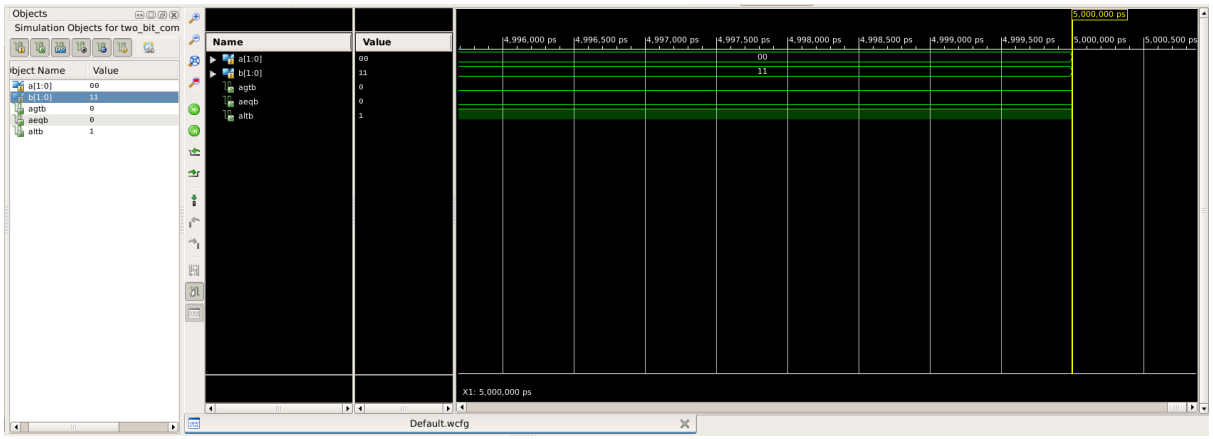
A [0 , 0] and B [0 , 1]:



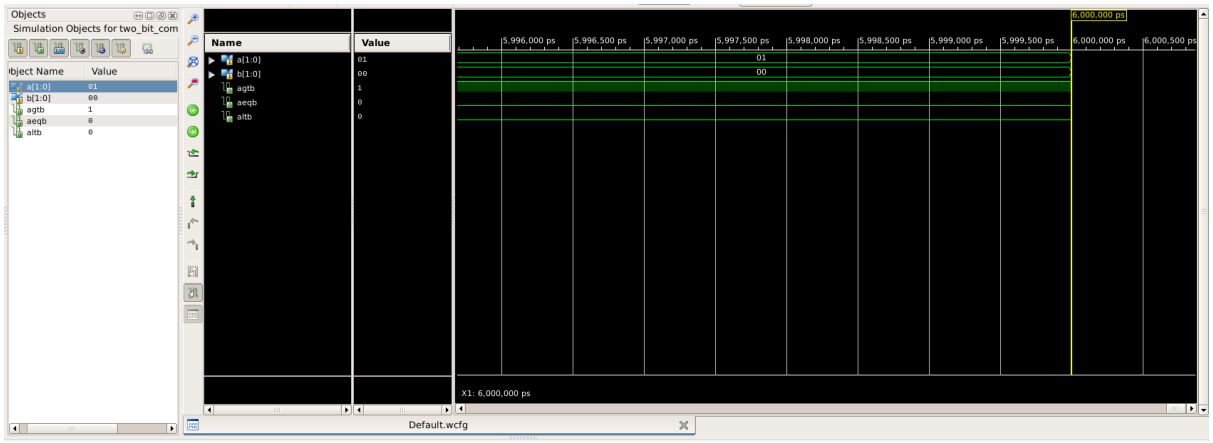
A [0 , 0] and B [1 , 0]:



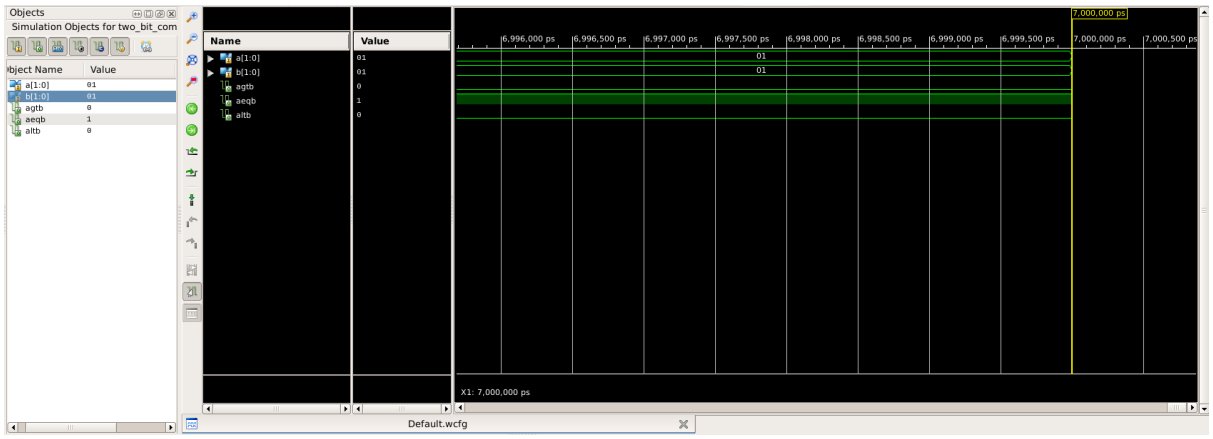
A [0 , 0] and B [1 , 1]:



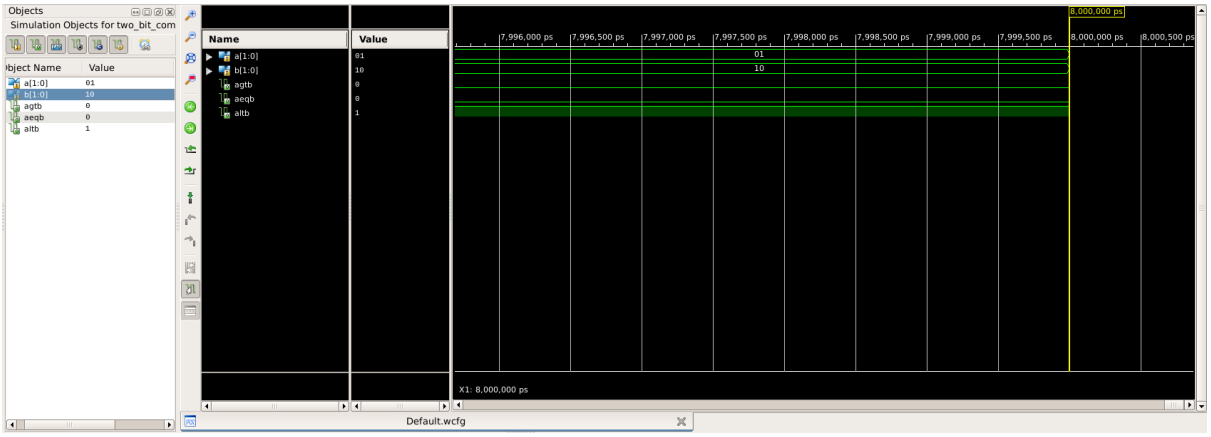
A [0 , 1] and B [0 , 0]:



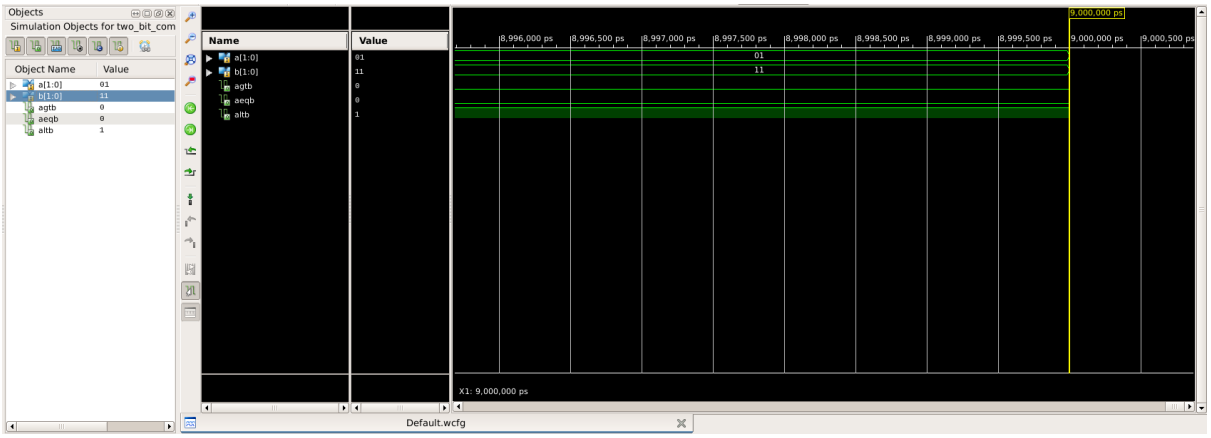
A [0 , 1] and B [0 , 1]:



A [0 , 1] and B [1 , 0]:



A [0 , 1] and B [1 , 1]:



A [1 , 0] and B [0 , 0]: