A Report on

Device Switch using Power Line Communication

for

Mini Project 2-a(REV-2019'C'Scheme) of Third Year, (TE Sem-V)

in

Electronics & Telecommunication Engineering

by

1. Chinmay Jadhav
2. Taraka Phadke
3. Parth Katkar
4. Harshal Kolhe

Under the guidance of

Prof. Yogesh Karunakar.

UNIVERSITYOFMUMBAI

AY2022-2023

Excelssior Education Society's
K.C. College of Engineering and Management Studies and Research
Mith Bunder Road, Near Hume Pipe, Kopri, Thane (E)-400603

CERTIFICATE

This is to certify that the project entitled **Device Switch Using Power Line Communication** is a Bonafede work of

1. Chinmay Jadhav
2. Taraka Phadke
3. Parth Katkar
4. Harshal Kolhe

submitted to the University of Mumbai in partial fulfillment of the requirement for the award of **Mini Project 2-a (REV- 2019 'C' Scheme) of Third Year, (TE Sem-V)** in **Electronics & Telecommunication Engineering** as laid down by **University of Mumbai** during academic year **2022-23**

(______________________) (______________________)

Examiner/Reviewer-1 **Examiner/Reviewer-2**

Prof. Yogesh Karunakar. Dr. Rajiv Iyer Dr. Vilas Nitnawre

Name Of Guide **Head of Department** **Principal**

INDEX

ABBREVIATION

1. V:Volt
2. DC: Direct Current
3. GND:Ground

4.VCC: Voltage At the Common Collector

5.VDD:VoltageSupplyforTransistorCollectors

LIST OF FIGURES

LIST OF TABLES

References **For Books:-**

Name of Author, "Title of Book", Name of Publisher, Vol. No., Year of Publication, Page no.

Example:

SingiresuRao, "The FEM in Engineering", BH Publication, 3rd Edition,1998, PP-22-30.

General Instructions

1 Text should be printed on front and correct side of the watermark on quality bond paper

Papersize-A4,70 to 85gsmpaper
Margins:Top-1”, Bottom-1”,Left-1.5”,Right-1”

2 **Font:** Times New Roman

- Font Size for Chapter heading -14(Bold uppercase)
- Font Size For main titles -12(Bold uppercase)
- Font Size for Subtitles -12(Bold Title case)
- Font Size for Text Matter -12
- Line Spacing -1.5Lines
- **Figure/Photo/Graph Caption:** Figure/Photo/Graph should be Central align to page. Figure/Photo/Graph caption should be below the Figure/Photo/Graph, left align to Figure/Photo/GraphinTitlecase,10TNR,Bold.
- **Table Caption:** Table should be Central align to page. Table caption should be above the Table, center align to Table inTitlecase,10TNR,Bold.
- Figure/Table/Photo/Graph Should Be Numbered Chapter Wise As Fig 1.1,1.2,2.1
- **Text:** Main Title No’s should be 1.1, 1.2 etc for chapter no 1, 2.1 2.2 for chapter 2etc.Subtitle1.1.1,1.1.2etc.
- Reference of Figure Should Be Given In Text Matter
- Total Number of Typed Pages Shall be minimum40

3. Students are supposed to encouraged for participation in inter and intra college level, University level and National level project competitions and demonstration.

CH-1. INTRODUCTION

1.1 NEED OF THE PROJECT

Power line communication (PLC) presents an interesting and economical solution for Automatic Meter Reading (AMR). If an AMR system via PLC is set in a power delivery system, a detection system for illegal electricity usage may be easily added in the existing PLC network. In the detection system, the second digitally energy meter chip is used and the value of energy is stored.

The detector and control system is proposed. The architecture of the system and their critical components are given. The measurement results are given. The target of this study is to discover new and possible solutions for this problem.

1.2 DEFINE

The Power Line Communication is the method of transferring power and data for communication through the same existing network of wires from one end to the other end. This can be done through the home or premises wiring and may also be done through the existing electric power distribution system.

It provides broadband data communications on conductors which are already in use for the transmission of electric power using a modular signal. The wide range of power-line communication technologies are needed for different applications, ranging from home automation to Internet access which is often called broadband over power lines (BPL).

CH-2. COMPARATIVE STUDY

1. Jovita Serrao et al. (2012): - This paper serves as a general and technical reference to transmission of data using a power line carrier communication system which is a preferred choice over Wireless or other Home Networking technologies due to the ease of installation, availability of AC outlets, higher throughput, low cost, reliability, and security.

2. Nitesh Kumar Jangir (2012): - This paper gives information of power handling by means of communication system and using their net for auto and manual power management at very cheap cost. Project proposes to use Power lines as a medium to carry control data to control a load.

3. Abdul Mannan et al. (2014): - In this paper, we give an overview of the power line communication (PLC) technology. This paper presents an overview of the research, applications, standards, and importance of the power line communication. Power line communication is an emerging home network technology that allows consumers to use their already existing wiring system to connect home appliances to each other and to the Internet. Noise in power line communication and impulsive noise are presented in this paper

Paper No.	**Year**	**Author**	**Literature**
Paper 1	2012	JovitaSerrao et al.	General and technical reference to transmission of data using a power line carrier communication system
Paper 2	2012	Nitesh Kumar Jangir	Project proposes to use Power lines as a medium to carry control data to control a load
Paper 3	2014	Abdul Mannan et al	PLC is an emerging home network technology that allows consumers to use their already existing wiring system to connect home appliances to each other and to the Internet

CH-3. PROBLEM STATEMENT

When appliances are working on generator, AC consumes more electricity and generator doesn't last for longer time.

CH-4. MINI PROJECT DESIGN (PRINCIPLE AND WORKING)

4.1 a) CIRCUIT DIAGRAM

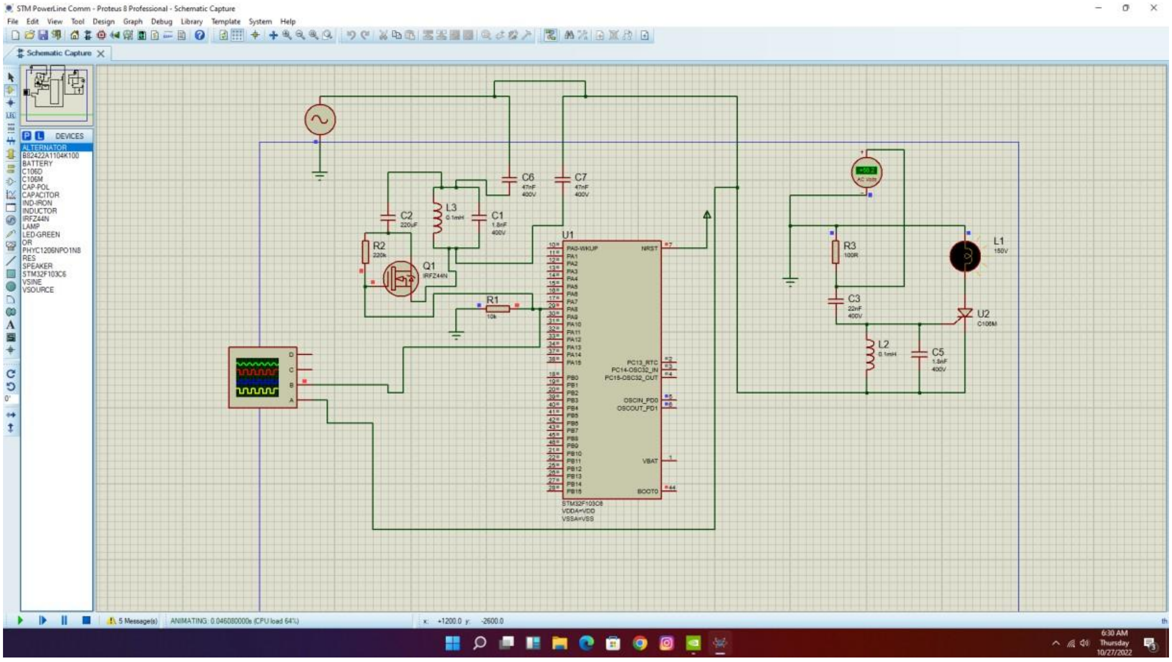

Figure 4.2.1 Circuit Diagram of Power Line Communication

4.2 b) WORKING

TRANSMITTER

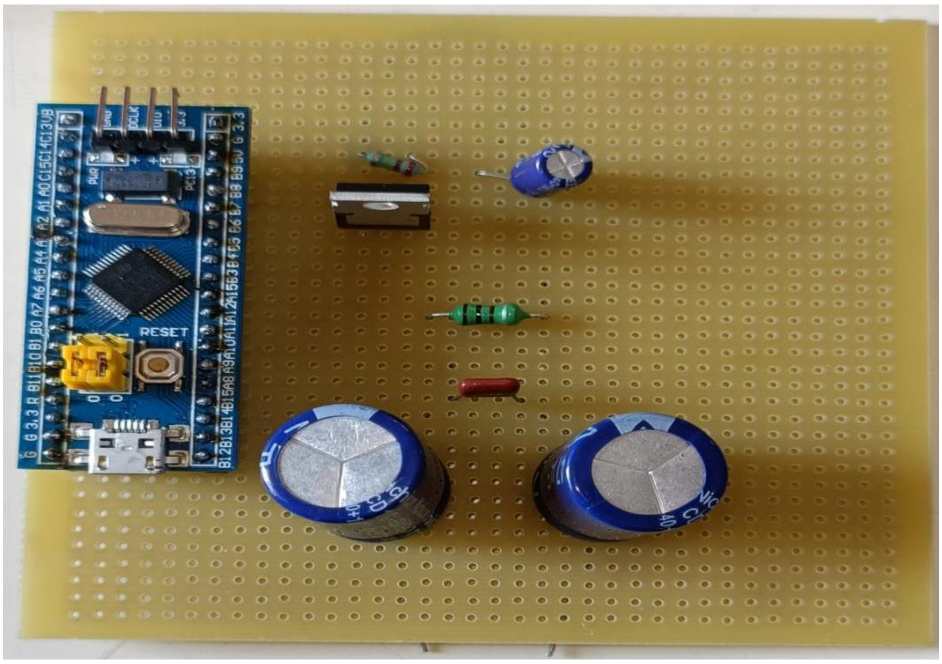

Fig 4.3.1: Circuit Diagram Of Transmitter

1. We are using STM32 board for generation of PWM signal. The PWM signal is then applied to the Line tuner. Line tuner is suitable matching unit.

2. The signal is then transmitted through the coupling capacitor. It protects the PLC equipment from low frequency, high voltage signal by acting as a High Pass filter. But it allows high frequency power signals to pass through it.

3. Signal is transmitted through the power line to the receiver end. In this process wave trap protects the electrical substances from high frequency communication signals by acting as a low pass filter. It opposes the signal to enter into the switch yard.

4. At the receiver, the coupling capacitor acts as High pass filter, it allows high frequency power signals to pass through it.

RECEIVER

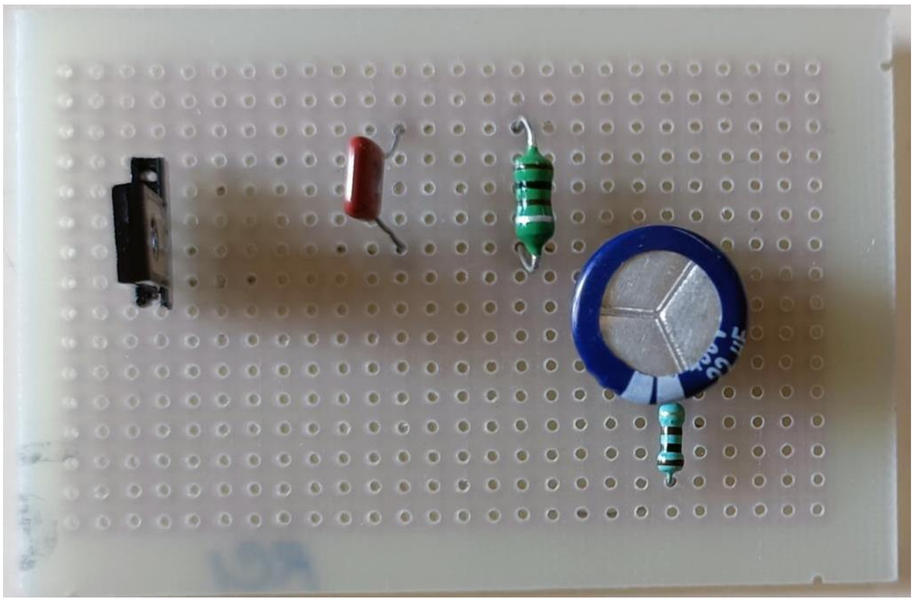

Fig 4.3.2 : Circuit Diagram Of Receiver

1. The high frequency signal transmitted by the transmitter is received to the receiver.

2. Receiver has LC circuit, which starts resonating when high frequency signal is received.

3. When the Gate of the C106M gets some triggered voltage, it start working as a short circuit.

4. Because of high frequency signal, LC circuit triggers the gate of the C106M, and the load is turned on.

5. When signal is not received the gate of C106M is not triggered and the load remains in off condition.

CH-5. COMPONENTS/TOOLS TO BE USED

5.1 COMPONENTS

1. STM 32 F103C6

STM32F103C6 is an ARM 32-bit Cortex-M3 Microcontroller, 72MHz, 32kB Flash, 10kB SRAM, PLL, Embedded Internal RC 8MHz and 32kHz, Real-Time Clock, Nested Interrupt Controller, Power Saving Modes, JTAG and SWD, 2 Synch. 16-bit Timers with Input Capture, Output Compare and PWM, 16-bit 6-ch Advanced Timer

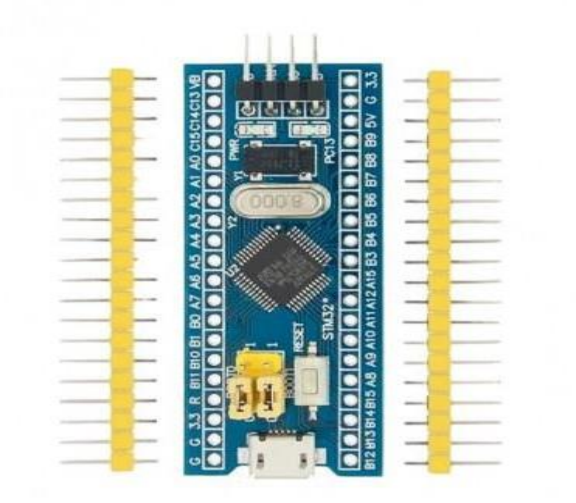

Figure 5.1.1: STM 32 F103C6

2. Capacitor

A capacitor is a device that stores electrical energy in an electric field. It is a passive electronic component with two terminals. The effect of a capacitor is known as capacitance. While some capacitance exists between any two electrical conductors in proximity in a circuit, a capacitor is a component designed to add capacitance to a circuit. The physical form and construction of practical capacitors vary widely and many types of capacitor are in common use. Most capacitors contain at least two electrical conductors often in the form of metallic plates or surfaces separated by a dielectric medium.

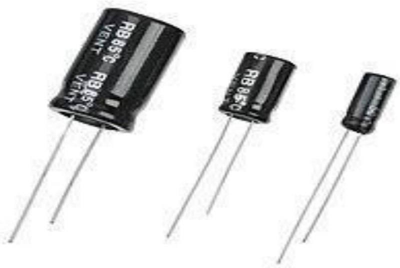

Figure 5.1.2: Capacitor

3. Resistor

A resistor is a passive two-terminal electrical component that implements electrical resistance as a circuit element. In electronic circuits, resistors are used to reduce current flow, adjust signal levels, to divide voltages, bias active elements, and terminate transmission lines, among other uses. High-power resistors that can dissipate many watts of electrical power as heat may be used as part of motor controls, in power distribution systems, or as test loads for generators. Fixed resistors have resistances that only change slightly with temperature, time or operating voltage. Variable resistors can be used to adjust circuit elements or as sensing devices for heat, light, humidity, force, or chemical activity.

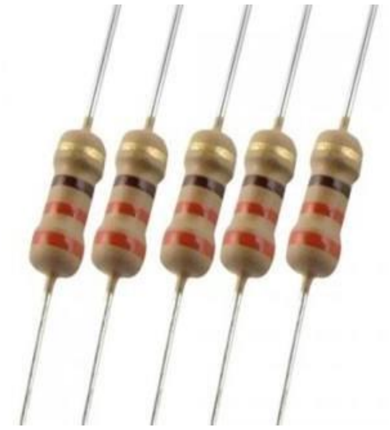

Figure 5.1.3: Resistor

4. IRFZ44N

The IRFZ44N is a N-channel MOSFET with a high drain current of 49A and low Rds value of 17.5 mΩ. It also has a low threshold voltage of 4V at which the MOSFET will start conducting. Hence it is commonly used with microcontrollers to drive with 5V. However a driver circuit is needed if the MOSFET has to be switched in completely. Gate Controls the biasing of the MOSFET. Current flows in through Drain. Source Current flows out through Source.

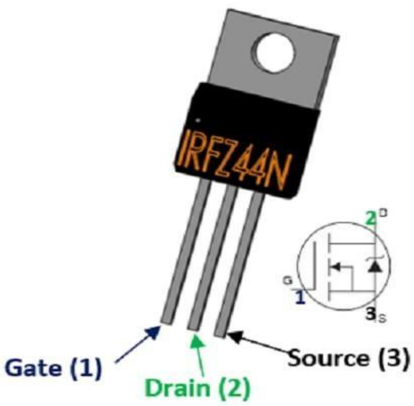

Figure 5.1.4:IRFZ44N

5. C106M Thyristor

Max off stage voltage is 600V. Max load current is 4A. Load current is 2.5A. Gate current is 50µA.

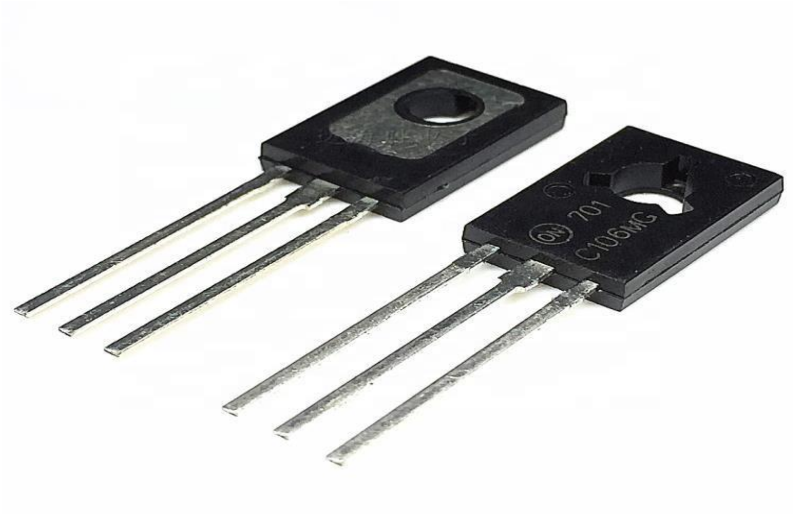

Figure5.1.5:C106M Thyristor

6. Inductor

Inductance is 33µH. Inductance Tolerance is ± 10%. DC Current Rating is 1A, Self-Resonant Frequency is 12MHz

Figure 5.1.6 : Inductor

5.2. SOFTWARE USED

Proteus 8 Professional is a software which can be used to draw schematics, PCB layout, code and even simulate the schematic. It is developed by Lab center Electronic. Drawing the schematic is very easy using Proteus.

STM32CubeIDE is an advanced C/C++ development platform with peripheral configuration, code generation, code compilation, and debug features for STM32 microcontrollers and microprocessors. It is based on the Eclipse®/CDT™ framework and GCC tool chain for the development, and GDB for the debugging.

STM32CubeIDE integrates STM32 configuration and project creation functionalities from STM32CubeMX to offer all-in-one tool experience and save installation and development time.

STM32CubeIDE includes build and stack analyzers that provide the user with useful information about project status and memory requirements.

STM32CubeIDE also includes standard and advanced debugging features including views of CPU core registers, memories, and peripheral registers, as well as live variable watch, Serial Wire Viewer interface, or fault analyzer.

CH-7. TROUBLESHOOTING

7.1 PROBLEMS/FAULTS IN PROJECT

1. Problem in PWM generation.

2. Not able to get required frequency which was 376 KHz.

Proteus crashed while checking the frequency.

Calculation error when generating the code in STM32 cube IDE.

Code uploading problem in STM32F103C6.

Calculation error in calculating the LC circuit for creating resonance for triggering the gate.

7.2 SOLUTION FOR PROBLEMS/FAULTS IN PROJECT

1. We got YouTube video for generation of PWM through STM32 on STM32 cube IDE.

2. For frequency generation we first got code for 50Hz frequency on STM32. And we applied same logic for generating our required frequency.

3. Uninstall proteus software and then again installed the software and we were able to calculate the frequency.

4. We got the formula for calculating the Prescalar , ARR and Pulse value and code generation was successful.

REFERENCES

1. https://www.researchgate.net/publication/239762728_Low_Complexity_Turbo_Code_Specification_for_Power-Line_Communication_PLC

2. https://circuitdigest.com/article/what-is-power-line-communication-plc-and-how-does-it-work

3. https://repository.najah.edu/bitstream/handle/20.500.11888/11737/power_line_communication.doc?sequence=1&isAllowed=y

23

APPENDIX

Data sheet of Components

IRFZ44N

ELECTRICAL CHARACTERISICS at Tj = 25°C Maximum. Unless stated Otherwise						
Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V_{DC}, I_D = 250μA	55	-	-	Volt
Drain to Source Leakage Current	I_{DSS}	V_{DS} = 55V_{DC}, V_{GS} = 0V_{DC}	-	-	25	
		V_{DS} = 44V_{DC}, V_{GS} = 0V_{DC} Tj=150 °C	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = +20V_{DC}	-	-	100	nA
		V_{GS} = -20V_{DC}	-	-	-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	Volt
Static Drain to Source On - Resistance	$R_{DS(on)}$	V_{GS}= 10V_{DC}, I_D = 10A	-	-	0.07	Ω
Gate Charge	Q_G	I_D = 25A V_{DS} = 44V_{DC}, V_{GS} = 10V_{DC}	-	-	63	nC
Gate to Source Charge	Q_{GS}		-	-	14	nC
Gate to Drain Charge	Q_{GD}		-	-	23	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V_{DC}, V_{GS}= 0V_{DC}, f = 1.0MHZ	-	1470	-	pF
Output Capacitance	C_{OSS}		-	360	-	pF
Transfer Capacitance	C_{RSS}		-	88	-	pF
Turn On Delay Time	$td_{(on)}$	V_{DD} = 28V_{DC}, I_D = 25A, R_G = 12Ω	-	12	-	nS
Turn Off Delay Time	$td_{(off)}$		-	44	-	nS
Rise Time	tr		-	60	-	nS
Fall Time	tf		-	45	-	nS
Continuous Source Current	I_S		-	-	49	A
Pulsed Source Current	I_{SM}		-	-	160	A
Forward Voltage (Diode)	V_{SD}	V_{GS} = 0V_{DC}, I_S =25A, Tp = 300μS	-	-	1.3	V
Single Pulse Avalanche Energy	E_{AS}				148	mj
Repetive Avalanche Energy	E_{AR}				9.4	mj
Avalanche Current	I_{AR}				25	A

STM 32

Part number		Program memory type	Prog. (Bytes)	RAM (Bytes)	Timer functions		Serial interface	I/Os (High current)	Packages	Supply voltage
		Flash			12 or 16-bit (IC/OC/PWM)	Others				
STM32 (ARM Cortex-M3) - 32-bit microcontrollers										
36 pins	STM32F101T6	•	32 K	6 K	2x16-bit (8/8/8)	2xWDG, RTC, 24-bit down counter	1xSPI/1xI^{2}C/2xUSART*	26(26)	QFN36	2 to 3.6 V
	STM32F101T8	•	64 K	10 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	26(26)	QFN36	2 to 3.6 V
48 pins	STM32F101C6	•	32 K	6 K	2x16-bit (8/8/8)		1xSPI/1xI^{2}C/2xUSART*	36(36)	LQFP48	2 to 3.6 V
	STM32F101C8	•	64 K	10 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	36(36)	LQFP48	2 to 3.6 V
	STM32F101CB	•	128 K	16 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	36(36)	LQFP48	2 to 3.6 V
64 pins	STM32F101R6	•	32 K	6 K	2x16-bit (8/8/8)		1xSPI/1xI^{2}C/2xUSART*	51(51)	LQFP64	2 to 3.6 V
	STM32F101R8	•	64 K	10 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	51(51)	LQFP64	2 to 3.6 V
	STM32F101RB	•	128 K	16 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	51(51)	LQFP64	2 to 3.6 V
100 pins	STM32F101V8	•	64 K	10 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	80(80)	LQFP100	2 to 3.6 V
	STM32F101VB	•	128 K	16 K	3x16-bit (12/12/12)		2xSPI/2xI^{2}C/3xUSART*	80(80)	LQFP100	2 to 3.6 V
36 pins	STM32F103T6	•	32 K	10 K	3x16-bit (12/12/14)		1xSPI/1xI^{2}C/2xUSART*/USB/CAN	26(26)	QFN36	2 to 3.6 V
	STM32F103T8	•	64 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	26(26)	QFN36	2 to 3.6 V
48 pins	STM32F103C6	•	32 K	10 K	3x16-bit (12/12/14)		1xSPI/1xI^{2}C/2xUSART*/USB/CAN	36(36)	LQFP48	2 to 3.6 V
	STM32F103C8	•	64 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	36(36)	LQFP48	2 to 3.6 V
	STM32F103CB	•	128 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	36(36)	LQFP48	2 to 3.6 V
64 pins	STM32F103R6	•	32 K	10 K	3x16-bit (12/12/14)		1xSPI/1xI^{2}C/2xUSART*/USB/CAN	51(51)	LQFP64	2 to 3.6 V
	STM32F103R8	•	64 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	51(51)	LQFP64	2 to 3.6 V
	STM32F103RB	•	128 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	51(51)	LQFP64	2 to 3.6 V
100 pins	STM32F103V8	•	64 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	80(80)	LQFP100/BGA100	2 to 3.6 V
	STM32F103VB	•	128 K	20 K	4x16-bit (16/16/18)		2xSPI/2xI^{2}C/3xUSART*/USB/CAN	80(80)	LQFP100/BGA100	2 to 3.6 V