

实验报告

课程名称:		DSP 的原理与	<u>i应用</u>				
实验名称:	实验 4 PWM 输出实验						
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实验日期:	2024 年 5 月	日					
			试验台	·号:			
			报告总	分数:			
教师评语:							
			助教签	字:_			
			教师签	字: _			
			日	期:			

一、实验目的

- 1. 了解 TMS320F28335 DSP 片内事件管理器模块的脉宽调制电路 PWM 的特性参数;
- 2. 掌握 PWM 电路的控制方法;
- 3. 学会用程序控制产生不同占空比的 PWM 波形。

二、实验过程

- 1. 导入工程并导入硬件仿真文件。
- 2. 打开程序并推测实验现象;
- 3. 下载并运行程序,观察实验现象。

三、实验结果

- 1. 导入工程并导入硬件仿真文件。
- 2. 阅读代码,编译并下载程序。

```
1. // For this example, only initialize the ePWM
2. void InitEPwm1Example()
3.
   {
      // 初始化TB 模块
4.
       EPwm1Regs.TBCTL.bit.CTRMODE = TB COUNT UP; // 设置计数模式为增计数
5.
6.
       EPwm1Regs.TBPRD = EPWM1 TIMER TBPRD;
                                              // 设置周期寄存器
7.
       EPwm1Regs.TBCTL.bit.PHSEN = TB DISABLE; // 失能相位控制
8.
       EPwm1Regs.TBPHS.half.TBPHS = 0 \times 00000;
                                               // 相位寄存器值清零
9.
                                              // 计数器清零
       EPwm1Regs.TBCTR = 0 \times 0000;
10.
       EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB DIV2;
                                               // 设置 TBCLK 频率
      EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV2; // 设置分频
11.
       // 初始化 CC 模块
12.
      EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC SHADOW; // 使能 CMPA 影子寄存器
13.
14.
       EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW; // 使能 CMPB 影子寄存器
15.
       EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // 影子寄存器在计数到 0 时装载
16.
       EPwm1Regs.CMPCTL.bit.LOADBMODE = CC CTR ZERO; // 影子寄存器在计数到 0 时装载
       EPwm1Regs.CMPA.half.CMPA = EPWM1_MIN_CMPA; // Set compare A value
17.
18.
       EPwm1Regs.CMPB = EPWM1 MIN CMPB;
                                              // Set Compare B value
19.
      // 初始化AQ 模块
20.
       EPwm1Regs.AQCTLA.bit.ZRO = AQ SET; // TB 计数器为 0 时置为高电平
21.
       EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR; // TB 计数器到达 CMPA 值时置为低电平
22.
       EPwm1Regs.AQCTLB.bit.ZRO = AQ SET; // TB 计数器为 0 时置为高电平
23.
       EPwm1Regs.AQCTLB.bit.CBU = AQ CLEAR; // TB 计数器到达 CMPB 值时置为低电平
24.
       // 初始化 ET 模块
25.
       EPwm1Regs.ETSEL.bit.INTSEL = ET CTR ZERO; // 时基计数器等于 0 时触发中断
                                              // 中断线使能
26.
       EPwm1Regs.ETSEL.bit.INTEN = 1;
27.
       EPwm1Regs.ETPS.bit.INTPRD = ET_3RD; // 每三个事件触发中断
28.
       // 设置自定义 ePWM 寄存器
29.
      // Start by increasing CMPA & CMPB
30.
       epwm1 info.EPwm CMPA Direction = EPWM CMP UP;
31.
       epwm1_info.EPwm_CMPB_Direction = EPWM_CMP_UP;
32.
       epwm1 info.EPwmTimerIntCount = 0; // Zero the interrupt counter
```

```
33.  // Set the pointer to the ePWM module
34.  epwm1_info.EPwmRegHandle = &EPwm1Regs;
35.  // Setup min/max CMPA/CMPB values
36.  epwm1_info.EPwmMaxCMPA = EPWM1_MAX_CMPA;
37.  epwm1_info.EPwmMinCMPA = EPWM1_MIN_CMPA;
38.  epwm1_info.EPwmMaxCMPB = EPWM1_MAX_CMPB;
39.  epwm1_info.EPwmMinCMPB = EPWM1_MIN_CMPB;
40. }
```

(1) 注意到 PWM1 和 PWM2 在程序中的配置如下:

HSPCLKDIV 为 2 分频; CLKDIV 为 2 分频;

通过公式:

$$f_{TBCLK} = \frac{SYSCLKOUT}{HSPCLKDIV \times CLKDIV}$$

$$T_{pwm} = (TBPRD + 1) \times T_{TBCLK}$$

由于为增计数模式, 计算得到 PWM 频率为 18740Hz。实际测得 PWM 频率符合上述条件。



(2) 由于中断程序中循环改变了 CMPA 和 CMPB 比较值,可以观察到 PWM 的占空比是增加(到 100%)-> 减少(到 0%)-> 增加循环变化的。

(3) 对于 PWM1A 和 PWM1B, 注意到两路 PWM 配置相同, 故波形相同, 如下图:



PWM2A 和 PWM1A 是反相的,如下图:



PWM2B 和 PWM2A 占空比相加得到 100%,如下图。

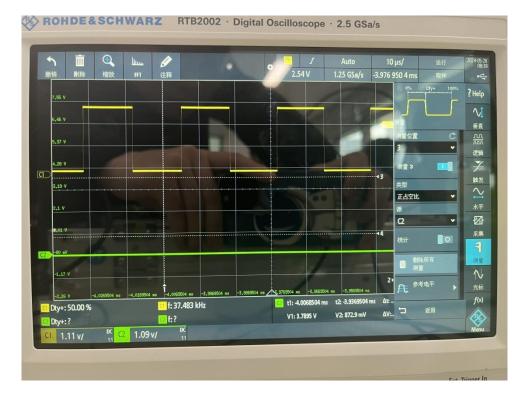


(3) PWM3 在程序中的配置如下:

HSPCLKDIV 为 1 分频; CLKDIV 为 1 分频; PWM 频率计算得到 74962Hz。

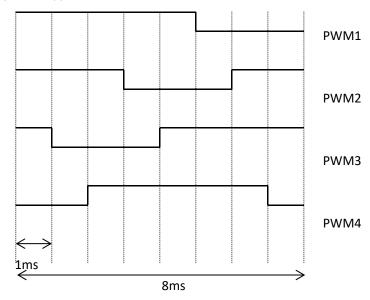


注意到 PWM3B 的动作是计数到 0 时反转,所以为 50%占空比的方波,频率为 37481Hz。



四、问题与思考

1、试设计四路(PWM1, PWM2, PWM3, PWM4)输出,载波频率为 8ms,波形关系如下(一个周期),要求写出设计思路、写出四路 PWM 的周期和占空比计算过程、画出四路 TB 计数器计数波形、画出四路 CC 模块的比较值波形、画出四路 AQ 模块的动作标识符号、提供程序代码、提供的示波器实验波形图标出要求的频率和相位关系。(4 分)



- (1) 设计思路,周期和占空比计算:
- 1. 考虑到如果使用增(减)计数模式得到的 TBPRD 值均大于 65535 (考虑 HSPCLKDIV 和 CLKDIV 均为 4 分频时)

$$f_{TBCLK} = rac{SYSCLKOUT}{HSPCLKDIV imes CLKDIV}$$

$T_{pwm} = (TBPRD + 1) \times T_{TBCLK}$

取 HSPCLKDIV 为 4 分频, CLKDIV 为 4 分频, 由 Tpwm = 8ms, 得到 TBPRD 值为 74999。大于 int 类型的限定值 65535。

使用增减计数模式:

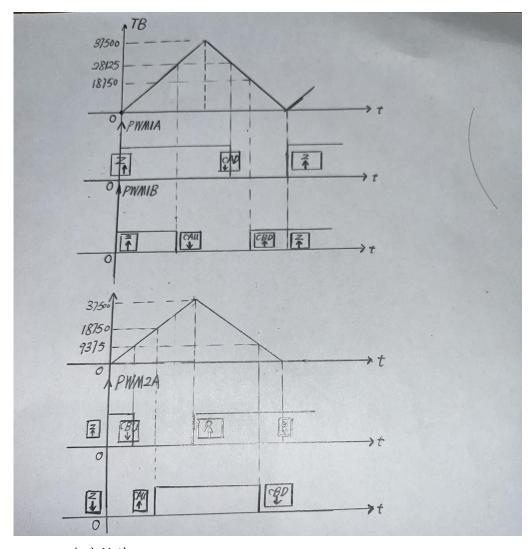
- 1. EPwm1Regs.TBCTL.bit.CTRMODE = TB COUNT UPDOWN;
- 2. EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;

由以下公式:

$$f_{TBCLK} = rac{SYSCLKOUT}{HSPCLKDIV imes CLKDIV}$$

$T_{pom} = 2 \times TBPRD \times T_{TBCLK}$

取 HSPCLKDIV 为 4 分频, CLKDIV 为 4 分频, 由 Tpwm = 8ms, 得到 TBPRD 值为 37500。 接下来设计四路波形,注意到为增减计数模式,每一个比较值有上升到达和下降到达两种形式,波 形设置如下:



PWM1: 占空比为 1-28125/75000 = 62.5%;

PWM2: 占空比为(28125+18750)/75000 = 62.5%; PWM3: 占空比为(9375+37500)/75000 = 62.5%; PWM3: 占空比为 1- (18750+9375)/75000 = 62.5%;

实验代码如下:

) <u></u> \(\frac{1}{2}\)	-1341 I :									
	1. // TI File \$Revision: /main/8 \$										
2.	// Checkin \$Date: August 10, 2007 09:04:53 \$										
3.	//#####################################										
	//										
5.	// F	FILE: Example_2833xEPwm3UpAQ.c									
6.	. //										
7.	// TITLE: Action Qualifier Module Upcount mode.										
8.	//										
9.	// A	/ ASSUMPTIONS:									
10.	//										
11.	//	This program	requires	the DSP283	33x heade	r files.					
12.	//										
13.	//	Monitor the	ePWM1 - e	PWM3 pins o	on a osci	Lloscope as					
14.	//	described below.									
15.	//										
16.	//	EPWM1A is on GPIO0									
17.	//	EPWM1B is on GPI01									
18.	//										
19.	//	EPWM2A is	on GPIO2								
20.	//	EPWM2B is	on GPIO3								
21.	//										
22.	//	EPWM3A is	on GPIO4								
23.	//	EPWM3B is	on GPI05								
24.	//										
25.	//	As supplied, this project is configured for "boot to SARAM"									
26.	//	operation. The 2833x Boot Mode table is shown below.									
27.	//	For information on configuring the boot mode of an eZdsp,									
28.	//	please refer to the documentation included with the eZdsp,									
29.	//										
30.	//	\$Boot_Tabl	e:								
31.	//										
32.	//	GPI087	GPI086	GPI085	GPI084						
33.	//	XA15	XA14	XA13	XA12						
34.	//	PU	PU	PU	PU						
35.	//	=======				====					
36.	//	1	1	1	1	Jump to Flash					
37.	//	1	1	1	0	SCI-A boot					
38.	//	1	1	0	1	SPI-A boot					
39.	//	1	1	0	0	I2C-A boot					
40.	//	1	0	1	1	eCAN-A boot					
41.	//	1	0	1	0	McBSP-A boot					
42.	//	1	0	0	1	Jump to XINTF x16					
43.	//	1	0	0	0	Jump to XINTF x32					
44.	//	0	1	1	1	Jump to OTP					

```
45. //
                                               Parallel GPIO I/O boot
46. //
                                               Parallel XINTF boot
                0
                                          1
47. //
                0
                        1
                                  0
                                               Jump to SARAM <- "boot to SARA
                                          0
 Μ"
48. //
                0
                        0
                                               Branch to check boot mode
                                  1
                                          1
49. //
                                          0 Boot to flash, bypass ADC cal
                0
                        0
50. //
                        0
                                               Boot to SARAM, bypass ADC cal
                0
                                  0
                                          1
51. //
                                              Boot to SCI-A, bypass ADC cal
52. //
                                               Boot Table End$
53. //
54. // DESCRIPTION:
55. //
56. //
        This example configures ePWM1, ePWM2, ePWM3 to produce an
57. //
        waveform with independant modulation on EPWMxA and
58. //
        EPWMxB.
59. //
60. //
        The compare values CMPA and CMPB are modified within the ePWM's ISR
61. //
62. //
        The TB counter is in upmode for this example.
63. //
64. //
        View the EPWM1A/B, EPWM2A/B and EPWM3A/B waveforms
65. //
       via an oscilloscope
66. //
67. //
69. // $TI Release: DSP2833x Header Files V1.01 $
70. // $Release Date: September 26, 2007 $
72.
73.
74. #include "DSP2833x_Device.h"
                                 // DSP2833x Headerfile Include File
75. #include "DSP2833x Examples.h" // DSP2833x Examples Include File
76.
77. // Prototype statements for functions found within this file.
78. void InitEPwm1Example(void);
79. void InitEPwm2Example(void);
80. interrupt void epwm1_isr(void);
81. interrupt void epwm2_isr(void);
82.
83. // Configure the period for each timer
84. #define EPWM1_TIMER_TBPRD 37500 // Period register
86. #define EPWM2 TIMER TBPRD 37500 // Period register
87.
88.
89. void main(void)
```

90. {

```
91. // Step 1. Initialize System Control:
92. // PLL, WatchDog, enable Peripheral Clocks
93. // This example function is found in the DSP2833x SysCtrl.c file.
      InitSysCtrl();
94.
95.
96. // Step 2. Initalize GPIO:
97. // This example function is found in the DSP2833x_Gpio.c file and
98. // illustrates how to set the GPIO to it's default state.
99. // InitGpio(); // Skipped for this example
100.
101. // For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
102. // These functions are in the DSP2833x_EPwm.c file
103. InitEPwm1Gpio();
104.
       InitEPwm2Gpio();
105.
106.
107. // Step 3. Clear all interrupts and initialize PIE vector table:
108. // Disable CPU interrupts
109. DINT;
110.
111. // Initialize the PIE control registers to their default state.
112. // The default state is all PIE interrupts disabled and flags
113. // are cleared.
114. // This function is found in the DSP2833x_PieCtrl.c file.
115. InitPieCtrl();
116.
117. // Disable CPU interrupts and clear all CPU interrupt flags:
118.
       IER = 0 \times 0000;
119. IFR = 0 \times 0000;
120.
121. // Initialize the PIE vector table with pointers to the shell Interrupt
122. // Service Routines (ISR).
123. // This will populate the entire table, even if the interrupt
124. // is not used in this example. This is useful for debug purposes.
125. // The shell ISR routines are found in DSP2833x_DefaultIsr.c.
126. // This function is found in DSP2833x PieVect.c.
127. InitPieVectTable();
128.
129. // Interrupts that are used in this example are re-mapped to
130. // ISR functions found within this file.
131. EALLOW; // This is needed to write to EALLOW protected registers
132.
       PieVectTable.EPWM1_INT = &epwm1_isr;
133. PieVectTable.EPWM2 INT = &epwm2 isr;
134.
       EDIS; // This is needed to disable write to EALLOW protected registers
135.
136. // Step 4. Initialize all the Device Peripherals:
137. // This function is found in DSP2833x_InitPeripherals.c
138. // InitPeripherals(); // Not required for this example
```

```
139.
140. // For this example, only initialize the ePWM
141.
142.
       EALLOW;
143.
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
144.
       EDIS:
145.
146.
       InitEPwm1Example();
147. InitEPwm2Example();
148.
149.
      EALLOW;
150.
       SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
151.
       EDIS;
152.
153.
154. // Step 5. User specific code, enable interrupts:
155.
156. // Enable CPU INT3 which is connected to EPWM1-3 INT:
157. IER |= M_INT3;
158.
159. // Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
160.
       PieCtrlRegs.PIEIER3.bit.INTx1 = 1;
161. PieCtrlRegs.PIEIER3.bit.INTx2 = 1;
162.
163. // Enable global Interrupts and higher priority real-time debug events:
164.
               // Enable Global interrupt INTM
       EINT;
165. ERTM; // Enable Global realtime interrupt DBGM
166.
167. // Step 6. IDLE loop. Just sit and loop forever (optional):
168.
       for(;;)
169. {
170.
           asm("
                          NOP");
171. }
172.
173. }
174.
175. interrupt void epwm1_isr(void)
176. {
177. // Clear INT flag for this timer
178.
       EPwm1Regs.ETCLR.bit.INT = 1;
179.
       // Acknowledge this interrupt to receive more interrupts from group 3
180.
       PieCtrlRegs.PIEACK.all = PIEACK GROUP3;
181.
182. }
183.
184.
185. interrupt void epwm2_isr(void)
```

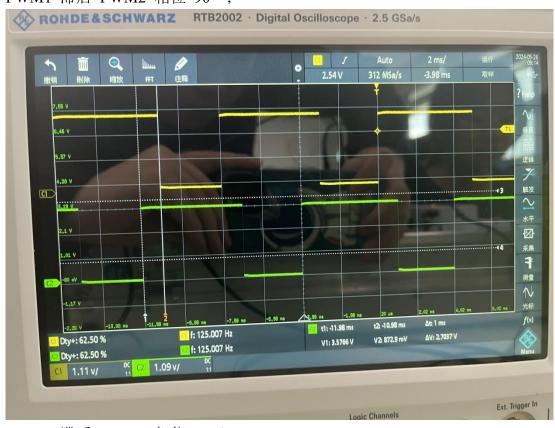
```
186. {
187.
      // Clear INT flag for this timer
188.
       EPwm2Regs.ETCLR.bit.INT = 1;
189.
       // Acknowledge this interrupt to receive more interrupts from group 3
190.
       PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
191.
192. }
193.
194. void InitEPwm1Example()
195. {
196.
197.
       // Setup TBCLK
       EPwm1Regs.TBCTL.bit.CTRMODE = TB COUNT UPDOWN; // Count up
198.
199.
       EPwm1Regs.TBPRD = EPWM1_TIMER_TBPRD;
                                                   // Set timer period
200.
       EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
                                                    // Disable phase loading
201.
       EPwm1Regs.TBPHS.half.TBPHS = 0 \times 0000;
                                                   // Phase is 0
                                                    // Clear counter
202.
       EPwm1Regs.TBCTR = 0 \times 0000;
203.
       EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB DIV4; // Clock ratio to SYSCLKOUT
204.
       EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV4;
205.
206.
       // Setup shadow register load on ZERO
207.
       EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC SHADOW;
208.
       EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC SHADOW;
209.
       EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
210.
       EPwm1Regs.CMPCTL.bit.LOADBMODE = CC CTR ZERO;
211.
212.
       // Set Compare values
       EPwm1Regs.CMPA.half.CMPA = 28125;  // Set compare A value
213.
214.
       EPwm1Regs.CMPB = 18750;
                                             // Set Compare B value
215.
216.
       // Set actions
217.
       EPwm1Regs.AQCTLA.bit.ZRO = AQ SET;
                                                       // Set PWM1A on Zero
218.
       EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
219.
220.
       EPwm1Regs.AQCTLB.bit.ZRO = AQ SET;
                                                       // Set PWM1B on Zero
221.
       EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
222.
       EPwm1Regs.AQCTLB.bit.CBD = AQ SET;
223.
224.
       EPwm1Regs.ETSEL.bit.INTSEL = ET CTR ZERO;  // Select INT on Zero event
225.
       EPwm1Regs.ETSEL.bit.INTEN = 1;
                                                       // Enable INT
226.
       EPwm1Regs.ETPS.bit.INTPRD = ET 3RD;
                                                       // Generate INT on 3rd event
227. }
228.
229.
230. void InitEPwm2Example()
```

```
231. {
232.
      // Setup TBCLK
233.
       EPwm2Regs.TBCTL.bit.CTRMODE = TB COUNT UPDOWN; // Count up
234.
       EPwm2Regs.TBPRD = EPWM2_TIMER_TBPRD;
                                                // Set timer period
235.
       EPwm2Regs.TBCTL.bit.PHSEN = TB DISABLE;
                                                // Disable phase Loading
236.
       EPwm2Regs.TBPHS.half.TBPHS = 0x0000;
                                                // Phase is 0
237.
       EPwm2Regs.TBCTR = 0 \times 0000;
                                                // Clear counter
238.
       EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB DIV4; // Clock ratio to SYSCLKOUT
239.
       EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV4;
240.
241.
       // Setup shadow register load on ZERO
242.
       EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC SHADOW;
243.
       EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC SHADOW;
       EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
244.
245.
       EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
246.
247.
       // Set Compare values
248.
       EPwm2Regs.CMPA.half.CMPA = 18750;
                                             // Set compare A value
249.
       EPwm2Regs.CMPB = 9375;
                                             // Set Compare B value
250.
251.
       // Set actions
252.
       EPwm2Regs.AQCTLA.bit.ZRO = AQ SET;
253.
       EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
254.
       EPwm2Regs.AQCTLA.bit.PRD = AQ SET;
255.
256.
257.
       EPwm2Regs.AQCTLB.bit.ZRO = AQ CLEAR;
258.
       EPwm2Regs.AQCTLB.bit.CAU = AQ SET;
259.
       EPwm2Regs.AQCTLB.bit.CBD = AQ CLEAR;
260.
261.
262.
     // Interrupt where we will change the Compare Values
263.
       EPwm2Regs.ETSEL.bit.INTSEL = ET CTR ZERO;
                                                      // Select INT on Zero event
264.
       EPwm2Regs.ETSEL.bit.INTEN = 1;
                                                      // Enable INT
       EPwm2Regs.ETPS.bit.INTPRD = ET 3RD;
265.
                                                      // Generate INT on 3rd event
266. }
267.
268. //=========
269. // No more.
```

示波器波形如下,上侧皆为 PWM1



PWM1 滞后 PWM2 相位 90°;



PWM1 滞后 PWM3 相位 180°;



PWM1 超前 PWM4 相位 90°。