武汉大学计算机学院

2020-2021 学年第二学期 2019 级弘毅班

《计算机系统基础 2》期末考试试卷

姓名_____ 学号_____

（注：①闭卷考试；②考试时间为 120 分钟；③所有解答必须写在答题纸上。）

Problem 1. (10pts):

1~5:b c e a a

Problem 2: CPU Performance (10pts)

(1)P1 instructions per second : $\frac{1}{1.5}\times 3\times 10^9 = 2.0\times 10^9$

P2 instructions per second: $\frac{1}{1.0}\times 2.5\times 10^9 = 2.5\times 10^9$

P2 is fast.

(2) P1 clock cycles: $10\times 3.0\times 10^9 = 3.0\times 10^{10}$

P1 Instruction count: $10\times 2.0\times 10^9 = 2.0\times 10^{10}$

P_2 clock cycles: $10\times 2.5\times 10^9 = 2.5\times 10^{10}$

P_2 Instruction count: $10\times 2.5\times 10^9 = 2.5\times 10^{10}$

(3)P_1 clock rate F: $\frac{10(1-20\%)}{1.5(1+20\%)}\times F\times 10^9 = 2.0\times 10^{10}$

$$F = \frac{20\times 1.5(1+20\%)}{10(1-20\%)} = \frac{36}{8} = 4.5(GHz)$$

P_2 clock rate F: $\frac{10(1-20\%)}{1.0(1+20\%)}\times F\times 10^9 = 2.5\times 10^{10}$

$$F = \frac{25\times 1.0(1+20\%)}{10(1-20\%)} = \frac{30}{8} = 3.75(GHz)$$

Problem 3: RISC_V Assembly (22pts)

1. (13pts)

a) RISC_V assembly code, Argument n in $x10, Result in $x1.

```
Loop: addi   sp ,   sp,   -16
      sd     x1 ,   8     (sp)
      sd     x10 ,  0(sp)
```

```
        bne   x10   ,   x0,   L1
        addi  x10 ,   x0,   1
        addi  sp ,    sp,   16
        jalr  x0,     0(x1)
L1:     addi  x10 ,   $x10,  -1
        jal   x1,     Loop
        ld    x10 ,   0(sp)
        ld    x1 ,    8(sp)
        addi  sp ,    sp,   16
        add   x10 ,   x10,  x10
        jalr  x0,     0(x1)
```

b) (2pts)

etc

2. (3pts)

```
lui x19, 0x200014
addi x19,19,0x924
```

a) (2pts)

Yes , 0x100000-0xFFFFE

b) (2pts)

No, 0x1000-0xFFE

Problem 4: Arithmetic (8 pts)

a) input signals: a、b、CarryIn

output signals: Result、CarryOut

control signals: Ainvert、Binvert、S1、S0

b)

Ainvert	Binvert	S1	S0	Function
0	0	0	0	a and b
0	0	0	1	a or b
0	0	1	0	a + b
0	1	1	0	a - b
1	1	0	0	a xor b

Problem 5: Single-Cycle (10 pts)

a) (4pts)

There needs to be a path from the ALU output to data memory's write data port. There also need to be a path from read data 2 directly to Data memory's Address input.

b) (6pts)

Step 1 Fetch instruction PC = PC+4

Step 2 Decode, read register file, Imm gen

Step 3 Add Reg[rs2] + immediate

Step 4 Write memory

Problem 6: Pipeline (15 pts)

a) (4 pts)

sub

nop

nop

beq

ld

nop

nop

beq

b) (4 pts)

i) from EX/MEM register to ID stage;

ii) from MEM/WB register to ID stage;

c) (7 pts)

etc

Problem 7: Caches (15 pts)

1. (10pts)

(a)

Address	Type	Hit or Miss	Compulsory	Capacity	Conflict
0x2A	Load	Miss	X		
0x23	Load	Miss	X		
0x14	Load	Miss	X		
0x29	Load	Hit			
0x18	Load	Miss	X		
0x21	Load	Miss			X
0x2B	Load	Miss			X
0x1C	Load	Miss	X		
0x2D	Load	Miss	X		
0x17	Load	Miss		X	
0x19	Load	Miss		X	
0x1D	Load	Miss			X

(b)

Number of bytes read and written from/to memory when the cache is write through:

Bytes read: 44

#Bytes written: 0

Number bytes read and written from/to memory when the cache is a write back:
#Bytes read: 44
#Bytes written: 6
2. (5pts)
memory access takes 10 cycles.
CPI = 1 + (1 – 0.85) * 10 + (0.25 + 0.3) * (1 – 0.9) * 10
+ (1 – 0.75) * 0.2 * 3 + 0.3 * 0.35 * 1 = 3.305

Problem 8: VM（10 pts）

a) (4 pts)

TLB tag 6 bit；
TLB index 1bit；
TLB capacity =16×（6+4+1） = 176 bit
Or =16×（6+4+1+1） = 192 bit

b) (6 pts)

Virtual Address	TLB Hit/Miss/NA	Physical Address
0x013C	M	0x0D3C
0x0E23	M	PF
0x0128	H	0x0D28
0x04FF	M	0x6FF
0x14DF	M	PF
0x1DDE	M	0x03DE

#bits used t