EC21-QuecOpen

Hardware Design of New standard

LTE Module Series

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Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
7th Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

History

Revision	Date	Author	Description
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1 Introduction

This document defines the EC21-QuecOpen module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application note and user guide, customers can use EC21-QuecOpen module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC21-QuecOpen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals,clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operatingover radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

QuecOpen™ is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of QuecOpen™ solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With QuecOpen™ solution, development flow for wireless application and hardware design will be simplified. Main features of QuecOpen™ solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware wirelessly
- Improves products' cost-performance ratio, and enhances products' competitiveness

EC21-QuecOpen module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.2GHz. Customers can use EC21-QuecOpen modules as the basis for development of QuecOpen™ applications.

EC21-QuecOpen is a series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity, and provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS[1)] and voice[2)] functionalities to meet customers' specific application demands.

NOTES

1. [1)] GNSS function is optional.
2. [2)] EC21-QuecOpen series module includes **Data-only** and **Telematics** versions. **Data-only** version does not support voice function, while **Telematics** version supports it.

With a compact profile of 32.0mm × 29.0mm × 2.4mm, EC21-QuecOpen can meet almost all requirements for M2M applications such as automobile, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC21-QuecOpen is an SMD type module which can be embedded in applications through its 144-pin pads, including 80 LCC signal pads and 64 LGA signal pads.

2.2. Key Features

The following table describes the detailed features of EC21-QuecOpen module.

Table 1: Key Features of EC21-QuecOpen Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 1 FDD and TDD Support 1.4 to 20MHz RF bandwidth Support MIMO in DL direction ● FDD: Max 10Mbps (DL), 5Mbps (UL) ● TDD: Max 8.96Mbps (DL), 3.1Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA Support QPSK, 16-QAM, 64-QAM and modulation ● DC-HSDPA: Max 42Mbps (DL) ● HSUPA: Max 5.76Mbps (UL) ● WCDMA: Max 384Kbps (DL)/384Kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL)/85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding

	Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL)/236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS*/SMTP*/ MMS*/FTPS*/SSL* protocols Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
SMS	Text and PDU modes Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 8-bit A-law*, μ-law* and 16-bit linear data formats Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave mode by default, support host mode); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging and firmware upgrade Support USB drivers for Windows XP, Windows Vista, Windows 7/8/8.1/10, Linux 2.6 or later, Android 4.x/5.x/6.x/7.x
UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rate reach up to 3000000bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console, log output 115200bps baud rate
SD Card Interface	Compliant with SD 3.0 protocol
SPI Interface	Support master mode only Maximum clock frequency rate: 50MHz
I2C Interface	Compliant with I2C specification 5.0 Multi-master is not supported

Wireless Connectivity Interfaces	Support a low-power SDIO 3.0 interface for WLAN and UART/PCM interfaces for Bluetooth*
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C-Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NET_STATUS is used to indicate network connectivity status
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (32.0±0.15)mm × (29.0±0.15)mm × (2.4±0.2)mm Weight: approx. 4.9g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC21-QuecOpen and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

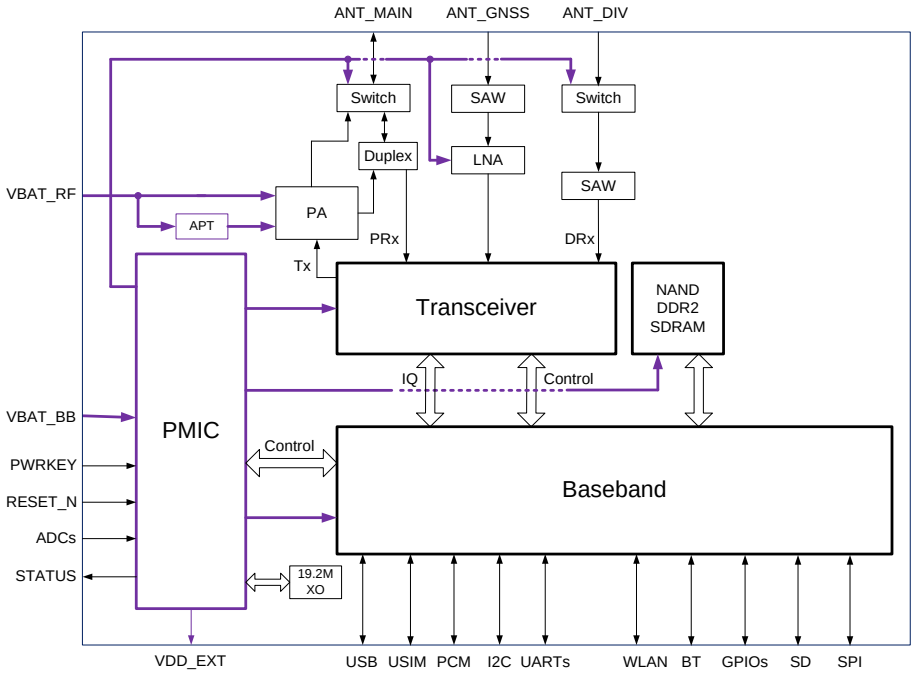


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications conveniently with EC21-QuecOpen module, Quectel supplies the evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EC21-QuecOpen is equipped with 80-pin LCC pads and 64-pin LGA pads. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- SPI interface
- Wireless connectivity interface
- SGMII interface
- ADC interface
- Status indication interfaces
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC21-QuecOpen module.

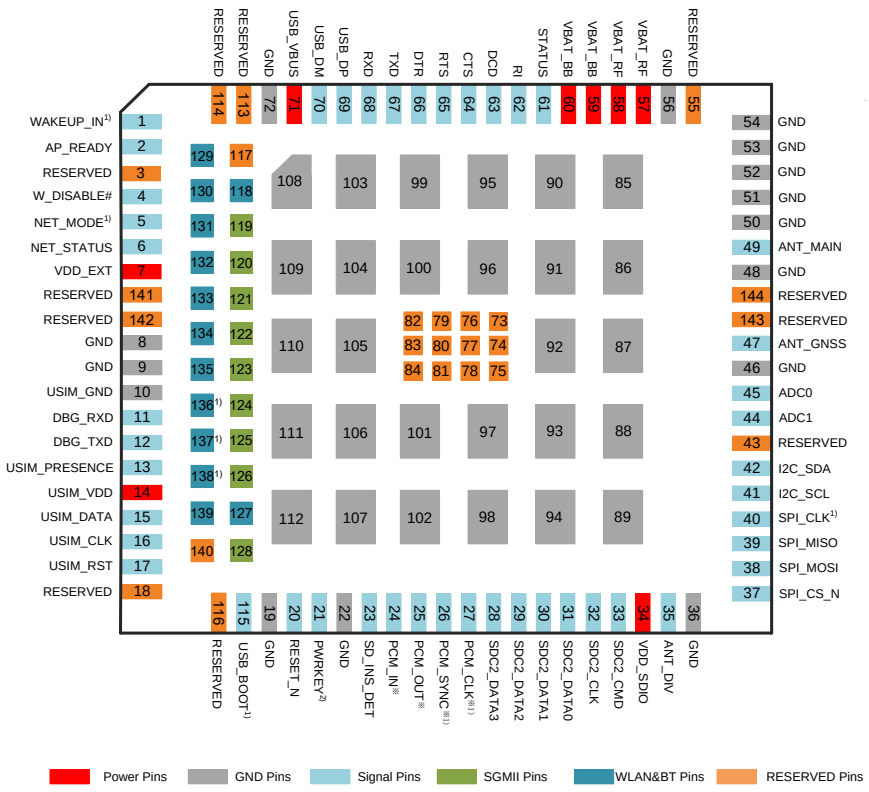


Figure 2: Pin Assignment (Top View)

NOTES

1. 1) means these pins cannot be pulled up before startup.
2. 2) PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. "※" means these interface functions are only supported on **Telematics** version.
4. Pads 37~40, 118, 127 and 129~139 are wireless connectivity interfaces, among which pads 127 and 129~138 are WLAN function pins, and others are Bluetooth (BT) function related pins. BT function is under development.

5. Pads 24~27 are multiplexing pins used for audio design on EC21-QuecOpen module and BT function on FC20 module.
6. Keep all RESERVED pins and unused pins unconnected.
7. GND pads 85~112 should be connected to ground in the design, and RESERVED pads 73~84 should not be designed in schematic and PCB decal.

3.3. Pin Description

The following tables show the pin definition, alternate function and GPIO pull up/down resistance of EC21-QuecOpen module.

Table 2: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain
B	Bidirectional digital with CMOS input
BH	High-voltage tolerant bidirectional digital with CMOS input
PU	Pull up
PD	Pull down
H	High level
L	Low level

Table 3: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	20	DI	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pull-up to 1.8V internally. Active low.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module's operating status	The drive current should be less than 0.9mA.	Require external pull-up. If unused, keep it open.
NET_MODE	5	DO	Indicate the module network registration mode	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. It cannot be pulled up before startup. If unused, keep it open.
NET_	6	DO	Indicate the	V_{OH}min=1.35V	1.8V power domain.

STATUS			module's network activity status	V_{OL}max=0.45V	If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	PI	USB connection detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	
USB_DP	69	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90 ohm.
USB_DM	70	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM_VDD	14	PO	Power supply for (U)SIM card	**For 1.8V USIM:** Vmax=1.9V Vmin=1.7V **For 3.0V USIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	**For 1.8V USIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V USIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	16	DO	Clock signal of (U)SIM card	**For 1.8V USIM:** V_{OL}max=0.45V V_{OH}min=1.35V	

				For 3.0V USIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	17	DO	Reset signal of (U)SIM card	**For 1.8V USIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V USIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DCD	63	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
CTS	64	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RTS	65	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DTR	66	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
TXD	67	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RXD	68	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	11	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	44	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it

					open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data		External pull-up resistor is required. 1.8V only. If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_ DATA3	28	IO	SDIO data signal (bit 3) for SD card	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_ DATA2	29	IO	SDIO data signal (bit 2) for SD card	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details. If unused, keep it open.

				V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	
SDC2_DATA1	30	IO	SDIO data signal (bit 1) for SD card	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA0	31	IO	SDIO data signal (bit 0) for SD card	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_CLK	32	DO	SDIO clock signal for SD card	**For 1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD3.0 protocol for more details. If unused, keep it open.
SDC2_CMD	33	IO	SDIO command signal for SD card	**For 1.8V signaling:** V_{OL}max=0.45V	SDIO signal level can be selected

				V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **For 3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	according to the one supported by SD card. Please refer to SD3.0 protocol for more details. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
VDD_SDIO	34	PO	SDIO pull up power source for SD card	$I_O$max=50mA	Configurable power source. 1.8V/2.85V power domain. If unused, keep it open.
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS_N	37	DO	SPI chip selection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MOSI	38	DO	SPI master out slave in	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MISO	39	DI	SPI master in slave out	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SPI_CLK	40	DO	SPI serial clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

EPHY_RST_N	119	DO	Ethernet PHY reset	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}max=0.58V V_{IH}min=1.27V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V V_{IL}max=0.71V V_{IH}min=1.78V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power source		Configurable power source. 1.8V/2.85V power domain. External pull-up for SGMII MDIO pins. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmission - minus		If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission - plus		If unused, keep it open.
SGMII_RX_P	125	AI	SGMII receiving - plus		If unused, keep it open.

SGMII_RX_M	126	AI	SGMII receiving - minus		If unused, keep it open.
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
PM_ENABLE	127	DO	External power enable control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SDC1_DATA3	129	IO	WLAN SDIO data bus (bit 3)	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA2	130	IO	WLAN SDIO data bus (bit 2)	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA1	131	IO	WLAN SDIO data bus (bit 1)	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_DATA0	132	IO	WLAN SDIO data bus (bit 0)	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_CLK	133	DO	WLAN SDIO clock signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SDC1_CMD	134	DO	WLAN SDIO command signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
WAKE_WLAN	135	DI	Wake up module via WLAN	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V	1.8V power domain. Active low. If unused, keep it

				V_{IH}max=2.0V	open.
WLAN_EN	136	DO	WLAN enable control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. If unused, keep it open.
COEX_ UART_RXD	137	DI	LTE/WLAN&BT coexistence signal	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
COEX_ UART_TXD	138	DO	LTE/WLAN&BT coexistence signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna interface	50Ω impedance	If unused, keep it open.
ANT_MAIN	49	IO	Main antenna interface	50Ω impedance	
ANT_GNSS	47	AI	GNSS antenna interface	50Ω impedance	If unused, keep it open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Cannot be pulled up before startup. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. At low voltage level, module can enter into airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
BT_EN*	139	DO	BT function enable control		This function is still under development.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3,18, 43, 55,73~84, 113, 114, 116, 117, 140~144		Reserved		Keep these pins unconnected.

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. "*" means under development.

Table 4: Alternate Functions of Multiplexing Pins

Pin Name	Pin No.	Model 1 (Default)	Model 2	Model 3	Reset [1)]	Wake-up Interrupt [2)]	Comment
USIM_ PRESENCE	13	USIM_ PRESENCE	GPIO_34	--	B-PD,L	YES	
SD_INS_DET	23	SD_INS_ DET	GPIO_26	--	B-PD,L	YES	
PCM_IN	24	PCM_IN	GPIO_76	--	B-PD,L	YES	
PCM_OUT	25	PCM_OUT	GPIO_77	--	B-PD,L	NO	
PCM_SYNC	26	PCM_SYNC	GPIO_79	--	B-PD,L	YES	BOOT_ CONFIG_7
PCM_CLK	27	PCM_CLK	GPIO_78	--	B-PD,L	NO	BOOT_ CONFIG_8
SPI_CS_N	37	SPI_CS_N_ BLSP6	GPIO_22	UART_RT S_BLSP6	B-PD,L	YES	

SPI_MOSI	38	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6	B-PD,L	YES	
SPI_MISO	39	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6	B-PD,L	YES	
SPI_CLK	40	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6	B-PU,H	NO	BOOT_CONFIG_4
I2C_SCL	41	I2C_SCL_BLSP2	GPIO_7	UART_CTS_BLSP2	B-PD,L	NO	
I2C_SDA	42	I2C_SDA_BLSP2	GPIO_6	UART_RTS_BLSP2	B-PD,L	NO	
STATUS	61	STATUS	PMD[3] (GPIO_04)	--	DO-Z	NO	
WLAN_SLP_CLK	118	WLAN_SLP_CLK	PMD[3] (GPIO_06)		DO-Z	NO	
EPHY_RST_N	119	EPHY_RST_N	GPIO_29*	--	BH-PD,L	YES	
EPHY_INT_N	120	EPHY_INT_N	GPIO_30*	--	B-PD,L	YES	
SGMII_MDATA	121	SGMII_MDATA	GPIO_28*	--	BH-PD,L	YES	
SGMII_MCLK	122	SGMII_MCLK	GPIO_27*	--	BH-PD,L	NO	
SGMII_TX_M	123	SGMII_TX_M	--	--	L	--	
SGMII_TX_P	124	SGMII_TX_P	--	--	L	--	
SGMII_RX_P	125	SGMII_RX_P	--	--	L	--	
SGMII_RX_M	126	SGMII_RX_M	--	--	L	--	
PM_ENABLE	127	PM_ENABLE	PMD[3] (GPIO_03)	--	DO-Z	NO	
SDC1_DATA3	129	SDC1_DATA3	GPIO_12	UART_TXD_BLSP1	B-PD,L	YES	
SDC1_DATA2	130	SDC1_DATA2	GPIO_13	UART_RXD_BLSP1	B-PD,L	YES	
SDC1_DATA1	131	SDC1_DATA1	GPIO_14	UART_RTS_BLSP1	B-PD,L	NO	
SDC1_DATA0	132	SDC1_DATA0	GPIO_15	UART_CTS_BLSP1	B-PD,L	NO	
SDC1_CLK	133	SDC1_CLK	GPIO_16	UART_TXD_BLSP4	B-NP,L	YES	

SDC1_CMD	134	SDC1_CMD	GPIO_17	UART_RXD_BLSP4	B-PD,L	YES	
WAKE_WLAN	135	WAKE_WLAN	GPIO_59	--	B-PD,L	YES	
WLAN_EN	136	WLAN_EN	GPIO_38	--	B-PD,L	YES	BOOT_CONFIG_12
COEX_UART_RXD	137	COEX_UART_RXD	GPIO_37	--	B-PD,L	YES	FORCE_USB_BOOT
COEX_UART_TXD	138	COEX_UART_TXD	GPIO_36	--	B-PD,L	NO	BOOT_CONFIG_3
BT_EN	139	BT_EN	PMD[3] (GPIO_02)	--	DO-Z	NO	

NOTES

1. The pin function in Model 2 and Model 3 takes effect only after software configuration.
2. [1] Please refer to ***Table 2*** for more details about the symbol description.
3. [2]All the GPIO_XX support interrupt function. But not all interrupts can wake up the sleeping module. The wake-up interrupt function is disabled by default.
4. [3]means the GPIO that on the PMD of Qualcomm chipset. These GPIOs do not support interrupt function and cannot wake up the sleeping module
5. All BOOT_CONFIG and FORCE_USB_BOOT pins are prohibited to be pulled up before the module is powered on.

Table 5: Pull-up/Pull-down Resistance of GPIOs

Symbol	Description	Min	Max	Unit
R_{PU}	Pull-up resistance	55	390	kohm
R_{PD}	Pull-down resistance	55	390	kohm

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN** command can set the module into airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EC21-QuecOpen is able to reduce its current consumption to a minimum value during the sleep mode. The following sub-chapters describe the power saving procedure of EC21-QuecOpen module.

3.5.1.1. Main UART Application

If the host communicates with module via main UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.

The following figure shows the connection between the module and the host.

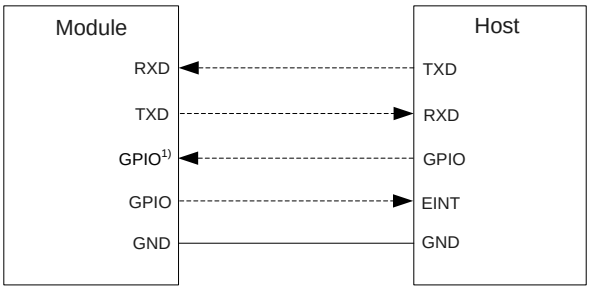


Figure 3: Sleep Mode Application via UART

- Drive the host GPIO to high/low level, or an edge-triggered interrupt will wake up the module (the module supports high/low level wakeup and edge-triggered interrupt wakeup functions which can be configured via software).
- Whenever receiving a phone call, short messages, network data or alarm ringing, EC21-QuecOpen will be woken up from sleep mode. The module's GPIO can be used to wake up the host.

NOTE

GPIO1): GPIOs that configured as wakeup interrupt function.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions must be met to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

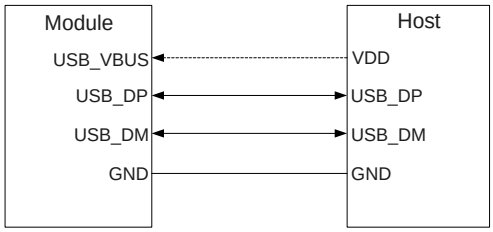


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC21-QuecOpen through USB will wake up the module.
- When EC21-QuecOpen has URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.3. USB Application without USB Remote Wakeup Function

If the host supports USB suspend/resume, but does not support remote wake-up function, it needs to be woken up via the module's GPIO.

There are three preconditions to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

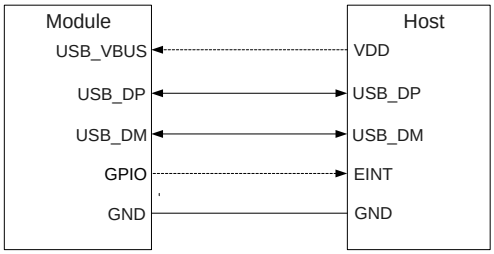


Figure 5: Sleep Mode Application without USB Remote Wakeup

- Sending data to EC21-QuecOpen through USB will wake up the module.
- When EC21-QuecOpen has URC to report, the module's GPIO signal can be used to wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupt in ***Table 4*** are under none-wakeup status.

- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

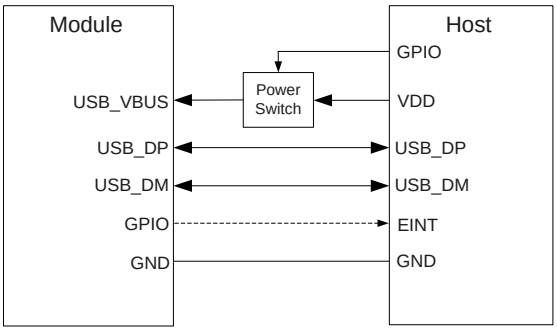


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Refer to ***document [1]*** for more details about the module's power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. The mode can be set via **AT+CFUN=<fun>** command. The parameter **<fun>** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EC21-QuecOpen provides four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Ground		0		V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

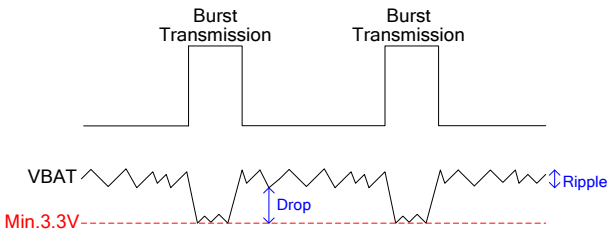


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-

layer ceramic chip (MLCC) capacitor array should also be used to provide the low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is suggested to use a zener diode with reverse zener voltage of 5.1V and dissipation power more than 0.5W, and place it as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

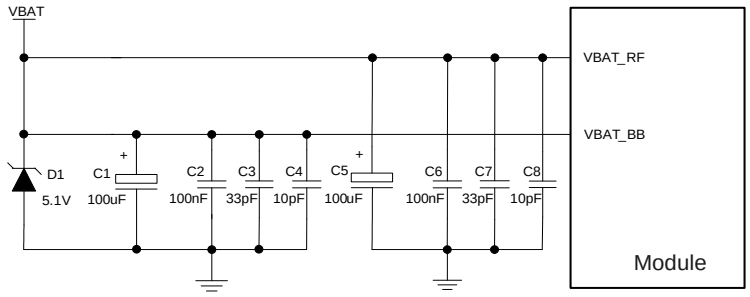


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply is capable of providing sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that you should use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.
The following figure shows a reference design for +5V input power source. The designed output for the power supply is about 3.8V and the maximum load current is 3A.

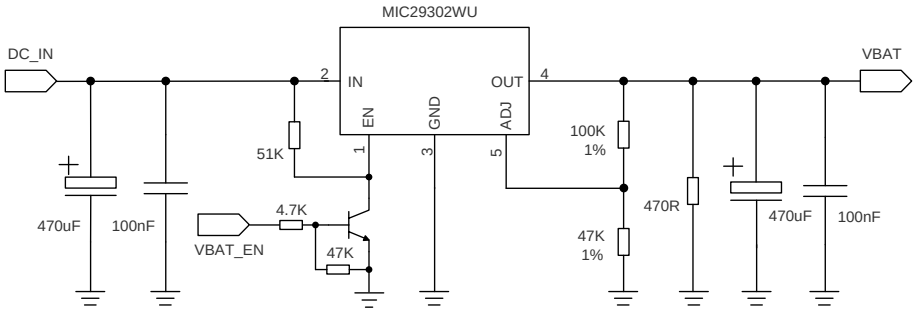


Figure 9: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. Please refer to ***document [2]*** for more details.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	21	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EC21-QuecOpen is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

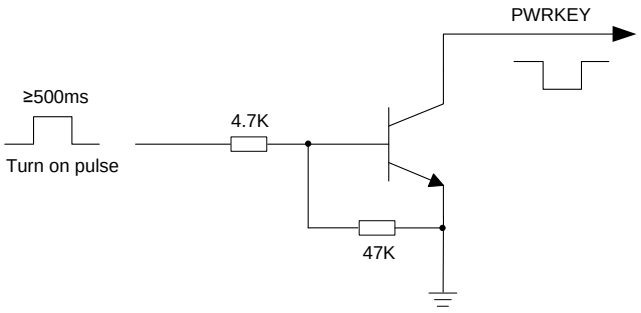


Figure 10: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

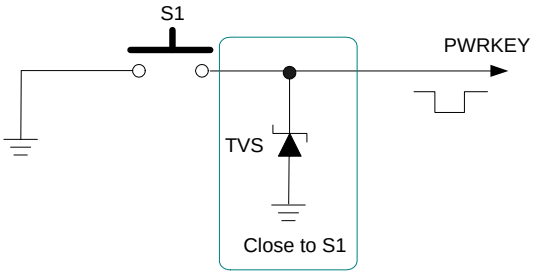


Figure 11: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

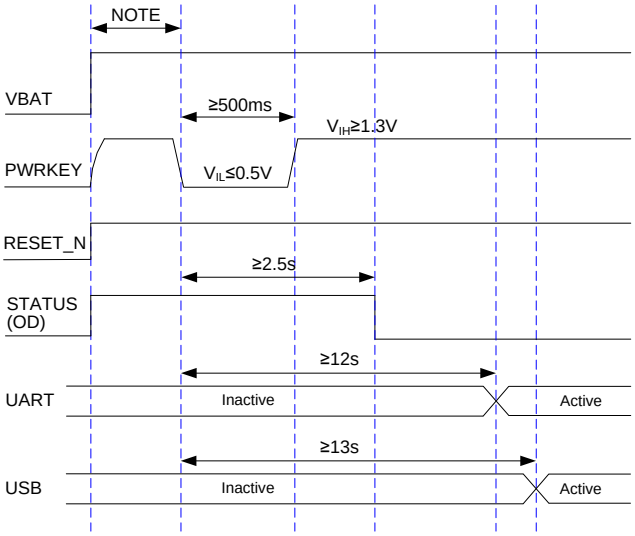


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.
2. Recommended pull up level range is 1.3V~2.1V if there is any pull up circuit added on PWRKEY pin.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using AT command or API interface.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

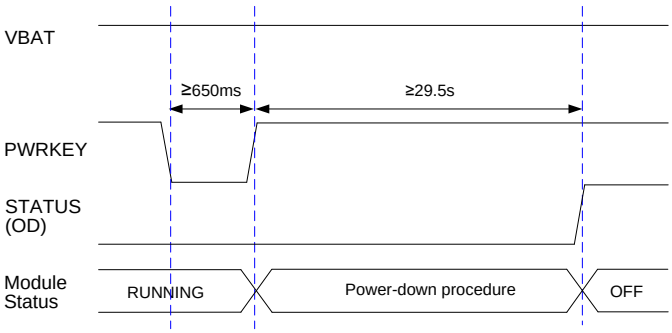


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command or API Interface

It is also a safe way to use AT command or API interface to turn off the module, which is similar to turning off the module via PWRKEY Pin.

Please refer to ***document [2]*** for details.

NOTES

1. In order to avoid damaging the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command or API interface, the power supply can be cut off.
2. When turn off module with AT command or API, please keep PWRKEY at high level after the execution of power off command. Otherwise the module will turn on again after successfully turn-off.

3.7.3. Reset The Module

The RESET_N can be used to reset the module. The module can be reset by driving the RESET_N to a low level voltage for time between 150ms and 460ms. As the RESET_N pin is sensitive to interference, the routing trace on the interface board of the module is recommended to be as short as possible and totally ground shielded.

Table 9: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment

RESET_N	20	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pull-up to 1.8V internally. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

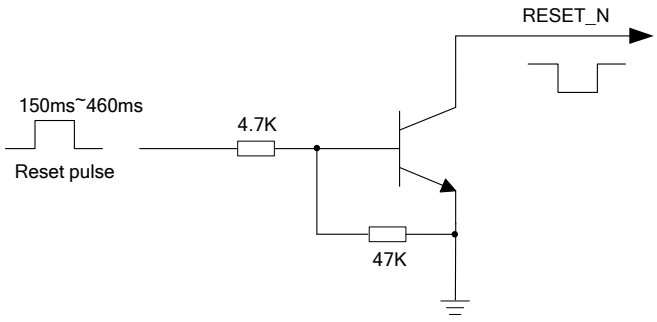


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

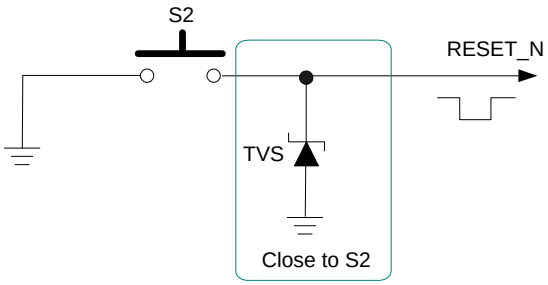


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

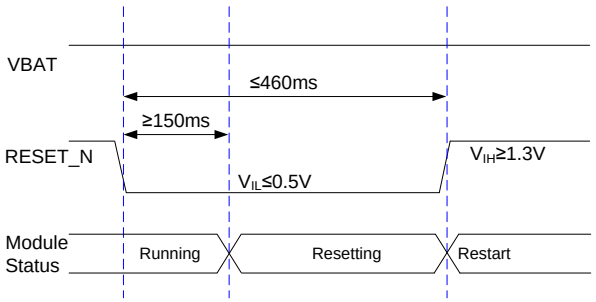


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by AT command, API interface and PWRKEY pin are all failed.
2. Please assure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 10: Pin Definition of the (U)SIM interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	
USIM_CLK	16	DO	Clock signal of (U)SIM card	
USIM_RST	17	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	
USIM_GND	10		Specified ground for (U)SIM card	

EC21-QuecOpen supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

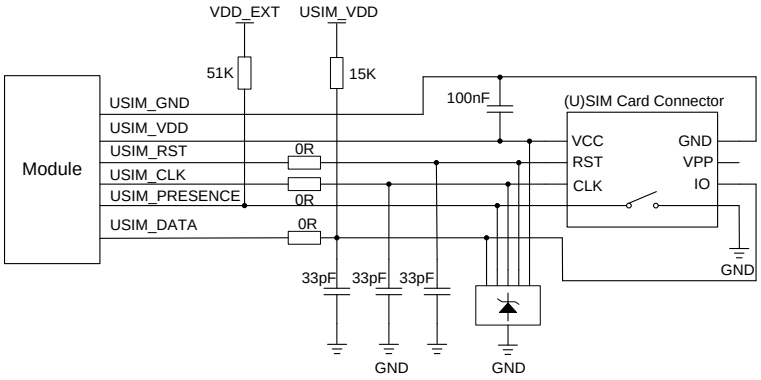


Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM card Connector

If (U)SIM card detection function is not needed, then USIM_PRESENCE can be used for other function. Please refer to ***Table 4*** for more details. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

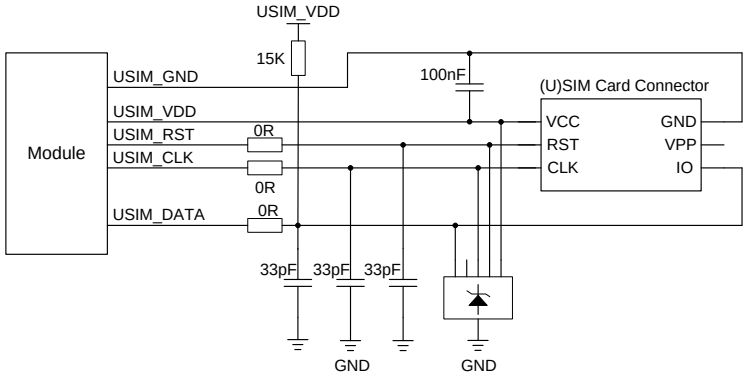


Figure 18: Reference Circuit of (U)SIM interface with a 6-Pin (U)SIM card Connector

In order to enhance the reliability and availability of the (U)SIM card in your application, please follow the criteria below in the USIM circuit design:

- Keep layout of (U)SIM card as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT trace.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 50pF. The 0 ohm resistors should be added in series between the module and the (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. The 33pF capacitors are used for filtering interference of GSM900. Please note that the USIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

EC21-QuecOpen contains one integrated Universal Serial Bus (USB) transceiver which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB Signal Part				
USB_DP	69	IO	USB differential data bus (positive)	Require differential impedance of 90Ω
USB_DM	70	IO	USB differential data bus (minus)	
USB_VBUS	71	PI	Used for detecting the USB connection	Typical 5.0V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

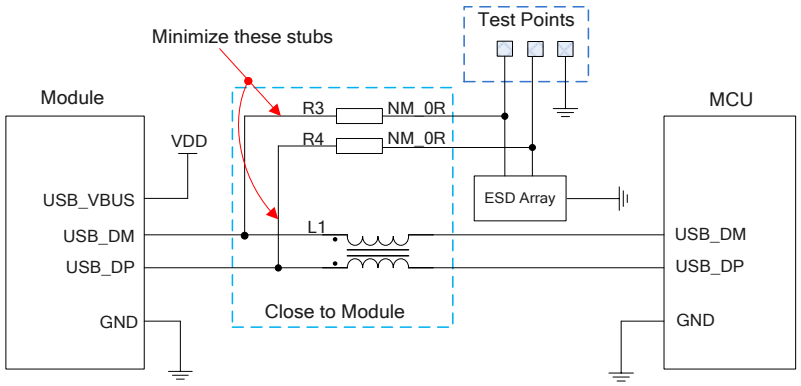


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please comply with the following principles:

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 ohm.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components as close to the USB connector as possible.

NOTES

1. EC21-QuecOpen module's USB interface work on slave mode by default, and support host mode~~can only be used as a slave device and does not support OTG~~.
2. "*" means under development.

带格式的：字体：(默认) Arial, (中文) Arial

3.10. UART Interfaces

The module provides multi-UART interfaces. Except for the MAIN UART interface and DEBUG UART interface, there are other three application UART interfaces: one UART that multiplexed with SPI interface (Pin37~40), two UARTs that multiplexed with WLAN interface (Pin129~134).

These application UARTs has the same function and can be used for communication and data transmission with peripherals.

The following are the features of these application UART interfaces.

- The UART that multiplexed with SPI interface (Pin37~40) supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000bps baud rates, and the default is 115200bps. It supports RTS and CTS hardware flow control.
- The UART that multiplexed with WLAN interface (Pin129~132) supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000bps baud rates, and the default is 115200bps. It supports RTS and CTS hardware flow control.
- The UART that multiplexed with WLAN interface (Pin133~134) supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000bps baud rates, and the default is 115200bps.

The following tables show the pin definition of the four UART interfaces.

Table 12: Pin Definition of the UART Interface (Multiplexed with SPI)

Pin Name	Pin No.	I/O	Description		
			Alternate function 1 (Default)	Alternate function 2	Alternate function 3
SPI_CS_N	37	DO	SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6
SPI_MOSI	38	DO	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6
SPI_MISO	39	DI	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6
SPI_CLK	40	DO	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6

Table 13: Pin Definition of the UART Interface (Multiplexed with WLAN interface)

Pin Name	Pin No.	I/O	Description		
			Alternate	Alternate	Alternate function 3

			function 1 (Default)	function 2	
SDC1_DATA3	129	IO	SDC1_DATA3	GPIO_12	UART_TXD_BLSP1
SDC1_DATA2	130	IO	SDC1_DATA2	GPIO_13	UART_RXD_BLSP1
SDC1_DATA1	131	IO	SDC1_DATA1	GPIO_14	UART_RTS_BLSP1
SDC1_DATA0	132	IO	SDC1_DATA0	GPIO_15	UART_CTS_BLSP1

Table 14: Pin Definition of the UART Interface (Multiplexed with WLAN interface)

Pin Name	Pin No.	I/O	Description		
			Alternate function 1 (Default)	Alternate function 2	Alternate function 3
SDC1_CLK	133	DO	SDC1_CLK	GPIO_16	UART_TXD_BLSP4
SDC1_CMD	134	DO	SDC1_CMD	GPIO_17	UART_RXD_BLSP4

NOTE

The non-default alternate functions mentioned in the above two tables take effect only after software configuration. Please refer to corresponding chapters for details.

The logic levels of the four UART interfaces are described in the table below.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interfaces. A level translator should be used if your application is equipped with a 3.3V UART interface. A level translator TXS0104EPWR provided by Texas Instrument is

recommended. The following figure shows a reference design.

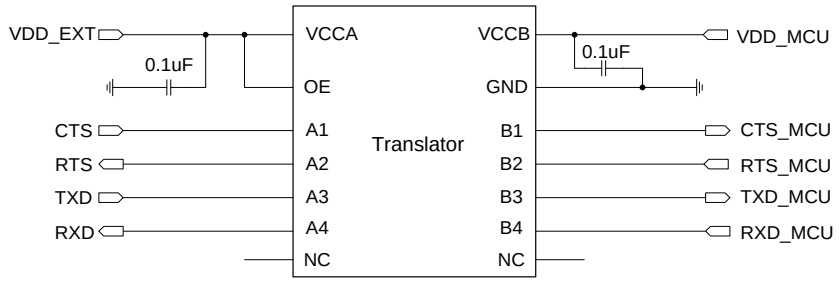


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

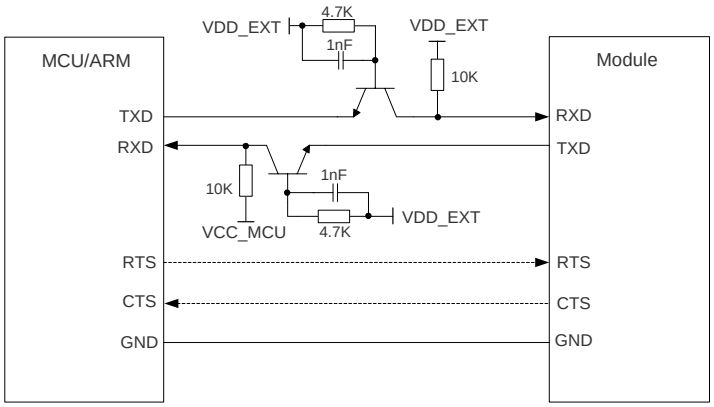


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. PCM and I2C Interfaces

EC21-QuecOpen provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 128, 256, 512, 1024 and 2048kHz for different speech codecs.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 128kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC only.

EC21-QuecOpen supports 8-bit A-law* and μ-law*, and also 16-bit linear data formats. The following figures show the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8kHz PCM_SYNC and 128kHz PCM_CLK.

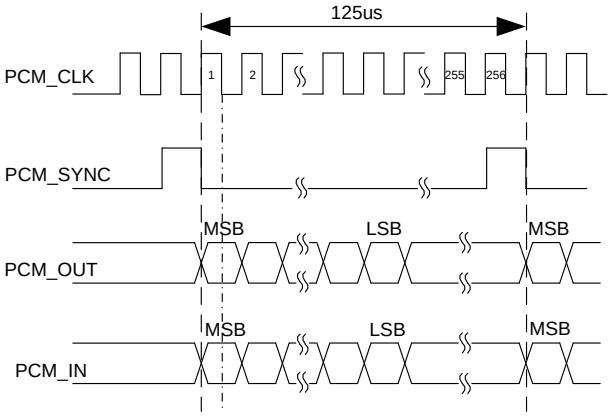


Figure 22: Primary Mode Timing

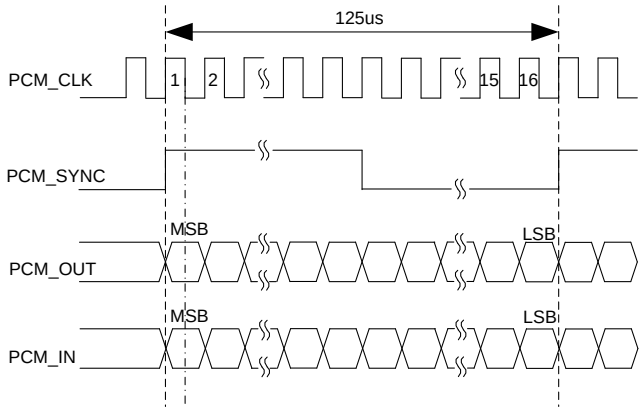


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 16: Pin Definition of PCM

Pin Name	Pin No.	I/O	Description		
			Alternate Function1(Default)	Alternate Function 2	Alternate Function 3
PCM_IN	24	DI	PCM_IN	GPIO_76	
PCM_OUT	25	DO	PCM_OUT	GPIO_77	
PCM_SYNC	26	IO	PCM_SYNC	GPIO_79	
PCM_CLK	27	IO	PCM_CLK	GPIO_78	

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description		
			Alternate Function 1(Default)	Alternate Function 2	Alternate Function 3
I2C_SCL	41	OD	I2C_SCL_BLSP2	GPIO_7	UART_CTS_BLSP2

I2C_SDA	42	OD	I2C_SDA_BLSP2	GPIO_6	UART_RTS_BLSP2

NOTES

1. For more details about non-default alternate functions for the pins mentioned in the above two tables, please refer to corresponding chapters.
2. "*" means under development.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048kHz PCM_CLK and 8kHz PCM_SYNC. Please refer to ***document [2]*** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM interface with an external codec IC.

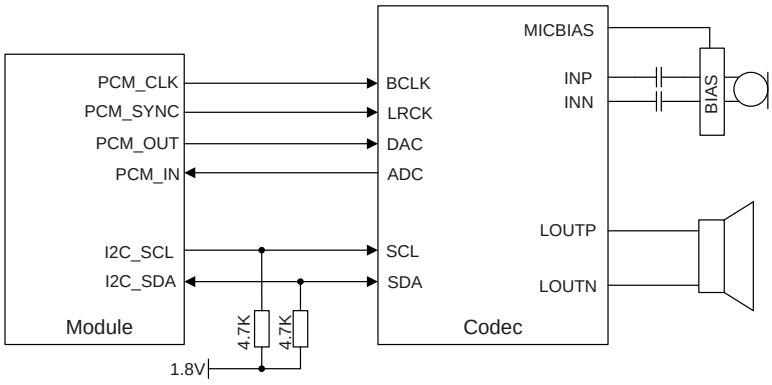


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22ohm, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EC21-QuecOpen works as a master device pertaining to I2C interface.

3.12. SD Card Interface

EC21-QuecOpen provides one SD card interface which supports SD 3.0 protocol. The following tables show the pin definition.

Table 18: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	IO	SD card SDIO bus DATA3	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA2	29	IO	SD card SDIO bus DATA2	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CLK	32	DO	SD card SDIO bus clock	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CMD	33	IO	SD card SDIO bus command	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull up power	1.8V/2.85V configurable. Cannot be used for SD

				card power. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detect	1.8V power domain. If unused, keep it open.

The following figure shows a reference design of SD card interface.

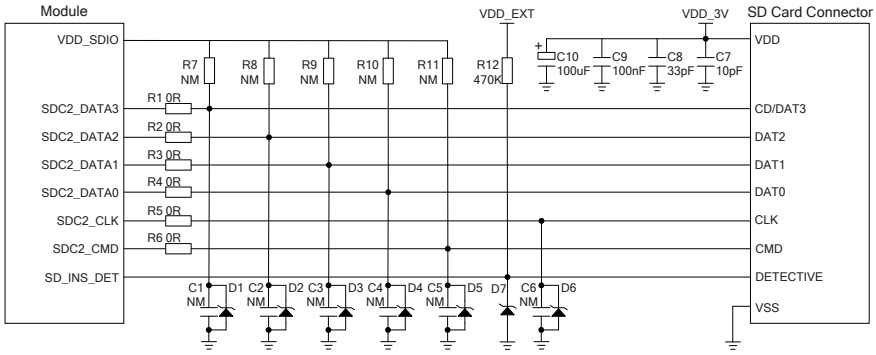


Figure 25: Reference Circuit of SD Card Application

Please follow the principles below in the SD card circuit design:

- The voltage range of SD card power supply VDD_3V is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10KΩ~100KΩ and the recommended value is 100KΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15pF.

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 27mm, so the

exterior total trace length should be less than 23mm.

3.13. SPI Interface

EC21-QuecOpen provides one SPI interface which supports only master mode with a maximum clock frequency up to 50MHz.

The following table shows the pin definition.

Table 19: Pin Definition of the SPI Interface

Pin Name	Pin No.	I/O	Description		
			Alternate function 1 (Default)	Alternate function 2	Alternate function 3
SPI_CS_N	37	DO	SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6
SPI_MOSI	38	DO	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6
SPI_MISO	39	DI	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6
SPI_CLK	40	DO	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6

NOTE

For more details about non-default alternate functions for the pins mentioned in the above table, please refer to corresponding chapters.

The following figure shows the timing relationship of SPI interface. The related parameters of SPI timing is shown in the table below.

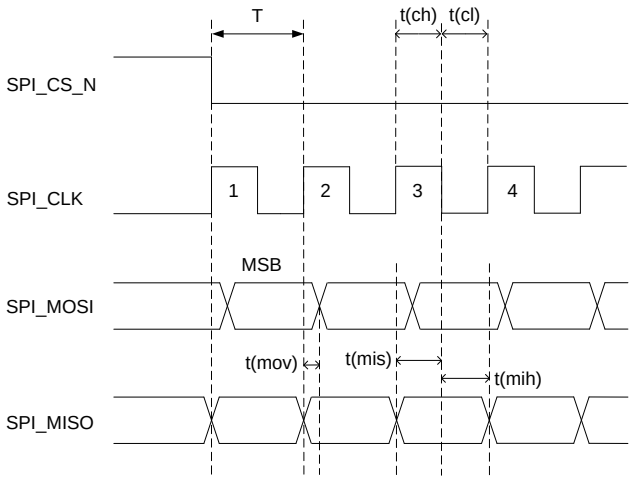


Figure 26: SPI Timing

Table 20: Parameters of SPI Interface Timing

Parameter	Description	Min	Typical	Max	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8V SPI interface. A level translator should be used between the module and the host if customer's application is equipped with a 3.3V processor or device interface.

3.14. Wireless Connectivity Interfaces

EC21-QuecOpen provides an SDIO 3.0 interface with low power consumption for WLAN function, and UART & PCM interfaces for BT function.

The following table shows the pin definition of wireless connectivity interfaces.

Table 21: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description		
Power Part			**Alternate Function 1 (Default)**	**Alternate Function 2**	**Alternate Function 3**
PM_ENABLE	127	DO	PM_ENABLE		
WLAN Part					
SDC1_DATA3	129	IO	SDC1_DATA3	GPIO_12	
SDC1_DATA2	130	IO	SDC1_DATA2	GPIO_13	
SDC1_DATA1	131	IO	SDC1_DATA1	GPIO_14	
SDC1_DATA0	132	IO	SDC1_DATA0	GPIO_15	
SDC1_CLK	133	DO	SDC1_CLK	GPIO_16	
SDC1_CMD	134	IO	SDC1_CMD	GPIO_17	
WLAN_EN	136	DO	WLAN_EN	GPIO_38	
WLAN_SLP_CLK	118	DO	WLAN_SLP_CLK		
WAKE_WLAN	135	DI	WAKE_WLAN	GPIO_59	
Coexistence Part					
COEX_UART_RXD	137	DI	COEX_UART_RXD	GPIO_37	
COEX_UART_TXD	138	DO	COEX_UART_TXD	GPIO_36	
BT Part*					
BT_EN*	139	DO	BT_EN*		

SPI_CS_N	37	DO	SPI_CS_N_BLSP6	GPIO_22	UART_RTS_BLSP6
SPI_MOSI	38	DO	SPI_MOSI_BLSP6	GPIO_20	UART_TXD_BLSP6
SPI_MISO	39	DI	SPI_MISO_BLSP6	GPIO_21	UART_RXD_BLSP6
SPI_CLK	40	DO	SPI_CLK_BLSP6	GPIO_23	UART_CTS_BLSP6
PCM_IN	24	DI	PCM_IN	GPIO_76	
PCM_OUT	25	DO	PCM_OUT	GPIO_77	
PCM_SYNC	26	IO	PCM_SYNC	GPIO_79	
PCM_CLK	27	IO	PCM_CLK	GPIO_78	

NOTES

1. For more details about non-default alternate functions for the pins mentioned in the above table, please refer to corresponding chapters.
2. When WLAN or BT function is used, the coexistence part mentioned in the above table must be used simultaneously.
3. "*" means under development.

The following figure shows a reference design for the connection between wireless connectivity interfaces and Quectel FC20 module.

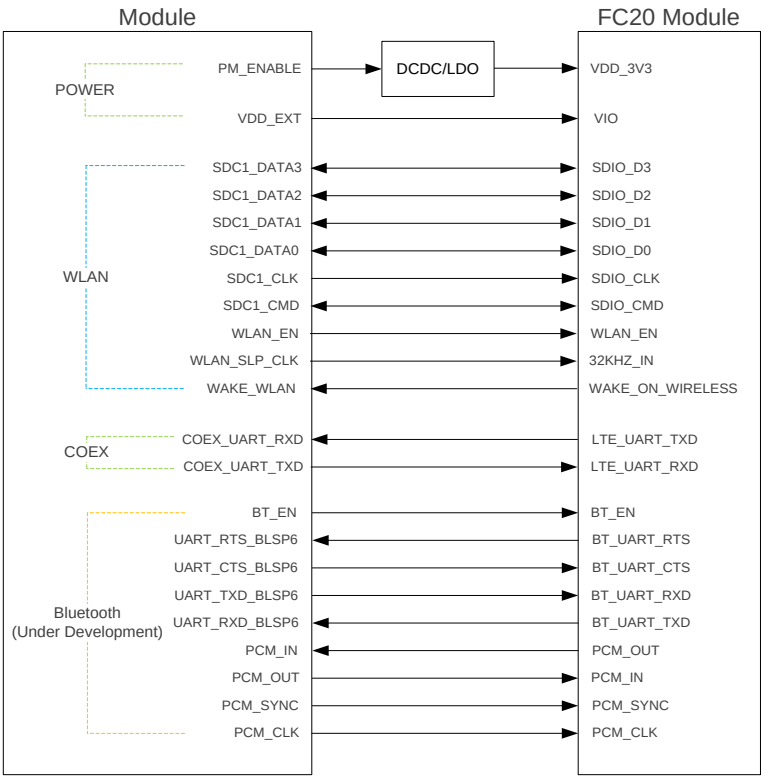


Figure 27: Reference Circuit of Wireless Connectivity Interfaces with FC20 Module

NOTES

1. FC20 module can only be used as a slave device.
2. When BT function is enabled on EC21-QuecOpen module, PCM_SYNC and PCM_CLK pins are only used to output signals.
3. For more information about wireless connectivity interfaces application, please refer to ***document [5]***.

3.14.1. WLAN Interface

EC21-QuecOpen provides a low power SDIO 3.0 interface and a control interface for WLAN design.

SDIO interface supports the following modes:

- Single data rate (SDR) mode (up to 200MHz)
- Double data rate (DDR) mode (up to 52MHz)

As SDIO signals are very high-speed signals, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 ohm (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm.
- Keep termination resistors within 15~24 ohm on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5mm.
- Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.

3.14.2. BT Interface*

More information about BT interface will be added in the future version of this document.

NOTE

"*" means under development.

3.15. SGMII Interface

EC21-QuecOpen includes an integrated Ethernet MAC with an SGMII interface and two management interfaces, key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Full duplex at 1000Mbps
- Half/full duplex for 10/100Mbps
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8V/2.85V

The following table shows the pin definition of SGMII interface.

Table 22: Pin Definition of the SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8V power domain
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	Configurable power source. 1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission-minus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII transmission-plus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	125	AI	SGMII receiving-plus	Connect with a 0.1uF capacitor, close to EC21 module.
SGMII_RX_M	126	AI	SGMII receiving-minus	Connect with a 0.1uF capacitor, close to EC21 module.

The following figure shows the simplified block diagram for Ethernet application.

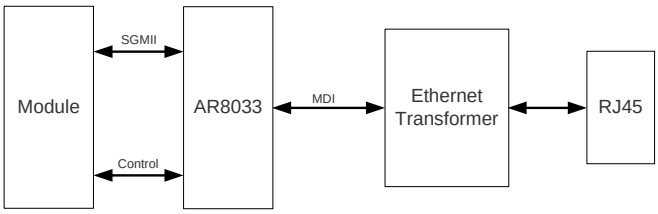


Figure 28: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

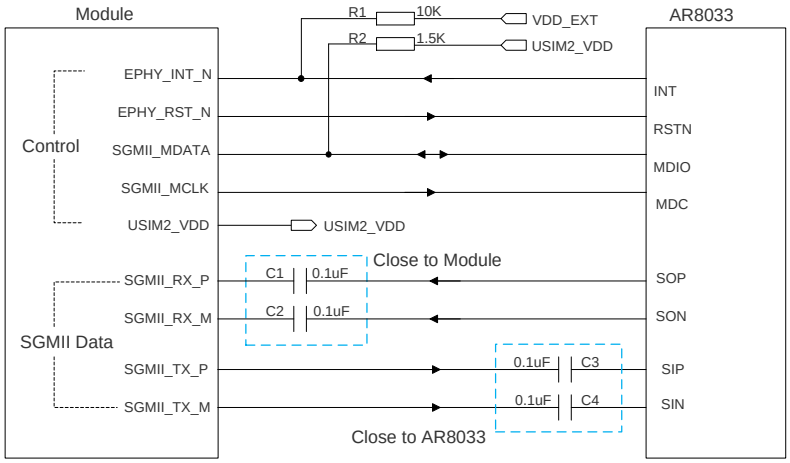


Figure 29: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in your application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from RF and VBAT trace.
- Keep the maximum trace length less than 10inch and keep skew on the differential pairs less than 20mil.
- The differential impedance of SGMII data trace is 100ohm±10%.
- To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40mil.

NOTE

For more information about SGMII application, please refer to ***document [5]*** and ***document [7]***.

3.16. ADC Function

The module provides two analog-to-digital converters (ADC). **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 23: Pin Definition of the ADC

Pin Name	Pin No.	Description
ADC0	45	General purpose analog to digital converter
ADC1	44	General purpose analog to digital converter

The following table describes the characteristic of the ADC function.

Table 24: Characteristic of the ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits

NOTES

1. ADC input voltage must not exceed VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.17. Network Status Indication

EC21-QuecOpen provides one network indication pin: NET_STATUS. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NET_STATUS in different network status.

Table 25: Pin Definition of Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	6	DO	Indicate the module's network activity status.	1.8V power domain

Table 26: Working State of the Network Status Indicator

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

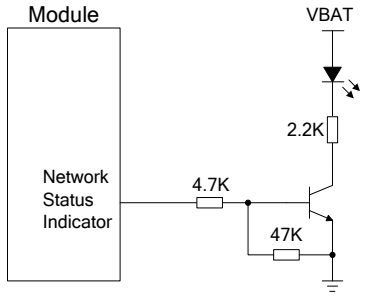


Figure 30: Reference Circuit of the Network Status Indicator

3.18. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pulled up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 27: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	Require external pull-up

The following figure shows different circuit designs of STATUS, and customers can choose either one according to specific application demands.

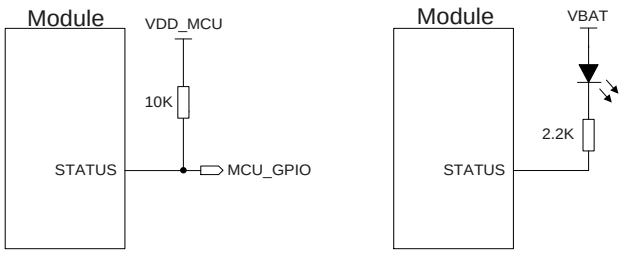


Figure 31: Reference Circuits of STATUS

3.19. USB_BOOT Interface

EC21-QuecOpen provides a USB_BOOT pin. Developers can pull up the USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into forced download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 28: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to boot from USB port	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

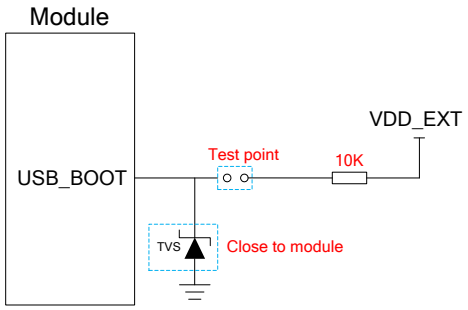


Figure 32: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

EC21-QuecOpen includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EC21-QuecOpen supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, GNSS engine of the module is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EC21-QuecOpen.

Table 29: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start	Autonomous	2.5	s

	@open sky	XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<1.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 ohm characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EC21-QuecOpen include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The antenna interfaces have an impedance of 50 ohm.

5.1. Main/Rx-diversity Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces are shown below.

Table 30: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna pad	50 ohm impedance
ANT_DIV	35	AI	Receive diversity antenna pad	50 ohm impedance

5.1.2. Operating Frequency

Table 31: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
B1	1920~1980	2110~2170	MHz
B2 (1900)	1850~1910	1930~1990	MHz
B3 (1800)	1710~1785	1805~1880	MHz
B4	1710~1755	2110~2155	MHz
B5 (850)	824~849	869~894	MHz
B7	2500~2570	2620~2690	MHz

B8 (900)	880~915	925~960	MHz
B12	699~716	729~746	MHz
B13	777~787	746~756	MHz
B18	815~830	860~875	MHz
B19	830~845	875~890	MHz
B20	832~862	791~821	MHz
B26	814~849	859~894	MHz
B28	703~748	758~803	MHz
B40	2300~2400	2300~2400	MHz
B41	2555~2655	2555~2655	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. It should reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

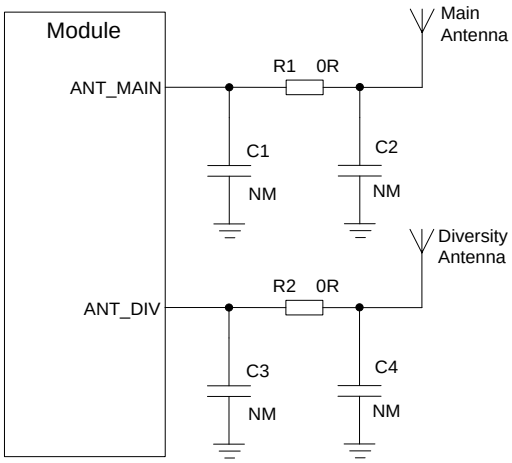


Figure 33: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity. Please refer to ***document [2]*** for details.
3. Place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 ohm. The impedance of the RF traces is determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with difference PCB structures.

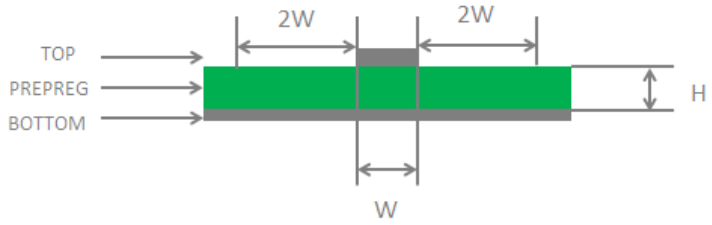


Figure 34: Microstrip Line Design on a 2-layer PCB

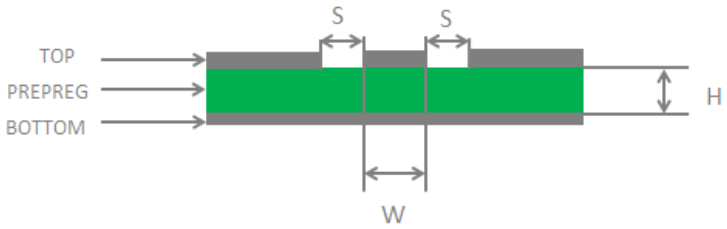


Figure 35: Coplanar Waveguide Line Design on a 2-layer PCB

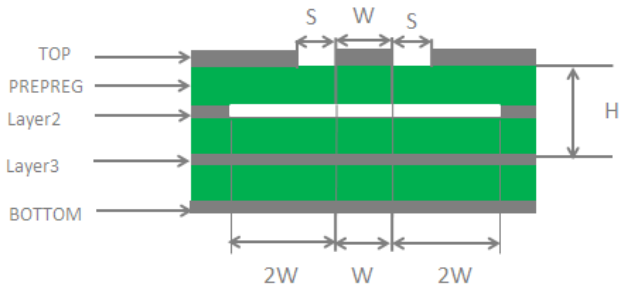


Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

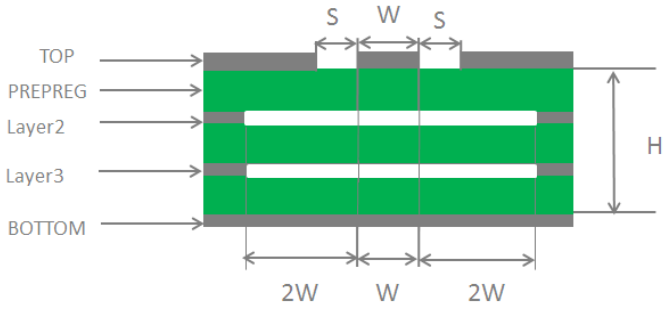


Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 ohm.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times of the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50 ohm impedance

Table 33: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

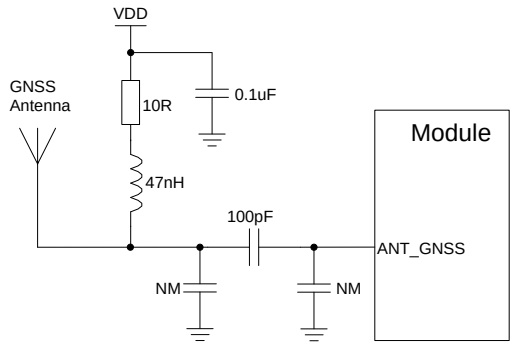


Figure 38: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 34: Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1561~1615MHz Polarization: RHCP or linear VSWR: <2 (Typ.) Passive antenna gain: >0dBi Active antenna noise figure: <1.5dB Active antenna gain: >-2dBi Active antenna embedded LNA gain: 20dB (Typ.) Active antenna total gain: >18dBi (Typ.)
GSM/WCDMA/LTE	VSWR: ≤2 Gain (dBi): 1 Max input power (W): 50 Input impedance (ohm): 50 Polarization type: Vertical Cable insertion loss: <1dB (GSM850, GSM900, WCDMA B5/B8, LTE B5/B8/B12/B13/B18/B19/B20/B26/B28) Cable insertion loss: <1.5dB (GSM1800, GSM1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4) Cable insertion loss <2dB (LTE B7/B40/B41)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by HIROSE.

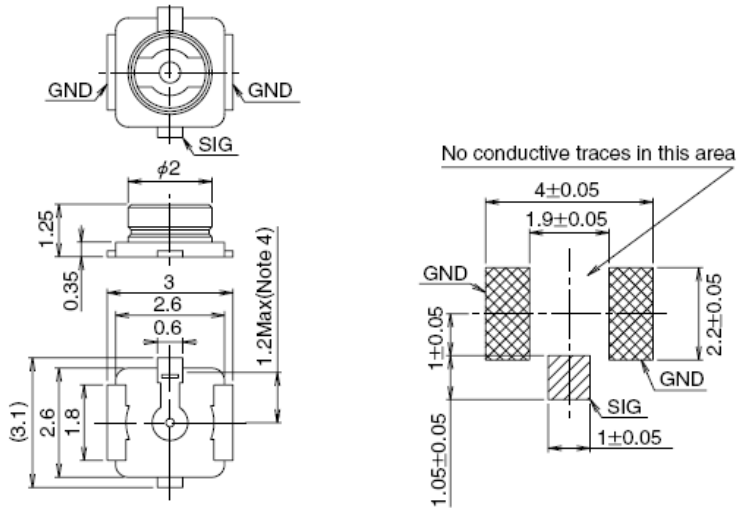


Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connector listed in the following figure can be used to match the U.FL-R-SMT.

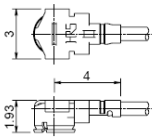
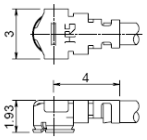
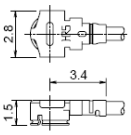
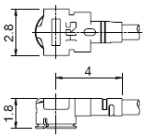
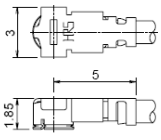
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of UF.L-LP Connectors

The following figure describes the space factor of mated connector.

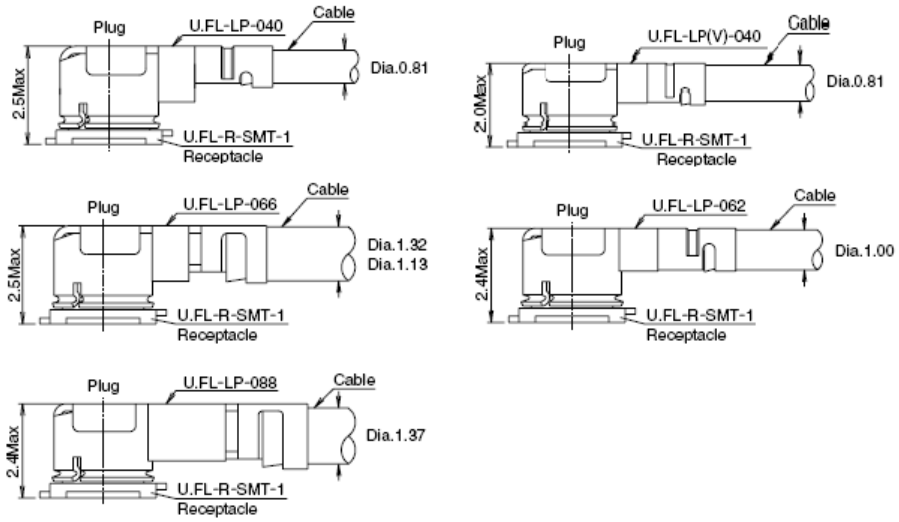


Figure 41: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on GSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on GSM900		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operating and Storage Temperatures

The operating temperature is listed in the following table.

Table 37: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications

again.

6.4. Current Consumption

Table 38: GNSS Current Consumption of EC21-QuecOpen Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	58	mA
		Lost state @Passive Antenna	58	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	33	mA
		Open Sky @Passive Antenna	35	mA
		Open Sky @Active Antenna	43	mA

6.5. RF Output Power

The following table shows the RF output power of EC21-QuecOpen module.

Table 39: RF Output Power

Frequency	Max.	Min.
GSM850/GSM900	33dBm±2dB	5dBm±5dB
DCS1800/PCS1900	30dBm±2dB	0dBm±5dB
GSM850/GSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800/PCS1900 (8-PSK)	26dBm±3dB	0dBm±5dB
WCDMA bands	24dBm+1/-3dB	<-49dBm
LTE-FDD bands	23dBm±2dB	<-39dBm
LTE-TDD bands	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 40: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.7. Thermal Consideration

In order to achieve a maximum performance, it is important to maintain the maximum temperature of the internal baseband chip below 105°C[1)]. Customers can execute **AT+QTEMP** command and get the maximum temperature from the first returned value. When the maximum temperature reaches or exceeds 105°C[1)], it is strongly recommended to comply with the following principles for thermal consideration.

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.

- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.

- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one of them according to their application structure.

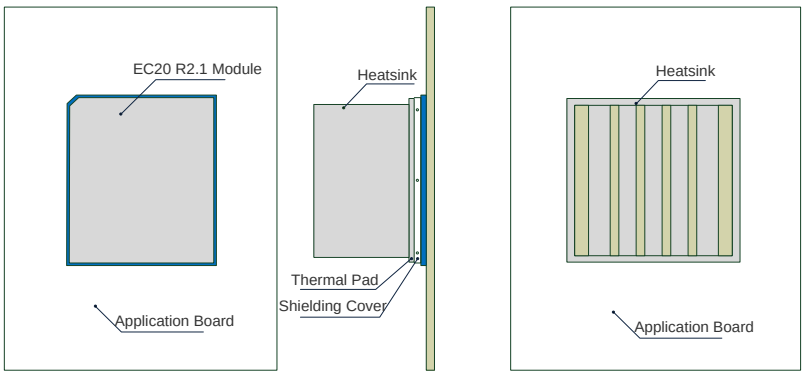


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module)

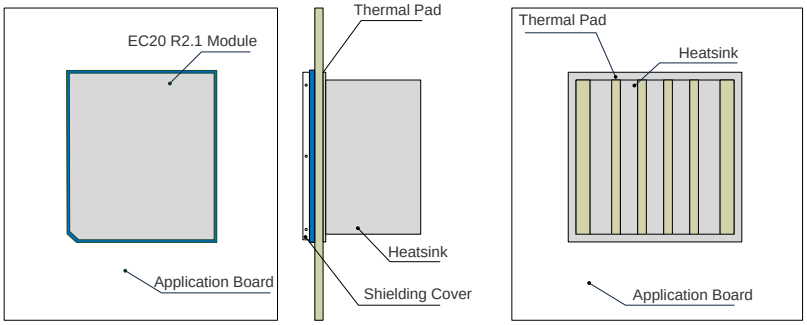


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

[1] When the maximum temperature of the internal baseband chip reaches or exceeds 105°C, the module can still work normally but its performance (RF power, network speed) may be limited. When the maximum temperature reaches or exceeds 115°C, the module will be offline, and then when the temperature reduces to 112°C, the module will be online again.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

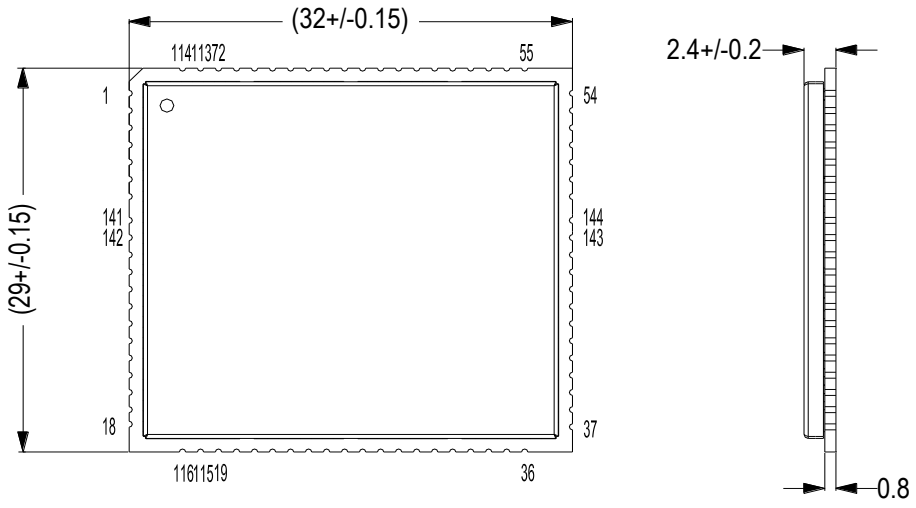


Figure 44: Module Top and Side Dimensions

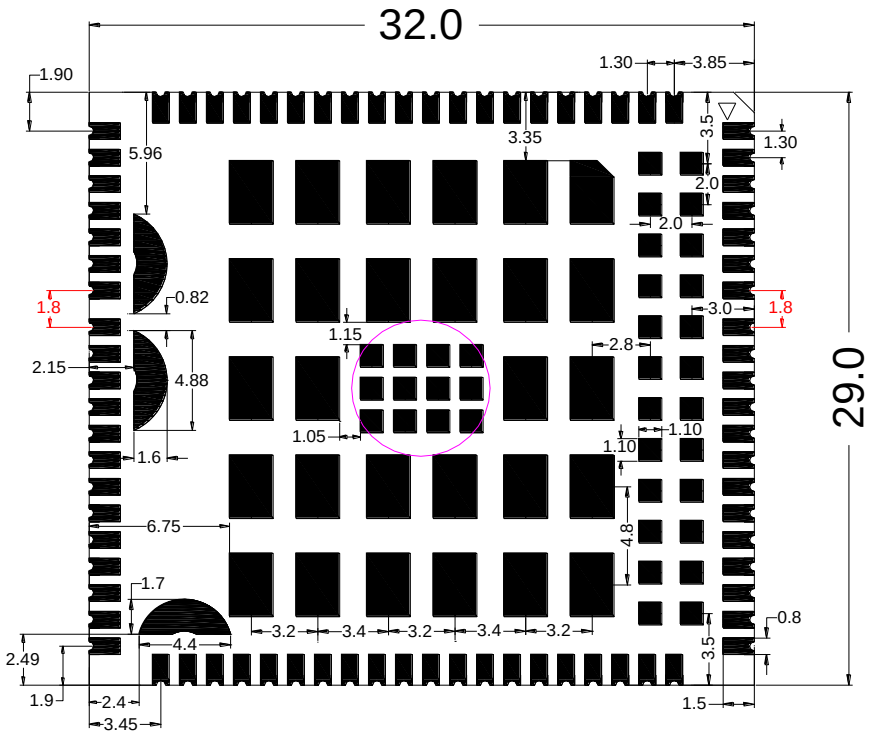


Figure 45: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

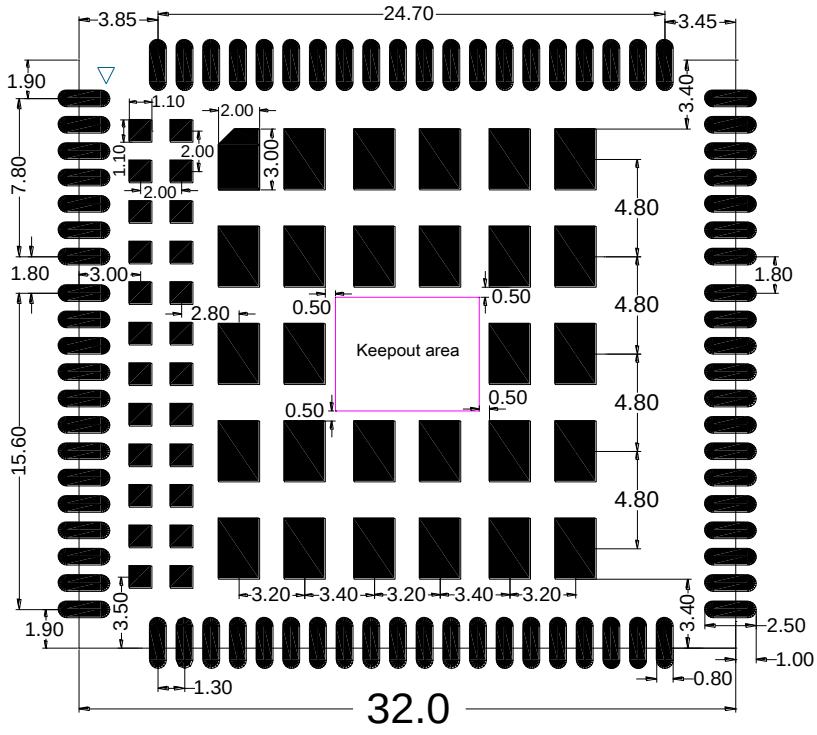


Figure 46: Recommended Footprint (Top View)

NOTES

1. Pads 73~84 should not be designed.
2. For easy maintenance of the module, please keep about 3mm between the module and other components on the host PCB.

7.3. Design Effect Drawings of the Module

Figure 47: Top View of the Module

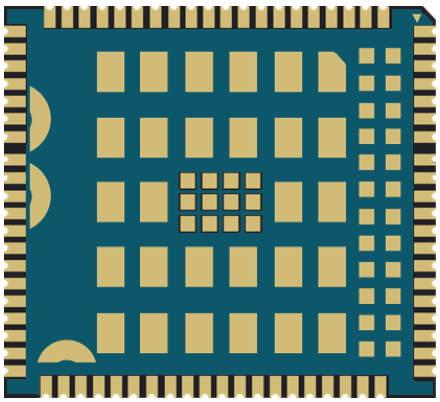


Figure 48: Bottom View of the Module

NOTE

These are design effect drawings of EC21-QuecOpen module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EC21-QuecOpen is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.
3. Devices require bake before mounting, if any circumstances below occurs:
   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.
   - Stored at >10% RH after the vacuum-sealed bag is opened.
4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.2mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 235 ~ 245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

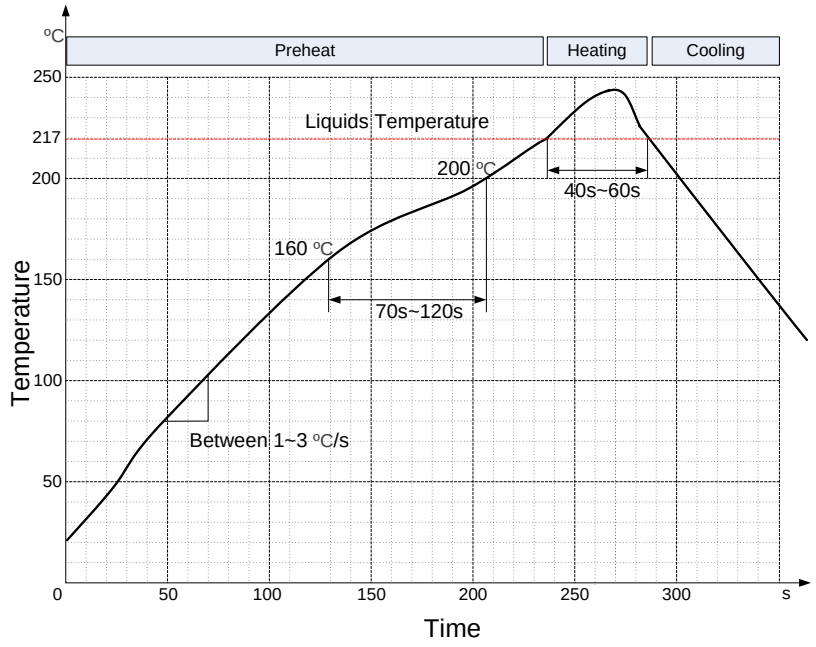


Figure 49: Reflow Soldering Thermal Profile

NOTE

During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module label with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc.

8.3. Packaging

EC21-QuecOpen is packaged in tape and reel carriers. One reel is 12.4m long and contains 250pcs modules. The reel diameter is 330mm.The figure below shows the package details, measured in mm.

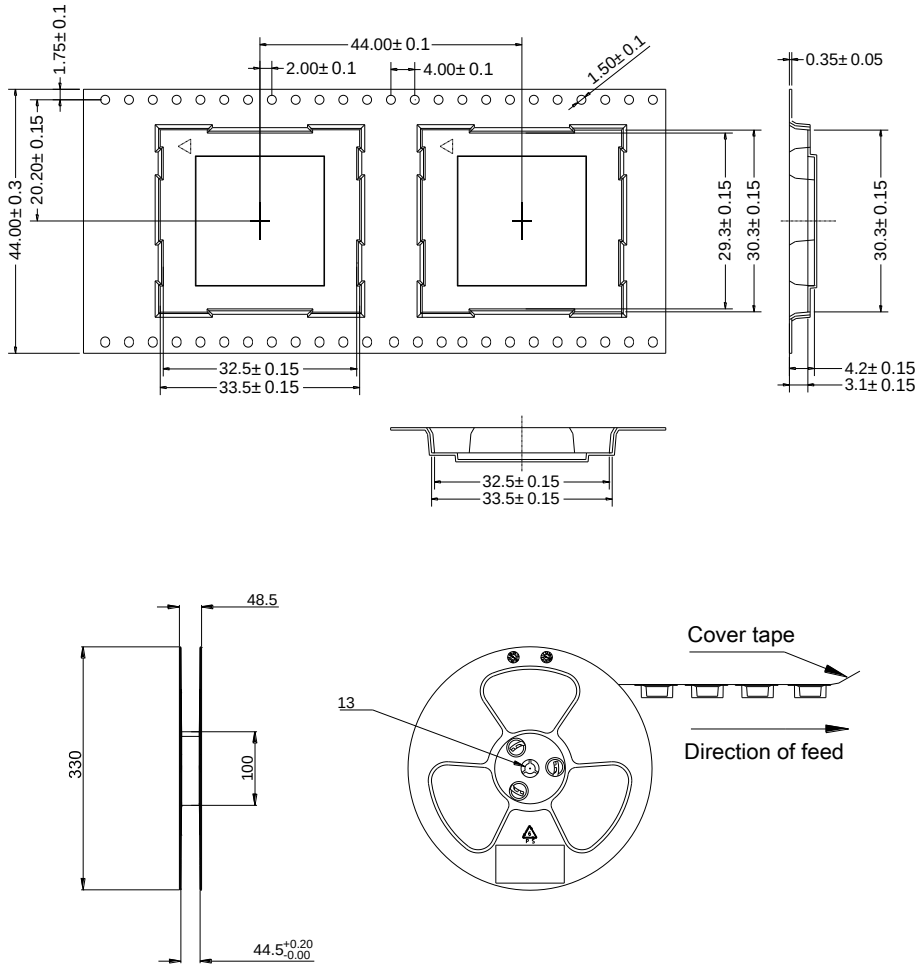


Figure 50: Tape and Reel Specifications

9 Appendix A References

Table 41: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x&EM05_Power_Management_Application_Note	EC21/EC25/EC20 R2.0/EC20 R2.1/EG91/EG95/EM05 Power Management Application Note
[2]	Quectel_EC21&EC21_AT_Commands_Manual	EC21 and EC21 AT Commands Manual
[3]	Quectel_EC2x&EM05_GNSS_AT_Commands_Manual	EC21/EC25/EC20 R2.0/EC20 R2.1/EM05 GNSS AT Commands Manual
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_EC21_Reference_Design	EC21 Reference Design
[6]	Quectel_RF_Layout_Application_Note	RF Layout Application Note

Table 42: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
API	Application Program Interface
bps	Bits Per Second
BT	Bluetooth
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access

DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)

MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMD	Power Management Device
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value

$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{I}max$	Absolute Maximum Input Voltage Value
$V_{I}min$	Absolute Minimum Input Voltage Value
$V_{OH}max$	Maximum Output High Level Voltage Value
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
$V_{OL}min$	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

10 Appendix B GPRS Coding Schemes

Table 43: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 44: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 45: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps