

計算機結構 Exercise 01

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1.5 a. $Instructions\ per\ second = \frac{Clock\ Rate}{CPI}$

P1 $\frac{3 \times 10^9}{1.5} = 2 \times 10^9$ (instructions per second)

P2 $\frac{2.5 \times 10^9}{1.0} = 2.5 \times 10^9$ (instructions per second)

P3 $\frac{4.0 \times 10^9}{2.2} = 1.82 \times 10^9$ (instructions per second)

Therefore, **P2** has the highest performance expressed in instructions per second.

b. $number\ of\ cycles = Clock\ Rate \times CPU\ Time$
 $number\ of\ instructions = \frac{Clock\ Rate \times CPU\ Time}{CPI}$

P1

– $number\ of\ cycles = (3 \times 10^9) \times 10 = 3 \times 10^{10}$

– $number\ of\ instructions = \frac{(3 \times 10^9) \times 10}{1.5} = 2 \times 10^{10}$

P2

– $number\ of\ cycles = (2.5 \times 10^9) \times 10 = 2.5 \times 10^{10}$

– $number\ of\ instructions = \frac{(2.5 \times 10^9) \times 10}{1.0} = 2.5 \times 10^{10}$

P3

– $number\ of\ cycles = (4.0 \times 10^9) \times 10 = 4.0 \times 10^{10}$

– $number\ of\ instructions = \frac{(4.0 \times 10^9) \times 10}{2.2} = 1.82 \times 10^{10}$

c. $CPU\ Time = \frac{Instruction\ Count \times CPI}{Clock\ Rate}$

When instruction count is fixed, $CPU\ Time \propto \frac{CPI}{Clock\ Rate}$. If CPI increases by 20%, and we want CPU time to reduce by 30%, clock rate should become $\frac{1.2}{0.7} = 1.714$ times. That is to say, clock rate should increase by 71.4%.

1.8.1 $Dynamic\ Power\ Consumption = Capacitive\ load \times Voltage^2 \times Frequency$

Prescott $Capacitive\ load = \frac{90}{1.25^2 \times (\frac{1}{2} \times 3.6 \times 10^9)} = 3.2 \times 10^{-8} (F)$

Ivy Bridge $Capacitive\ load = \frac{40}{0.9^2 \times (\frac{1}{2} \times 3.4 \times 10^9)} = 2.905 \times 10^{-8} (F)$

1.8.2 Prescott

– $Percentage = \frac{10}{10+90} \times 100\% = 10\%$

– $Ratio = \frac{10}{90} = 0.1111$

Ivy Bridge

- *Percentage* $\frac{30}{30+40} \times 100\% = 42.86\%$
- *Ratio* $\frac{30}{40} = 0.75$

1.8.3 Static Power Consumption = $V \times I_{leakage}$

Prescott

$$I_{leakage} = \frac{10}{1.25} = 8$$

To maintain the same leakage current and reduce the total dissipated power by 10%, the new equation becomes

$$(10 + 90) \times 90\% = V \times 8 + 3.2 \times 10^{-8} \times V^2 \times \left(\frac{1}{2} \times 3.6 \times 10^9\right)$$

Solve the equation to get $V = 1.1825, -1.3214$. Therefore, the voltage should be reduced to $1.1825V$.

$$\text{Ivy Bridge } I_{leakage} = \frac{30}{0.9} = 33.33$$

To maintain the same leakage current and reduce the total dissipated power by 10%, the new equation becomes

$$(30 + 40) \times 90\% = V \times 33.33 + 2.905 \times 10^{-8} \times V^2 \times \left(\frac{1}{2} \times 3.4 \times 10^9\right)$$

Solve the equation to get $V = 0.8413, -1.5163$. Therefore, the voltage should be reduced to $0.8413V$.

1.12.1 CPU Time = $\frac{\text{Instruction Count} \times CPI}{\text{Clock Rate}}$

$$\text{P1 } \frac{(5.0 \times 10^9) \times 0.9}{4 \times 10^9} = 1.125 \text{ (s)}$$

$$\text{P2 } \frac{(1.0 \times 10^9) \times 0.75}{3 \times 10^9} = 0.25 \text{ (s)}$$

P1 has a larger clock rate, but its performance is worse than **P2**.

1.12.2 $\frac{(1.0 \times 10^9) \times 0.9}{4 \times 10^9} = \frac{\text{Instruction Count} \times 0.75}{3 \times 10^9}$, Instruction Count = 0.9×10^9

P2 can execute 0.9×10^9 instructions in the same time that **P1** needs to execute 1.0×10^9 instructions.

1.12.3 MIPS = $\frac{\text{Clock Rate}}{CPI \times 10^6}$

$$\text{P1 } \frac{4 \times 10^9}{0.9 \times 10^6} = 4444.44 \text{ (MIPS)}$$

$$\text{P2 } \frac{3 \times 10^9}{0.75 \times 10^6} = 4000 \text{ (MIPS)}$$

P1 has a larger MIPS, but its performance is worse than **P2**.

1.12.4 MFLOPS = $\frac{\text{No.FP operations}}{\text{execution time} \times 10^6}$

$$\text{P1 } \frac{5.0 \times 10^9 \times 40\%}{1.125 \times 10^6} = 1777.78 \text{ (MFLOPS)}$$

$$\text{P2 } \frac{1.0 \times 10^9 \times 40\%}{0.25 \times 10^6} = 1600 \text{ (MFLOPS)}$$

$$\begin{aligned}
1.15 \text{ per processor execution time} &= \frac{100}{\text{processor num}} + 4 \\
\text{speedup} &= \frac{100}{\frac{100}{\text{processor num}} + 4} \\
\text{ideal speedup} &= \frac{100}{\frac{100}{\text{processor num}}} = \text{processor num}
\end{aligned}$$

2 processors

$$\begin{aligned}
- \text{ per processor execution time} &= \frac{100}{2} + 4 = 54 \\
- \text{ speedup} &= \frac{100}{54} = 1.85 \\
- \text{ ratio} &= \frac{1.85}{2} = 0.9260
\end{aligned}$$

4 processors

$$\begin{aligned}
- \text{ per processor execution time} &= \frac{100}{4} + 4 = 29 \\
- \text{ speedup} &= \frac{100}{29} = 3.45 \\
- \text{ ratio} &= \frac{3.45}{4} = 0.8621
\end{aligned}$$

8 processors

$$\begin{aligned}
- \text{ per processor execution time} &= \frac{100}{8} + 4 = 16.5 \\
- \text{ speedup} &= \frac{100}{16.5} = 6.06 \\
- \text{ ratio} &= \frac{6.06}{8} = 0.7576
\end{aligned}$$

16 processors

$$\begin{aligned}
- \text{ per processor execution time} &= \frac{100}{16} + 4 = 10.25 \\
- \text{ speedup} &= \frac{100}{10.25} = 9.76 \\
- \text{ ratio} &= \frac{9.76}{16} = 0.6098
\end{aligned}$$

32 processors

- *per processor execution time* = $\frac{100}{32} + 4 = 7.13$

- *speedup* = $\frac{100}{7.13} = 14.04$

- *ratio* = $\frac{14.04}{32} = 0.4386$

64 processors

- *per processor execution time* = $\frac{100}{64} + 4 = 5.56$

- *speedup* = $\frac{100}{5.56} = 17.98$

- *ratio* = $\frac{17.98}{64} = 0.2809$

128 processors

- *per processor execution time* = $\frac{100}{128} + 4 = 4.78$

- *speedup* = $\frac{100}{4.78} = 20.92$

- *ratio* = $\frac{20.92}{128} = 0.1634$