計算機結構 Exercise 04

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5.3.1 5 bits are used for the offset, which means the cache block size is 32 byte = 8 words

5.3.2 5 bits are used for the index, which means the cache have 32 entries.

5.3.3 $$\frac{2^5 \times (2^5 \times 8\ (block\ size) + 22\ (tag\ size) + 1\ (valid\ field\ size))}{2^5 \times (2^5 \times 8)} = 1.090$$

5.3.4

byte address	block address	block number	hit / miss
0	$\lfloor 0/32 \rfloor = 0$	0 mod 32 = 0	miss
4	$\lfloor 4/32 \rfloor = 0$	0 mod 32 = 0	hit
16	$\lfloor 16/32 \rfloor = 0$	0 mod 32 = 0	hit
132	$\lfloor 132/32 \rfloor = 4$	4 mod 32 = 4	miss
232	$\lfloor 232/32 \rfloor = 7$	7 mod 32 = 7	miss
160	$\lfloor 160/32 \rfloor = 5$	5 mod 32 = 5	miss
1024	$\lfloor 1024/32 \rfloor = 32$	32 mod 32 = 0	miss (0 → 32)
30	$\lfloor 30/32 \rfloor = 0$	0 mod 32 = 0	miss (32 → 0)
140	$\lfloor 140/32 \rfloor = 4$	4 mod 32 = 4	hit
3100	$\lfloor 3100/32 \rfloor = 96$	96 mod 32 = 0	miss (0 → 96)
180	$\lfloor 180/32 \rfloor = 5$	5 mod 32 = 5	hit
2180	$\lfloor 2180/32 \rfloor = 68$	68 mod 32 = 4	miss (4 → 68)

4 replacement

5.3.5 Hit ratio = $\frac{4}{12} = 0.33$

5.3.6 <index, tag, data>
<00000_2, $0000 \cdots 0011_2$ (22 bits), mem[3072]>
<00100_2, $0000 \cdots 0010_2$ (22 bits), mem[2176]>
<00101_2, $0000 \cdots 0000_2$ (22 bits), mem[160]>
<00111_2, $0000 \cdots 0000_2$ (22 bits), mem[224]>

5.6.1 **P1** : $\frac{1}{0.66ns} = 1.52$ GHz
P2 : $\frac{1}{0.90ns} = 1.11$ GHz

5.6.2 **P1** : 0.66 ns + 8% × 70 ns = 6.26 ns
P2 : 0.90 ns + 6% × 70 ns = 5.1 ns

5.6.3 **P1** : $1.0 + 36\% \times 8\% \times \dfrac{70}{0.66} = 4.05 \rightarrow 2.68$ ns per instruction

P2 : $1.0 + 36\% \times 6\% \times \dfrac{70}{0.90} = 2.68 \rightarrow 2.41$ ns per instruction

$\longrightarrow$ **P2** is faster

5.6.4 AMAT $= 0.66$ ns $+ 8\% \times 5.62$ ns $+ 8\% \times 95\% \times 70$ ns $= 6.43$ ns

$\longrightarrow$ worse

5.6.5 $1 + 36\% \times 8\% \times \dfrac{5.62}{0.66} + 36\% \times 8\% \times 95\% \times \dfrac{70}{0.66} = 4.15$

5.6.6 **P1** : 2.74 ns per instruction

P2 : 2.41 ns per instruction

$\longrightarrow$ **P2** is faster

$0.66 + 36\% \times \text{miss rate} \times 5.62 + 36\% \times \text{miss rate} \times 95\% \times 70$

$= 0.90 + 36\% \times 6\% \times 70$

$\longrightarrow$ **P1** needs miss rate in its L1 cache to be 6.75% to match **P2**'s performance