Project: WATCHMAN
University of Hawaii at Manoa

Meeting : Tuesday, 17th of October 2018, Week 5

Participants: Anthony Schluchin schluchi@hawaii.edu
Jonathan Hendriks jhendrik@hawaii.edu
Jose Duron jduron@hawaii.edu
Kurtis Nishimura kurtisn@phys.hawaii.edu

Ky:
Left the Watchman Project.

Vasily :
Out of project til November, in Japan for B2GM (Belle 2 General Meeting).

General:
Vivado does not update the DDR timings from one board to another! The parameters for vivado DDR are, command to run in tcl console :

set_property -dict [list CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0 {-0.073} CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 {-0.072} CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 {0.024} CONFIG.PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 {0.023} CONFIG.PCW_UIPARAM_DDR_BOARD_DELAY0 {0.294} CONFIG.PCW_UIPARAM_DDR_BOARD_DELAY1 {0.298} CONFIG.PCW_UIPARAM_DDR_BOARD_DELAY2 {0.338} CONFIG.PCW_UIPARAM_DDR_BOARD_DELAY3 {0.334} CONFIG.PCW_PRESET_BANK0_VOLTAGE {LVCMOS 3.3V} CONFIG.PCW_UIPARAM_DDR_PARTNO {MT41K256M16 RE-125}] [get_bd_cells processing_system7_0]

This will set the correct DDR timings for using the microzed board and check that the memory is : MT41K256M16 RE-125

SDK has problems if running alone and not launched from Vivado to build the hardware (BSP project) from the hdf file.

TCL script updated to copy bitstream and hdf for launching more efficiently SDK. Kurtis propose to look into Non-Project Mode … A possible way to avoid all those problems.

Jose:
Working on the 6U-VME board by proposing, hopefully Friday, a proposal for this board connections and FPGA to use, signals
Idea discussed at the meeting:

- Deserializer
- I2C GPIO for HW address
- Level shifting with FPGA
- Use of two microzeds

>> Waiting on Jose's proposal Friday!

Jonathan:
Test pattern Generator readout from TARGETC >> OK.
Looking now for the bigger picture to sample 511 windows with specific waveform from generator and reconstruct it by reading out the storage area. This will give full readout of TargetC.

Anthony :
Merging projects with UDP to test full loop PL-PS-PC- Gui Python. Improving the GUI to analyse the data received.