Project: WATCHMAN
University of Hawaii at Manoa

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Participants:

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In reference from image in attachment

Discussion on the advancement of the project :

PL side of the zynq:
The PL side is equipped with an Axi-Lite interface to start and define parameters for the TARGETC as well as defining test pattern for different stages of the readout. The Clock Management as been redone, earlier design was using PLL (Xilinx IP's), the newer design is composed of Xilinx Primitives to be able on placing the design directly in the block diagram of Vivado. The reason for this is the IP Integrator is running problem where there is none.

Each communication interface to TARGETC is tested and verified. The change in readout technique from prototype to enhanced version is creating some troubleshooting.

The Round Buffer Circuit is very basic for the moment a newer version is ongoing to be able to encounter the different situation, this first version will work for feeding data to the PS side and so Anthony could analyze and correct the data.

The Fifo Management design and axi-Stream interface are both working with test patterns.

The only circuit or firmware is the trigger circuit, which has to be tested. Hopefully this will be done during this week, if the debugging is successful.

PS side of the zynq :

Some temporary function are written to communicate with the PL side, to write in the registers the values received by UDP.

A chained list need to be put in place, to receive the data from the PL side. The data will be send window by window, but then the PS must work on the complete frame (1 to 4 windows). There are different things to do on those data:

1. Find the good gain stage (there are 4 channels per PMT with 4 different gains, the smaller channel has the bigger gain). To do so, we need to pass through the complete frame and see if the pulse pass under the threshold. We start with the bigger gain, and in case, we change for un smaller one
2. Subtract the pedestal to every sample in function of the location in the analog memory of the ASIC (memory size = 512 windows -> 512 wdo * 16ch/wdo * 32sample/ch * 2bytes)
3. Apply the transfer function to every sample in function of the location in the analog memory of the ASIC because each comparator (inside the ASIC, to convert the analog into digital) is different.
4. They are two type of format for the data sent to the PC:
    - Full waveform: when the pulse is too long or that even with the smaller gain stage the pulse goes under the threshold.
    - Amplitude and time (when the pulse was at 20%)

Trigger Circuit:

Two options :

- Single Photon, the data out through UDP is Amplitude and Time
- Wide Pulse: All wave form

The trigger system has to decide for itself if the pulse is a long or short pulse depending on the trigger signal from the comparator off board.