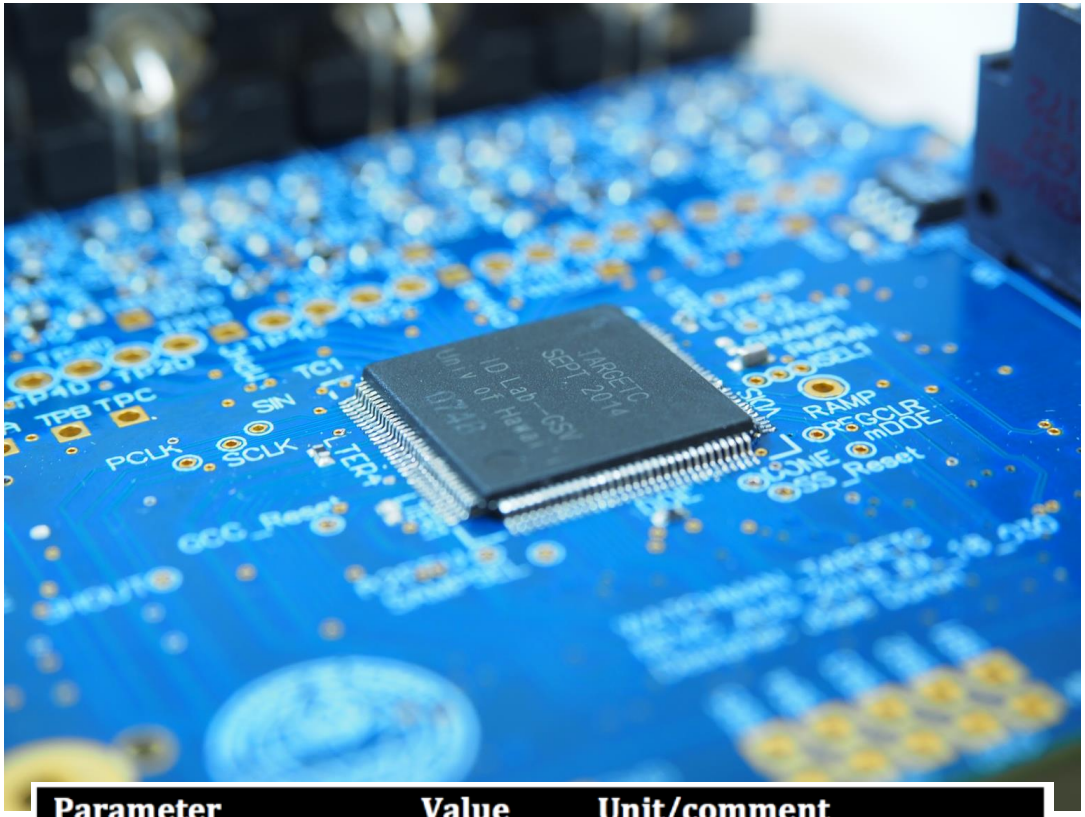
TARGET Readout Status

Jose Duron, Jonathan Hendriks,
Kurtis Nishimura,
Anthony Schluchin, Gary Varner

University of Hawaii

WATCHMAN DAQ Pre-Meeting
January 10, 2019

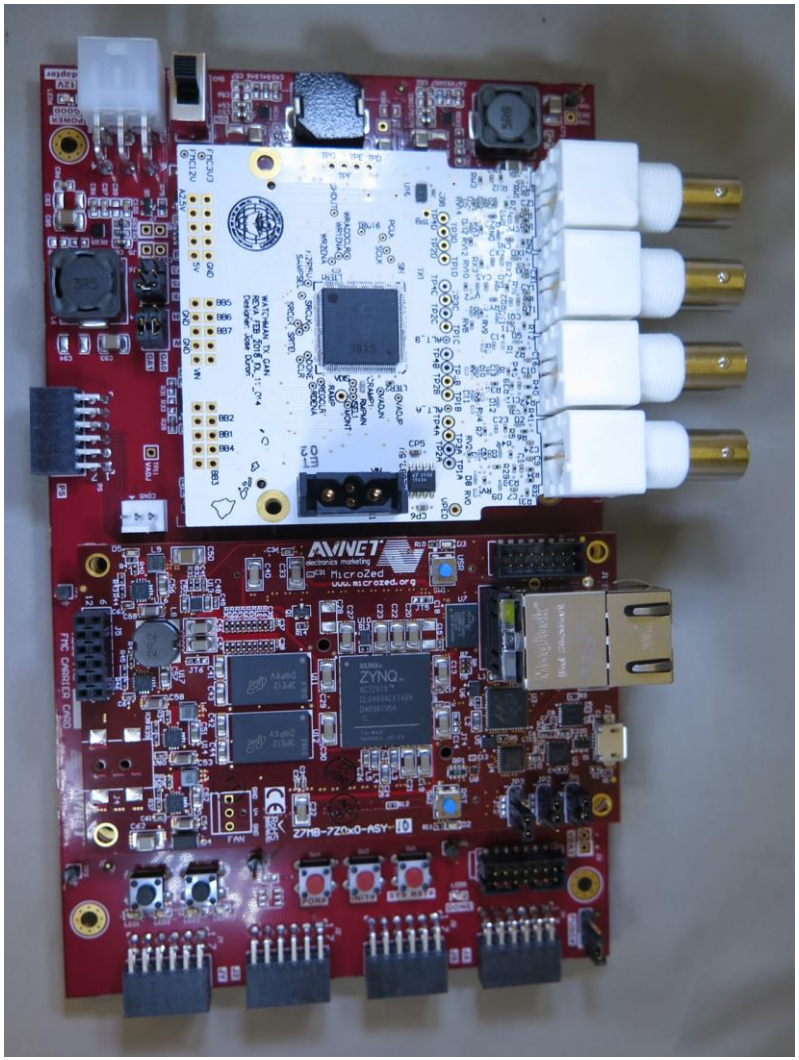
TARGET Introduction/Reminder



Parameter	Value	Unit/comment
Number of channels	16	
Sampling rate	0.4 – 1.2	GSPS
Storage depth	16,384	512 windows of 32 samples
Digitizer	On-chip	Wilkinson
Dynamic range	9-10	bits ENOB
Digitization time	2-8	µs
Trigger output		Varies by ASIC

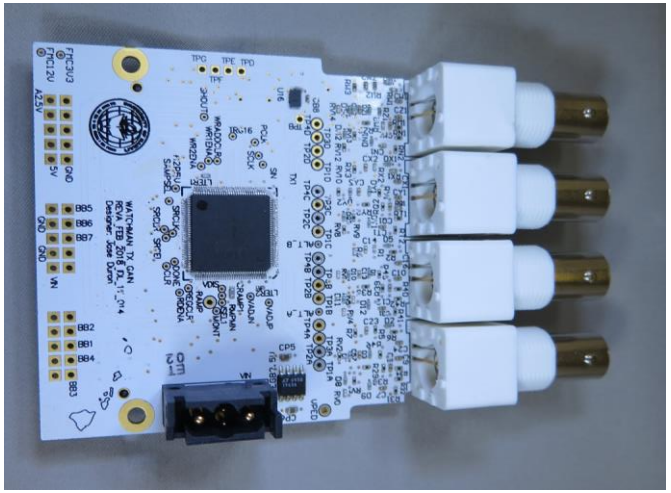
- TARGET series of ASICs are fast (~1 GSPS) waveform samplers developed by G. Varner.
- Switched-capacitor based sampling with deep analog storage.
- Main variants of interest for this talk:
  - TARGETX: >20k channels installed in Belle II.
  - TARGETC: used in Cherenkov Telescope Array.
  - (More on technical differences on next slide.)
- FMC prototype cards for WATCHMAN developed for both of these ASICs…

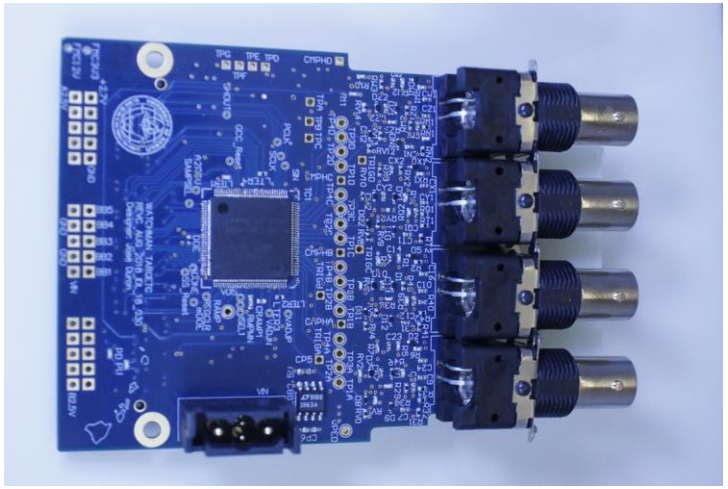
FMC Prototype Cards – Common



- FMC connector to FPGA card.
  - Tested/developed on µZed & Xilinx AC701.
- 4 PMT inputs (BNC).
- 4 gain stages per input:
  - X10
  - X1
  - x1/10
  - x1/100
- TARGET ASIC records waveforms from 16 total channels, on-chip Wilkinson ADC for digitization.
- What's the difference between TARGETX/C?

Two FMC TARGET Cards





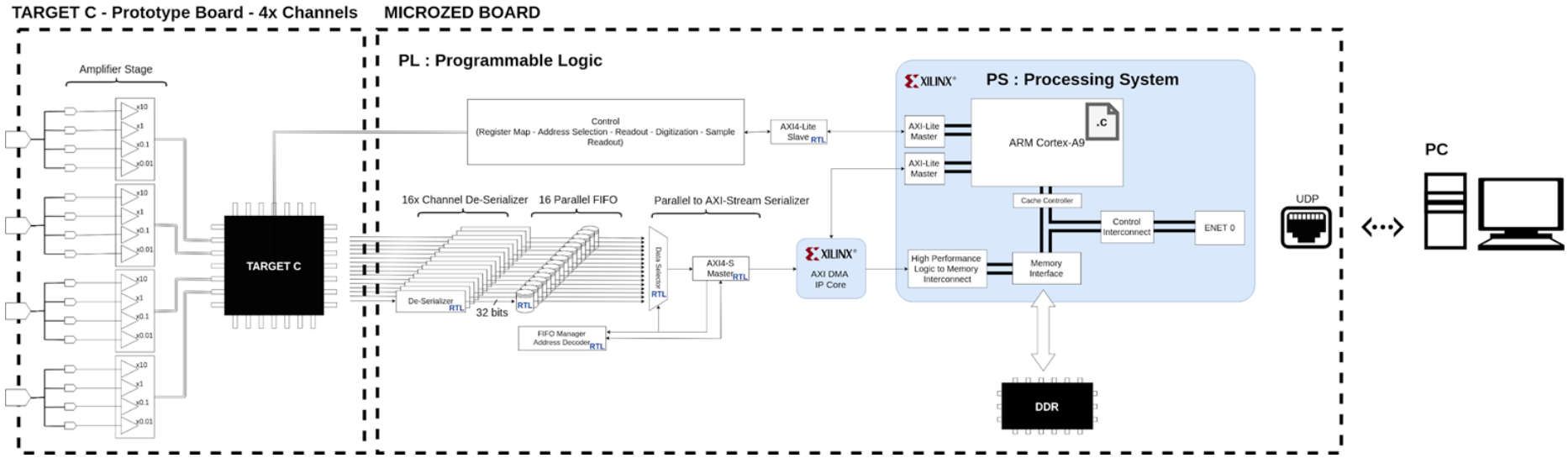
TARGETX Card (first):

- First prototype, based on another similar design.
- TARGETX has internal trigger comparators, so does not require external components for identifying hits...
- …but potentially can miss pulses (only has a “write enable” control to avoid overwriting.

TARGETC Card (present):

- TARGETC has no on-chip comparators…
  - Card uses external comparators (ADCMP601) on 10x gain channels to get maximum sensitivity.
- …but TARGETC has full control over analog memory write addresses, can truly run dead time-less.
- ***Firmware and software development is currently focused on this card.***

TARGETC Firmware & Readout – Data Flow



- Note that Zynq devices are FPGA fabric (PL) coupled with ARM microprocessor (PS).
- Present scheme uses PL for ASIC interfaces & readout.
- PL sends data to PS for processing (pedestal subtraction, feature extraction) and readout.
- PS interfaces to PC (GbE), data path for waveforms, control path for register interfaces.

➔ Development is for FMC prototype, but straightforward scalable to full system.

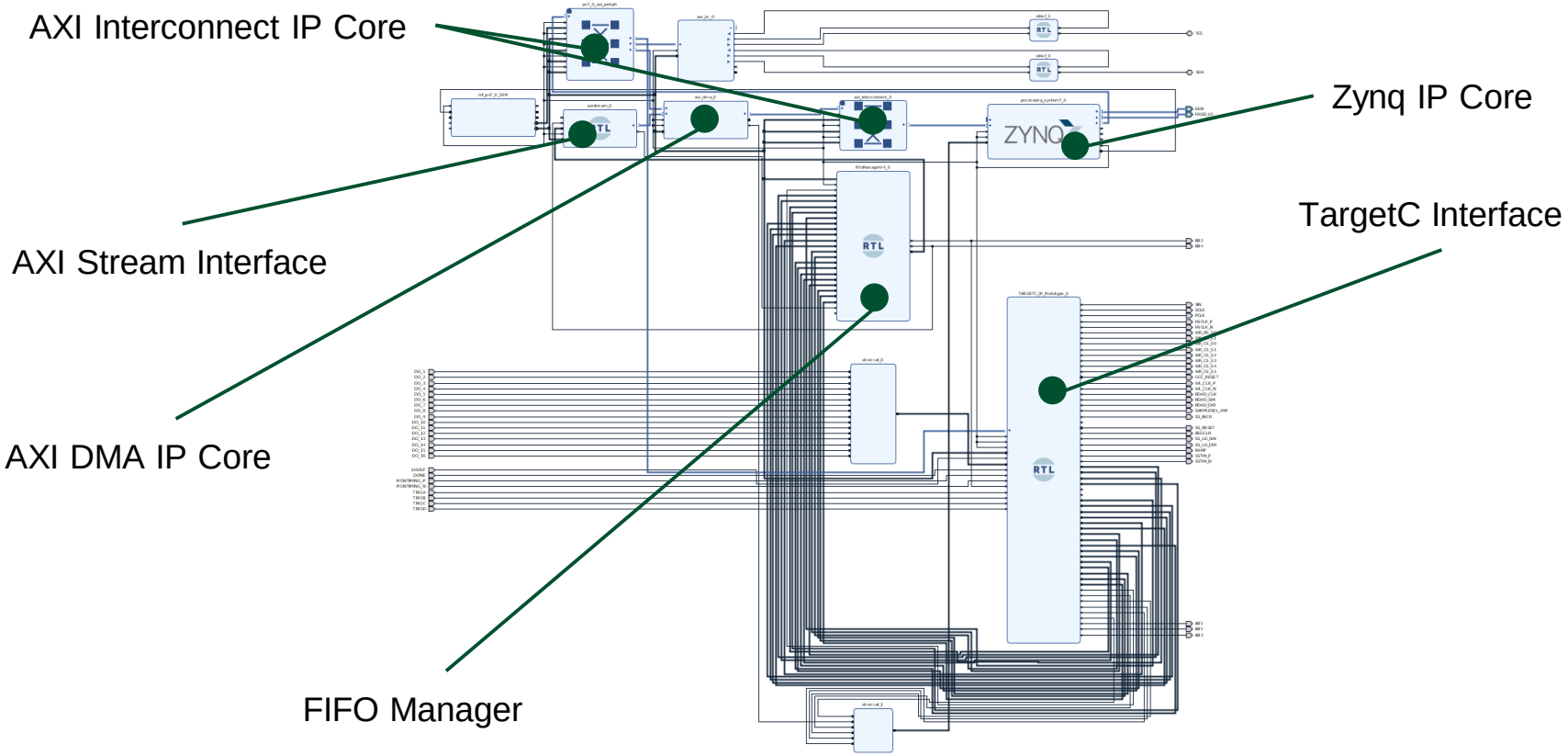
Status of UH TARGET Design, FW & SW

- **Prototype Version - (4x Channels)**
- Prototype design is well understood and is capable to meet the expectations.

- Validated :
  - Target C design.
  - VHDL system description.
  - Ethernet design readout.
  - Python Gui application.

- Ongoing:
  - Optimization of System (Fine tune of parameters of the ASIC).
  - Trigger system Hardware issue (VHDL simulated and validated).
  - Signal processing on full wave after signal compensation.
  - Real test with PMT signals.

Firmware Structure



- Developed using Vivado IP integrator, but important TARGET control blocks are VHDL.
- Project lives in github for version control.

Validation and Verification - Timing/Data Rate (Non-Optimized)

1

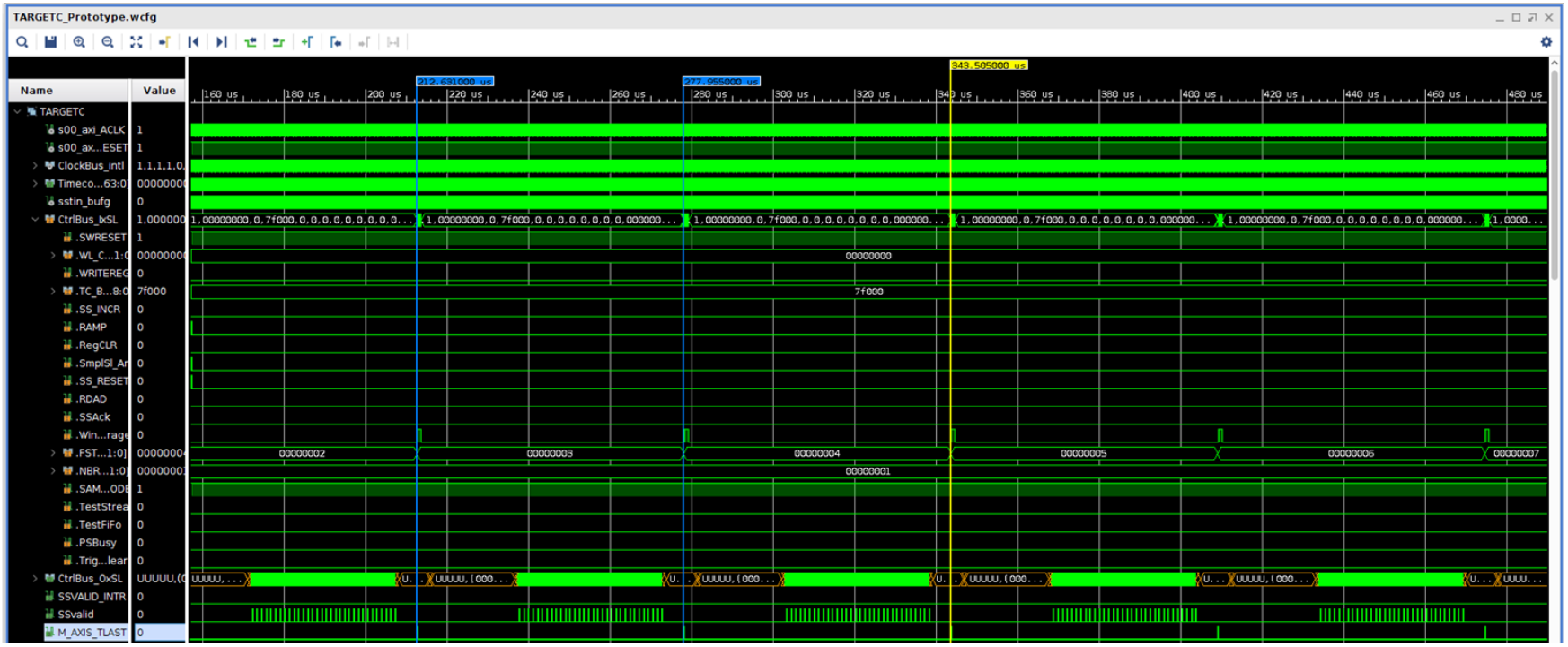
Sampling frequency 1GS/s

If the parameters of TARGET C ASIC are well optimized and calibrated the sampling frequency is up to 1GS/s in accordance with the TARGET Architecture.

Validation and Verification - Timing/Data Rate (Non-Optimized)

2

Readout latency WCS : AVG 65.53 us(sampling till readout 1st window : 32 samples)
Readout frequency : 15kHz



Validation and Verification - Timing/Data Rate (Non-Optimized)

2

Readout latency WCS :	AVG 65.53 us(sampling till readout 1st window : 32 samples)
Readout frequency :	15kHz

Values using non-optimized firmware. Optimization to be done :

- Ramp Charge (~20us overall charge => divide by 4 so 5 us)
  Estimated reduction : **- 15 us**
- Increment Sample (wait ~500 ns for 1 sample increment => 16 us for 32 samples readout, could be reduced probably to 125 ns)
  Estimated reduction : **- 12 us**

Overall reduction : 65us - 15 us - 12 us = 38 us
Frequency : 26 kHz

Validation and Verification - Timing/Data Rate (Non-Optimized)

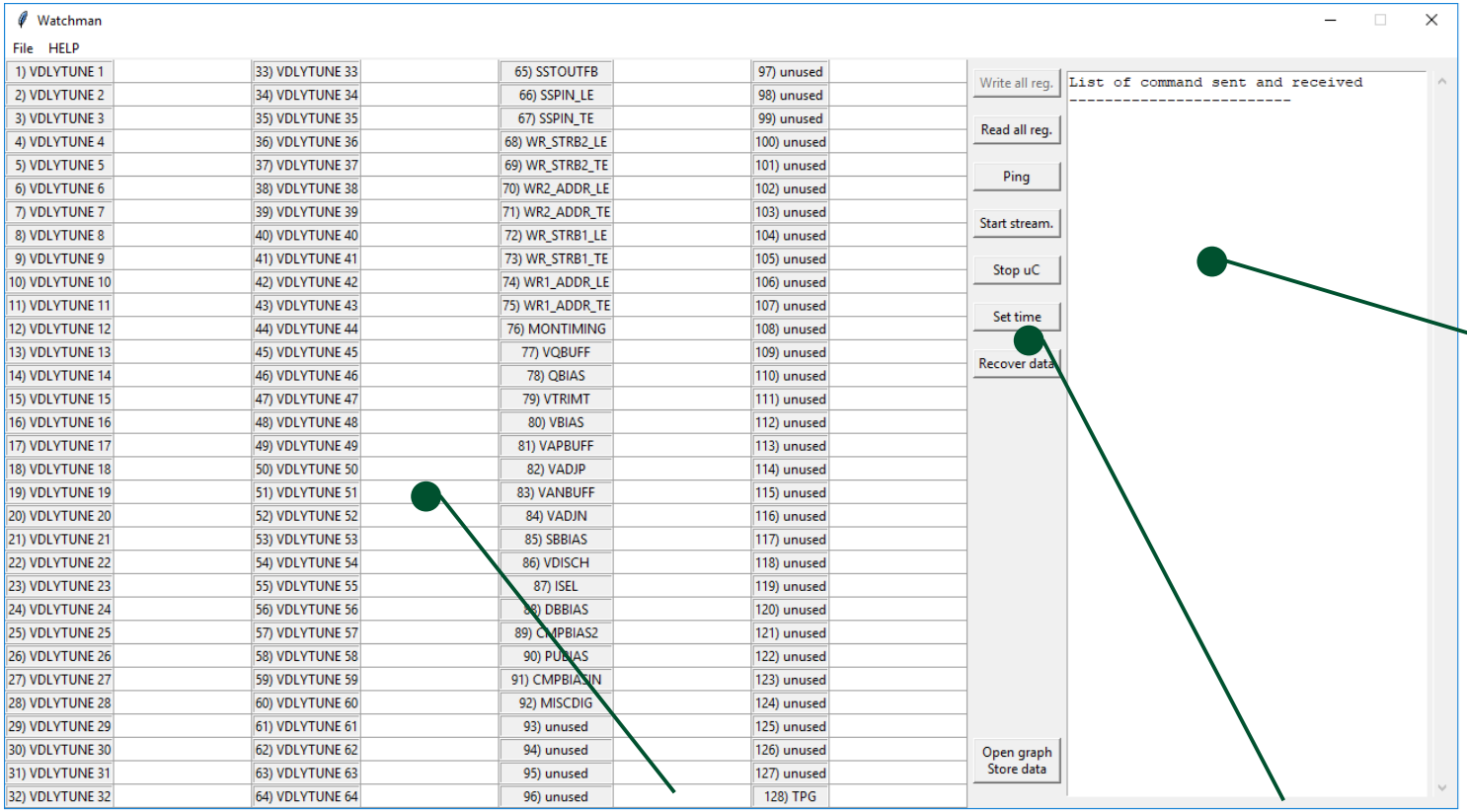
2

Readout latency WCS :	AVG 65.53 us(sampling till readout 1st window : 32 samples)
Readout frequency :	15kHz

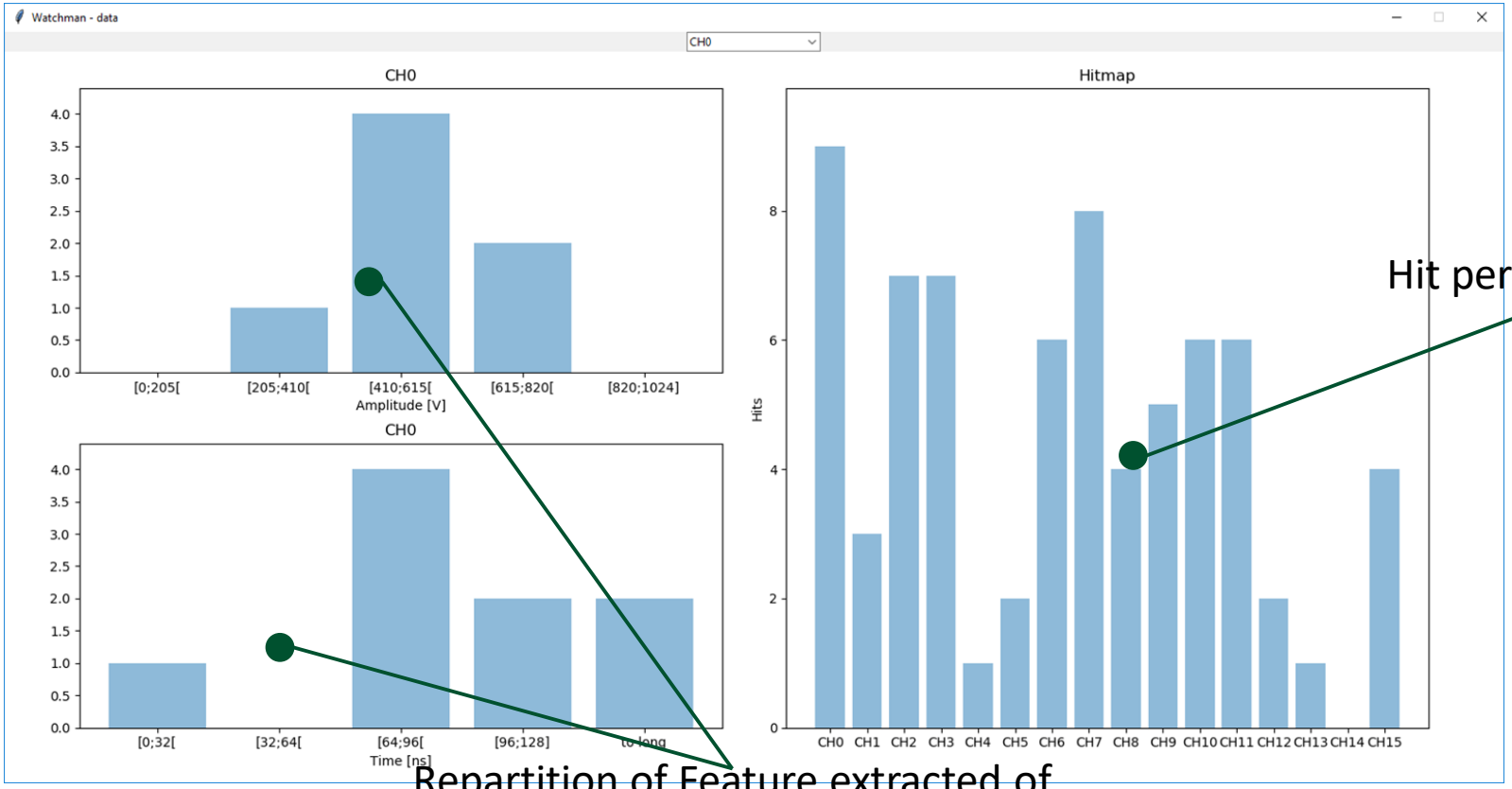
Additional speed-up :

- Frequency increase on the different interfaces of TARGET C
- Data Minimizer send 2x 12bits on a single data of 32bits on AXI stream

Software Development – Python GUI



Software Development – Python GUI

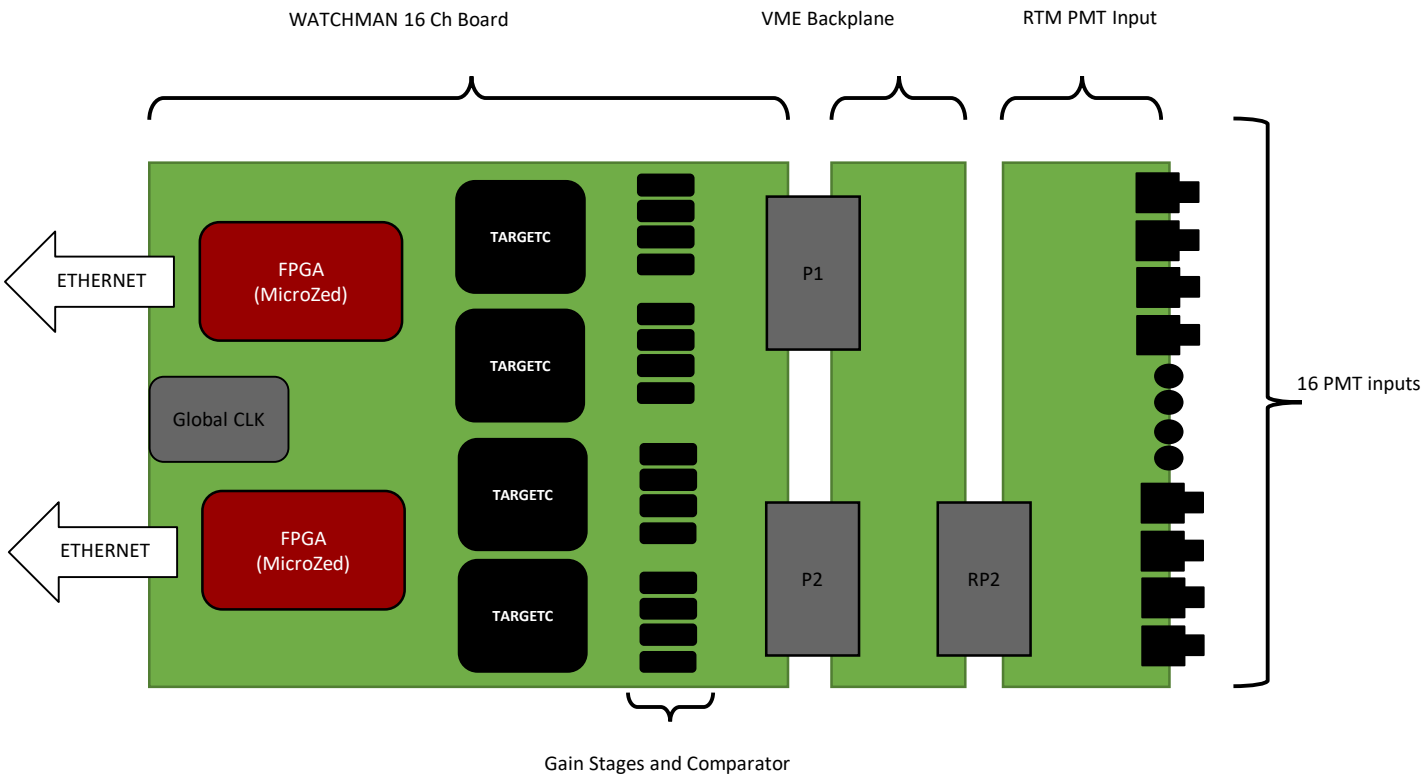


Hit per Channel

Repartition of Feature extracted of Channel 0

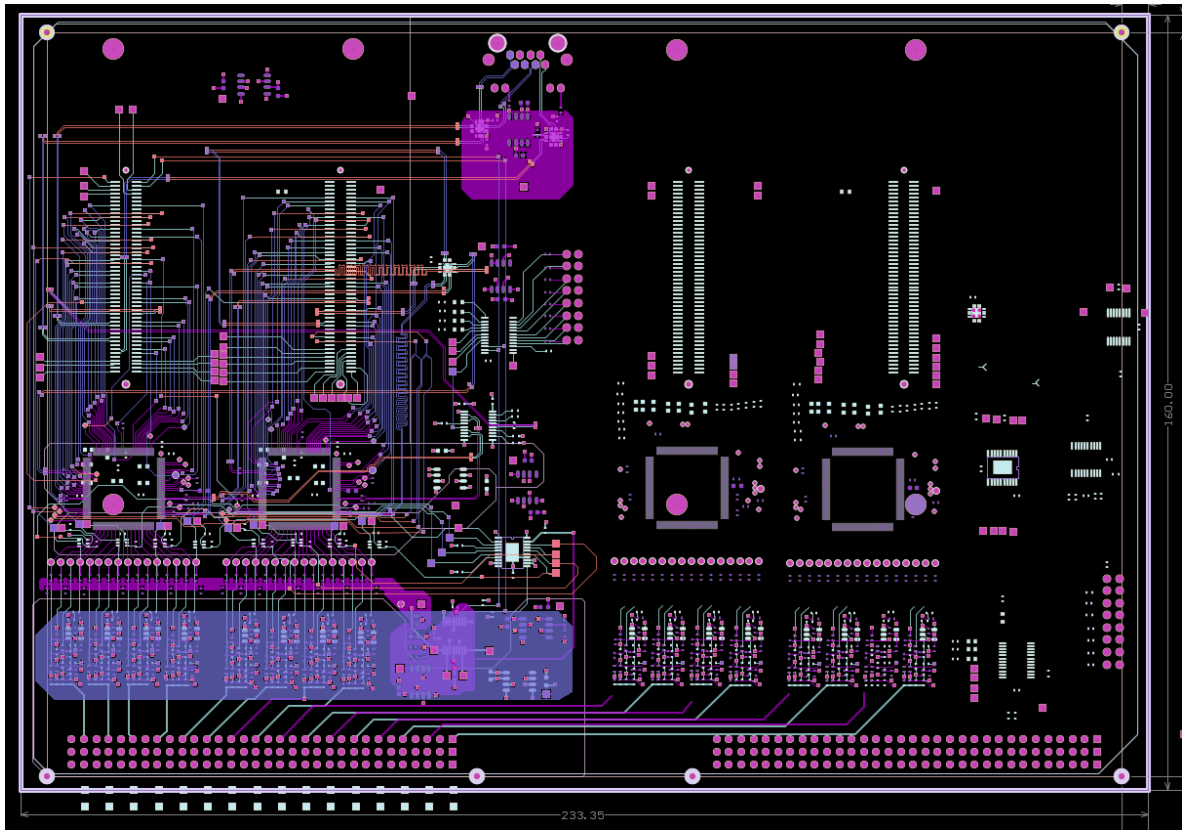
HW Development – Toward 16 Channel VME

16x Channel Version - Conceptual Design



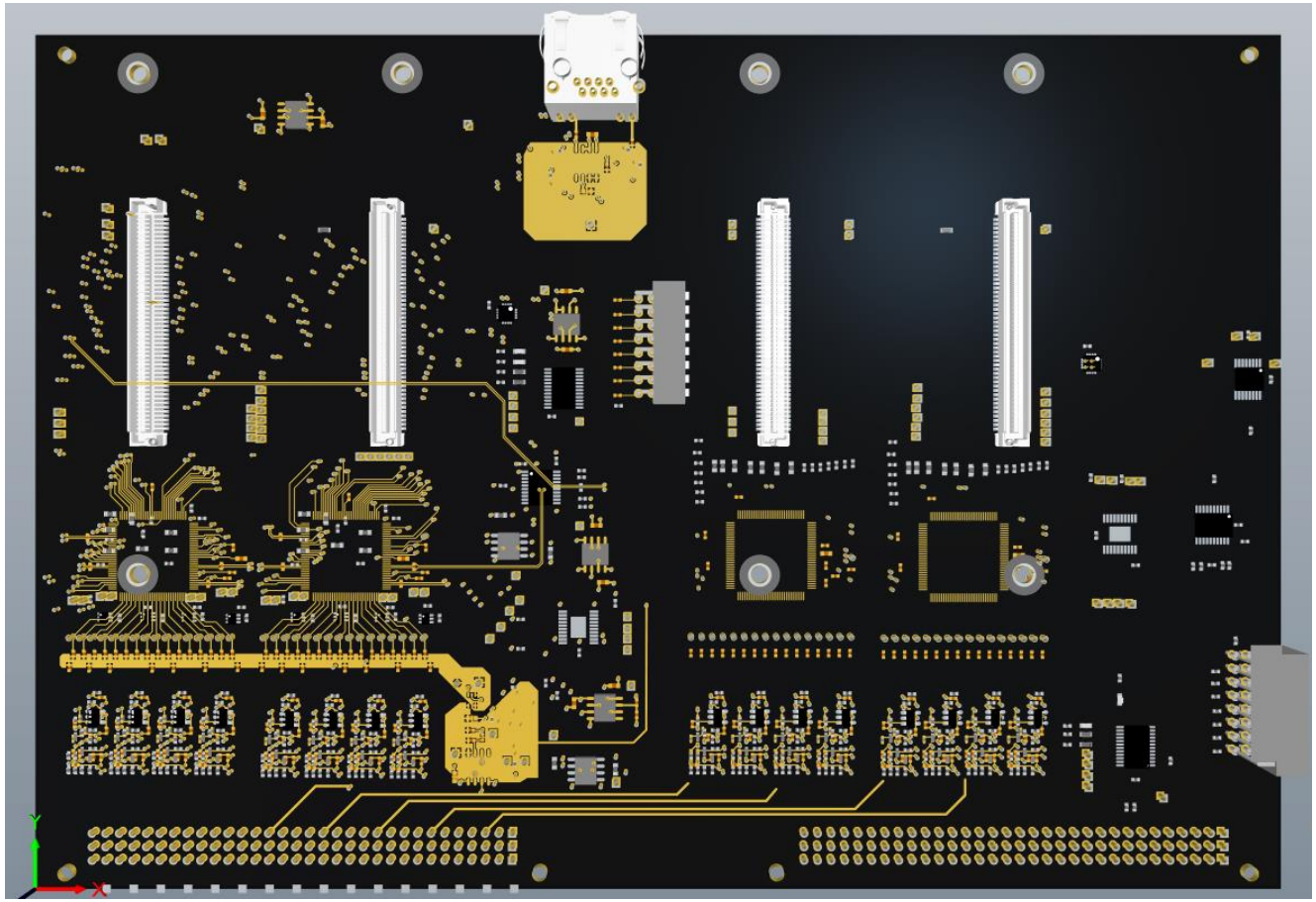
- First VME version uses dual MicroZed boards for rapid development.
  - This version is presently in layout.
- FPGA can be pulled onto board in next revision.

Initial VME Board – Layout in Progress



- Final layout pending some final work on TARGETC FMC prototype:
  - Debugging of trigger comparators, verification of gain stages through full flow.

Initial VME Board – Layout in Progress

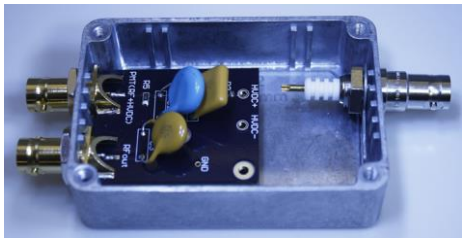


- Final layout pending some final work on TARGETC FMC prototype:
  - Debugging of trigger comparators, verification of gain stages through full flow.

Hardware, Firmware Status

Hardware	Status
TARGET C Prototype Board 4x Channel	ACHIEVED
- Final analog verification (comparators, amplifiers).	1-2 weeks
- Investigate power supply noise.	1 week
Use PMT as test input with HV splitter.	1 week
Complete initial 16 channel TARGET C VME board.	3-4 weeks

Firmware	Status
PL ➔ PS DMA Interface (AxiStream).	ACHIEVED
TARGET C interface & control: - Registers, sample readout, & digitization.	ACHIEVED
Circular buffer – design, simulation with trigger system).	ACHIEVED
Circular buffer – optimization for resource utilization.	1 week
Project cleanup.	1-3 day
System test of trigger & circular buffers.	1-2 week
Adapt firmware to 16 channel VME board.	1-2 week



PMT HV/signal splitter based on UCD schematics

Software & Operations	Status
Initial python GUI.	ACHIEVED
Interrupt systems - timers, watchdogs, data, GbE.	ACHIEVED
UDP communication - commands, data, registers.	ACHIEVED
Timestamping.	ACHIEVED
Log files saved into the SD card.	ACHIEVED
Data processing - pedestals.	ACHIEVED
Data processing – transfer functions.	3 days
Data processing - feature extraction.	ACHIEVED
Optimize TARGET C parameters.	1-2 weeks
Integrated test with PMT.	2 weeks

Current Manpower

Hardware development:

- Jose Duron [Master Student] – graduating spring/summer

Firmware development:

- Jonathan Hendriks [visiting Master's student] – departing February.

Software development:

- Anthony Schluchin [visiting Master's student] – departing February.

Advising/supervising:

- Gary Varner
- Kurtis Nishimura

➔ Searching for ≥50% postdoc to handoff development.
➔ Vasily Shebalin [postdoc] ramping up in a few months.
➔ Jeff Kleyner [EE Ph.D. student] joining later this semester.

Summary and Outlook

- 4-channel TARGETC FMC prototype:
  - Firmware and software development is nearly complete for performance evaluations.
  - Should wrap up this month, cards can then be fully characterized.

- 16-channel VME prototype:
  - Layout underway on a first version, fabrication pending some final debugging and performance checks on FMC card.
  - Firmware for this version should be straightforward adaptation of FMC prototypes.
  - A second streamlined version is envisioned shortly after.

- Personnel changes:
  - A number of these coming in the next months.
  - Working to ensure smooth transition, sufficient coverage for work through downselect – V. Shebalin [Postdoc], J. Kleyner [EE Grad].

BACKUP

Feature Extraction

- **Example from another Zynq system (Belle II TOP):**

- Rough benchmarking: 3.6 µsec to process each pair of hits using 1 core of ARM PS.
  - 1.5 µsec for pedestal subtraction, 2.1 µsec for feature extraction.
  - Corresponds to ~550 kHz hits processed.
  - Not very optimized, may be able to speed up FE code in the PS, or can move some of it to PL.

- Roughly consistent with initial results seen on TARGETX w/ µZed.