



TARGETC - DataSheet

at the University of Hawaii

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Abbreviation

Term	Description
PL	Programmable Logic



Contents

1	Introduction	5
2	Overall Architecture	6
3	New Features	12
3.1	External Trigger	12
3.2	External Storage Control	12
4	Register Map	13
4.1	Time Register	14
4.2	Vramp Registers	17
4.3	Comparator Parameters	20
5	Pinout	22
5.1	Register Write Interface	26
5.2	Delay Lock Loop	28
5.3	Storage Control	28
5.4	Window Readout	30
5.5	Wilkinson Digitization	32
5.6	Sample Readout	33





1 Introduction

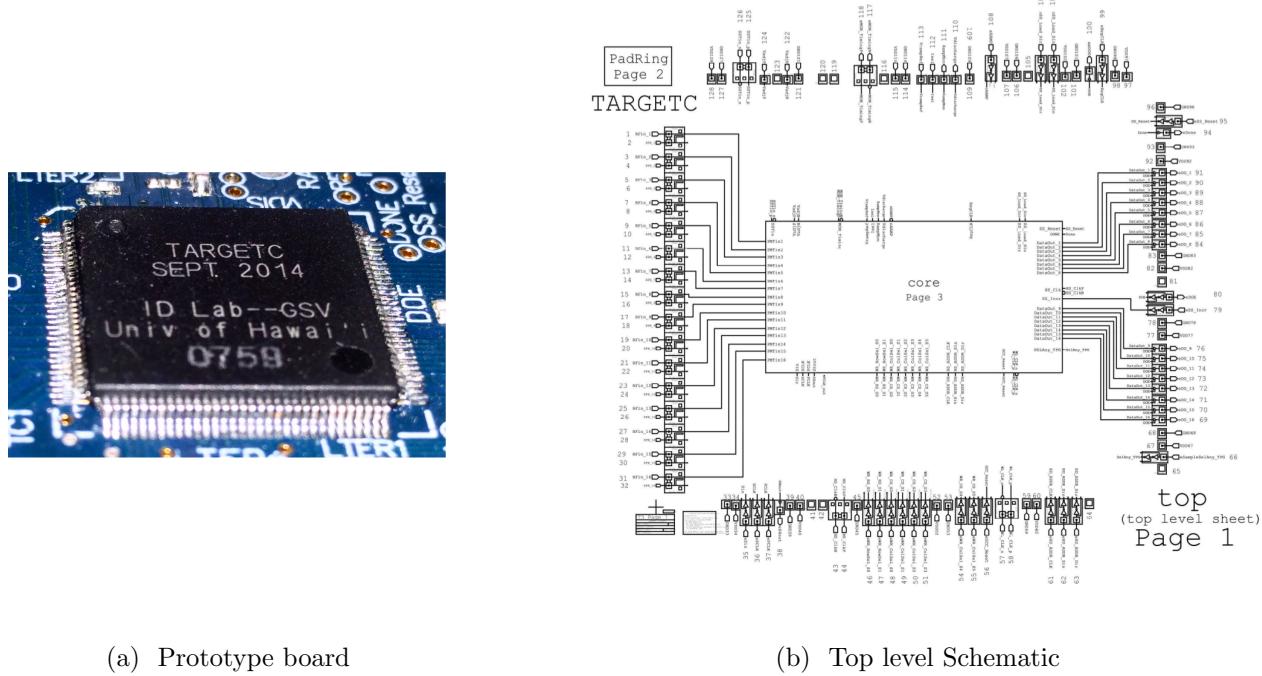


Figure 1: TARGETC

TARGET C is a new application-specific integrated circuit (ASIC) of the TARGET family, which stands for TeV Array Readout Gigasample-per-second Electronics without Trigger (TARGET). This circuit is designed by Dr. Gary Varner at the University of Manoa Hawai'i. This ASIC is designed for the readout of signals from photosensors in the cameras of imaging atmospheric Cherenkov telescopes (IACTs) for ground-based gamma-ray astronomy. The TARGET family is composed of :

- TARGET 5
- TARGET 7
- TARGET X
- TARGET C

The main difference from the TARGETX to C is the control over storage cells and the triggering system, these details are explained later in this document.

2 Overall Architecture

The TARGETC can sample 2×32 samples $\times 16$ channels at once. To do so a capacitor array composed of 64 sampling capacitors (SaC0 to SaC63) which are charged by a switch command signal generated by the SSTIN provided by the FPGA and SSPIN clock internally generated, see figure 2. For simplicity, this illustration only shows the channel RFIN_1 but there is 16 of them in parallel, consequently all sampling on the 16 channels is done at the same time. The sampling frequency depends on the SSTIN signal, generally the clock period is set to 64 ns. Each switch command is delayed by 1ns, but the width of the pulse is larger than 1ns giving the time for the capacitor to charge up. The delay circuit is composed of two inverters, one fixed delay and the other is adjustable (coarse and fine tune). Adjustment value is determined by a DLL (Delay Lock Loop) or can be written in a register. The signal SW0 is formed by logic combination of the superposition of two clocks and is enabled 1ns earlier than SW1 signal and 2ns earlier than SW2 signal, see figure 3. Assuming that each capacitor is switched ON and OFF at 1ns of interval, the input signal is sampled at a frequency of 1 Giga-Sample per second (1GS/s).

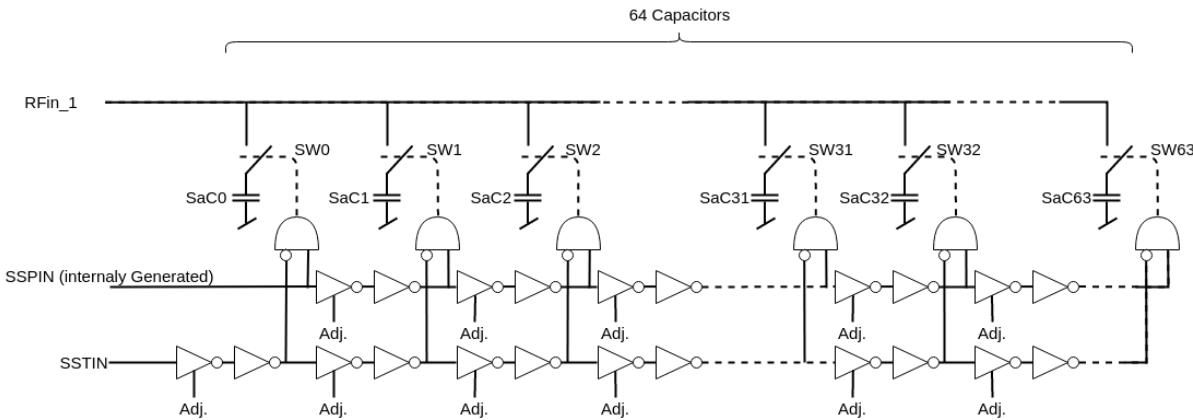


Figure 2: Capacitor array for sampling analog input

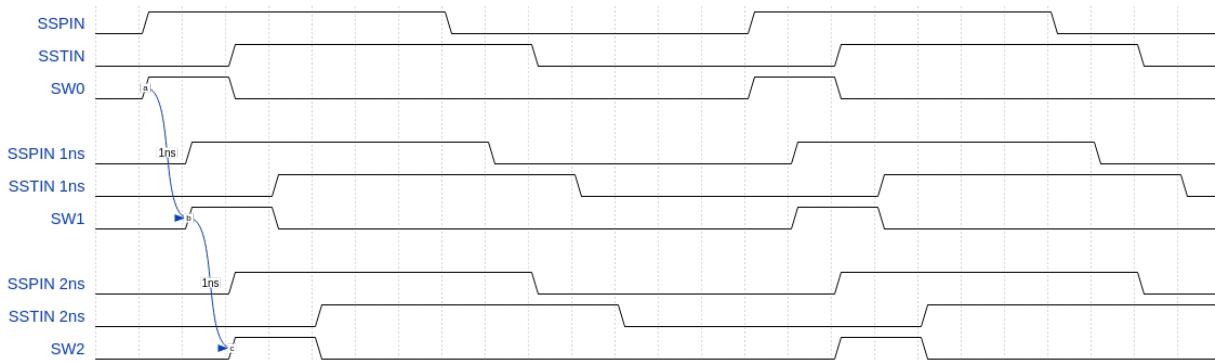


Figure 3: Switch command Pulse Generator for 1ns delay between samples

The storage address is commanded by the FPGA side using the ASIC input pins, WR_COL_SEL(5:0) and WR_ROW_SEL(1:0). The storage location is formed of capacitors (StC0 to StC63). The



location addressed is latched onto the internal address bus by a write address sync (internal signal). Once the address is stable inside the ASIC, a second internal signal is enabled (write strobe). This signal switches ON and OFF the transmission lines to store the analog value from SaC0-SaC63 into the storage cells StC0-StC63. The 64 samples are stored in two different parts of the analog memory. The ASIC separates the 64 samples into 2 windows of 32 samples (EVEN and ODD part). The LSB bit for row selection is this EVEN and ODD window select. The total analog memory is 32 samples x 8 rows x 64 columns = 16K samples. The FPGA must keep track which part of memory is occupied and which is free. This write command is done in parallel for the 16 channels of the TARGETC.

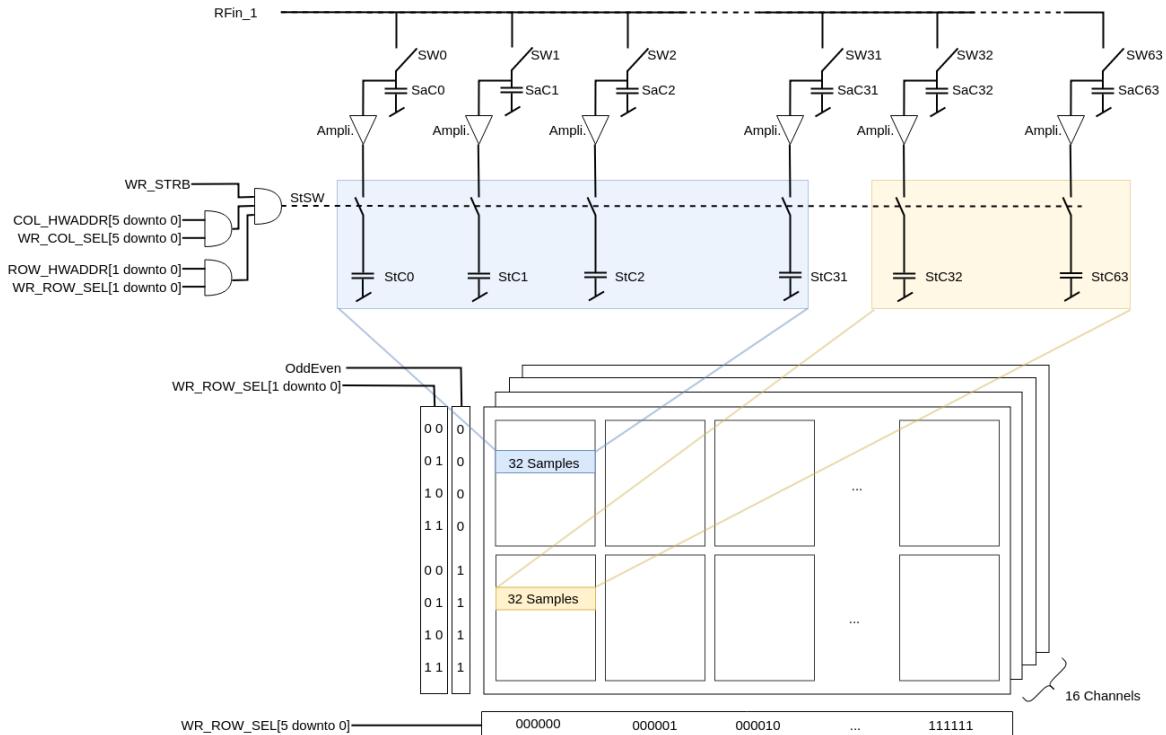


Figure 4: Analog storage area of 16K cells per channel

The digitalization is performed in parallel for the 32 samples per channel. It is triggered by sending the address through a serial communication (RDAD_clk, RDAD_sin and RDAD_dir). The address is decoded and triggers a read command which turns on the Wilkinson comparators of the memory location (normally off for power consumption).

The Wilkinson ramp is started by enabling the ramp signal. The ramp parameters are defined by a simple linear function $y = a * x + b$. The argument a is the slope of the ramp commanded by the ISEL register. The second argument b is defining the offset voltage of the function, this offset is the voltage discharge of the wilkinson capacity defined by a register VDISH. The Wilkinson ADC compares the voltage of a capacitor to a digital counter, when the comparison is equal the analog value is represented by the digital value inside the counter. Therefore the frequency at which this counter is increment must be linked to charge speed of the capacitor. So the Wilkinson clock period multiplied by the counter's length defines the total time of charge. The gray code is used for changing only 1 bit at the time and avoiding dangerous transition levels and meta-stabilities, like

for example the transition from 127 to 128 (0111111_2 to 10000000_2).

The figure 5 shows the different actors for varying the charge parameters of the capacitor.

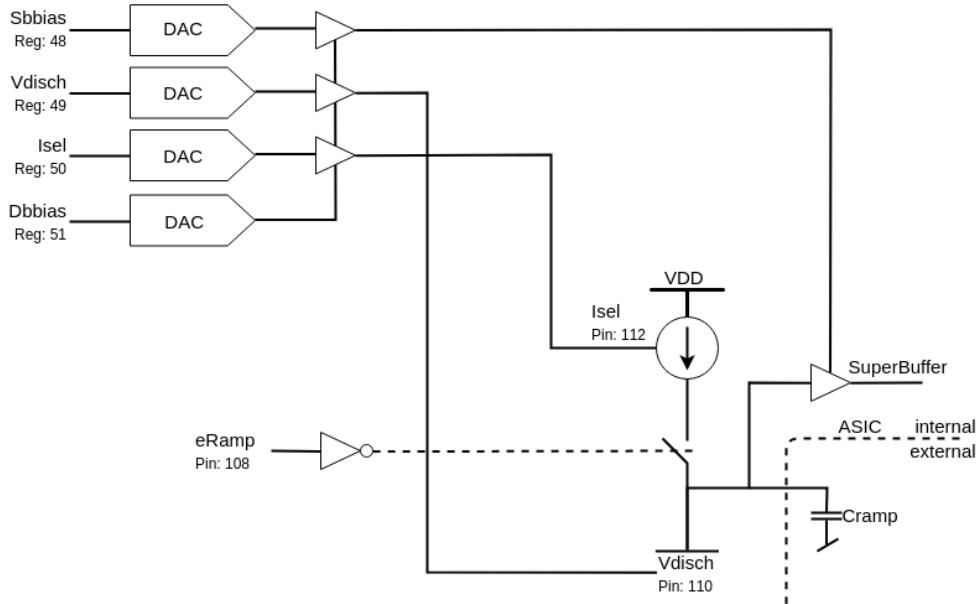


Figure 5: Principle scheme for Vramp

Once the voltage of the charge capacitor is above the storage cell voltage, the comparator switches from LOW to HIGH. This transaction latches the content of the Gray counter into a sample register. This digital value is the representation of the analog value in memory. The digitization process is finished. The eDONE signal is pulled high when all conversions are over. To put in another way, all comparators have switched from LOW to HIGH, when the 32 samples of each 16 channels are digitized. Only then is the eDONE signal pulled HIGH, see Figure 6.

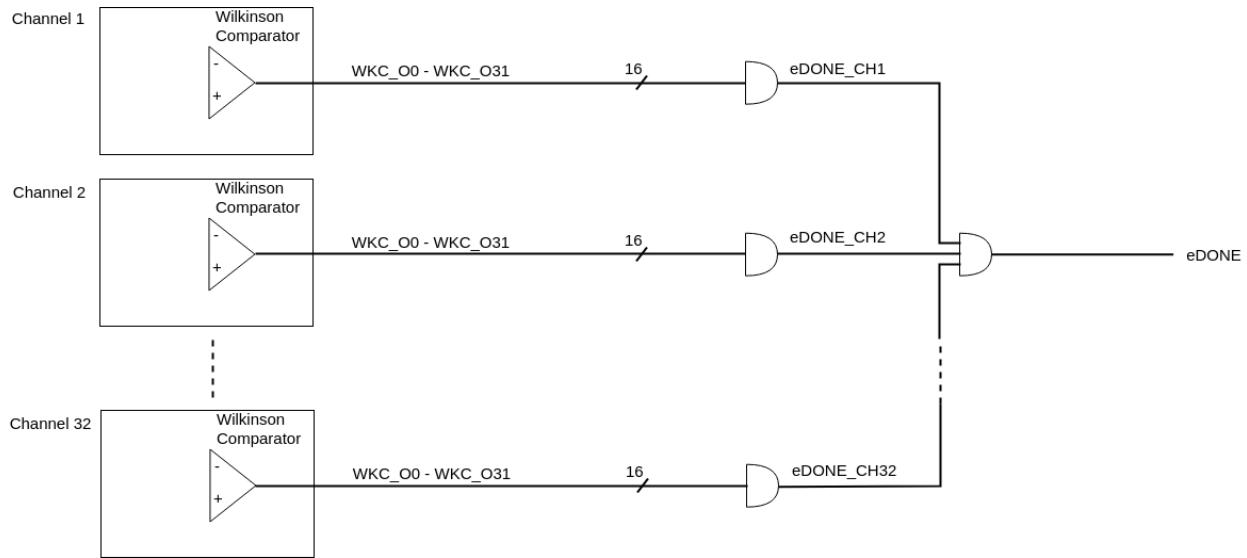


Figure 6: Logic circuit for **eDONE** signal

All samples of the 16 channels are serialized on the Data output pins DO0 to DO15. The **SS_INCR** signal pulled HIGH loads a sample register onto the data line, on the HIGH to LOW transition the data line is latched into the shift register. This generated pulse on **SS_INCR** will also increase the sample counter, on the next HIGH transition the next sample will be loaded and so on.

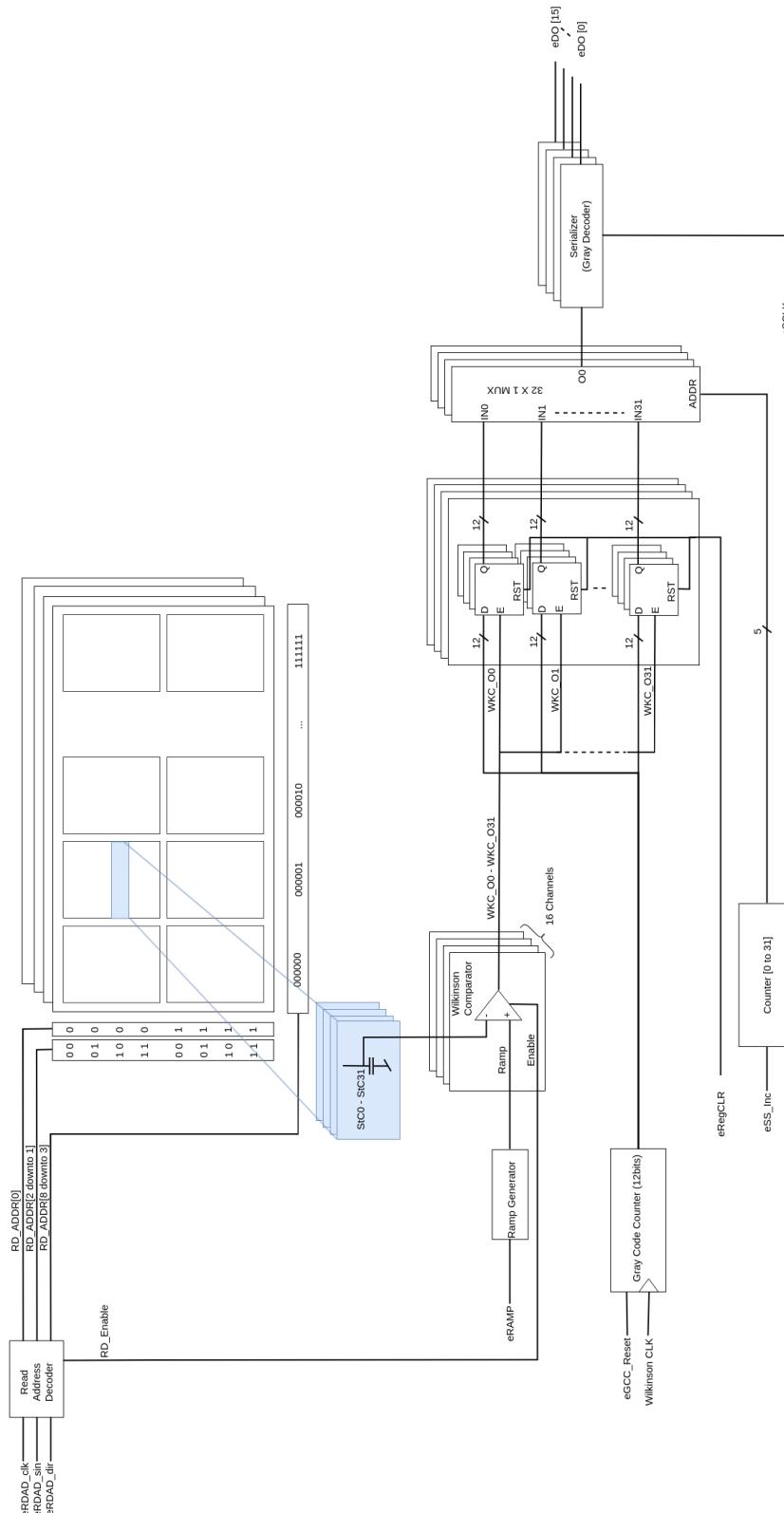


Figure 7: Full Readout and Digitalization

The ASIC has a built-in Delay Lock Loop, that once enabled and stable, will adjust the timing to temperature fluctuation. The figure 8 illustrates the DLL's different parameters.

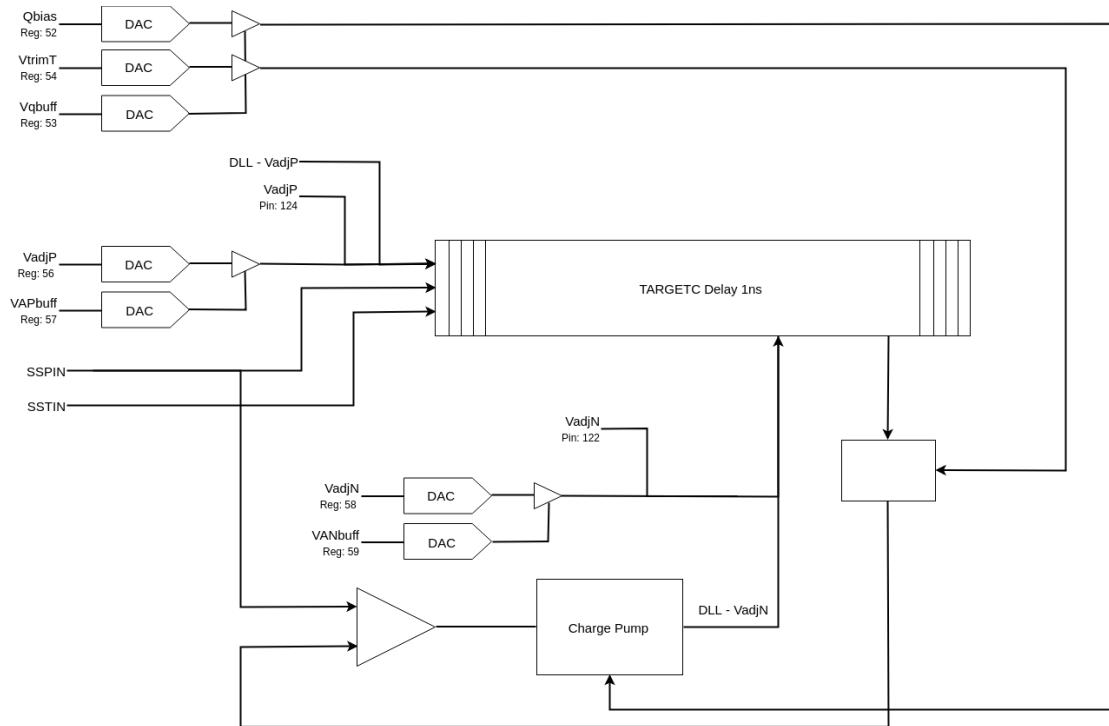


Figure 8: Principle scheme for DLL

3 New Features

3.1 External Trigger

The first difference from previous design like TARGETX, which is used in Belle II detector (over 20k channels), is the triggering system. On the TARGET X, the trigger circuit is internally managed and has the capabilities to trigger on any of the 16 channels. In TARGETC design the trigger system is removed, which means that the full control comes back to the FPGA or the interfacing device. As a consequence, the WATCHMAN TARGETC prototype board uses four operational amplifiers used as comparators. Four independent and adjustable threshold voltages are compared the highest gain lines ($x10$), which are Channel input 3, 7, 11 and 15 (see figure 9).

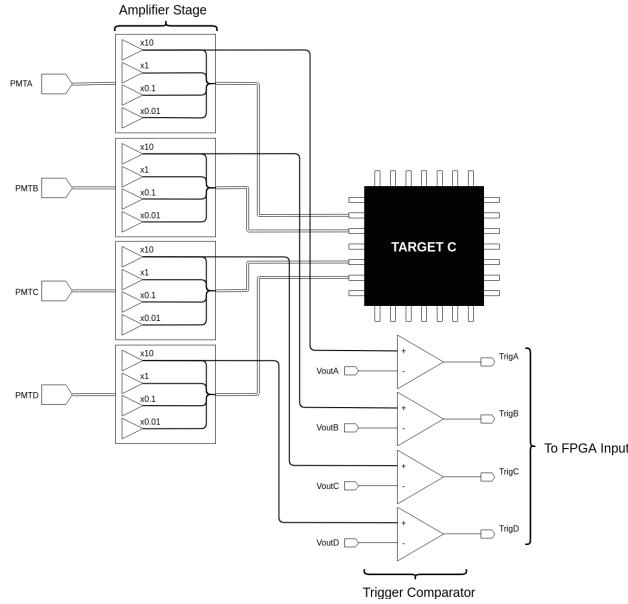


Figure 9: Principle scheme for External Trigger Circuit on the TARGET C Prototype

3.2 External Storage Control

The second difference from previous designs is the control over the analog memory storage. Earlier versions used an internal counter with a write enable, the parameter was turned OFF if the cell was not to be re-written. Unfortunately this also means that the data at that exact moment is not written in any memory or anywhere else, it is simply lost. In order to avoid this issue, the control circuit is brought out of the TARGET and left to the user to implement any algorithm to deal with storage control.



4 Register Map

Table 1: TARGETC Register Map

Reg #	Reg Name	Description/Comment
1 .. 64	VdlyTune	Delay samples 1 - 64 Default to zero (max on)
65	SSToutFB	Timebase 8 bit time
66	SSPin LE	Timebase 8 bit time
67	SSPin TE	Timebase 8 bit time
68	WR_STRB2 LE	Timebase 8 bit time
69	WR_STRB2 TE	Timebase 8 bit time
70	WR_ADDR_Incr2 LE	Timebase 8 bit time
71	WR_ADDR_Incr2 TE	Timebase 8 bit time
72	WR_STRB1 LE	Timebase 8 bit time
73	WR_STRB1 TE	Timebase 8 bit time
74	WR_ADDR_Incr1 LE	Timebase 8 bit time
75	WR_ADDR_Incr1 TE	Timebase 8 bit time
76	MonTiming SEL	Timebase
77	Vqbuff	PLL
78	Qbias	PLL Vqbuff
79	VtrimT	PLL Vqbuff
80	Vbias	sampling Vqbuff
81	VAPbuff	Timebase
82	VadjP	Timebase VAPbuff
83	VANbuff	Timebase
84	VadjN	Timebase VANbuff
85	Sbbias	Vramp Dbbias
86	Vdisch	Vramp Dbbias
87	Isel	Vramp Dbbias
88	Dbbias	Vramp
89	CMPbias2	Wilk Sbbias
90	Pubias	Wilk Sbbias
91	CMPbias	Wilk Sbbias
92	Misc Digital Reg	5-bit == at right
93 .. 127	(Unused)	
128	TPGreg	12 bit pattern



4.1 Time Register

Reg 1-64 - VdTrim1-64 - 0x01-0x40

Bits	Function	R/W	Default
11 - 0	Voltage adjust for each delay cell (Fine Tune)	W	0

Table 2: Reg 1-64 - VdTrim1-64 - 0x01-0x40

Reg 65 - SSToutFB - 0x41

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 3: Reg 65 - SSToutFB - 0x41

Reg 66 - SSPIN LE - 0x42

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Leading Edge of SSPIN signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 4: Reg 66 - SSPIN LE - 0x42

Reg 67 - SSPIN TE - 0x43

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Trailing Edge of SSPIN signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 5: Reg 67 - SSPIN TE - 0x43



Reg 68 - WR_STRB2 LE - 0x44

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Leading Edge of Write Strobe 2 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 6: Reg 68 - WR_STRB2 LE - 0x44

Reg 69 - WR_STRB2 TE - 0x45

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Trailing Edge of Write Strobe 2 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 7: Reg 69 - WR_STRB2 TE - 0x45

Reg 70 - WR2_ADDR_INCR LE - 0x46

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Leading Edge of Write Address 2 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 8: Reg 70 - WR2_ADDR_INCR LE - 0x46

Reg 71 - WR2_ADDR_INCR TE - 0x47

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Trailing Edge of Write Address 2 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 9: Reg 71 - WR2_ADDR_INCR TE - 0x47

**Reg 72 - WR_STRB1 LE - 0x48**

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Leading Edge of Write Strobe 1 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 10: Reg 72 - WR_STRB1 LE - 0x48

Reg 73 - WR_STRB1 TE - 0x49

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Trailing Edge of Write Strobe 1 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 11: Reg 73 - WR_STRB1 TE - 0x49

Reg 74 - WR1_ADDR_INCR LE - 0x4A

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Leading Edge of Write Address 1 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 12: Reg 74 - WR1_ADDR_INCR LE - 0x4A

Reg 75 - WR1_ADDR_INCR TE - 0x4B

Bits	Function	R/W	Default
11 - 6	(unused)	-	-
5 - 0	Trailing Edge of Write Address 1 signal, Pulse selection from the TC_dly64 (Delay chain)	W	0

Table 13: Reg 75 - WR1_ADDR_INCR TE - 0x4B



Reg 76 - MonTiming - 0x4C

Bits	Function	R/W	Default
11 - 8	(unused)	-	-
7 - 4	Monitor Timing selection on MonTiming LVDS output 0000 ₂ : SSPout 0001 ₂ : SSTout 0010 ₂ : SSToutFB 0011 ₂ : SSPIN 0100 ₂ : WR_STRB1 0101 ₂ : WR1_ADDR_INCR 0110 ₂ : WR_STRB2 0111 ₂ : WR2_ADDR_INCR 1xxx ₂ : VDD (Tied to power supply)	W	0000 ₂
3	(unused)	-	-
2	Cload is for adding an additional capacitor for low pass filter	W	0
1 - 0	(unused)	-	-

Table 14: Reg 76 - MonTiming - 0x4C

4.2 Vramp Registers

Reg 77 - VQbuff - 0x4D

Bits	Function	R/W	Default
11 - 0	Voltage bias for Register (Disable=0) : - Reg 78 - Qbias - 0x4E - Reg 79 - VtrimT - 0x4F - Reg 80 - Vbias - 0x50	W	0

Table 15: Reg 77 - VQbuff - 0x4D

Reg 78 - Qbias - 0x4E

Bits	Function	R/W	Default
11 - 0	Voltage bias for the DLL	W	0

Table 16: Reg 78 - Qbias - 0x4E

**Reg 79 - VtrimT - 0x4F**

Bits	Function	R/W	Default
11 - 0	Voltage parameter for fine tune of SSToutFB signal	W	0

Table 17: Reg 79 - VtrimT - 0x4F

Reg 80 - Vbias - 0x50

Bits	Function	R/W	Default
11 - 0	Voltage parameter for a global fine tune of Vdly1 to Vdly64 voltages from Reg1 to Reg64	W	0

Table 18: Reg 80 - Vbias - 0x50

Reg 81 - VAPbuff - 0x51

Bits	Function	R/W	Default
11 - 0	Voltage bias for Register (Disable=0) : - Reg 82 - VadjP- 0x52	W	0

Table 19: Reg 81 - VAPbuff - 0x51

Reg 82 - VadjP - 0x52

Bits	Function	R/W	Default
11 - 0	Voltage for the DLL	W	0

Table 20: Reg 82 - VadjP - 0x52

Reg 83 - VANbuff - 0x53

Bits	Function	R/W	Default
11 - 0	Voltage bias for Register (Disable=0) : - Reg 84 - VadjN- 0x54	W	0

Table 21: Reg 83 - VANbuff - 0x53



Reg 84 - VadjN - 0x54

Bits	Function	R/W	Default
11 - 0	Voltage for the DLL	W	0

Table 22: Reg 84 - VadjN - 0x54

Reg 85 - SSBias - 0x85

Bits	Function	R/W	Default
11 - 0	Voltage bias for Register and SuperBuffer :	W	0

Table 23: Reg 85 - SSBias - 0x85

Reg 86 - VDisch - 0x86

Bits	Function	R/W	Default
11 - 0	Voltage discharge value for the Ramp Capacitor for the Wilkinson Comparator :	W	0

Table 24: Reg 86 - VDisch - 0x86

Reg 87 - Isel - 0x87

Bits	Function	R/W	Default
11 - 0	Parameter for slope selection, therefore charging slower or faster the capacitor	W	0

Table 25: Reg 86 - VDisch - 0x86

**Reg 88 - DDBias - 0x88**

Bits	Function	R/W	Default
11 - 0	Voltage bias for Register (Disable=0) : - Reg 85 - SSBias - 0x85 - Reg 86 - VDisch - 0x86 - Reg 87 - Isel - 0x87	W	0

Table 26: Reg 88 - DDBias - 0x88

4.3 Comparator Parameters**Reg 89 - CMPBias2 - 0x89**

Bits	Function	R/W	Default
11 - 0	Second Stage Mosfet for voltage level	W	0

Table 27: Reg 89 - CMPBias2 - 0x89

Reg 90 - PUBias - 0x8A

Bits	Function	R/W	Default
11 - 0	Current selection for the Mosfet acting like Pull-Up Resistor	W	0

Table 28: Reg 90 - PUBias - 0x8A

Reg 91 - CMPbias - 0x8B

Bits	Function	R/W	Default
11 - 0	Current source for the Wilkinson Comparator	W	0

Table 29: Reg 91 - CMPbias - 0x8B



Reg 92 - MiscDig - 0x8C

Bits	Function	R/W	Default
11 - 5	(unused)	-	-
4 - 3	SHout Selection	W	00 ₂
	0x ₂ : SHout Data		
	10 ₂ : RD_SHout		
	11 ₂ : SS_SHout		
2	nWR2_Enable, Global write enable for second 32 samples, enable at 0 (Low value)	W	0
1	nWR1_Enable, Global write enable for first 32 samples, enable at 0 (Low value)	W	0
0	nRD_Enable, Global read enable for digitization of samples, enable at 0 (Low value)	W	0

Table 30: Reg 92 - MiscDig - 0x8C

Reg 128 - TPG - 0x100

Bits	Function	R/W	Default
11 - 0	Test Pattern, if enabled data output will be the test pattern	-	-

Table 31: Reg 128 - TPG - 0x100



5 Pinout

Pinout Legend

	VDD : Power Supply		GND : Ground
	ASIC Digital Input		ASIC Digital Output
	ASIC LVDS Input		ASIC LVDS Output

Table 32: TARGETC Pinout

Pin#	Pin Name	Description	Comment
1	RFIn_1	PMT input Ch. 1	
2	RFN_1	Termination ref input Ch. 1	
3	RFIn_2	PMT input Ch. 2	
4	RFN_2	Termination ref input Ch. 2	
5	RFIn_3	PMT input Ch. 3	
6	RFN_3	Termination ref input Ch. 3	
7	RFIn_4	PMT input Ch. 4	
8	RFN_4	Termination ref input Ch. 4	
9	RFIn_5	PMT input Ch. 5	
10	RFN_5	Termination ref input Ch. 5	
11	RFIn_6	PMT input Ch. 6	
12	RFN_6	Termination ref input Ch. 6	
13	RFIn_7	PMT input Ch. 7	
14	RFN_7	Termination ref input Ch. 7	
15	RFIn_8	PMT input Ch. 8	
16	RFN_8	Termination ref input Ch. 8	
17	RFIn_9	PMT input Ch. 9	
18	RFN_9	Termination ref input Ch. 9	
19	RFIn_10	PMT input Ch. 10	
20	RFN_10	Termination ref input Ch. 10	
21	RFIn_11	PMT input Ch. 11	
22	RFN_11	Termination ref input Ch. 11	
23	RFIn_12	PMT input Ch. 12	
24	RFN_12	Termination ref input Ch. 12	
25	RFIn_13	PMT input Ch. 13	
26	RFN_13	Termination ref input Ch. 13	
27	RFIn_14	PMT input Ch. 14	
28	RFN_14	Termination ref input Ch. 14	
29	RFIn_15	PMT input Ch. 15	
30	RFN_15	Termination ref input Ch. 15	
31	RFIn_16	PMT input Ch. 16	
32	RFN_16	Termination ref input Ch. 16	
33	GND33	0V power (GND = VSS)	
34	VDD34	2.5V power (VDD)	

next page...



Table 32 continued

Pin#	Pin Name	Description	Comment
35	SIN	Serial Input data	
36	SCLK	Serial clock advance	
37	PCLK	Parallel clock load	
38	SHout	Serial Shift Out	
39	GND39	0V power (GND = VSS)	
40	VDD40	2.5V power (VDD)	
41	-	-	
42	-	-	
43	HSclkN	Data Shift-out Clock	
44	HSclkP	LVDS	
45	GND43	0V power (GND = VSS)	
46	WR_RS_S0	WR Row Select Addr. 0	
47	WR_CS_S1	WR Row Select Addr. 1	
48	WR_CS_S0	WR Column Select Addr. 0	
49	WR_CS_S1	WR Column Select Addr. 1	
50	WR_CS_S2	WR Column Select Addr. 2	
51	WR_CS_S3	WR Column Select Addr. 3	
52	VDD52	2.5V power (VDD)	
53	GND53	0V power (GND = VSS)	
54	WR_CS_S4	WR Column Select Addr. 4	
55	WR_CS_S5	WR Column Select Addr. 5	
56	GCC_Reset	Gray Code Counter Reset	
57	WL_CLK_n	Wilkinson Clock LVDS	
58	WL_CLK_p	Wilkinson Clock LVDS	
59	GND59	0V power (GND = VSS)	
60	VDD60	2.5V power (VDD)	
61	RDAD_clk	Read Address Set SCLK	
62	RDAD_sin	Read Address Set Serial Input	
63	RDAD_dir	Read Address Set DIR	
64	-	-	
65	-	-	
66	SmplSl_Any	Sample Select between TPG and sample value	'0' : Test Pattern Generator '1' : Sample Select
67	VDD67	2.5V power (VDD)	
68	GND68	0V power (GND = VSS)	
69	DO_16	Serial Data Out Ch. 16	
70	DO_15	Serial Data Out Ch. 15	
71	DO_14	Serial Data Out Ch. 14	
72	DO_13	Serial Data Out Ch. 13	
73	DO_12	Serial Data Out Ch. 12	
74	DO_11	Serial Data Out Ch. 11	
75	DO_10	Serial Data Out Ch. 10	
76	DO_9	Serial Data Out Ch. 9	
77	VDD77	2.5V power (VDD)	

next page...



Table 32 continued

Pin #	Pin Name	Description	Comment
78	GND78	0V power (GND = VSS)	
79	SS_Incr	Sample Select increment	
80	DOE	Data Output Enable	'0' : Data Output Disabled '1' : Data Output Enabled
81	-	-	
82	VDD82	2.5V power (VDD)	
83	GND83	0V power (GND = VSS)	
84	DO_8	Serial Data Out Ch. 8	
85	DO_7	Serial Data Out Ch. 7	
86	DO_6	Serial Data Out Ch. 6	
87	DO_5	Serial Data Out Ch. 5	
88	DO_4	Serial Data Out Ch. 4	
89	DO_3	Serial Data Out Ch. 3	
90	DO_2	Serial Data Out Ch. 2	
91	DO_1	Serial Data Out Ch. 1	
92	VDD92	2.5V power (VDD)	
93	GND93	0V power (GND = VSS)	
94	DONE	AND of all DONE	Tied to VDD
95	eSS_Reset	Sample Select reset	
96	GND96	0V power (GND = VSS)	
97	VDD97	2.5V power (VDD)	
98	GND98 0V	power (GND = VSS)	
99	eRegCLR	Global register clear	
100	emDOE	Monitor DOE (was PCLK2)	
101	GND101	0V power (GND = VSS)	
102	VDD102	2.5V power (VDD)	
103	eSS_LD_sin	Sample select load data	
104	eSS_LD_dir	Sample select load ctrl	
105	-	-	
106	GND106	0V power (GND = VSS)	
107	VDD107	2.5V power (VDD)	
108	eRamp	Wilkinson Ramp control	
109	GND109	0V power (GND = VSS)	
110	Vdischarge	Wilkinson Ramp Start voltage	
111	RampMon	Buffered copy of Wilk Ramp	
112	ISEL	Monitor for Wilk Ramp I (V out)	
113	VrampRef	Charging node	
114	GND114	0V power (GND = VSS)	
115	VDD115	2.5V power (VDD)	
116	-	-	
117	eMonTimeN	Monitor internal Timebase gen	
118	eMonTimeP		
119	-	-	
120	-	-	

next page...



Table 32 continued

Pin#	Pin Name	Description	Comment
121	GND121	0V power (GND = VSS)	
122	VadjN	Sampling NMOS current Adj	
123	-	-	
124	VadjP	Sampling PMOS current Adj	
125	SSTin_p	SSTin LVDS	
126	SSTin_n	SSTin LVDS	
127	GND127	0V power (GND = VSS)	
128	VDD128	2.5V power (VDD)	



5.1 Register Write Interface

The ASIC contains a set of registers to enable internal DACs, which have different purposes such as fine tune of current charge, enable/disable Test Pattern Register, and so on. These register can only be accessed through the register interface pins, see table 33. This type of communication is a 19-Bit wide word followed by a signal transaction between SIN and PCLK, see figure 10. The SIN signal must be shifted out on each rising edge of the SCLK clock, the ASIC samples the SIN input on the falling edge.

Pinout(s)

Pin#	Pin Name	Pin Type	Description
35	SIN	Digital Input	Serial Input data
36	SCLK	Digital Input	Serial clock advance
37	PCLK	Digital Input	Parallel clock load
38	SHout	Digital Output	Serial Shift Out

Table 33: Register interface Pins

Requirement(s)

Req#	Description
1	PCLK Pulse shall be at least 100 ns wide
2	SIN shall start before PCLK last pulse
3	MSB First
4	ASIC samples on falling edge, data is shifted out on the rising edge

Table 34: Requirement for the register write interface

Payload

Bits	Description
18 - 12	Register Address
11 - 0	12-Bit Data

Table 35: TARGETC 19-Bit Register payload



Interface sequence

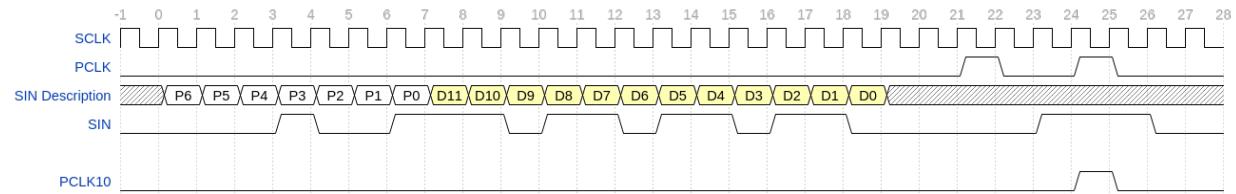


Figure 10: Register Write Sequence for register 10 with the binary data 110110110110_2



5.2 Delay Lock Loop

The Delay Lock Loop is one of the main reasons that the Target C can sample at 1GS/s and it is very important to initialize it correctly. To work with the DLL a few parameters must be written.

- Qbias controls the charge pump of the DLL.
- VQBUFF enables the DAC Qbias
- VADJP controls the Trailing edge (TE) of the signals
- VADJN controls the Leading edge (LE) of the signals
- VAPBUFF enables the DAC VADJP
- VANBUFF enables the DAC VADJN

Requirement(s)

Req#	Description
1	VadjN must be stable in order to consider the DLL locked.

Table 36: Requirement for DLL

Interface Sequence

1. At initialization, VQBUFF and VANBUFF are set to 0
2. VADJN set to approximative value close to the locked one $y = 4095 * x/2.5$
3. VANBUFF set 1100, kisck-start the DLL
4. VQBUFF set to 1062, VADJN value are fighting
5. VANBUFF set to 0, DLL is going to stabilize itself
6. Wait until VADJN is stable
7. Control the MonTiming signals, the LE and TE parameters have to be set correctly for signals to perform as expected.

5.3 Storage Control

UPDATE, 28th of January 2019 : The storage address update sequence was wrongly understood and implemented due to lack of documentation. The previous project implementation will not be discussed and only the actual design is discussed, the correct storage address sequence is illustrate in figure 11.

The real address is the current window being sampled, the sampling value is however only valid a small amount of time after the sampling process due to the capacitor. A rising edge on the write

address sync signal will latch the address in the storage memory lines to select the correct storage cell. This signal is initiated prior to a write strobe sequence, because , these previous lines must stabilize themselves. The write strobe signal is level sensitive, a HIGH level will transfer the voltage from sampling to storage cells.

In summary the storage address is updated on each falling edge of SSTIN, in order to prepare a new memory location for the next sample cycle. The storage address is 8-bit wide bus. The TARGETC has a total of 512 windows and two of which are sampled sequentially during a SSTIN period, as a result the storage address is only 8-bit long.

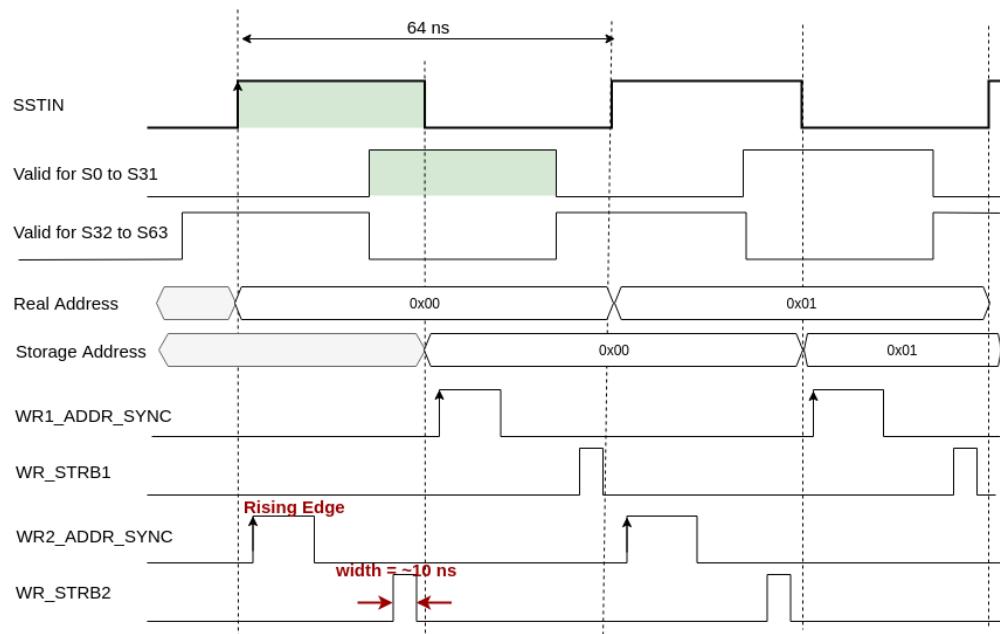


Figure 11: Timing principle for write address and write strobe signals

Pinout(s)

WR_RS_S are the lower bits and WR_CS_S are the upper bits of the storage address.

Pin#	Pin Name	Pin Type	Description
46	WR_RS_S0	Digital Input	WR Row Select Addr. 0
47	WR_RS_S1	Digital Input	WR Row Select Addr. 1
48	WR_CS_S0	Digital Input	WR Column Select Addr. 0
49	WR_CS_S1	Digital Input	WR Column Select Addr. 1
50	WR_CS_S2	Digital Input	WR Column Select Addr. 2
51	WR_CS_S3	Digital Input	WR Column Select Addr. 3
54	WR_CS_S4	Digital Input	WR Column Select Addr. 4
55	WR_CS_S5	Digital Input	WR Column Select Addr. 5

Table 37: Storage address interface Pins



Requirement(s)

Req#	Description
1	WR_RS_S(1-0) and WR_CS_S(5-0) shall be updated on the falling edge.

Table 38: Requirement for the register write interface (Update : 28th of January 2019)

Interface sequence

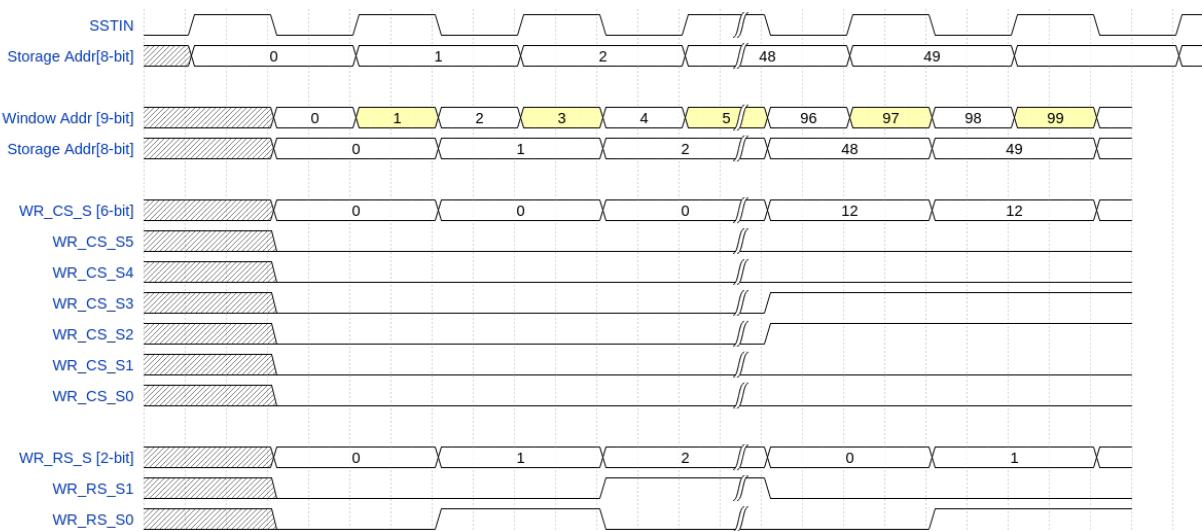


Figure 12: Storage address update sequence (Update : 28th of January 2019)

5.4 Window Readout

As mentioned the storage address is a 8-Bit wide address. The readout is a 9-Bit address, the extra bit enables the selection between the 1st or 2nd window sampled. In the TARGET world, we speak of EVEN or ODD window, the 1st window being the EVEN and respectively the 2nd the ODD window.

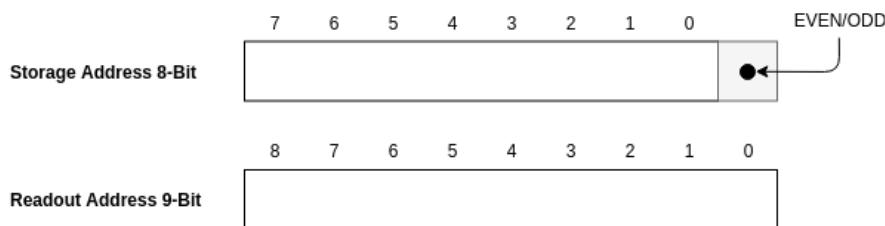


Figure 13: Storage VS Readout address

From previous TARGET designs, the readout address is swapped and the extra bit is placed in different places. This should not be the case for TARGETC.



Pinout(s)

Pin#	Pin Name	Pin Type	Description
61	RDAD_clk	Digital Input	Read Address Set SCLK
62	RDAD_sin	Digital Input	Read Address Set Serial Input
63	RDAD_dir	Digital Input	Read Address Set DIR

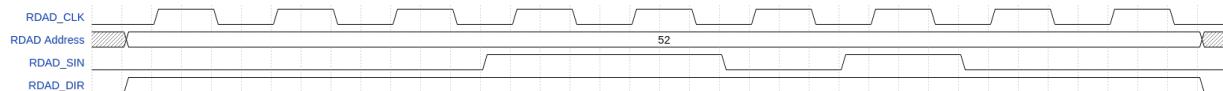
Table 39: Read address interface Pins

Requirement(s)

Req#	Description
1	TARGETC samples on the rising edge of RDAD_CLK. Data shall be shifted during the LOW period of the clock on SIN.
2	MSB is shifted out first on RDAD_SIN

Table 40: Requirement for the readout interface

Interface sequence

Figure 14: Example of Readout Address sequence for window 52_{10}



5.5 Wilkinson Digitization

The read module inside the ASIC decodes the address entered on the readout interface and the corresponding internal switches are powered on, connecting the window's cells comparator outputs to the latch inputs of the sample registers (Output shift register). The Wilkinson counter is reset using the signal GCC_Reset (11-Bit Gray Code Counter). The ramp signal (eRamp) is enabled, which enables the charge of the Wilkinson capacitor. It is important to synchronize eRamp signal with the release of GCC_reset signal, because the counter is incrementing on every rising edge of the Wilkinson clock. Once the comparator stored value is equal to the capacitor's value, the comparator's output switches from LOW to HIGH, this has the effect of latching the counter's value in the sample register. This latched value corresponds to the gray coded digital value of the stored sample. After the digitization is completed the eRamp signal must be kept HIGH during all the sample readout. Finally the Wilkinson capacitor should have enough time to discharge completely.

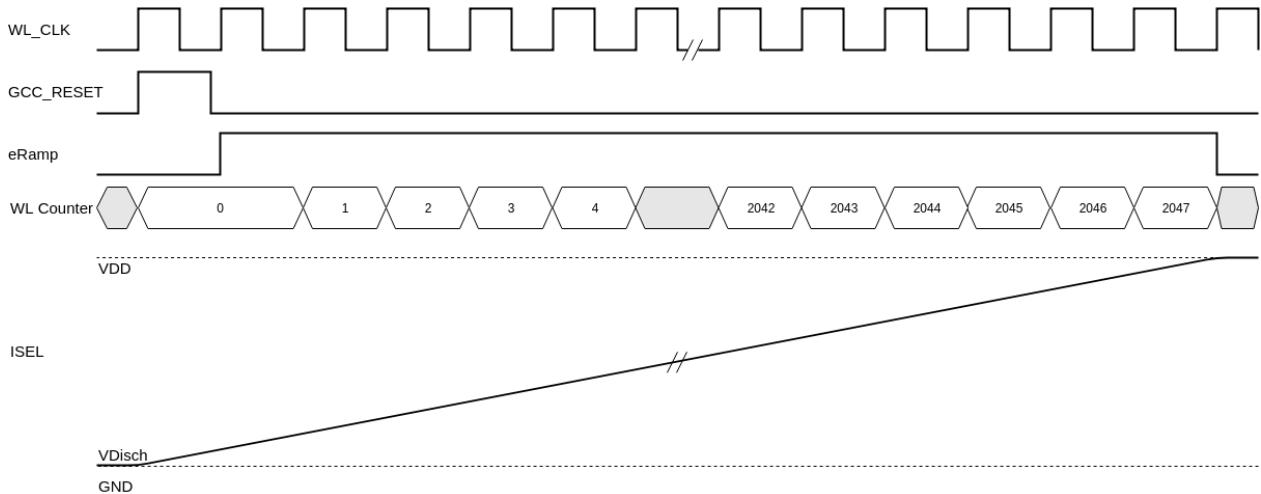


Figure 15: Wilkinson conversion signals for full range ($VDD=2047$)

Pinout(s)

Pin#	Pin Name	Pin Type	Description
56	GCC_Reset	Digital Input	Gray Code Counter Reset
57	WL_CLK_n	LVDS Input	Wilkinson Clock LVDS
58	WL_CLK_p	LVDS Input	Wilkinson Clock LVDS
108	eRamp	Digital Input	Wilkinson Ramp control
110	Vdischarge	Analog Output	Wilkinson Ramp Start voltage
111	RampMon	Analog Output	Buffered copy of Wilk Ramp
112	ISEL	Analog Output	Monitor for Wilk Ramp I (V out)
113	VrampRef	Analog Output	Charging node

Table 41: Storage address interface Pins



Requirement(s)

Req#	Description
1	The Wilkinson frequency must correspond with the charge of the capacitor defined by the DAC register ISEL.
2	The counter must be reset before starting a new conversion.
3	The eRamp signal is held HIGH during all sample readout.

Table 42: Requirement for the wilkinson interface

Interface sequence

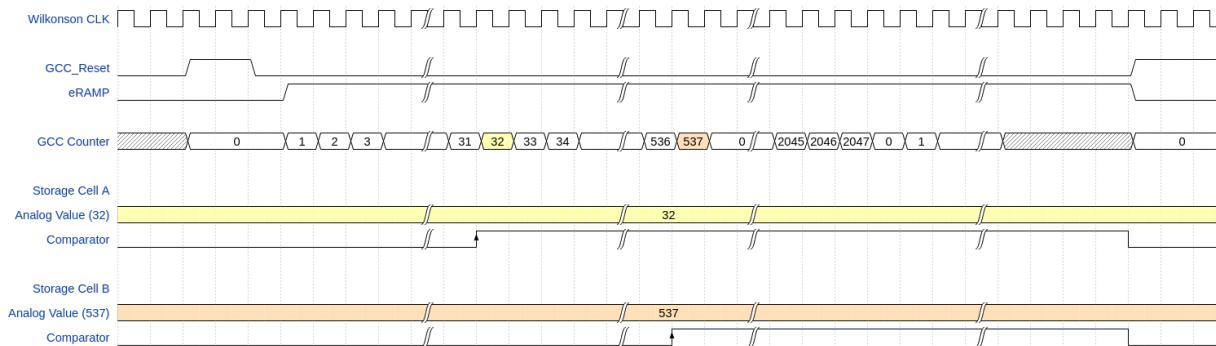


Figure 16: Wilkinson sequence for the digitization of a selected window

5.6 Sample Readout

The sample readout is an internal counter that can be incremented on the rising edge of SS_Incr or reset using eSS_Reset (Active HIGH). Once the 32 samples from all channels have been read, the counter goes back to sample 0 by applying a pulse on SS_Incr. The falling edge of SS_Incr charges the values into the registers. This is why the pulse width is important, because of the disposition of the registers in the ASIC, some lines take longer than others to arrive. The pulse should be long enough for the data to be stable before latching it into the output registers.



Pinout(s)

Pin#	Pin Name	Pin Type	Description
43	HSclkN	LVDS Input	Data Shift-out Clock
44	HSclkP	LVDS Input	LVDS
66	SmplSl_Any	Digital Input	Select between TPG or sample value
79	SS_Incr	Digital Input	Sample Select increment
80	DOE	Digital Input	Data Output Enable
69	DO_16	Digital Output	Serial Data Out Ch. 16
70	DO_15	Digital Output	Serial Data Out Ch. 15
71	DO_14	Digital Output	Serial Data Out Ch. 14
72	DO_13	Digital Output	Serial Data Out Ch. 13
73	DO_12	Digital Output	Serial Data Out Ch. 12
74	DO_11	Digital Output	Serial Data Out Ch. 11
75	DO_10	Digital Output	Serial Data Out Ch. 10
76	DO_9	Digital Output	Serial Data Out Ch. 9
84	DO_8	Digital Output	Serial Data Out Ch. 8
85	DO_7	Digital Output	Serial Data Out Ch. 7
86	DO_6	Digital Output	Serial Data Out Ch. 6
87	DO_5	Digital Output	Serial Data Out Ch. 5
88	DO_4	Digital Output	Serial Data Out Ch. 4
89	DO_3	Digital Output	Serial Data Out Ch. 3
90	DO_2	Digital Output	Serial Data Out Ch. 2
91	DO_1	Digital Output	Serial Data Out Ch. 1
95	eSS_Reset	Digital input	Sample Select reset

Table 43: Sample Readout interface Pins

Requirement(s)

Req#	Description
1	SS_Incr pulse shall be wide enough (latency in ASIC).

Table 44: Requirement for the sample select interface

Interface sequence

The interface sequence is very particular for the first sample. The SS_Reset is brought LOW and after the SS_INCR is brought HIGH. Internally this effect will load the register of sample 0 on the bus. After a stabilization time, SS_Reset is disabled and then SS_INCR is set LOW. The data of the register will be latched into the output shift register.

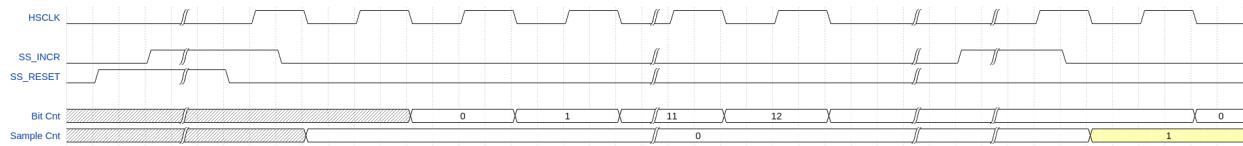


Figure 17: Sample select readout sequence