Project: WATCHMAN
University of Hawaii at Manoa

Meeting : Tuesday, 24th of October 2018, Week 6

Participants:

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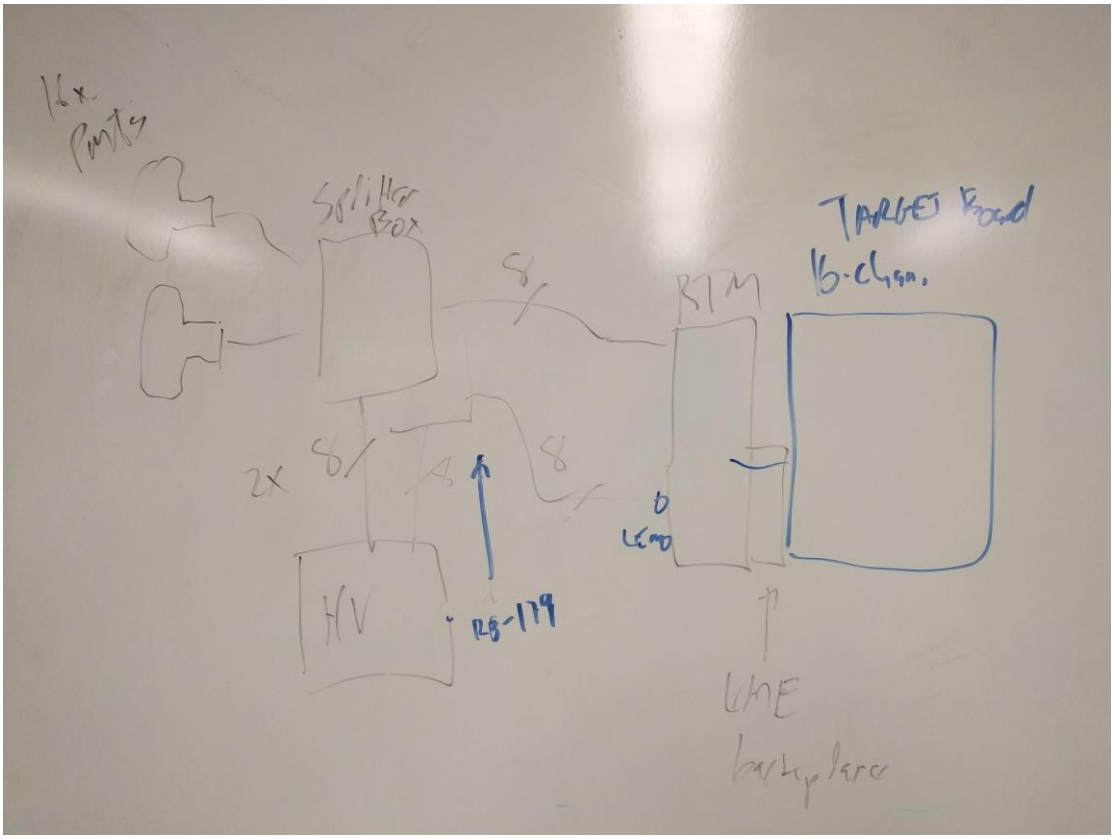
Testing PMT Diagram:

Gary explained the testing diagram from clarification of Monday's (22nd of October 2018) DAQ Meeting WATCHMAN. In brief, a total of 16 PMTs are connected to 2 Splitter Box (8 PMTs each) who are then connected to RTM through RG-179 (Lemo connectors). The RTM is in the crate and is the the backplane interface for the 6U VME boards. (see board drawing below)



Jose and 6U VME PCB:
The idea is to go with the 2 Microzed options. The pin list is okay after review yesterday, but should be double checked.

The incoming lines from the backplane connector should be Ground - signal - Ground - Signal - … to avoid as far as possible any interference.

Crate Control Bus should not be forgotten, maybe not for the 1st version on January but for the next generation.

To do next, map the pins to the microzed and see if all fits.

Jonathan, Readout ASIC TARGETC

Architecture is refined and previous tests are ok, this is to say :
Write/"Read" ASIC Registers (Test adjustment of RAM, ISEL and VAdj)
Load TPG (Test Pattern Generator) and see it on DO[16:1]

The goal is to readout some sampling values from the ASIC. Architecture is ready and testbench looks promising, the ASIC however is not exactly the same as TARGETX. A good start for investigation is to look into :

RAMP:	See if the ramp is increasing
Done signal:	Done signal should trigger is all comparators are done conversion
GCC_RST:	Positive Pulse to reset the counter

Anthony, python app and merging john's soft and his

The python app is fully working with multiple windows and multiple thread. With the very maximum data rate is 60MB/s, data are lost (~25%, but it depends of the power of the computer), but the typical should be less than 1MB/s, so the app would be able to handle it.
The merging is done, but there are some problem to coordinate the timer and axidma interrupts.