Project: WATCHMAN

University of Hawaii at Manoa



Meeting: Tuesday, 27th of November 2018, Week 11

Participants: Jonathan Hendriks <u>jhendrik@hawaii.edu</u>

Anthony Schluchin

Jose Duron

Kurtis Nishimura

Gary Varner

Vasiliy Shebalin

Schluchi@hawaii.edu

jduron@hawaii.edu

kurtisn@phys.hawaii.edu

Varner@phys.hawaii.edu

vasiliy.shebalin@gmail.com

Reminder:

Week 7 to 9 were working weeks but there were a lots of public holidays, most of them fell on Tuesday. Also the team was away for some time and now everybody is back. This is why there is a gap of MoMs during this period.

Altium License Expired

The license expired so before we can keep on going with the schematic, we have to wait a hopefully a week before Jose can restart.

HV Splitter

Change the capacitor and probably the the resistors by some through holes components HV rated. The PMT rating is 2000V (from datasheet: R7081-100). Gary suggest adding a safety factor to the components to avoid using them at their limit.

The metal casing is suitable for testing, it will be ground using the board screw connections to ground. The BNC connector must be changed of place and leave a reasonable clearance to the HV connector and BNC.

Pulse Trigger Comparator

The pulse is definitely not good and the hysteresis pin on the FPGA must be driving low to enable this feature (test on Wednesday 28th of November 2018). The pulse is only a few mV high with the gain stage we should see something around 10-20mV.

The test will use the sync out generator and using a capacitor and resistor circuit (high pass filter) we should be able to reproduce a dummy pulse from a PMT.

Project: WATCHMAN

University of Hawaii at Manoa



Readout TARGETC

TargetC readouts were not convincing but apparently the only thing now is to take into account the transfer function of the comparator and readjust the readout. This means:

- 1) Fix Vped at 1.25V
- 2) Fix ISEL to match raw readout around 512
- 3) Pedestal calculation
- 4) Using pedestal substraction vary Vped and find out the transfer function of the comparator. This gives the adjustment from nominal voltage Vped.

Jitter on readings and linear decay

This problem is maybe from the sampling to storage operation, the time is maybe just on the limit for the address to be stable for the first WRITE_ADDR1 signal.

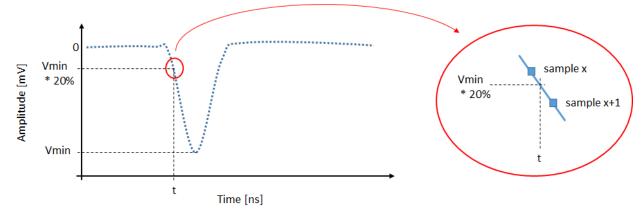
Kurtis suggest delaying the address for storage (ROW and COLUMN) by a few nanoseconds. Investigation in the sampling and storage sequence.

Doxygen

The idea is to generate doxygen documentation for all the softwares, so everybody is working on their code to write the comments in the right form.

Features extraction

There are two types of data transferred to the computer, and it depends on the duration of the PMT pulse. The first type is the complete waveform for pulses that are to long. The second one is the "minimal" amplitude of the pulse and the time when it started (when the amplitude was at 20% of Vmin). To get the time, we will extrapolate the curve and extract the exact moment. It will be equal to x*1ns + c*1ns with c a real number between 0 and 1.



The choice of sending the full waveform or not is made in the PL side of the zynq and based on the information recovered from the comparator.