Project: WATCHMAN
University of Hawaii at Manoa

Meeting :   Tuesday, 21th of December 2018, Week 14

Participants: Jonathan Hendriks   jhendrik@hawaii.edu
                      Jose Duron   jduron@hawaii.edu
                      Kurtis Nishimura   kurtisn@phys.hawaii.edu

---

Hardware:

1) ADCMP601, comporator output goes low after FPGA is programmed

- ❏ Check the pinout
- ❏ Pull Up / Pull Down on XDC constraint file for FPGA
- ❏ Try the IOBUF on the XDC file and put it on tri-state
- ❏ Single ADC plugged in some other circuit, does it do the same thing?

2) Vped Oscillation

The problem is coming from the FMC board power supply. Should disappear with the new VME board.

- ❏ Check with Matt if an inductor on the main power supply

3) PMT

The PMT should be tested with the High Voltage Board, but parts are not in yet. The HV board needs to be tested before connecting the PMT and the case must be milled.

Firmware:

Timing and metastable data is fixed by using a single reference from Zynq and single MMCM for clock management. All windows are readout without problem, so errors are gone.

Trigger system for one trigger is up and running but the TargetC has 4 triggers, so more development is needed for entire trigger system and also the long pulse detection must be written.

To test the trigger and full loop data flow and also the performance of the round buffer, an AXI-Lite Dummy Trigger component is a temporary solution.

Project Merge:

Data flow from TargetC is sampled and sent to the PS of the Zynq and through UDP to the PC. The registers are written/readable by UDP through the Python GUI. The next step is to identify the transfer function of the comparator.

For Meeting on January:

The presentation is 30 min long. We shall focus on the infrastructure and what we have. The technical details to expect are :

- timings
- data rate
- performance

We should draft a few slides explaining the project and send it out during the holidays. We can iterate the presentation and details after New Year when everybody is back.

Heads Up:

After Watchman Meeting in January, Anthony and Jonathan will focus on documentation and Master Thesis due for February 7th.

We should also see for project handoff to the new Watchman collaborators.