Project: WATCHMAN
University of Hawaii at Manoa

Meeting : Tuesday, 8th of January 2019, Week 17

Participants: Jonathan Hendriks jhendrik@hawaii.edu
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Comments on the presentation draft for Kurtis:

Block diagram

Few comments on the blocks diagram:

- Make labels with bigger writing
- Explanation brackets in case it is too small
- Add the control blocks to show interaction between PS-PL-Target C

HV Splitter board

Maybe the connector of the high voltage isn't the best. BNC can be used for testing, but this question should be answered during the Watchman meeting.
Add a real photo of the board to the presentation.

Python GUI

Add a few screen shots of the GUI to the presentation and comments on the possibilities.

Oversize LUTs utilization

The design of the round buffer uses too much LUTs. One solution is to switch from LUTs to BRAM blocks. The use of primitives from Xilinx isn't necessary, with an attribute comment Vivado Synthesis should understand it should use the BRAM and not LUTs.

Meeting on Thursday

Anthony and Jonathan should assist if possible, to the 8:00 to 10:15 presentations.

Software

Recover data from the Target C to see the behavior of the transfer function for each sample of each window of each channels.


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