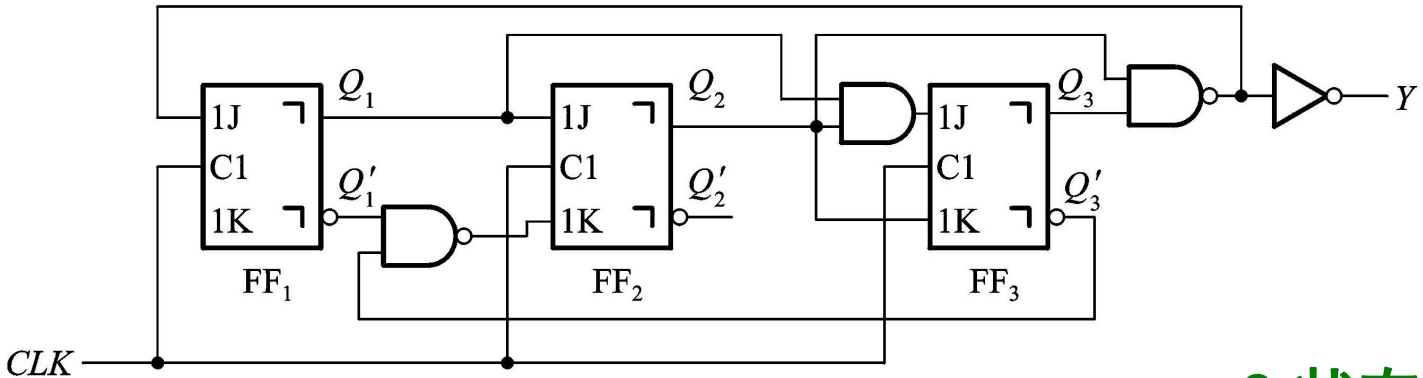
第六章 时序逻辑电路

主要要求：

- 熟练掌握时序逻辑电路的描述方法；
- 掌握时序逻辑电路的分析、设计；
- 掌握寄存器计数器等典型时序逻辑部件的功能和应用。

回顾：计数器分析



1) 驱动方程：

$$\begin{cases} J_1 = (Q_2Q_3)', & K_1 = 1 \\ J_2 = Q_1, & K_2 = (Q_1'Q_3')' \\ J_3 = Q_1Q_2, & K_3 = Q_2 \end{cases}$$

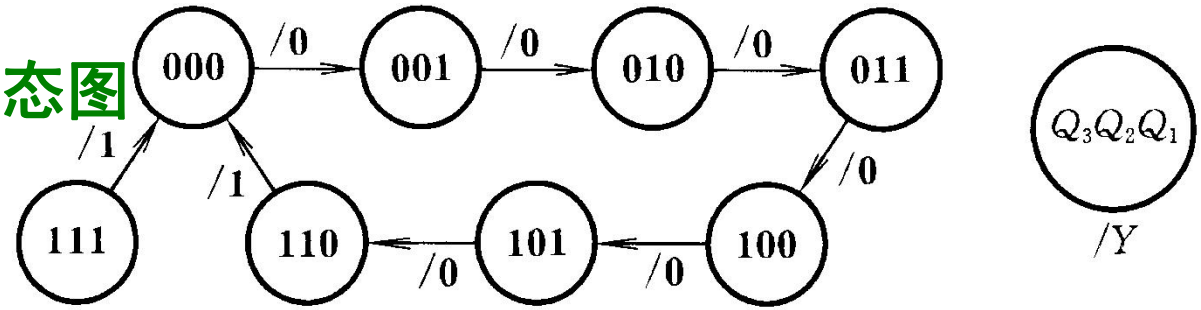
2.状态方程

$$\begin{cases} Q_3^* = Q_1Q_2Q_3' + Q_2'Q_3 \\ Q_2^* = Q_1Q_2' + Q_1'Q_2Q_3' \\ Q_1^* = (Q_2Q_3)' \cdot Q_1' \end{cases}$$

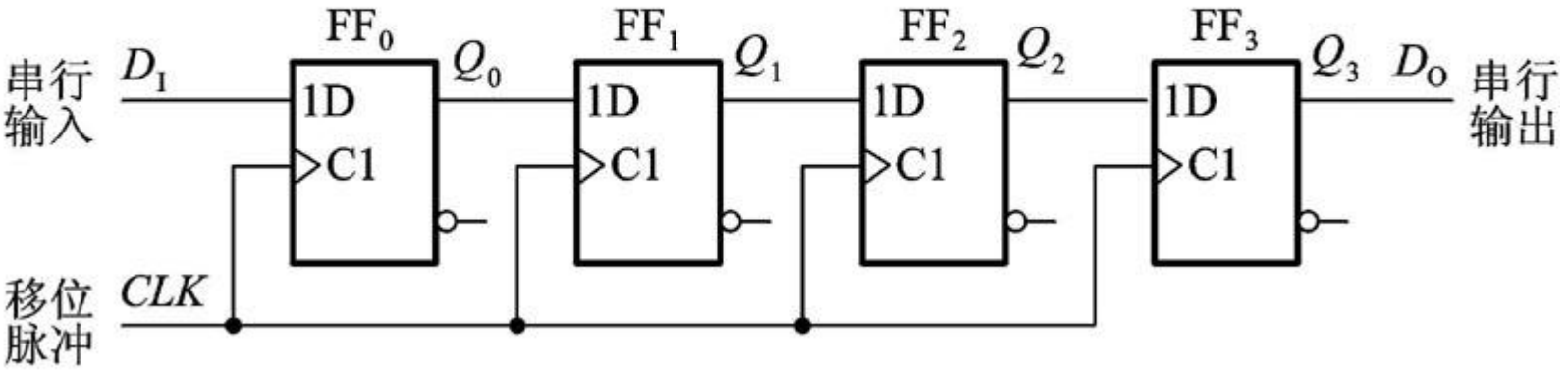
3.状态转换表

Q_3	Q_2	Q_1	Q^*_3	Q^*_2	Q^*_1	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	1	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	1	0	0	0	1

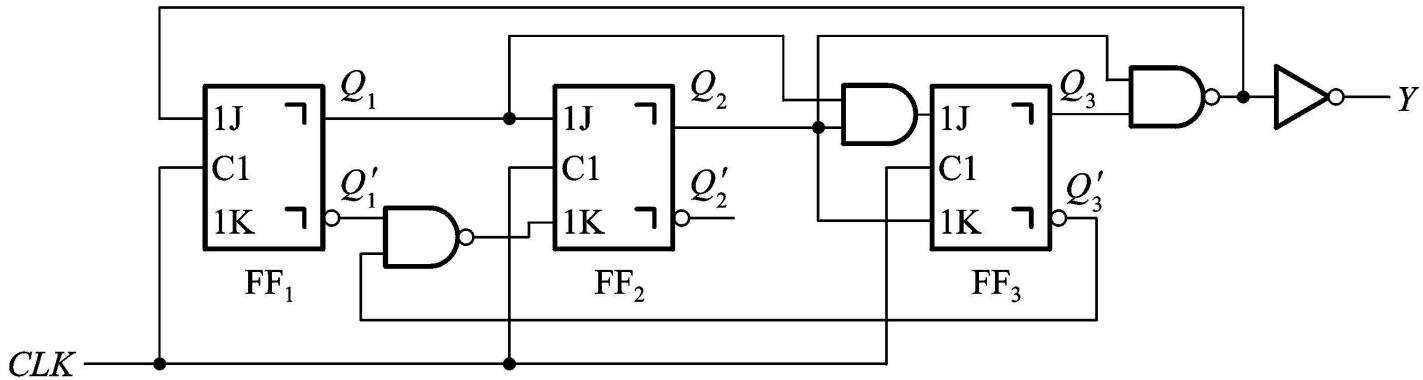
4.状态图



回顾：移位寄存器

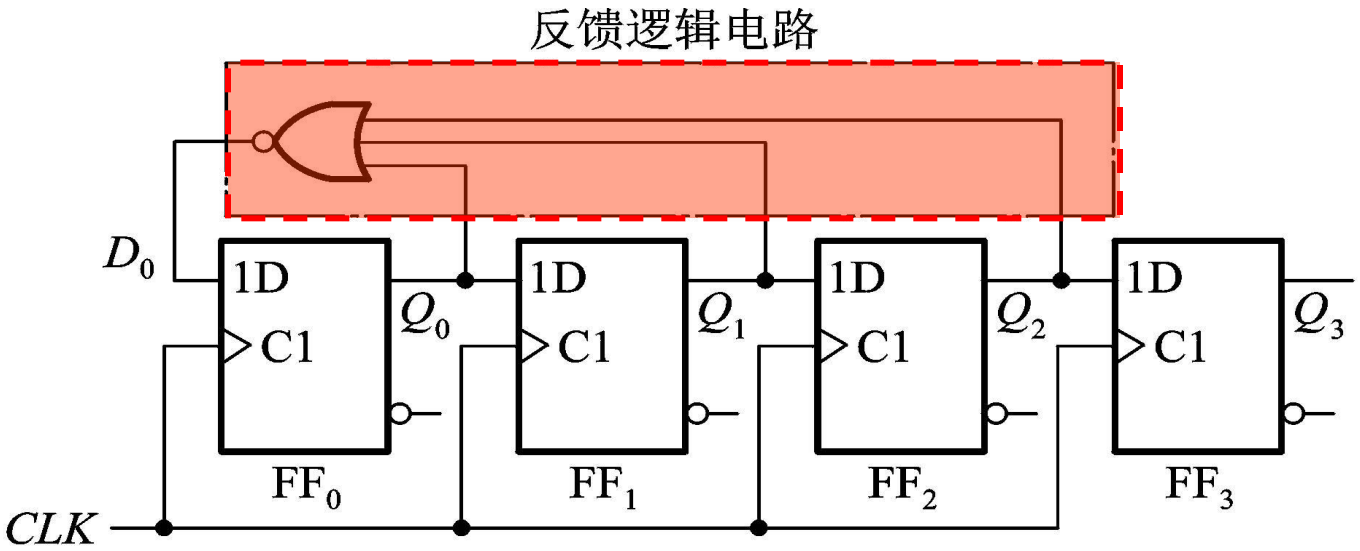


比较：计数器



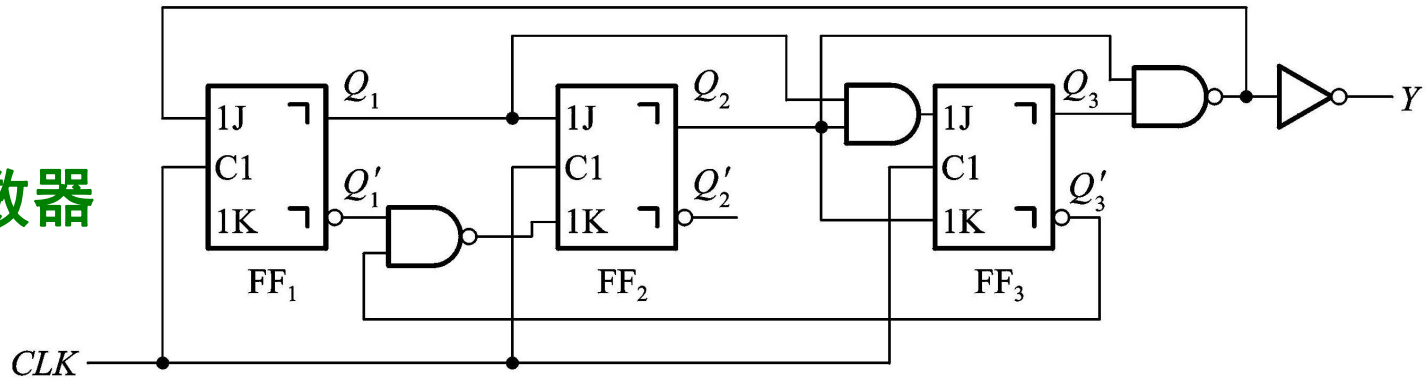
FF输入端复杂，需巧妙设计

6.3.4 移位型同步计数器



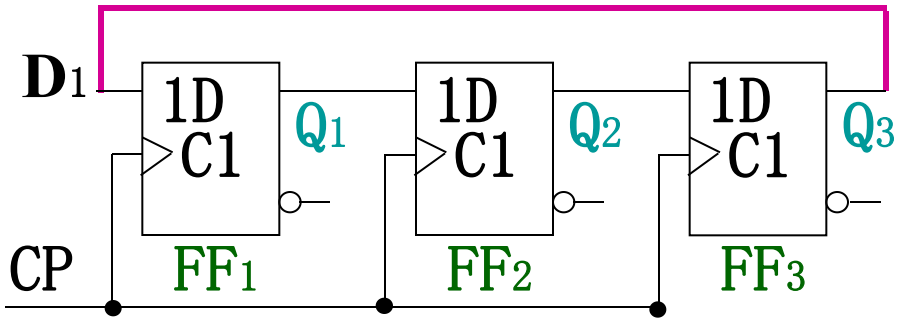
移位寄存器+反馈电路构成计数器，FF输入端简单，只需设计D0

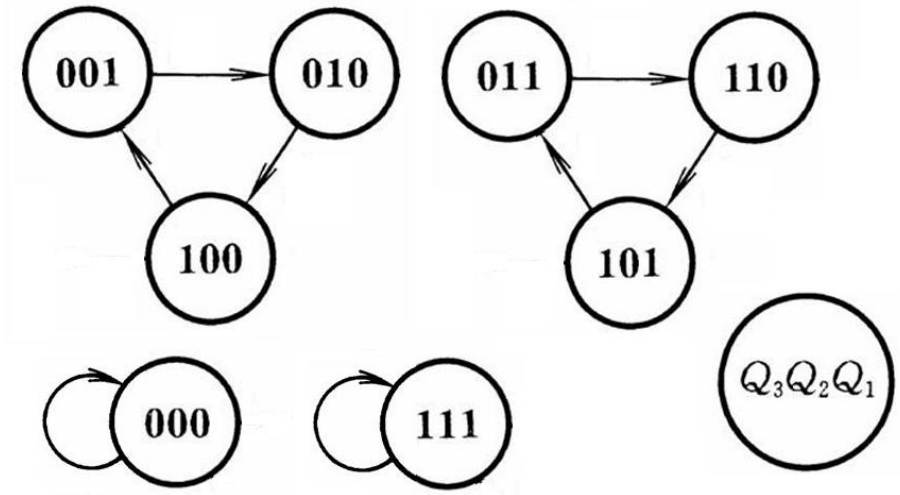
比较：计数器



FF输入端复杂，需巧妙设计

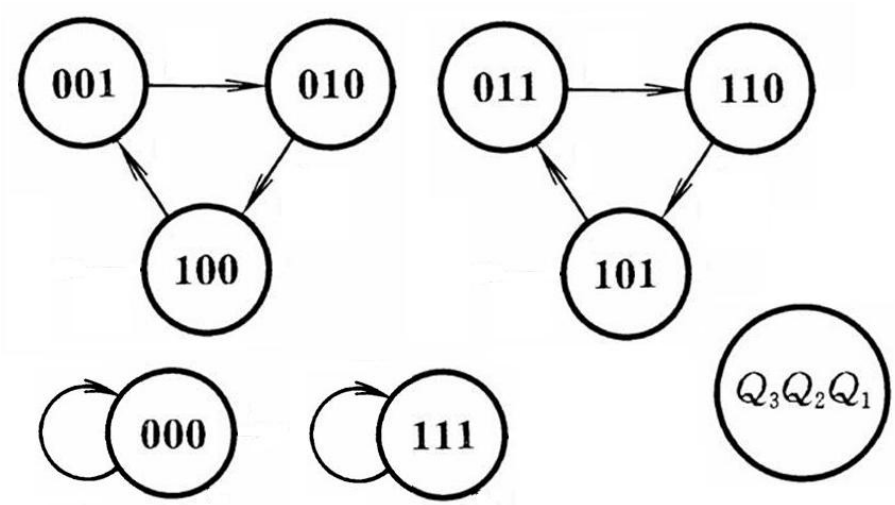
例：设计能自启动的模3环形计数器

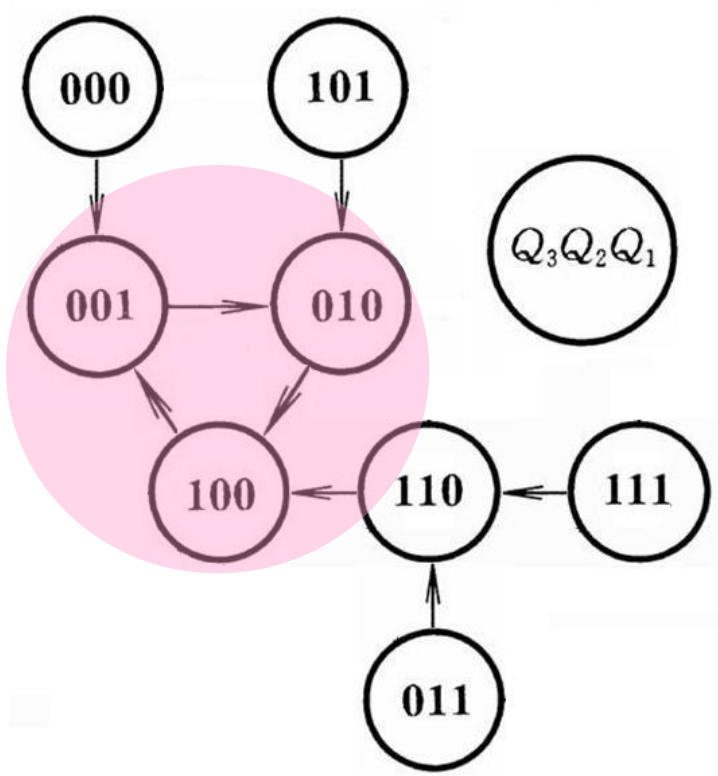




$Q_3Q_2Q_1$(现态）	$Q_3Q_2Q_1$(次态)
0 0 0	0 0 0
0 0 1	0 1 0
0 1 0	1 0 0
0 1 1	1 1 0
1 0 0	0 0 1
1 0 1	0 1 1
1 1 0	1 0 1
1 1 1	1 1 1

例：设计能自启动的模3环形计数器





次态K图

Q_3 \ Q_2Q_1	00	01	11	10
0	00x	010	11x	100
1	001	01x	11x	10x

$Q_3^*Q_2^*Q_1^*$

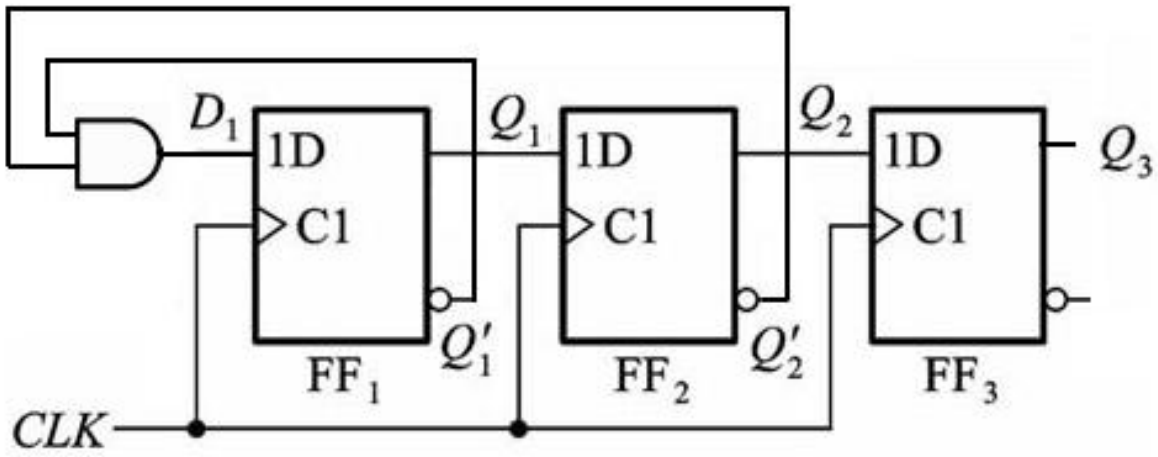
Q_3 \ Q_2Q_1	00	01	11	10
0	x	0	x	0
1	1	x	x	x

Q_1^*

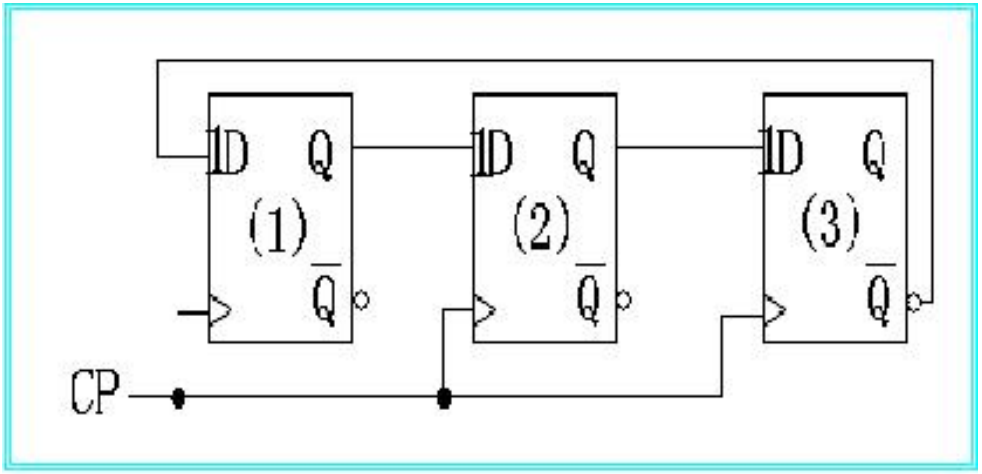
$$D_1 = Q_2'Q_1'$$

例：设计能自启动的模3环形计数器

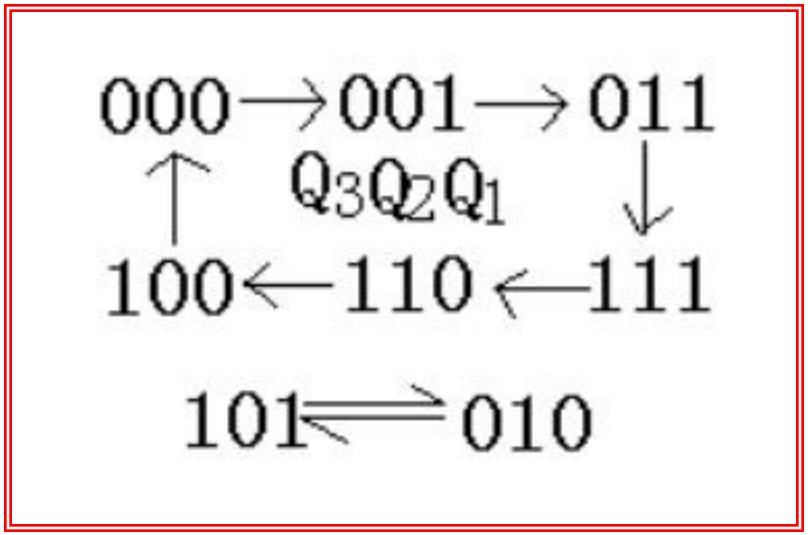
$$D_1 = Q_2'Q_1'$$

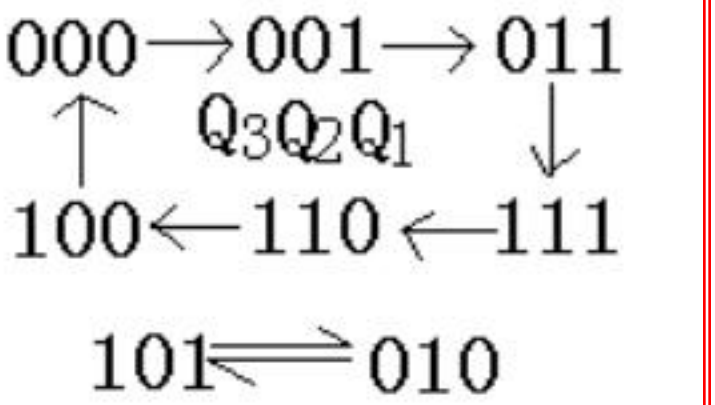


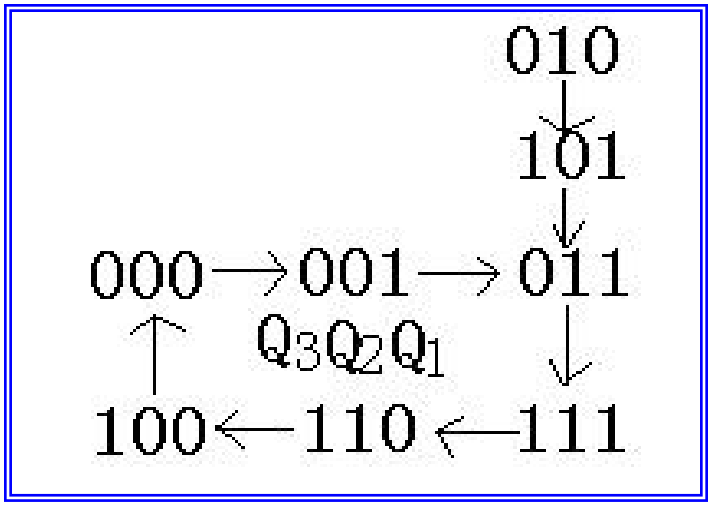
扭环形移位型计数器



$Q_3Q_2Q_1$(现态）	$Q_3Q_2Q_1$(次态)
0 0 0	0 0 1
0 0 1	0 1 1
0 1 0	1 0 1
0 1 1	1 1 1
1 0 0	0 0 0
1 0 1	0 1 0
1 1 0	1 0 0
1 1 1	1 1 0







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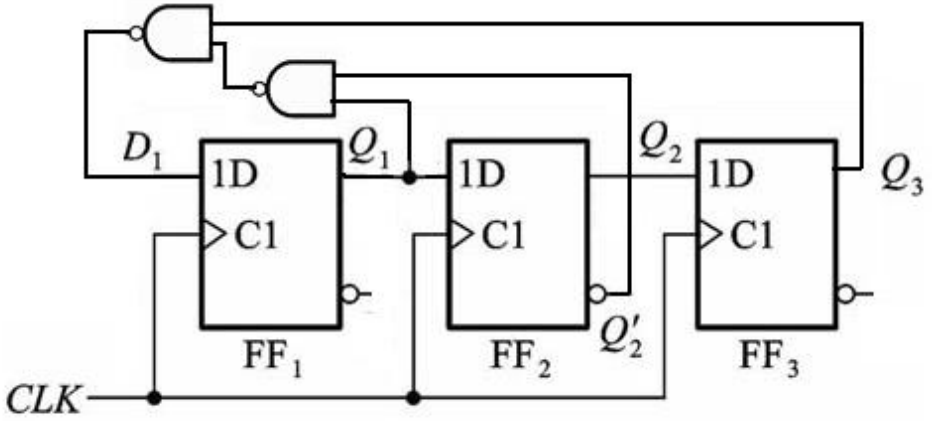
Q_3 \ Q_2Q_1	00	01	11	10
0	1	1	1	1
1	0	1	0	0

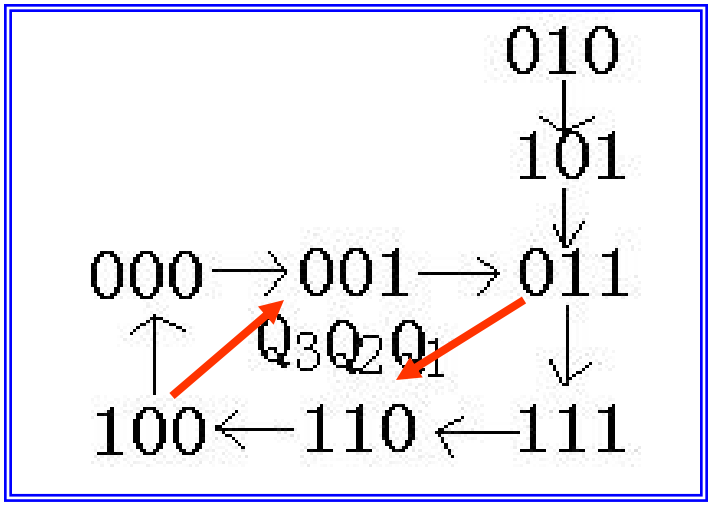
Q_1^{n+1}

$$D_1 = Q_1^* = Q_3' + Q_2' Q_1$$



例：设计计数器

	环形	扭环形
M6	6个FF	3个FF
M8	8个FF	4个FF
M5	5个FF	？个FF



Q_3 \ Q_2Q_1	00	01	11	10
0	001	011	111	101
1	001	011	110	100

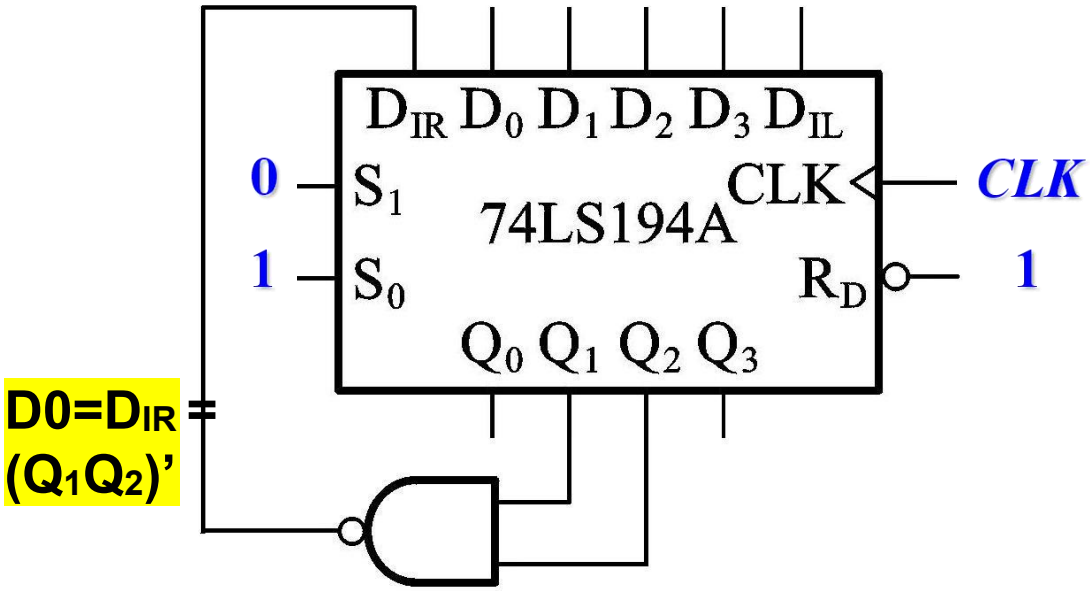
$(Q_3\,Q_2\,Q_1)^{n+1}$

Q_3 \ Q_2Q_1	00	01	11	10
0	1	1	1	1
1	1	1	0	0

Q_1^{n+1}

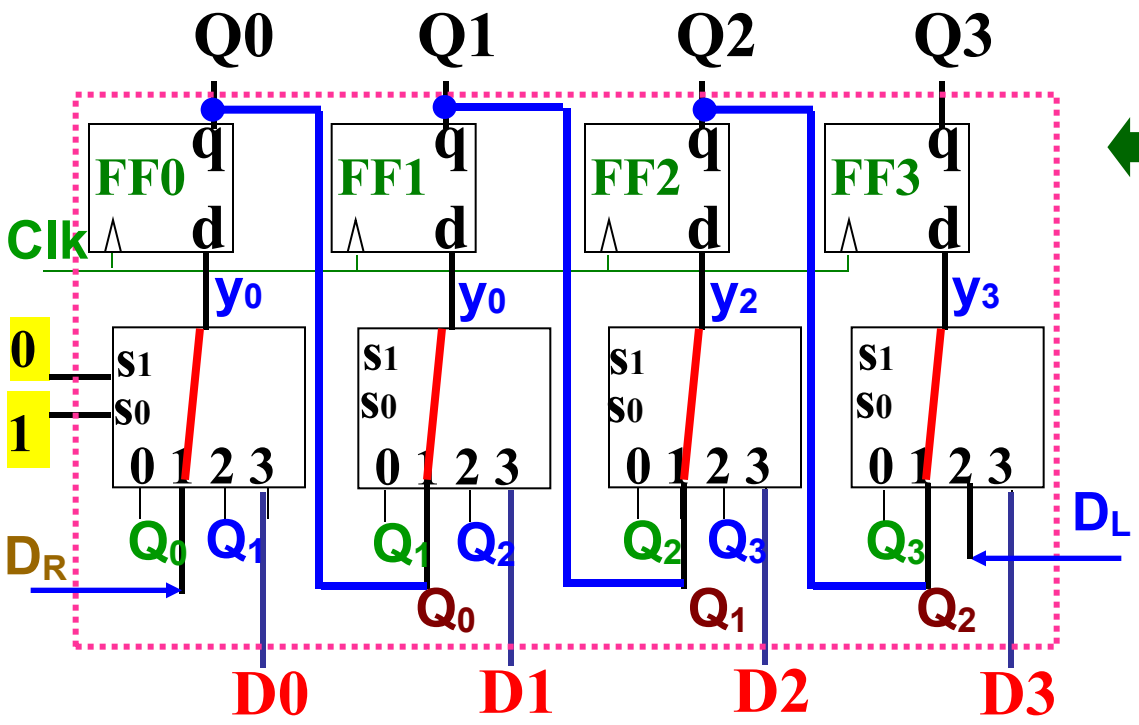
$$D_1 = Q_1^{n+1} = Q'_3 + Q'_2$$

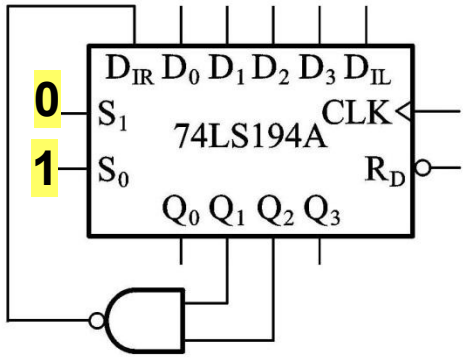
练习 74LS194A连接如下，成为一个移位型计数器。问，是几进制计数器，能否自启动。



双向移存器74LS194功能表

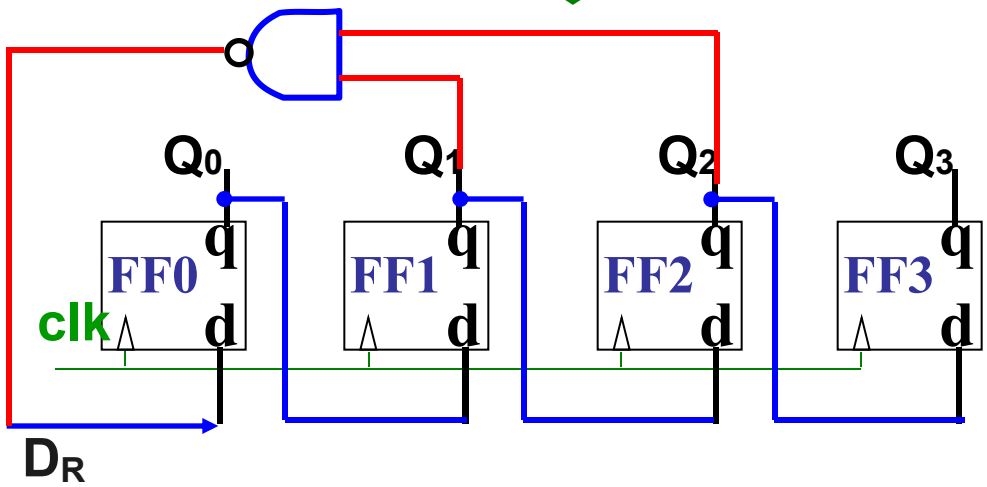
R'_D	S_1	S_0	工作状态
0	X	X	置零
1	0	0	保持
1	0	1	右移
1	1	0	左移
1	1	1	并行输入

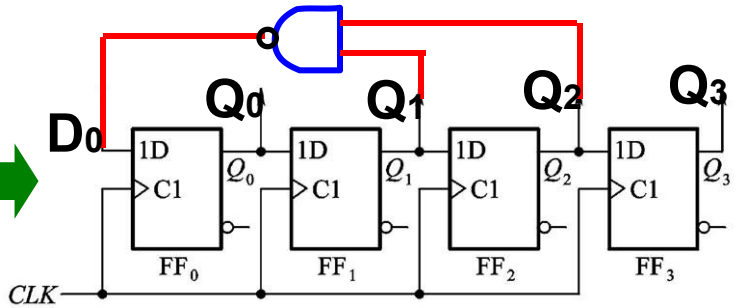




74LS194A功能表

S1	S0	Q_0^*	Q_1^*	Q_2^*	Q_3^*	
0	0	Q_0	Q_1	Q_2	Q_3	保持
0	1	D_R	Q_0	Q_1	Q_2	右移
1	0	Q_1	Q_2	Q_3	D_L	左移
1	1	D_0	D_1	D_2	D_3	置数





1)驱动方程

$D_3=Q_2$

$D_2=Q_1$

$D_1=Q_0$

$D_0=(Q_2Q_1)'$

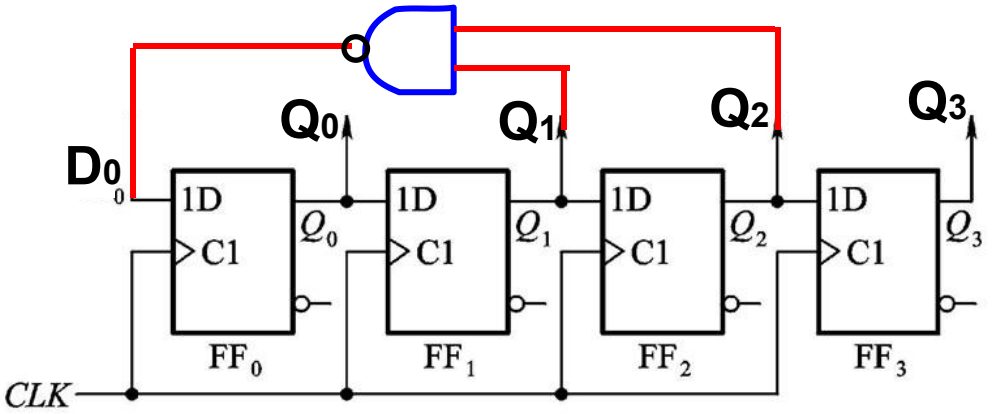
状态方程

$Q^*_3=Q_2$

$Q^*_2=Q_1$

$Q^*_1=Q_0$

$Q^*_0=D_0$



2)状态转换表

Q_3	Q_2	Q_1	Q_0	Q_3^*	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0

1)驱动方程

$D_3=Q_2$

$D_2=Q_1$

$D_1=Q_0$

$D_0=(Q_2Q_1)'$

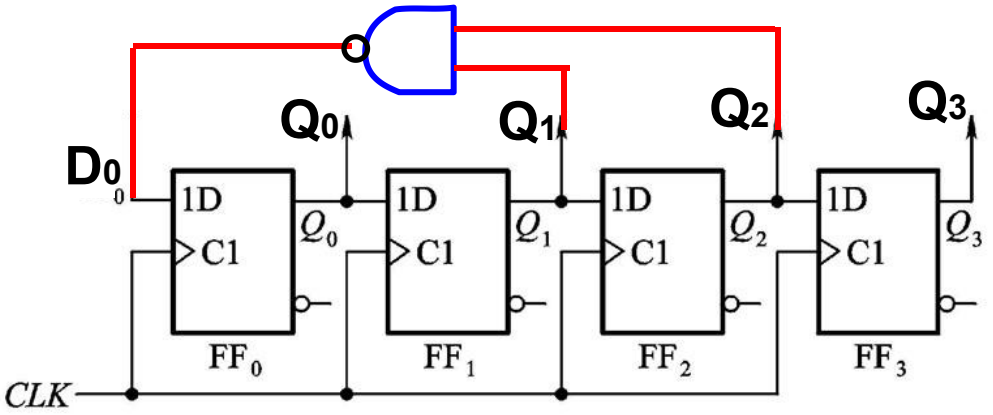
状态方程

$Q^*_3=Q_2$

$Q^*_2=Q_1$

$Q^*_1=Q_0$

$Q^*_0=D_0$

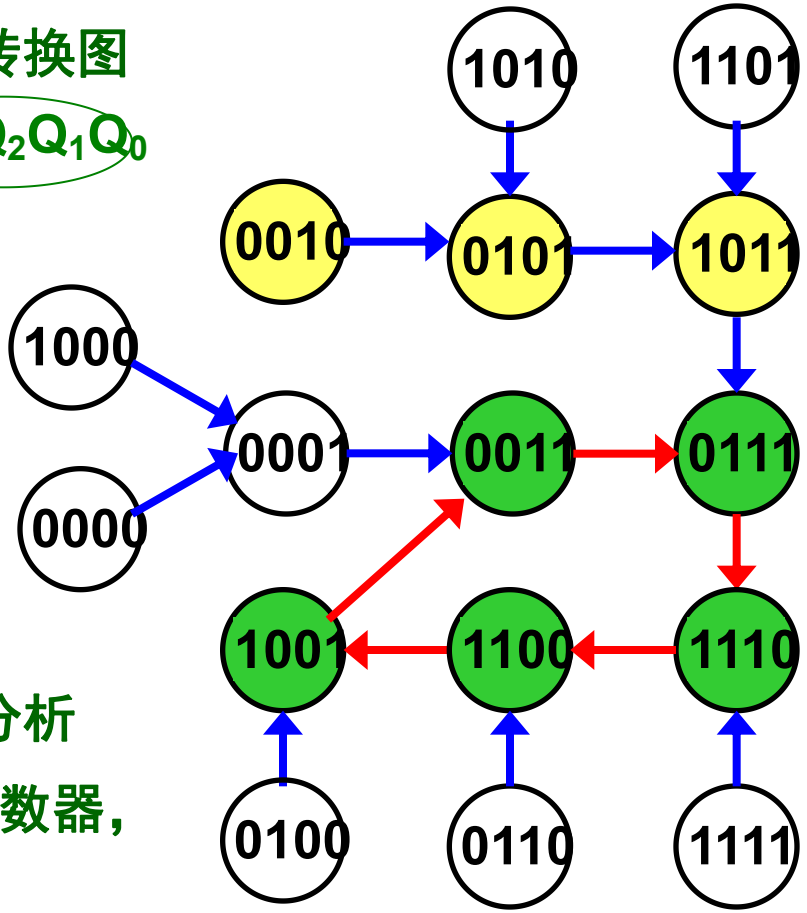


2)状态转换表

Q_3	Q_2	Q_1	Q_0	Q_3^*	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0

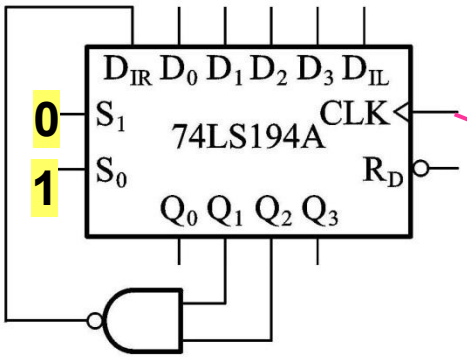
3)状态转换图

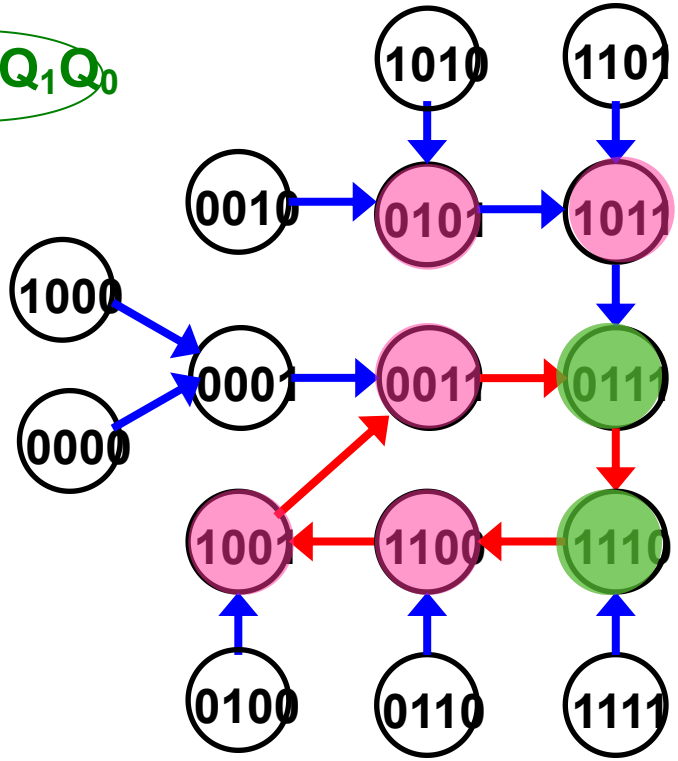
$Q_3Q_2Q_1Q_0$



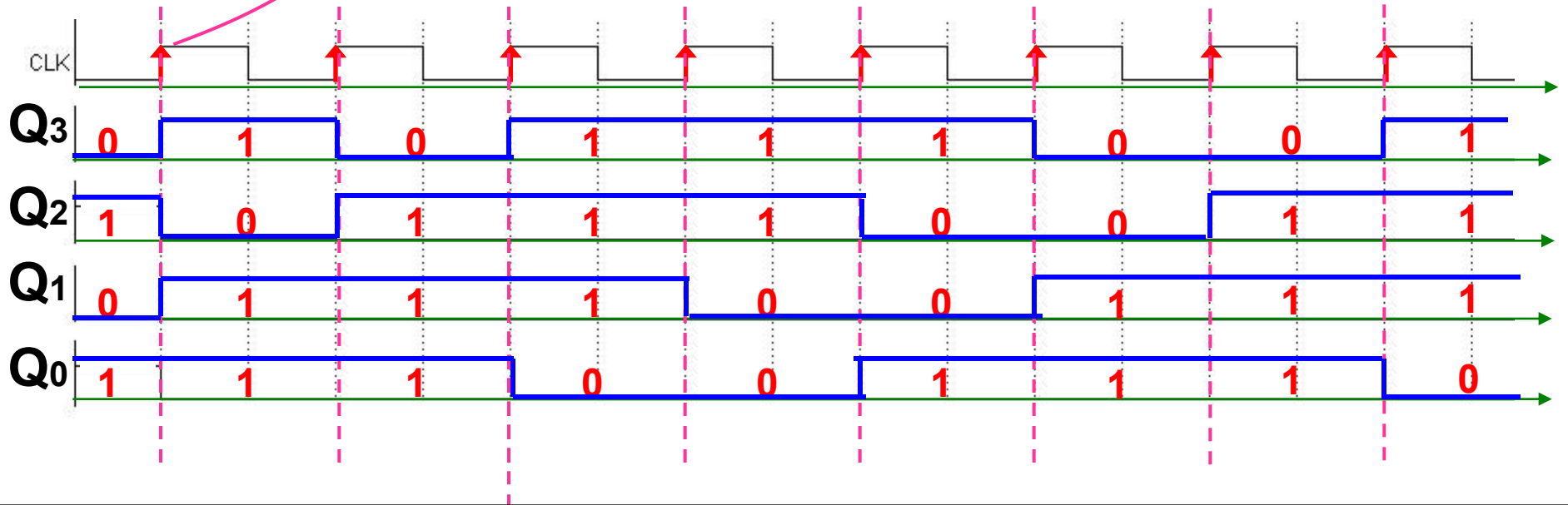
4)功能分析

五进制计数器，能自启动





5) 波形图, 假设Q3Q2Q1Q0初值为0101



6.3.2 计数器

应用：用于计数、分频、定时、产生节拍脉冲等

分类：按时钟分，同步、异步

按计数过程中数字增减分，加、减和可逆

按计数器中的数字编码分，二进制、二-十进制和循环码…

按计数容量分，十进制，六十进制…

一、同步计数器

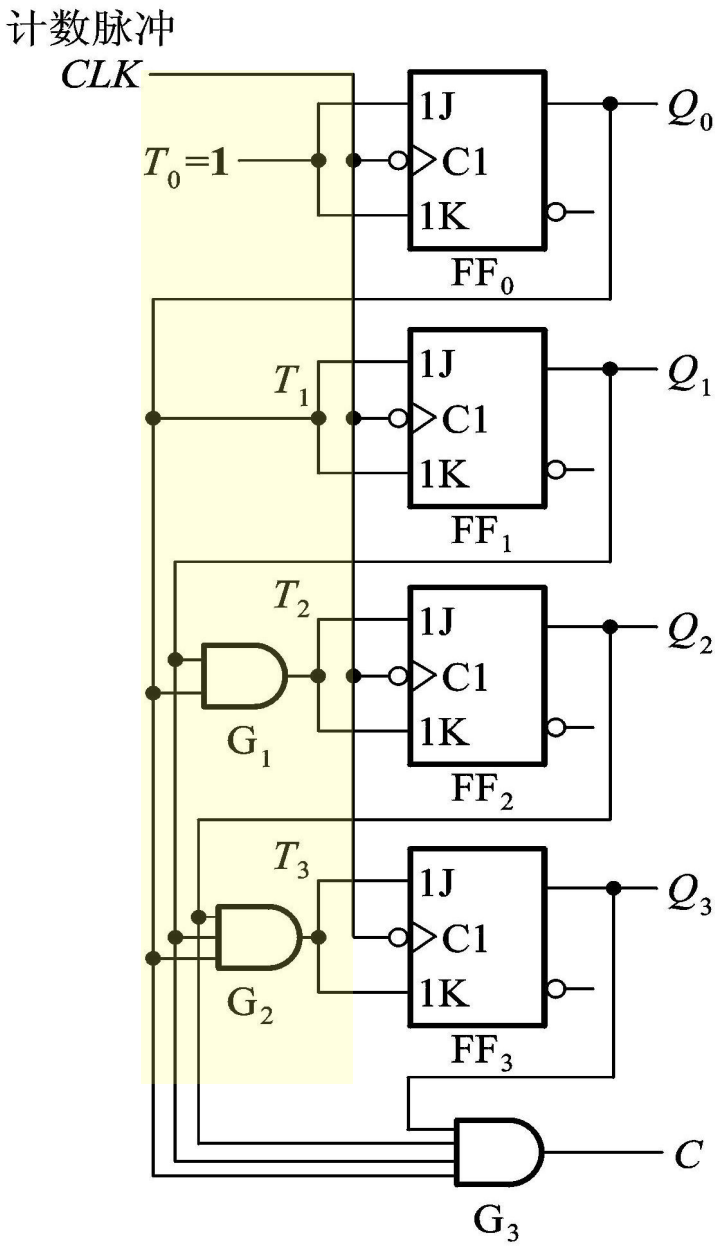
1、同步二进制加法计数器

原理：根据二进制加法运算规则可知：在多位二进制数末位加1，若第i位以下皆为1时，则第i位应翻转。

由此得出规律，若用T触发器构成计数器，则第i位触发器输入端T_i的逻辑式应为：

$$T_i = Q_{i-1}Q_{i-2}\cdots Q_0$$

$$T_0 \equiv 1$$

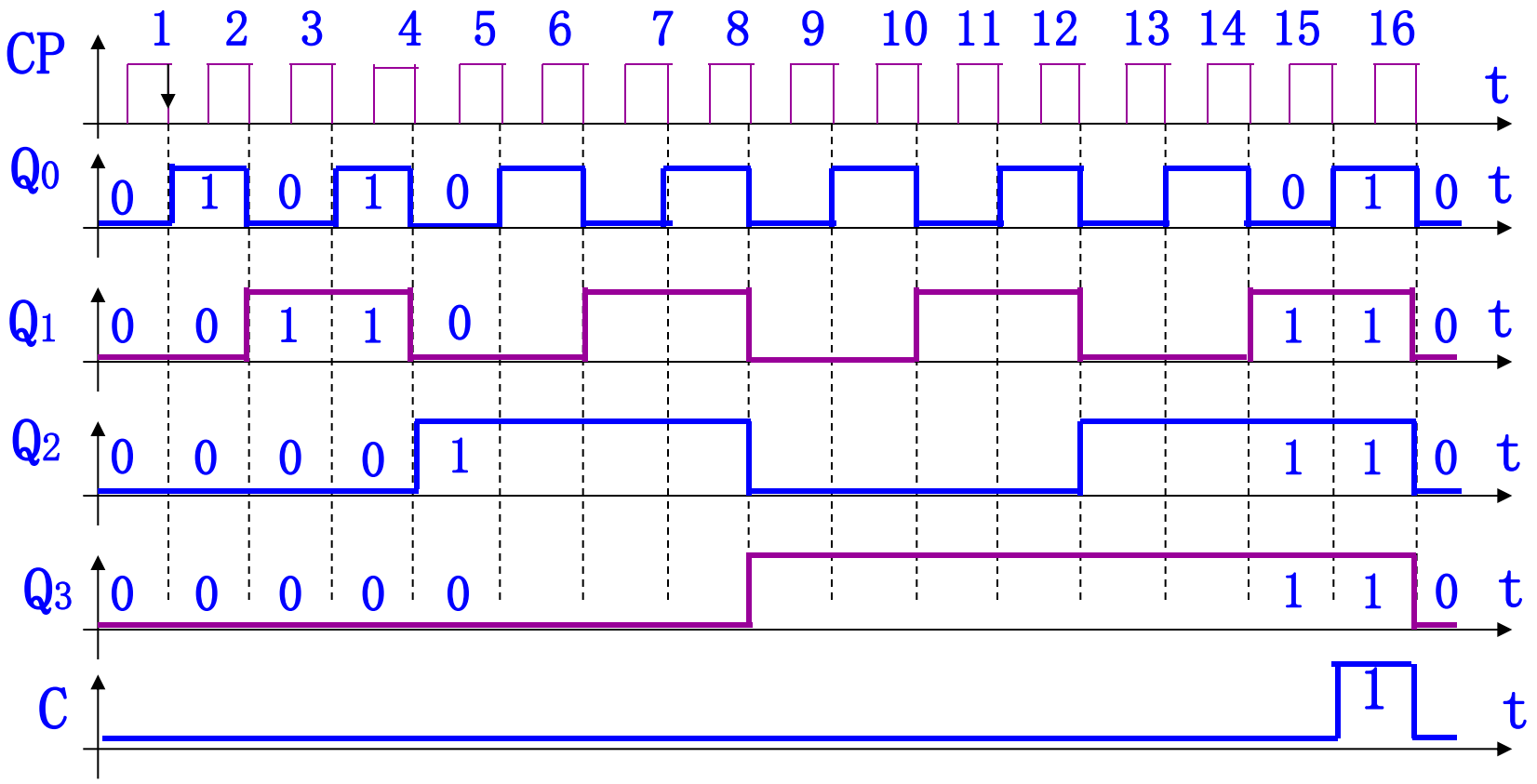


(3)时序波形图

已知：

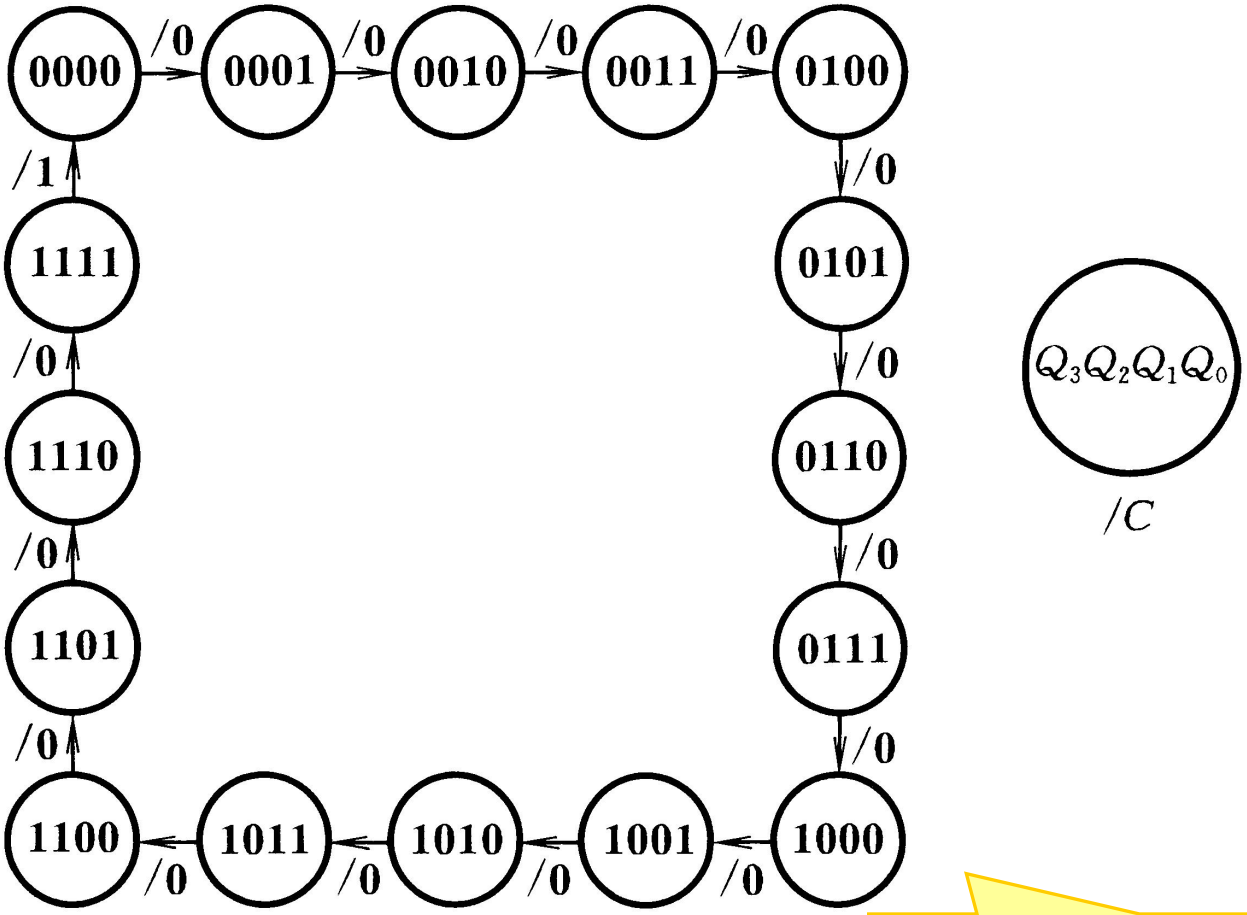
$$\begin{cases} T_0=1 \\ T_1=Q_0 \\ T_2=Q_1Q_0 \\ T_3=Q_2Q_1Q_0 \end{cases}$$

$C=Q_3Q_2Q_1Q_0$



(4) 状态转换情况

状态转换图



逻辑功能：4位同步二进制加法计数器

分析功能

这是二进制加法计数器。

计数器的另一个作用是分频：

若CLK的频率为 f

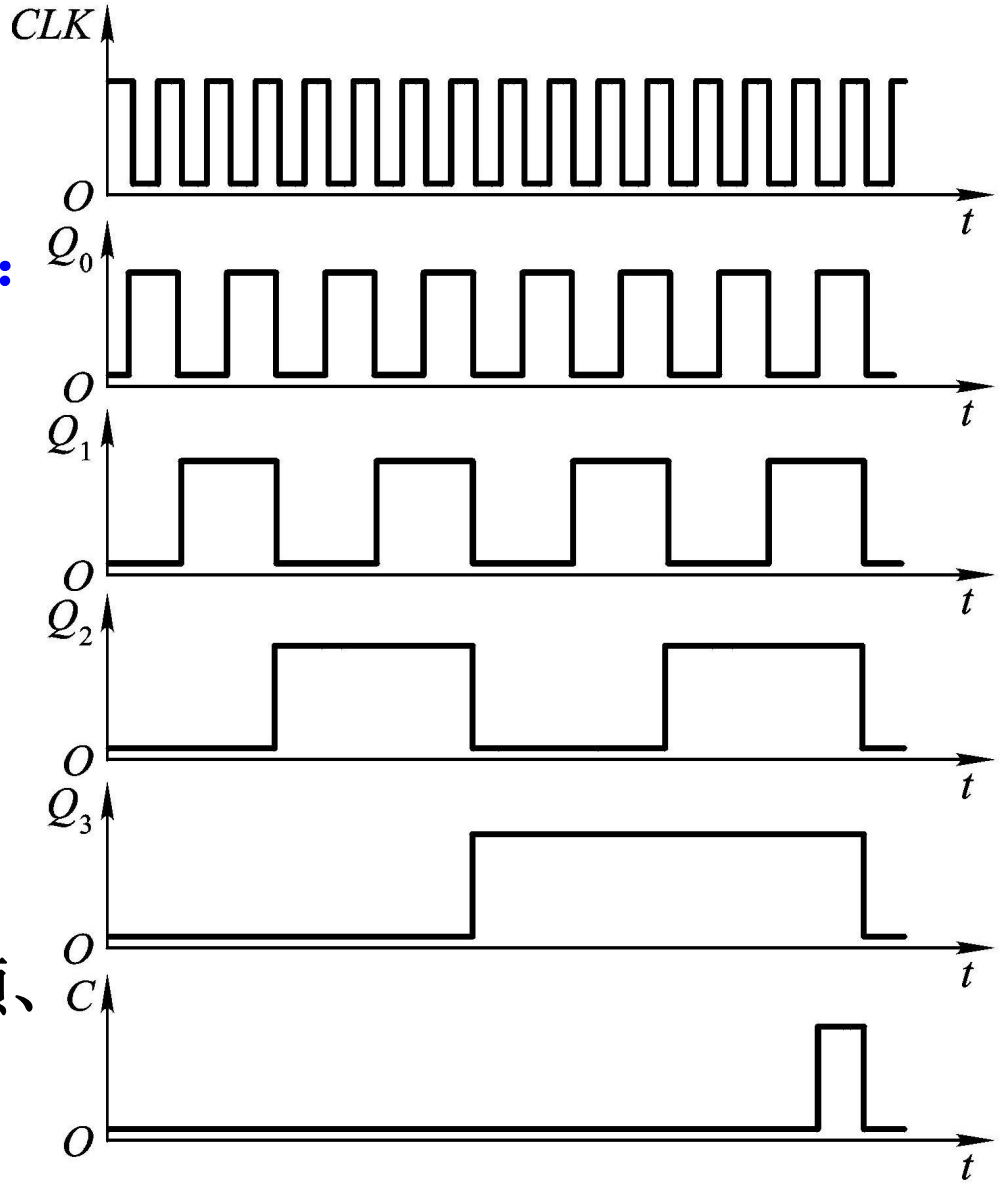
则Q_0端输出脉冲频率为$1/2\,f$

Q_0端为二分频端

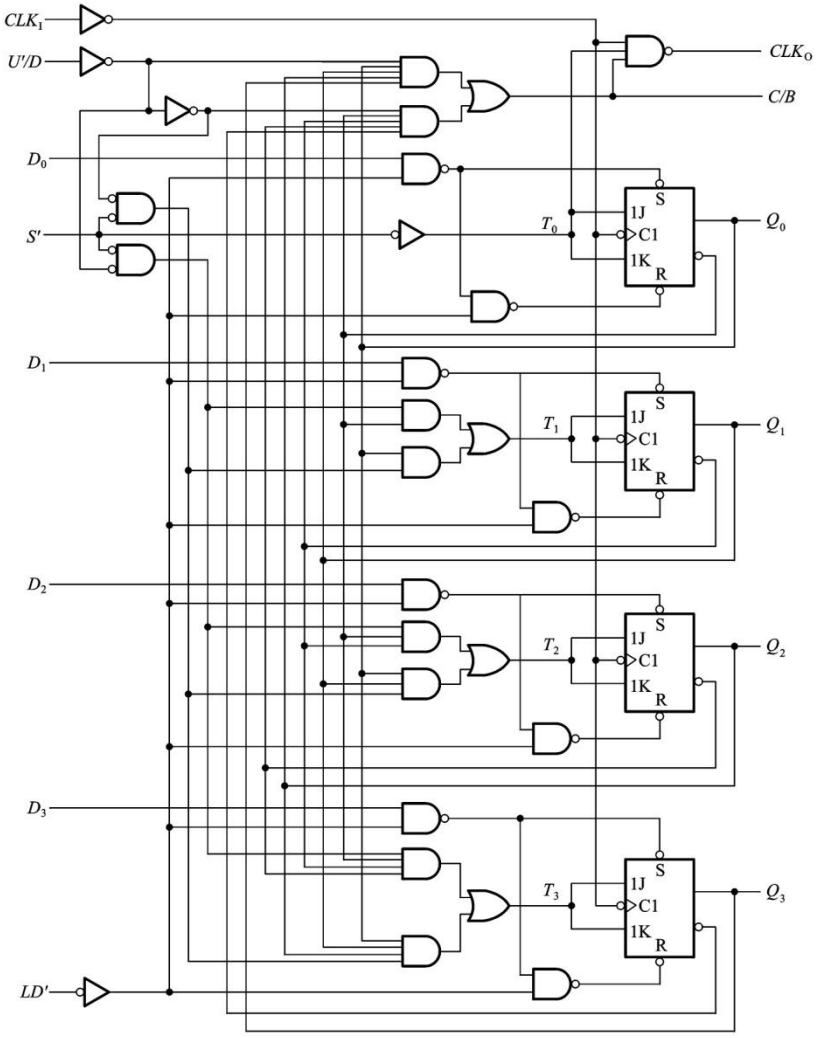
同理：

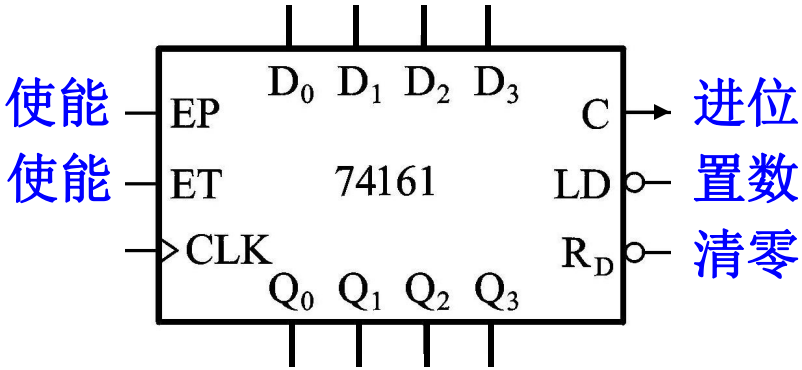
Q_1、Q_2、Q_3端分别为四分频、八分频和十六分频端。

时序图



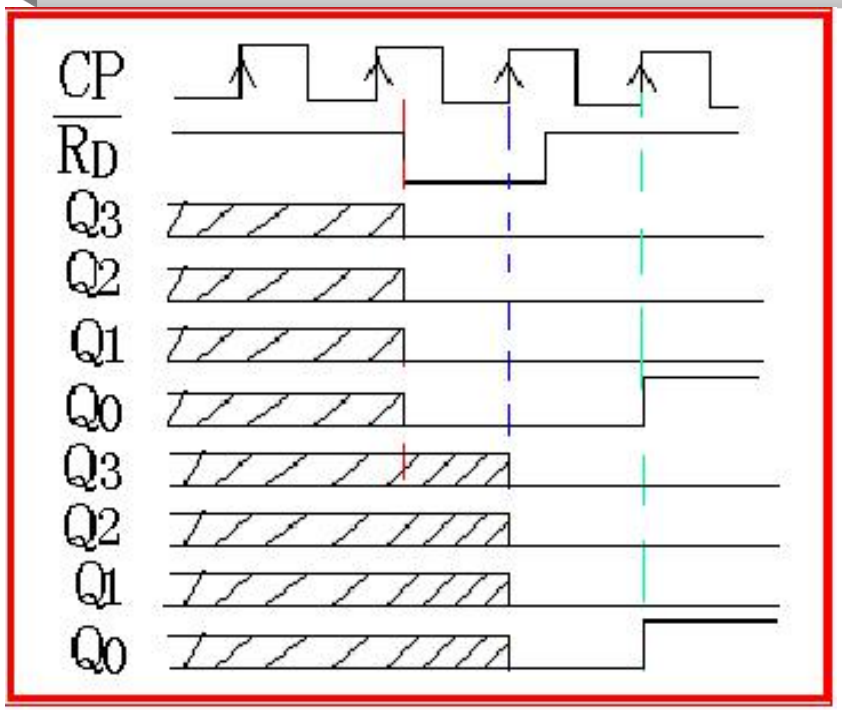
器件实例： 74LS161 4位同步二进制计数器

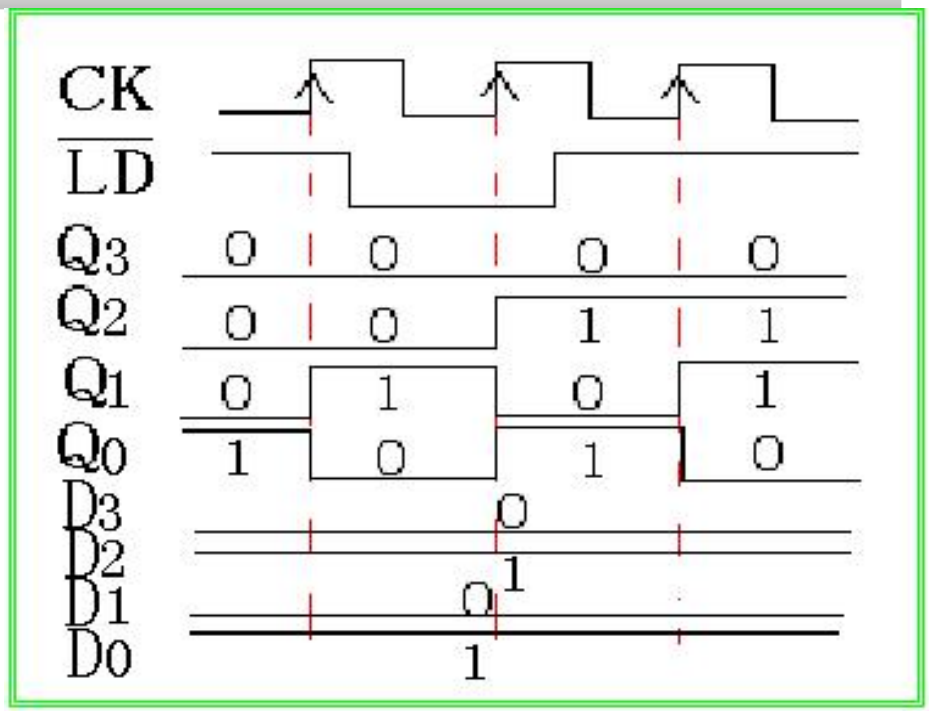


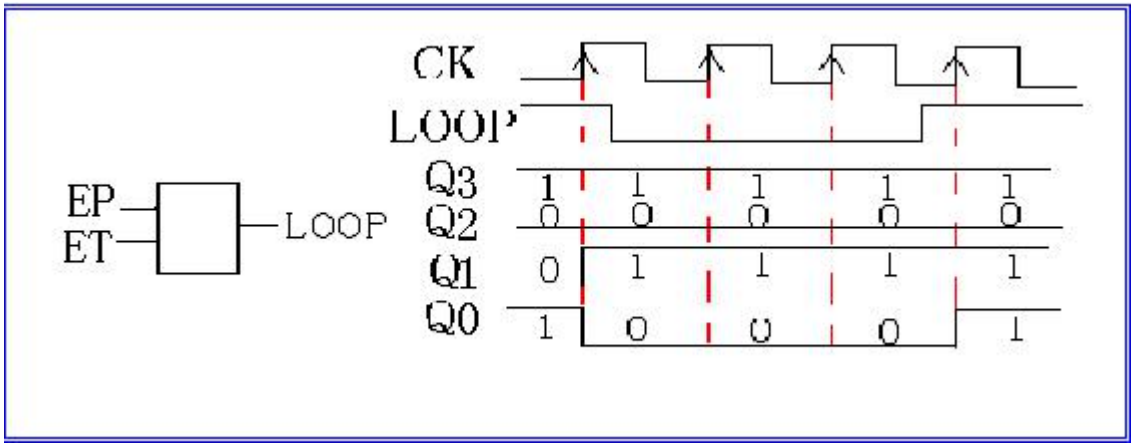


CLK	R'_D	*LD'*	*EP*	*ET*	工作状态
X	0	X	X	X	置 0（异步）
↑	1	0	X	X	预置数（同步）
X	1	1	0	1	保持（包括C）
X	1	1	X	0	保持（C=0）
↑	1	1	1	1	计数

四位二进制同步计数器

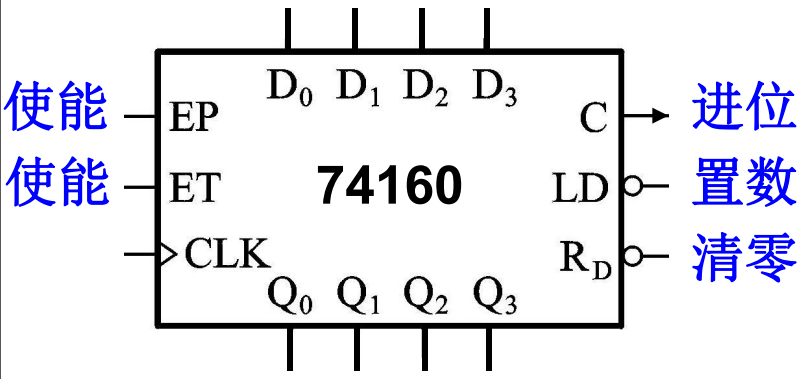

CP
$\overline{R_D}$
Q3
Q2
Q1
Q0
Q3
Q2
Q1
Q0


CK
$\overline{LD}$
Q3 0 0 0 0
Q2 0 0 1 1
Q1 0 1 0 1
Q0 1 0 1 0
D3 0
D2 1
D1 0
D0 1


EP
ET
LOOP
CK
LOOP
Q3 1 1 1 1 1
Q2 0 0 0 0 0
Q1 0 1 1 1 1
Q0 1 0 0 0 1

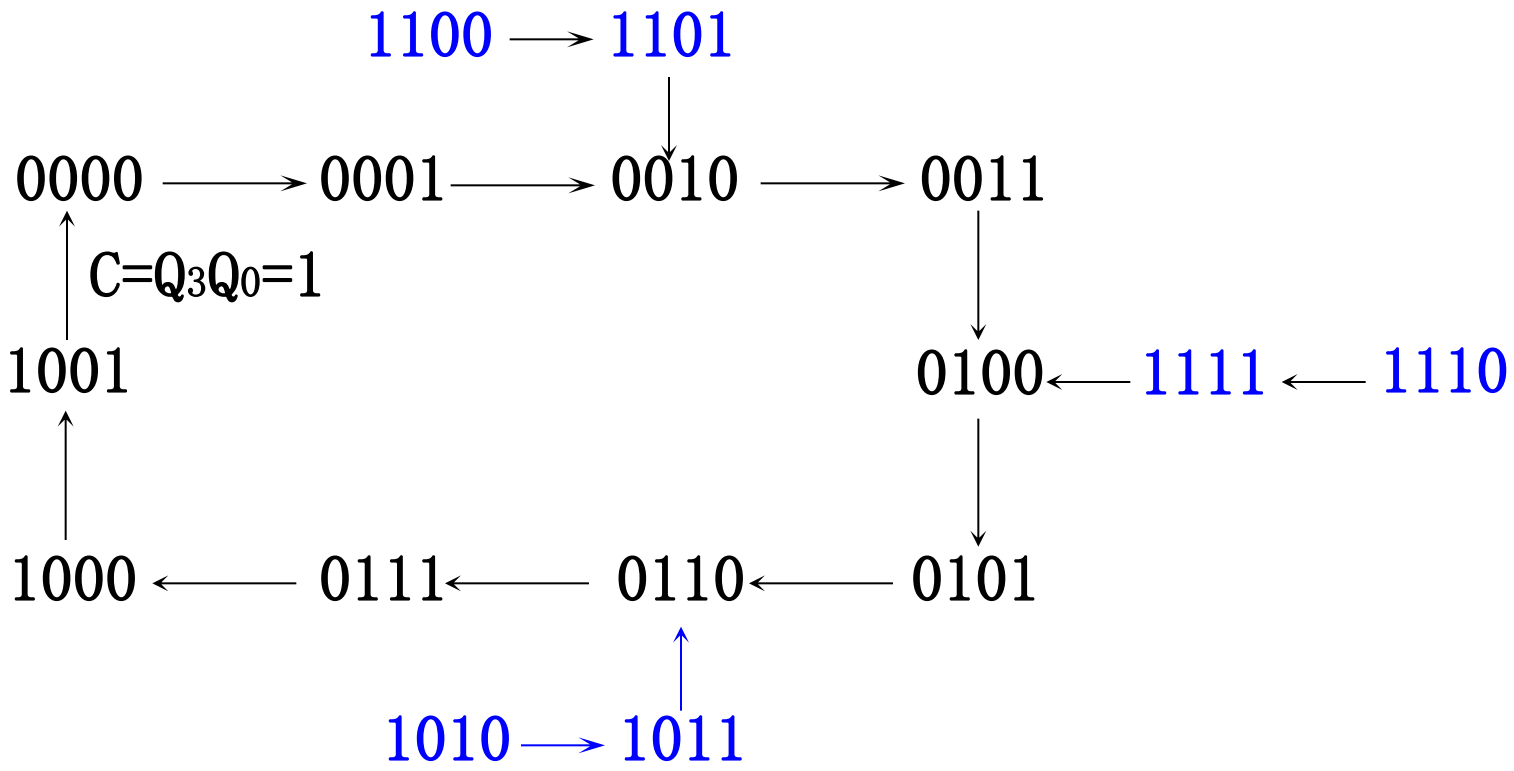
器件实例： 74LS160 4位同步十进制计数器

- 集成同步十进制加法计数器74LS160。电路框图、功能表和74LS161相同，但输出只有0000－1001十个稳定状态。



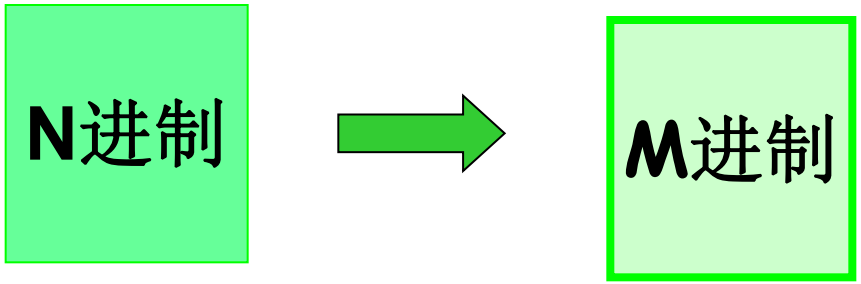
CLK	R'_D	*LD'*	*EP*	*ET*	工作状态
X	0	X	X	X	置 0（异步）
↑	1	0	X	X	预置数（同步）
X	1	1	0	1	保持（包括C）
X	1	1	X	0	保持（C=0）
↑	1	1	1	1	计数

74LS160的状态转换图（$Q_3Q_2Q_1Q_0$）



三、任意进制计数器的构成方法

将已有的N进制芯片，组成M进制计数器，是常用的方法。



有两种情况：$\begin{cases} N > M \\ N < M \end{cases}$

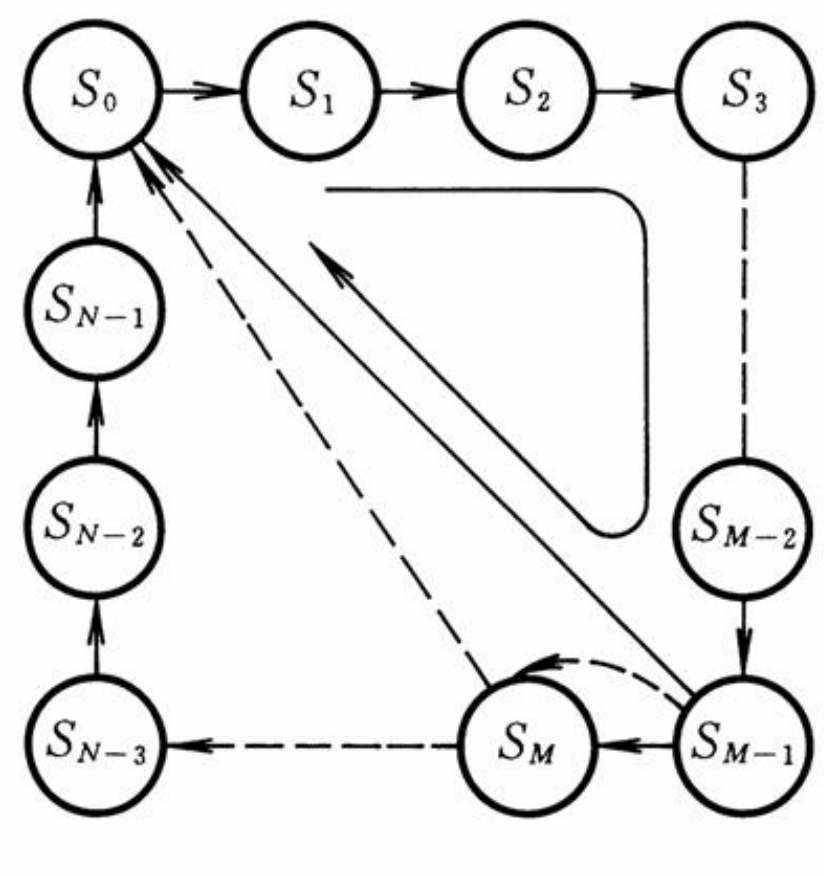
1、N > M

原理：计数循环过程中设法跳过N-M个状态。

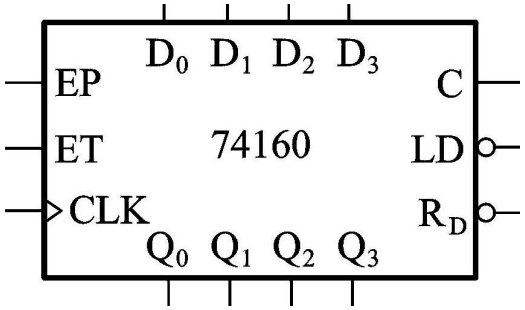
具体方法：置零法和置数法两种。

（1）置零法

- 异步置零法
- 同步置零法



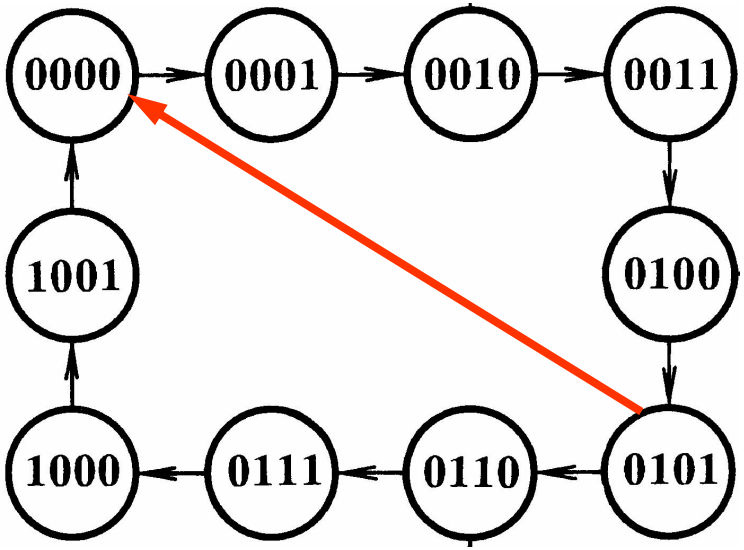
例：将十进制的74160接成六进制计数器

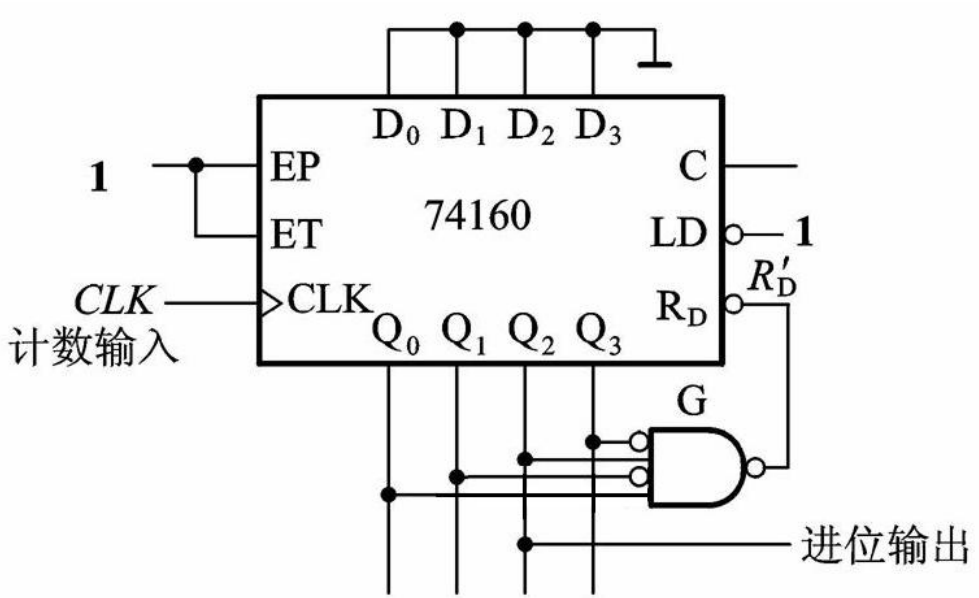


CLK	R'_D	*LD'*	*EP*	*ET*	工作状态
X	0	X	X	X	置 0（异步）
↑	1	0	X	X	预置数（同步）
X	1	1	0	1	保持（包括C）
X	1	1	X	0	保持（C=0）
↑	1	1	1	1	计数

例：将十进制的74160接成六进制计数器

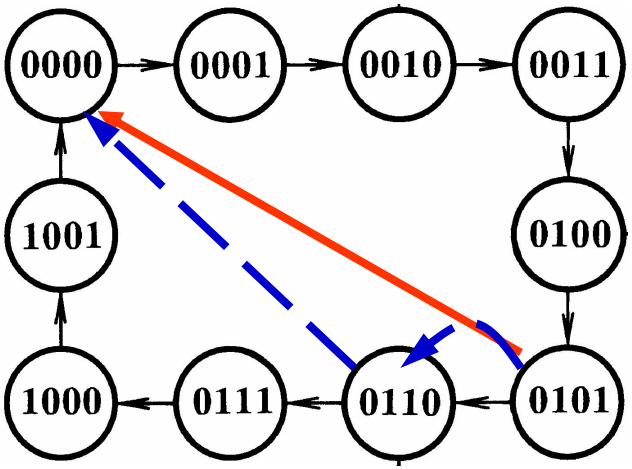
异步置零法

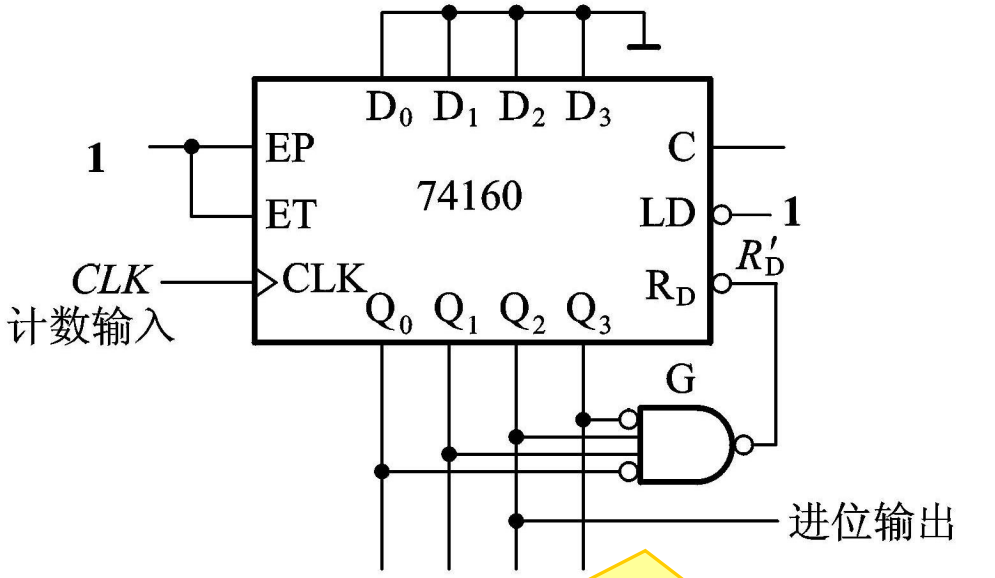




这样连接对吗？

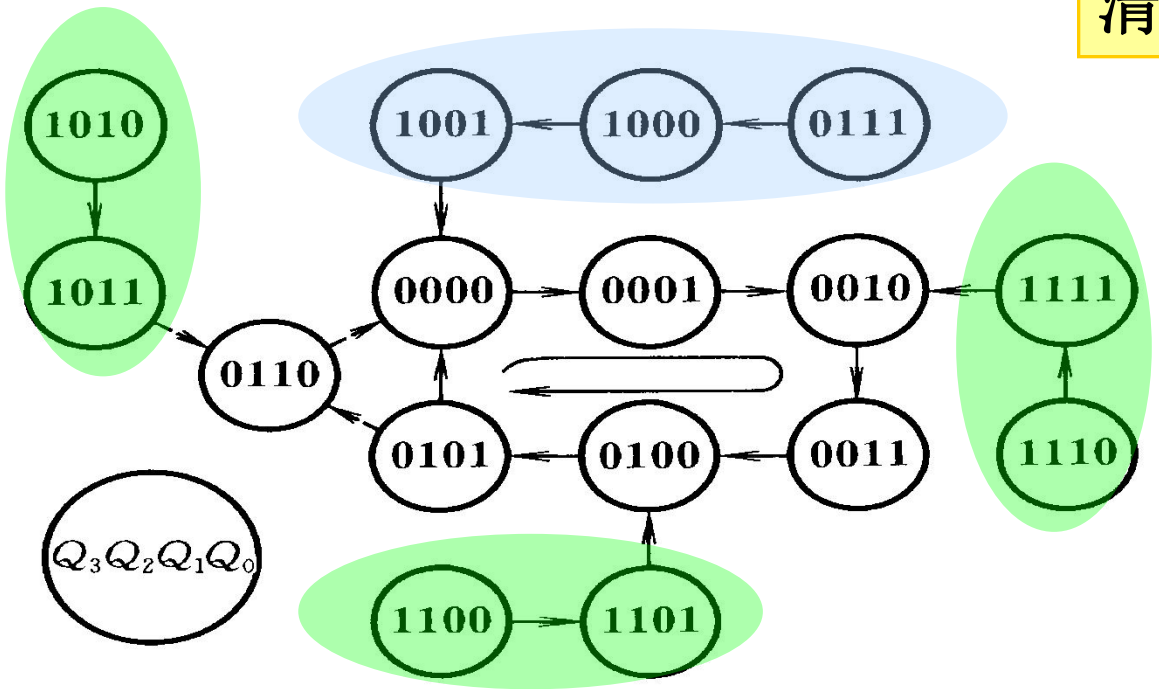
异步置零法

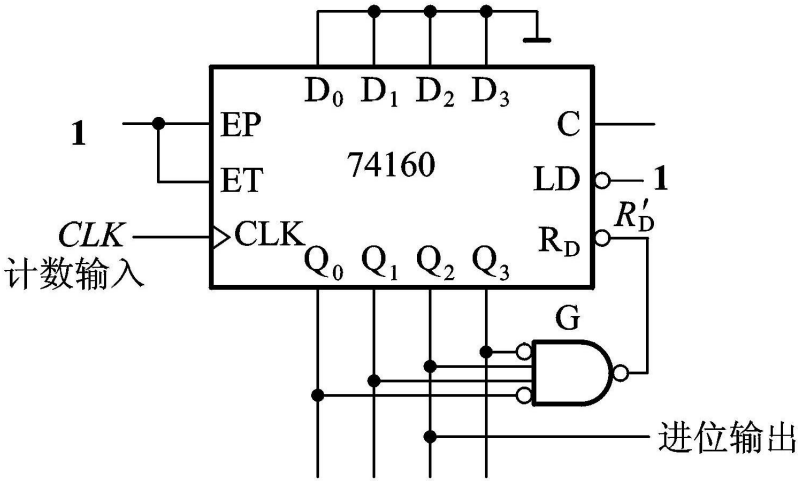


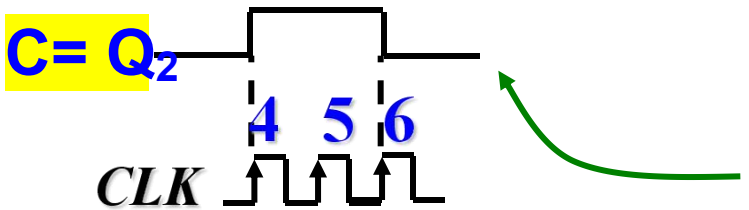


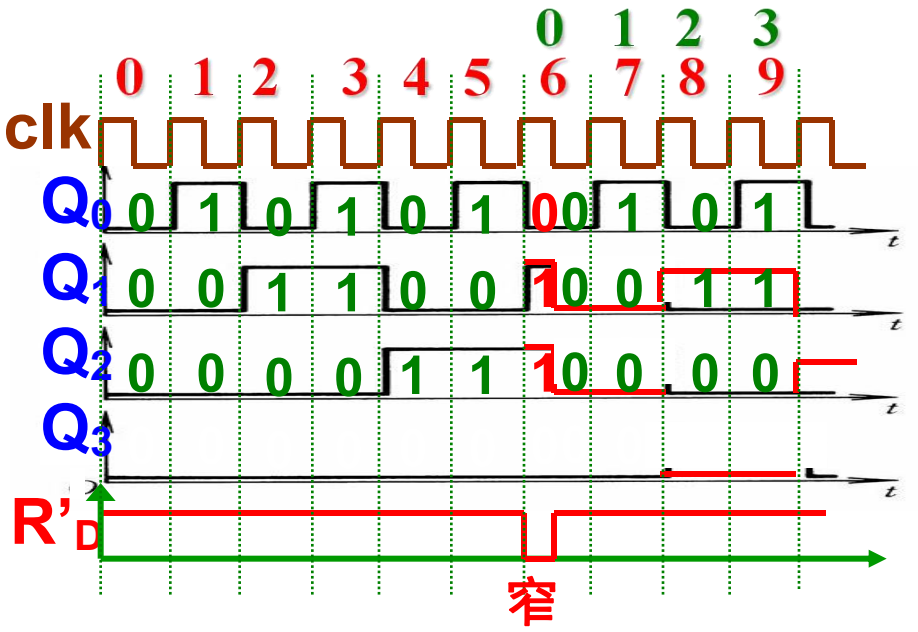
清零信号取0110

状态转换图

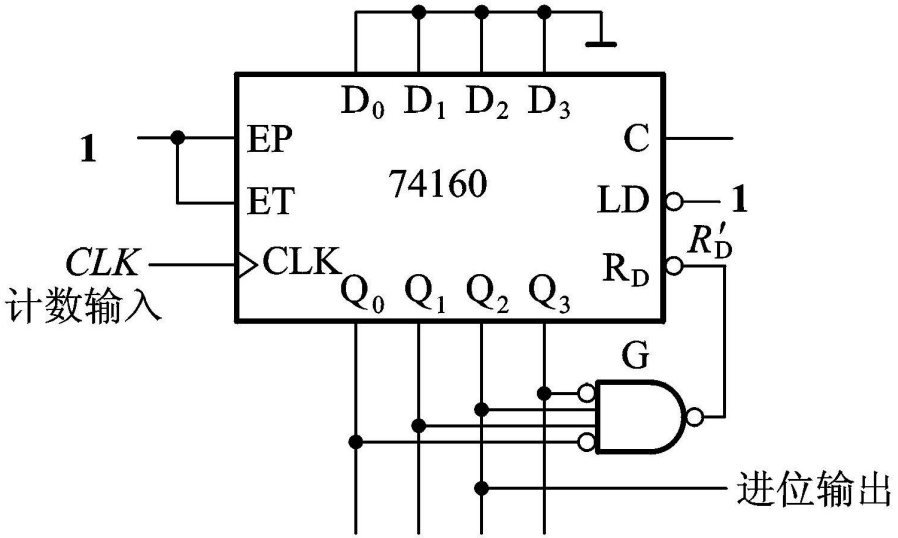




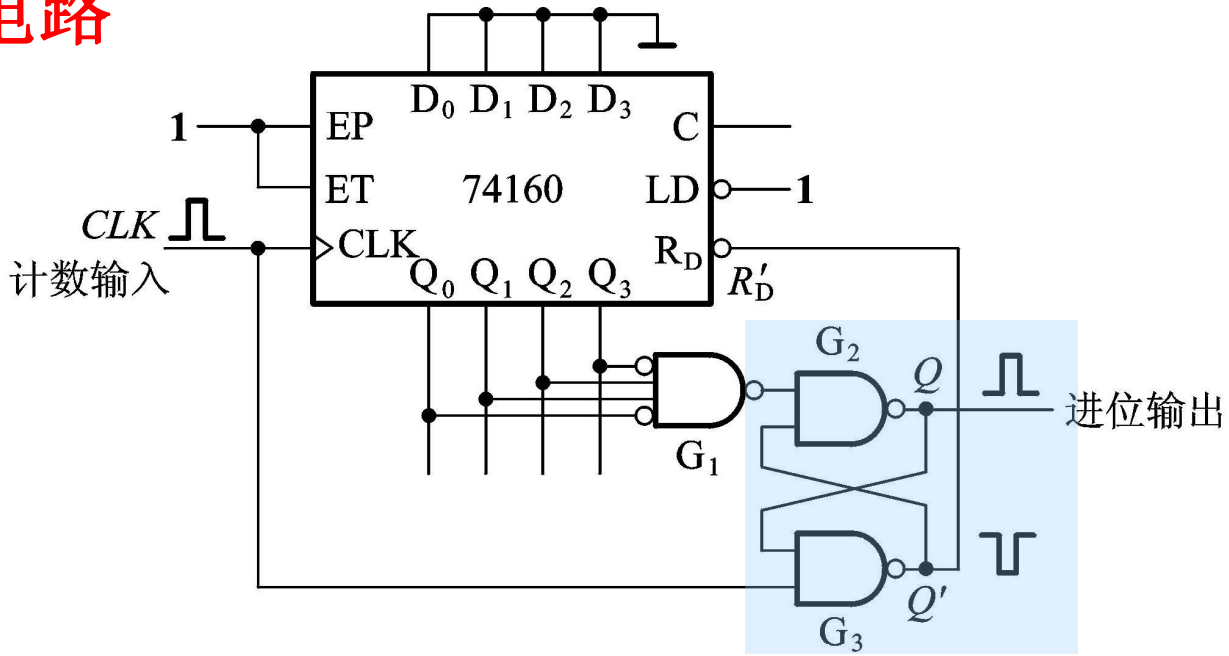


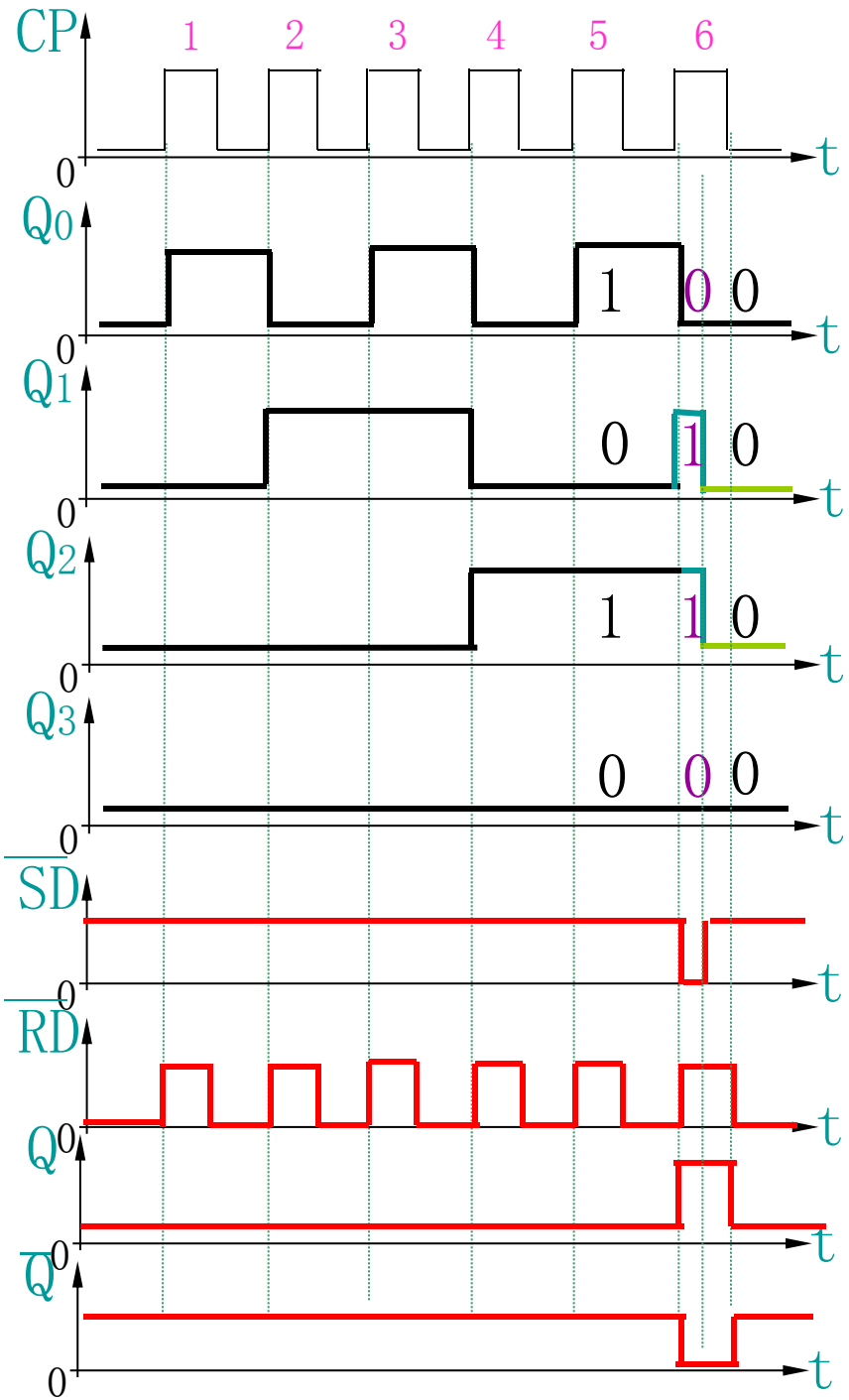


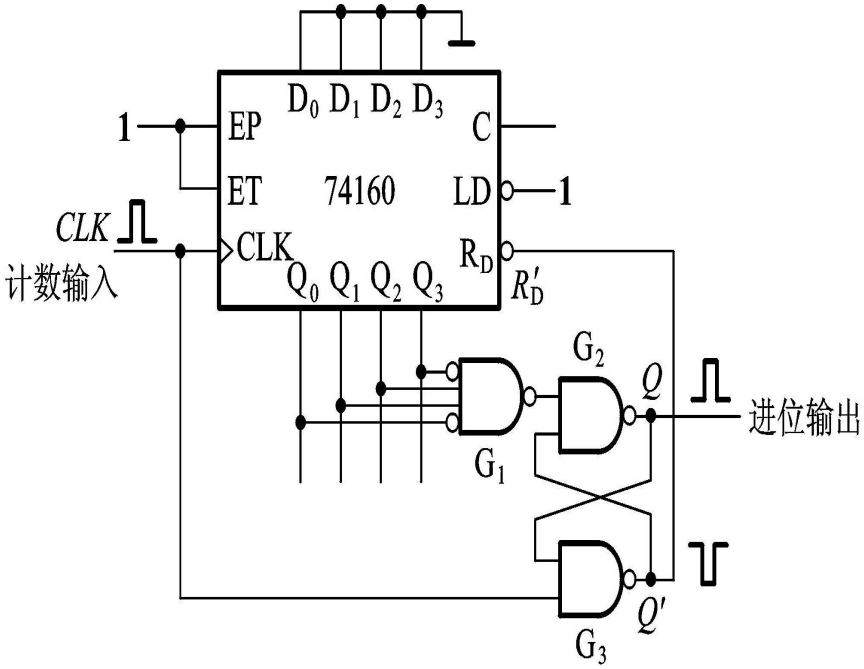
缺点：置0信号作用时间短


D0 D1 D2 D3
1
EP
ET
CLK
计数输入
74160
C
LD
1
R'D
RD
Q0 Q1 Q2 Q3
G
进位输出

改进电路


D0 D1 D2 D3
1
EP
ET
CLK
计数输入
74160
C
LD
1
RD
R'D
Q0 Q1 Q2 Q3
G2
Q
进位输出
G1
Q'
G3


CP
1 2 3 4 5 6
0
t
Q0
1 0 0
Q1
0 1 0
Q2
1 1 0
Q3
0 0 0
SD
RD
Q
Q'


1
EP
ET
CLK
计数输入
CLK
74160
D0 D1 D2 D3
C
LD
1
RD
R'D
Q0 Q1 Q2 Q3
G1
G2
G3
Q
Q'
进位输出