

Digital Logic Design

- Lecture 0
- Workstation and Linux -

2025 Spring



Agenda .

- 1. Login Workstation
- 2. Linux / VIM Basic Commands
- 3. CAD / VIM Environment Setting
- 4. Verdi / nWave Basic Operations
- 5. Git Version Control

Login Workstation •

Open MobaXterm



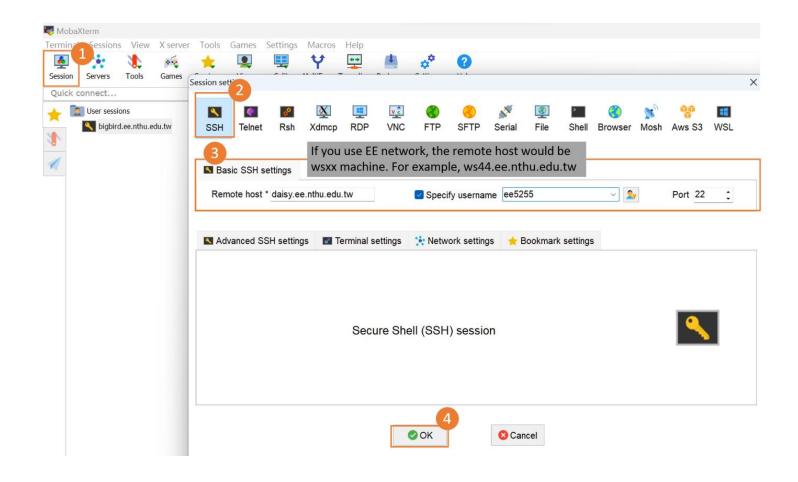
Host:

if not in EE network

- daisy.ee.nthu.edu.tw
- bigbird.ee.nthu.edu.tw

if in EE network

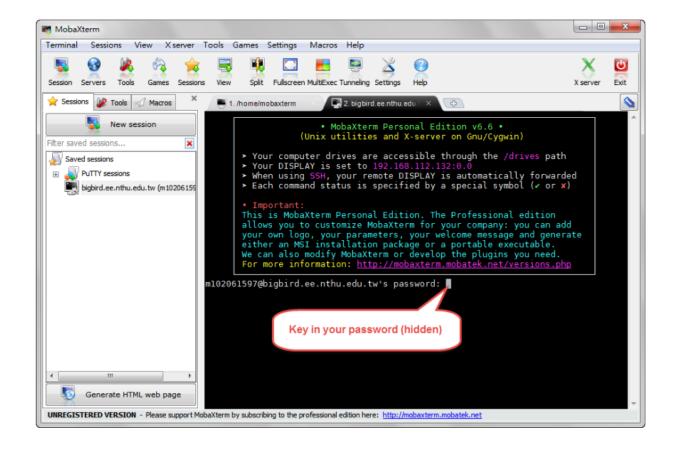
- wsXX.ee.nthu.edu.tw
- (wsXX from ws25~ws48)
- Username:
 - <your account>



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Login Workstation •

- Enter password
- If you are in daisy or bigbird
 - \$ ssh -X wsXX
 - (wsXX from ws25~ws48)
- 登入後請用 yppasswd 指令 來更改您的密碼。



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Reference -

- EE工作站 登入說明
 - https://web.ee.nthu.edu.tw/var/file/175/1175/img/1191/1030310-LoginWS.pdf
- EE工作站 常見問題
 - https://web.ee.nthu.edu.tw/var/file/175/1175/img/1191/wsqq.pdf
- CAD Tool List
 - https://web.ee.nthu.edu.tw/p/405-1175-169285,c4918.php?Lang=zh-tw

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Linux Basic Commands ...

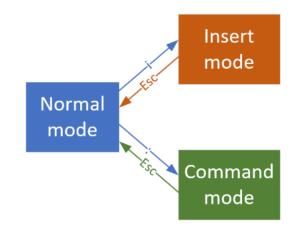
- \$ pwd
 - print working directory
- \$ mkdir
 - make directory
- \$ Is
 - list the contents of a directory
- \$ cd
 - change directory
- \$ rm
 - remove (delete)
- \$ cp
 - Copy
- \$ mv
 - move (rename)

- \$ touch
 - create an empty file
- \$ chmod
 - change mode (permission)

- "Tab" key
 - for command or filename completion

Vim mode ...

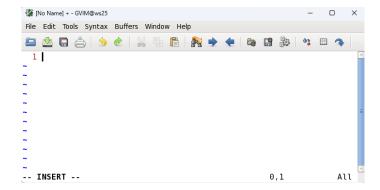
- Vim is a powerful text editor in Linux
- \$ vim
- \$ gvim (with GUI)
- \$ vim <filename>
 - Open a file named <filename>



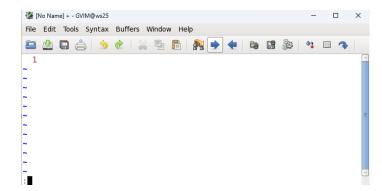
Normal mode



Insert mode



Command mode



Vim Normal mode command ...

- Enter insert mode to edit the file
- Enter command mode
- V
 - Enter visual mode (still in normal mode)
 - For selecting text
- - Enter visual mode (still in normal mode)
 - For selecting line
- gg
 - Move to first row
- G
 - Move to last row
- ggVG
 - Select all lines in the file

- У
 - copy
- р
 - paste
- delete

VIM Command mode Commands ...

Esc

Exit Command mode and return to Normal mode

i.W

Write (save file)

p:

Quit vim

wq:

Write and Quit

:w!

Force write (a read-only file)

! p:

Quit without saving

• :wq!

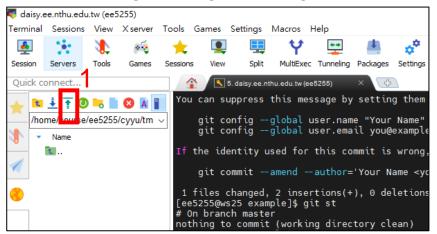
Force write and quit

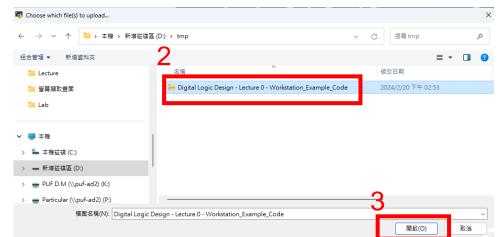
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CAD Environment Setting .

Or upload Digital_logic_Design_Lecture0.zip (/home/course/<username>/)





- \$ unzip Digital_Logic_Design_Lecture0.zip
- \$ cd Digital_Logic_Design_Lecture0

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CAD Environment Setting .

- \$ cd
 - To your user directory (/home/course/<username>/)
- \$ touch .tcshrc
- \$ vim .tcshrc

- \$ source .tcshrc
- (or re-login, will automatic source .tcshrc)
- (or copy Digital_Logic_Design_Lecture0/,tcshrc to user directory
- \$ls –la
 - To find .tcshrc in Digital_Logic_Design_Lecture0 folder

#vcs
source /usr/cadtool/user_setup/08-vcs.csh

#verdi nWave
source /usr/cadtool/user_setup/08-verdi.csh

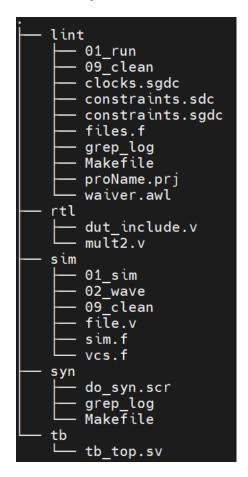
#Design Compiler
source /usr/cadtool/user_setup/08-synthesis.csh

#Spyglass
source /usr/cadtool/user_setup/08-spyglass.csh

#vcs-mx
alias src_dve 'source /usr/cadtool/user_setup/08-vcs-mx.csh'

#others
alias grep 'grep --color=auto'

\$ unzip module_mult2.zip



\$ cd module_mult2

Setup Example Folder •

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Run Lint ...

- \$ cd lint/
- ./01_run
 - pass

```
Goal Violation Summary:
Waived Messages:
Reported Messages:
O Fatals, O Errors, O Warnings, O Infos
Reported Messages:
Spyglass.log successfully updated with goal summary
```

- no pass
lint check fail !!! Severity: Warning

./09_clean

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Run Simulation Using VCS .

- \$ cd ../sim/
- \$./01_sim

Time: 100000 ps

```
0.640 seconds;
                                                    Data structure size:
                                                                       0.0Mb
                    CPU Time:
                    Fri Feb 24 16:04:29 2023
                    CPU time: .433 seconds to compile + .379 seconds to elab + .493 seconds to link + .687 seconds in simulation
                    simulation pass
                               01 sim VCS.f sim.f file.v
                                 1 -P /usr/cadtool/cad/synopsys/verdi/cur/share/PLI/
                                                                                                        module mult2/
                                 2 /usr/cadtool/cad/synopsys/verdi/cur/share/PLI/VCS
                                                                                                         rtl/
                                 3 -sverilog
01_sim vcs.f sim.f file.v
                                                                                                             dut include.v
                                                                                                             mult2.v
 1 rm -rf simv
                               01_sim vcs.f sim.f file.v
                                                         01 sim vcs.f sim.f file.v
                                                                                                         sim/
 2 rm -rf simv.daidir
                                                                                                             01 sim*
                                 1 //time scale
   vcs -full64 -R
                                                                                                             02 wave*
                                 2 //waveform
                                                          2 `timescale lns/lps
        -f vcs.f \
                                                                                                             09 clean*
                                 3 +define+USE FSDB
                                                                                                             file.v
        -f sim.f ∖
                                 4 +FSDB
                                                          4 //testbench
        -l sim.log \
                                                                                                             sim.f
                                                             `include "../tb/tb top.sv
        "$@"
                                                                                                             vcs.f
                                 6 //////////////
                                                                                                           tb/
                                 7 //files
                                                          7 //design
                                                                                                             tb top.sv
                                                          8 `include "../rtl/dut include.v
                                 8 +incdir+./
                                 9 file.v
```

Report

Simulation

Synthesize .

- cd ../syn
- \$ make 01
- \$ gvim syn_timing.log
 - check timing

```
61 -----62 data required time 9.47
63 data arrival time -5.66
64 -----65 slack (MET) 3.81
```

- \$ gvim syn_area.log
 - check area

\$ make 90

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Vim Environment Setting .

- \$ cd
 - To your user directory (/home/course/<username>)
- \$ touch .vimrc
- Edit .vimrc

set guifont=monospace\ 12 set autoindent expandtab tabstop=3 shiftwidth=3 set number

- Press "tab" to enter 3 spaces
- Keep indent during newline.
- Display line number

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Vim Environment Setting .

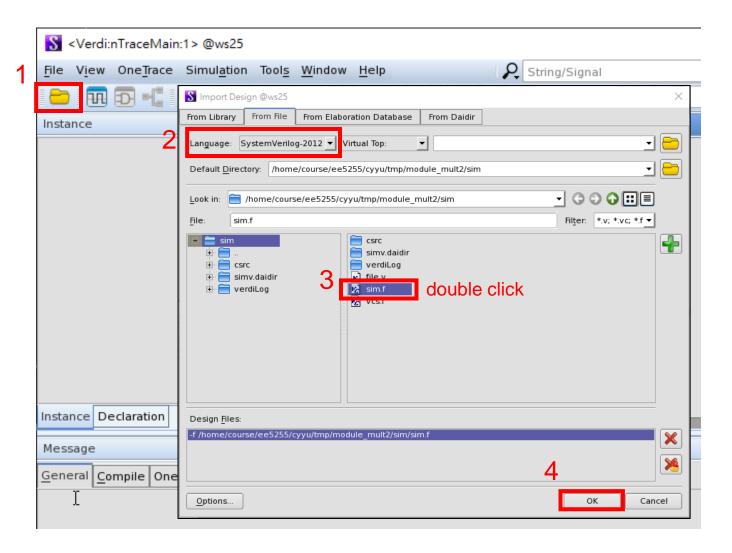
- \$ cd
 - To your user directory (/home/course/<username>)
- \$ mkdir -p .vim/syntax/
- Upload file filetype.vim to
 - .vim/
- Upload file systemverilog.vim to
 - vim/syntax/
- \$ vim module_mult2/tb/tb_top.sv
 - Will see code with highlight

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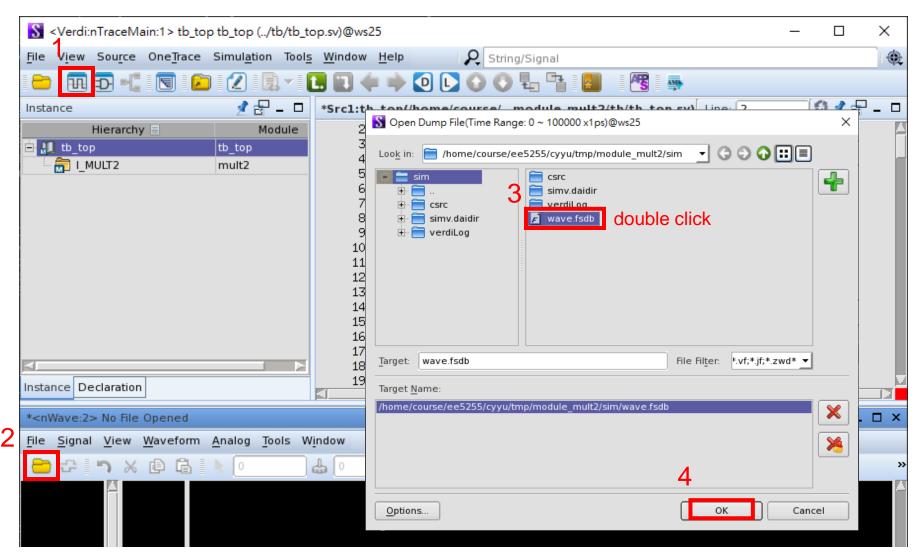
Open Verdi .

- \$ cd module_mult2/sim/
- \$ verdi &
- adding "&" after a command runs in the background, allowing you to continue using the terminal



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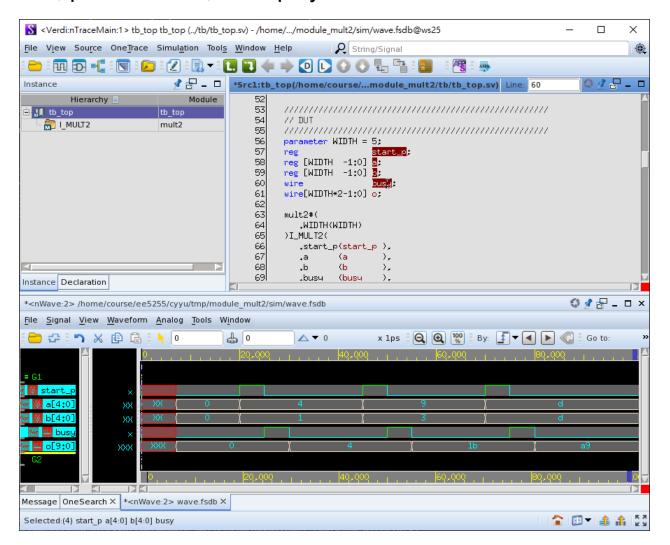
Open nWave in Verdi



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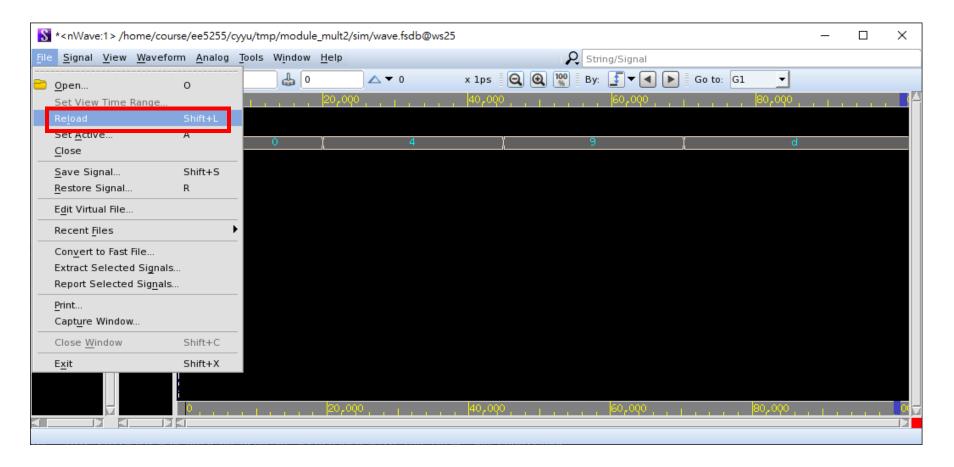
View Signal in Verdi and nWave

Select the signal in Verdi, press "ctl+w", to display the waveform on the nWave



Reload waveform -

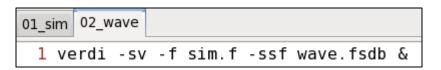
You can use "shift+L" to reload fsdb after changing the code or simulation.



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View Signal in Verdi and nWave

Or use\$./02_wave

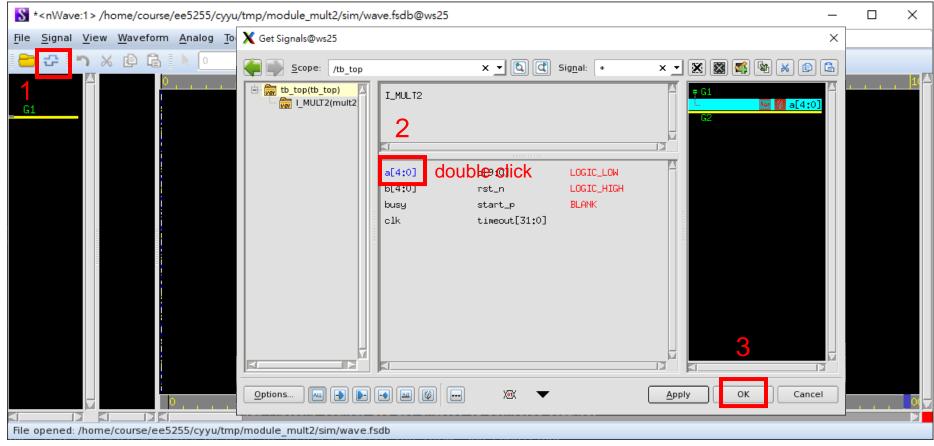


to open Verdi and nWave

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Open nWave Only ...

- Because Verdi take more resources, sometimes it is very slow. If necessary, you can only open nWave.
- \$ nWave &



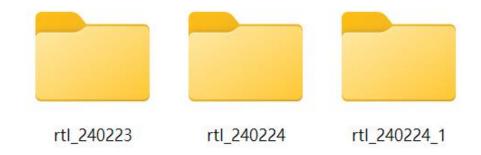
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Git Introduction ...

Without version control, workspaces can become complex over time.



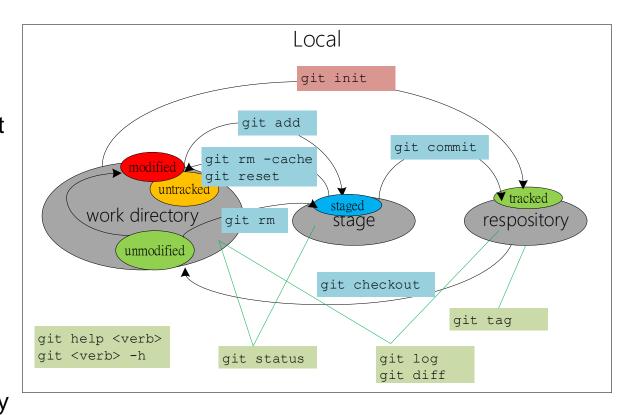
With version control, your workspace will be clean and your editing information will be preserved.

```
[ee5255@ws25 rtl]$ git log --pretty=format:"%h %ad : %s"
21e4430 Thu Feb 22 23:11:02 2024 +0800 : clear the lint warning
cc82ec2 Thu Feb 22 22:48:55 2024 +0800 : finish the design
d342f23 Thu Feb 22 22:44:34 2024 +0800 : create alu.v file
```

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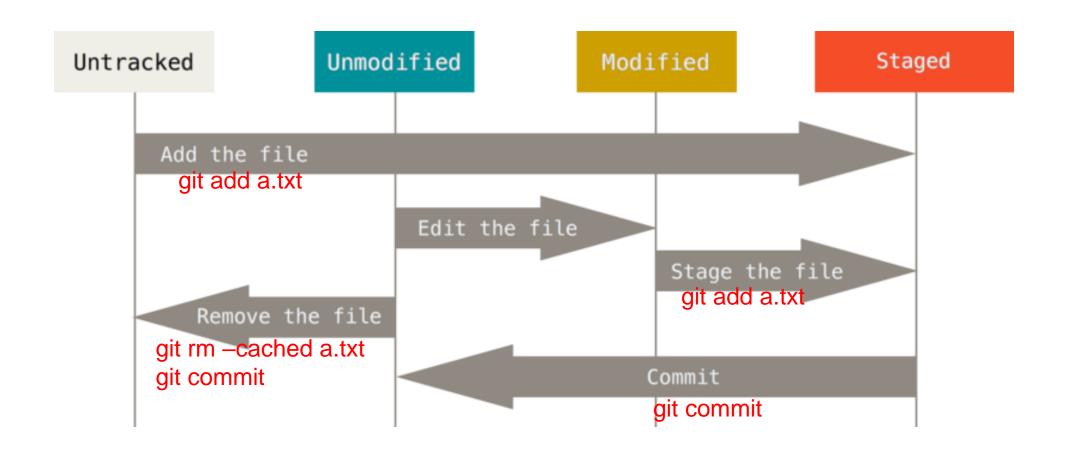
Git Quick Guide ...

- Git is a version control system that helps developers to track changes to their source code.
- Create a new Git repository in the current directory\$ git init
- Making untracked or modified files be tracked in Git
 \$ git add <filename> → staged
 \$ git commit → unmodified in work directory
 tracked in repository
- Deleting unmodified files in Git
 \$ git rm <filename> → staged
 remove in work directory
 \$ git commit → remove be tracked in git repository



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Git file status



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Git Quick Guide ...

- \$ cd <new_dir>
 - which you want to use it as the root of this git project.
- \$ git init
 - create a new Git repository in the current directory
- \$ git status
 - shows the current status of the repository
- \$ git add <filename>
 - add the specified file to the staging area
- \$ git commit -m "commit message"
 - save the changes to the repository with a message describing the changes
- \$ git rm <filename>
 - remove a file from the Git repository

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Git Quick Guide

- \$ git log
 - shows the commit history, type "q" to exit
- \$ git reset
 - Reset a files or commit (discard followed by commit)(won't modify files)
- \$ git checkout
 - checkout a file or commit (discard changes of files)(will modify the files)

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Feedback to us -



https://forms.office.com/r/DYDu8vLaWN

Thank you!



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