Design Project: Charge Pump Circuit for embedded NVM

Deadline: June 4th 2025

Please upload your report and the .sp files to EEclass.

1. Report: ID_name.pdf
2. .sp files: ID_name.zip

I. Project description:

This project is to design a Charge Pump for embedded NVM applications. Use HSPICE or other SPICE-like simulator to demonstrate that the design meets the targets below and to generate all required plots. List reference papers for the design you adapted.

Design Targets

Design Charge Pumps that generate the V_{PP} for embedded NVM applications. Design targets are listed below.

V_{PP} = 10V for a load of (C_L=100pF, I_L=500μA). The target transient time < 0.1ms.

Transistor Model:

V_{DD} = 1.8V

Operation Clock Period (T_{CK}) = 50ns

Operation Temperature at 25°C

Based on 0.18-μm CMOS Model.

Specify types of Capacitors used (MIM, MOM or MOS-Cap) for area estimation as well as parasitic capacitance effect simulation.

Note:

It's free to design duty ratio of your clock, as long as the period of the clock is 50ns.

II. Summary Report (Less than 5 pages):

It is very important that the reported include clear descriptions of the design methodology. Do not just present final design without any reasoning and discussion

Requirements for the report:

A. Performance Summary Table [MUST BE ON COVER PAGE OR POINTS WILL BE DEDUCED]
B. Plot 1: Pumping Stage Circuit Schematic with detailed W, L sizing.
C. Plot 2: V_{out} Ramp Up waveform from V_{DD} to Target Voltage level under pure capacitive load.
D. Plot 3: V_{out} Voltage level at the Steady State at I_L of target.
E. Plot 4: Layout of the charge pump with DRC and LVS clean.
F. Determine the Minimum required # of stages needed in the design for reaching the required V_{PP} level under the design load.
G. Determine the Minimum area needed for this circuit.

H. Show the ripple voltage at the charge pump output.

I. Design Netlist and SPICE deck/result (.sp file)

J. References

*Performance Table Example.

PERFORMANCE PARAMETERS	
TYPE OF CP	*Dickenson/ Bootstrap /Latched/?*
# OF V_{CK} PHASES	
# OF STAGES	
TRANSIENT TIME	*µsec*
CIRCUIT AREA	*μm^2*
PUMPING CAPACITOR SIZE	*pF*
RIPPLE VOLTAGE	*mV*
POWER CONSUMPTION	*mW*
EFFICIENCY (POWER OUT/POWER IN)	*%*

You may expand the table to more parameters if needed.