國立清華大學 電機工程學系

114 學年度第一學期

EE-5216 時序電路設計及應用 (Timing Circuit Designs and Their Applications)

Homework #2 (Individual Homework)

Due Date：23:59pm, Nov. 30 (Sunday), 2025, (逾時不收)

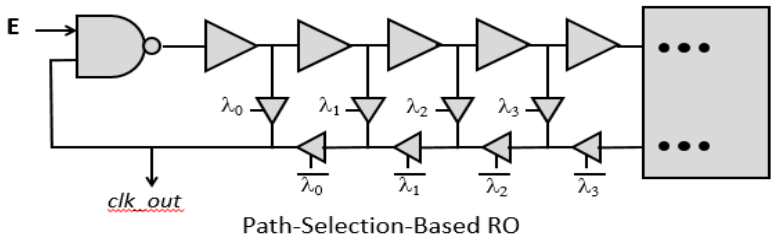
Submission: https://eeclass.nthu.edu.tw/ 作業區

- **Objective: To design a simple cell-based Phased-Locked Loop (PLL) and perform frequency acquisition.**

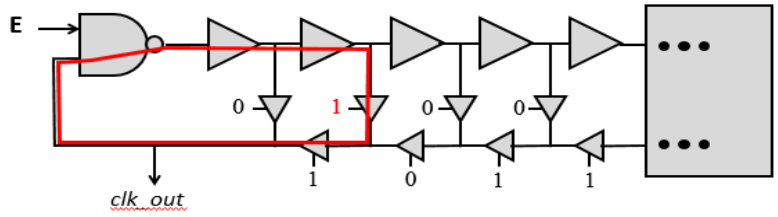
- **Step-by-Step Procedure**

Design a low-resolution Phase-Locked Loop to produce a 1GHz clock signal, denoted as *clk_out*, from a 100MHz reference clock signal, *clk_ref*.

(a) Design a **path-selection-based Digital Controlled Oscillator (DCO)** as indicated below. Report the oscillation frequency of your DCO under various control code values. Note that you may need to use a longer buffer chain and a control code with more bits than what is shown in the figure to ensure that the oscillation frequency fits your needs. (30%)



Path-Selection-Based RO



Oscillation ring when λ-code = (0010)

(b) Design a **frequency divider** and a **controller** that works with your **DCO** and some Phase Detector (**PD**) we have discussed in class so that your PLL will produce a frequency closest to the designated clock frequency after **frequency acquisition**. Verify your DLL design by Verilog simulation using as accurate delay model as possible for your DCO, frequency divider, and controller. Use the behavior model you have constructed in homework #1 for your PD. **Show the average clock cycle times of *clk_out* observed over 10 clock cycles after the frequency acquisition and its error as compared to the ideal clock cycle time at 1GHz (which is 1000ps).** (40%)

(c) Try to use SOC Encounter to **generate the layout** of your design. What is the size of your layout? (15%)

(d) Try to do **post-layout Verilog simulation** for your PLL. The netlist should be back-annotated with the post-layout SDF information. Compare your results with those derived in the pre-layout simulation. (15%)

- **Deliverables: Submit the following documents (combined into a PDF file) to our EECLASS system.**
  - A cover page containing 你的系所，中英文姓名，學號等資訊
  - Your results to questions (a)-(d).