

國立清華大學 電機工程學系

114 學年度第 1 學期

**EE-5216 時序電路設計及應用 (Timing Circuit Designs and Their Applications)**

Homework #3 (Individual Homework)

Due Date : 23:59pm, Dec. 22 (Monday), 2025, (逾時不收)

Submission: <https://eeclass.nthu.edu.tw/> 作業區

◆ **Objective: Duty-Cycle Correction Circuit Design**

◆ **Experience to be Learnt from this Homework:**

To get familiar with the design process of a timing circuit that correct a clock signal's duty cycle to 50%.

◆ **Step-by-Step Procedure**

Consider a design process for a duty-cycle corrector for a 1GHz input clock signal, denoted as *clk\_in*. The output clock signal is denoted as *clk\_dcc*. Once locked, *clk\_dcc* will have a duty cycle very close to 50%.

- (a) (20%) Draw a **block diagram** of your design and summarizing how you plan to achieve the duty-cycle correction with a paragraph.
- (b) (40%) **Realize the design as a synthesizable Verilog code.** (Your design can be a mixed format containing both netlists and RTL codes). (Hint: you may need Tunable Delay Lines, A Phase Detector, and a Controller, etc.) In this homework, we only need to use simple TDLs, e.g., path-selection-based TDLs, and some cell-based Phase Detector). Estimate your time resolution.
- (c) (15%) Try to use Design Compiler to **synthesize your design into standard-cell netlists**. Report the gate count of your netlist.
- (d) (15%) Verify the correctness of your design by running gate-level Verilog simulation using as accurate delay model as possible. Show the waveforms of *clk\_in* and *clk\_dcc*. Try the following input duty cycle samples for *clk\_in* – {30%, 70%}. **Report the final duty cycle for each input samples.**

◆ **Deliverables: Submit the following documents (combined into a PDF file) to our EECLASS system.**

- ◆ A cover page containing 你的系所，中英文姓名，學號等資訊
- ◆ Your results to questions (a)-(d).