2024 EE5250 VLSI Design Homework 3 <version 2>

Due date: 2024/11/21 (upload to eeclass)

Note

1. Please generate report with pdf format and name report as HWX_112XXXXXX_謝 OO.pdf. At first page please add your student ID and name.
2. Please hand in the 0.18um HSPICE simulation file & netlist (.sp, .spi).
3. Try to make the information "readable". (Don't use black color in background for your screen capture figures).
4. Make sure to mark the **titles** and **units** of x-axis and y-axis in all waveforms.
5. Please note that pin names on your layout should be marked on **metal layers**, not on diffusion or poly.
6. Discussion is encouraged, but the results and comments can't be shared.

Report (100%)

In this homework, we are going to simulate some important features of **positive-edge-triggered D flip-flops**, including "setup time," "hold time," "CLK-to-Q delay," "minimum/maximum delay failure condition," with respect to different pseudo processes, 0.18um & 16nm(ADFP).

Please write the report according to the following format:

1. (47%) One type of circuit implementation of positive-edge-triggered D flip-flops (positive-ET DFFs) is based on NAND gates, as shown in Fig. 1.

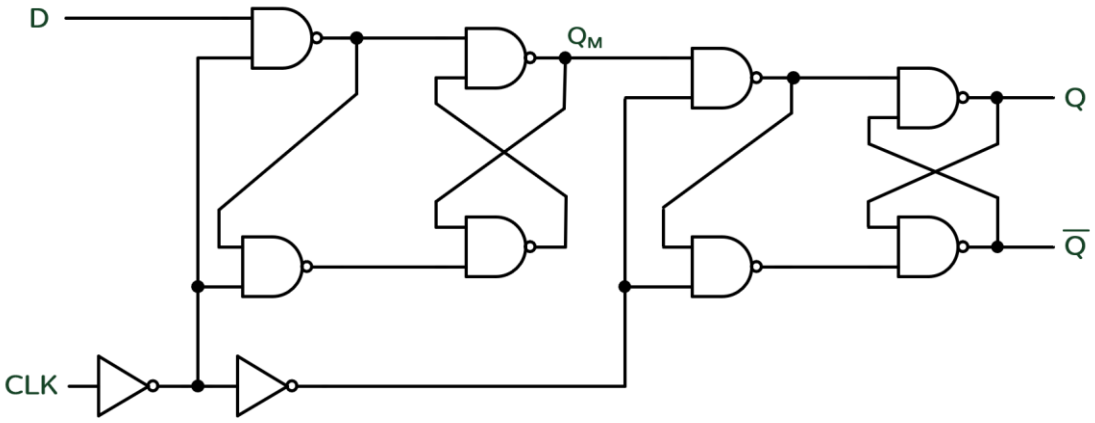


Fig. 1. NAND-based positive-ET DFF

Process	(1) 0.18um technology	(2) 16nm technology (ADFP)
CLK	100MHz with t_r=t_f=50ps, duty cycle=50%	
V_{DD}	1.8V	1V
Unit inverter size	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu m}{0.18\mu m}$; $\left(\frac{w}{L}\right)_p = \frac{1.85\mu m}{0.18\mu m}$	L=16nm, $nfin_n$=2, $nfin_p$=2

Table 1. Specification for Q1.

With the specification in Table 1, please answer the following questions:

(a). Explain what "setup time" and "hold time" of a positive-ET DFF are. (**Multiple choice**, with only one correct answer for each _/_.) (2%)

> ***Setup time*** *of a positive-ET DFF means the maximum/minimum allowable time duration that the inputted data at pin D / the outputted data at pin Q needs to be stable/unstable before/after CLK rising/falling edge.*
> *On the other hand,* ***hold time*** *of a positive-ET DFF means the maximum/minimum allowable time duration that the inputted data at pin D / the outputted data at pin Q needs to be stable/unstable before/after CLK rising/falling edge.*

(b). **Draw** some waveform(s) to show the concept of "setup time" and "hold time." In the waveform(s), there must be "D," "CLK," "Q" signals of a positive-ET DFF, and clearly mark "setup time" and "hold time." (You don't need to simulate this question with HSPICE.) (2%)

(c). Do setup time and hold time depend on the frequency of CLK? That is, when we change CLK signal from 100MHz to 200MHz with the same t_r, t_f, and duty cycle, do setup time and hold time remain the same? **Explain** with the reasoning. It's better to draw some figure or waveform to help. (You don't need to simulate this question with HSPICE.) (1%)

0.18um technology (pre-layout simulation & post-layout simulation):

(d). Based on the unit inverter size shown in Table 1, design the size of NAND logic gates **by hand-calculation**, with the following requirements: (You don't need to simulate this question with HSPICE.) (3%)

i. The pull-up resistance of NAND should be the same as that of unit inverter.

ii. The pull-down resistance of NAND should be the same as that of unit inverter.

iii. Due to no output loading in this question, you can design all NAND gates with exactly the same size (W, L, m).

iv. Answer this question **for 0.18um technology**

(e). Using the sizes you have designed in (d), build up the schematic of DFF using Composer. **Screenshot** the schematic of your DFF. Schematics inside **all blocks** (including NAND2, inverter) should be provided. (1%)

(f). With specifications in Table 1, run HSPICE simulation (pre-layout simulation) to find the **setup time** of this DFF. The input D signal will be designed by yourself. Answer the following questions **for 0.18um technology**.

(f-1). **Describe** in detail how you design the input D signal to get the **setup time** of this DFF. It is better to echo with the definition of setup time in (a). (2%)

(f-2). For rising input (D), **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

(f-3). For rising input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time on the waveform. Here we define the transition point of signals as $0.5V_{DD}$. (1%)

(f-4). For falling input, **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

(f-5). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time on the waveform. (1%)

(f-6). Compare setup time between rising input and falling input. Which one has larger setup time? Why? It's better to explain with the circuit in Fig. 1. (1%)

(f-7). When the setup-time constraint of this DFF is **violated**, what will happen? Please provide with some **comments** and use **simulation waveform** to verify your idea. (2%)

(g). With specifications in Table 1., run HSPICE simulation (pre-layout simulation) to find the **hold time** of this DFF. The input D signal will be designed by yourself. Answer the following questions **for 0.18um technology**.

(g-1). **Describe** in detail how you design the input D signal to get the **hold time** of this DFF. It is better to echo with the definition of hold time in (a). (1%)

(g-2). For rising input (D), **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

(g-3). For rising input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the hold time on the waveform. (1%)

(g-4). For falling input, **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

(g-5). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the hold time on the waveform. (1%)

(g-6). When the hold-time constraint of this DFF is **violated**, what will happen? Please provide with some **comments** and (if the hold time of your DFF is not 0) use **simulation waveform** to verify your idea. (2%)

(h). With specifications in Table 1, run HSPICE simulation (pre-layout simulation) to find the **clock to Q delay (CLK-to-Q delay)** of this DFF. The input D signal will be designed by yourself. Answer the following questions **for 0.18um technology**.

(h-1). When simulating CLK-to-Q delay, what kind of requirements does input D signal have? (1%)

(h-2). For rising input (D), **screenshot** the simulation waveform of "D," "CLK," "Q" signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (0.5%)

(h-3). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q" signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (0.5%)

(i). Using the sizes you have designed in (d), finish the layout of your DFF. Answer the following questions **for 0.18um technology**.

(i-1). There is a requirement that the layout needs to be able to be **contained inside a "15um × 15um" box** (which means that neither the width nor the height of your layout can be larger than 15um). Please **screenshot** your layout. **Mark** the total width and height on the layout. (5%) If your layout cannot meet the "15um × 15um" requirement, but can be contained inside a "**20um × 20um**" box, you can still get 2.5%.

(i-2). **Screenshot** your DRC result. Make sure there is no DRC violation. (1%)

(i-3). **Screenshot** your LVS result. Make sure you get a smile *‿*. (1%)

(j). Run the post-layout simulation.

(j-1). For rising input (D), **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time, hold time, and CLK-to-Q delay on the waveform. (2%)

(j-2). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time, hold time, and CLK-to-Q delay on the waveform. (2%)

(j-3). **Build a table** to compare the setup time, hold time, and CLK-to-Q delay performance between pre-sim and post-sim (for both rising input and falling input). **Where** do the differences (between pre-sim and post-sim) come from? (1.5%)

16nm (ADFP) technology (only pre-layout simulation):

(k). Repeat question (d) **for 16nm (ADFP) technology**. (2%)

(l). Repeat question (e) **for 16nm (ADFP) technology**. (1%)

(m). Repeat question (f-2)~(f-5) **for 16nm (ADFP) technology**. [Please title as (m-2)~(m-5).] (2%)

(n). Repeat question (g-2)~(g-5) **for 16nm (ADFP) technology**. [Please title as (n-2)~(n-5).] (2%)

(o). Repeat question (h-2)~(h-3) **for 16nm (ADFP) technology**. [Please title as (o-2)~(o-5).] (1%)

~~(p). **Build a table** to compare the setup time, hold time, and CLK-to-Q delay performance (for both rising input and falling input) between 0.18um pre-sim and 16nm pre-sim. Which technology performs better, and for how much %? ($\left|\frac{\text{better}-\text{worse}}{\text{worse}}\right| \times 100\%$) (1.5%)~~ **You don't need to answer this question. (You can get 0.5% for free.)**

2. (14%) Another type of circuit implementation of positive-ET DFFs is based on transmission gates (TGs), as shown in Fig. 2. The circuit implementation of TG is shown in Fig. 3.

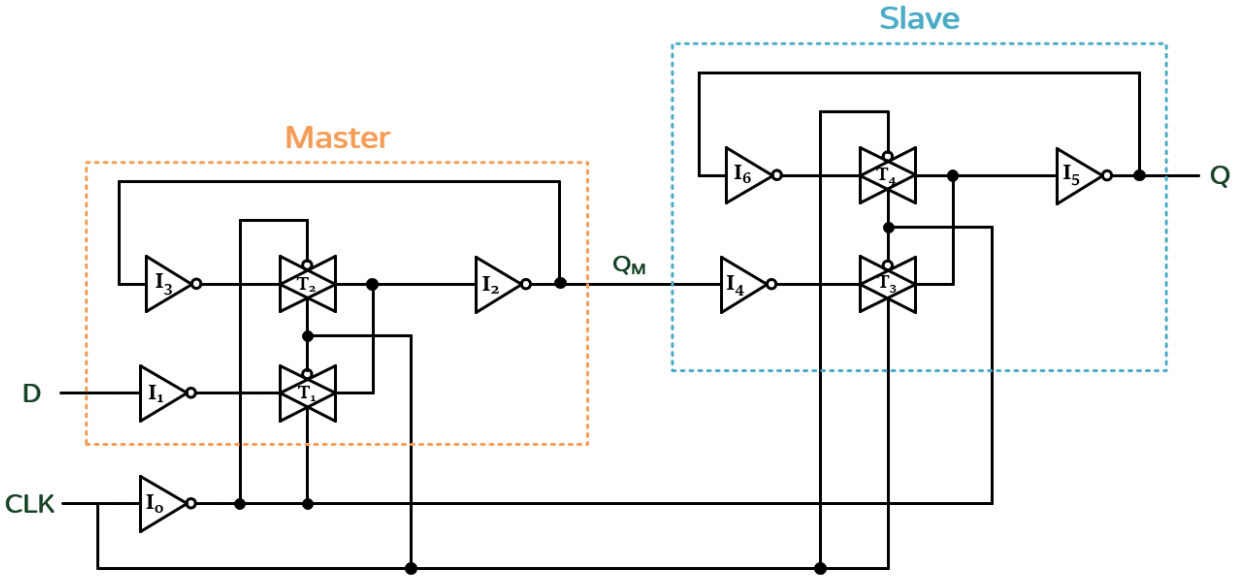
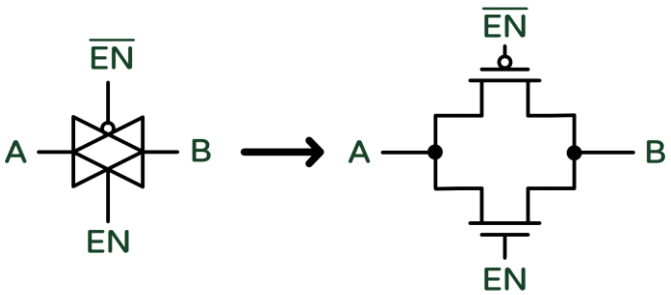


Fig. 2. TG-based positive-ET DFF



by CCHsieh

Fig. 3. Circuit implementation of TG

Process	0.18um technology
CLK	100MHz with t_r=t_f=50ps, duty cycle=50%
V_{DD}	1.8V
Unit inverter size	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu m}{0.18\mu m}; \left(\frac{w}{L}\right)_p = \frac{1.85\mu m}{0.18\mu m}$
TG size	$\left(\frac{w}{L}\right)_n = \frac{1\mu m}{0.18\mu m}; \left(\frac{w}{L}\right)_p = \frac{1\mu m}{0.18\mu m}$

Table 2. Specification for Q2.

Notation:

t_{pd_inv} = the propagation delay of an inverter

t_{pd_TG} = the propagation delay of a TG

$t_{pd}(I_{XX})$ = the propagation delay of I_{XX}

$t_{pd}(T_{OO})$ = the propagation delay of T_{OO}

With the specification in Table 2, please answer the following questions:

(a). Assume that there is no contamination delay and $t_{pd}(I_0)$=0. What will the **setup time (t_{setup})** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

Theoretically, the setup time of a TG-based positive-ET DFF is "___ t_{pd_inv} + ___ t_{pd_TG}." (Please fill in a non-negative integer number into each blank; for example, "6t_{pd_inv} + 4t_{pd_TG}")
More specifically, t_{setup} = "_____." (Please list out **the most fundamental sources** of setup time, in terms of each **element**; for example, "$t_{pd}(I_1)$+$t_{pd}(I_2)$+$t_{pd}(T_4)$")
The reason is _____. (It's better to describe with the help of Fig. 2.)

(b). Assume that there is no contamination delay and $t_{pd}(I_0)$=0. What will the **hold time (t_{hold})** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

Theoretically, the hold time of a TG-based positive-ET DFF is "___ t_{pd_inv} + ___ t_{pd_TG}." (Please fill in a non-negative integer number into each blank; for example, "6t_{pd_inv} + 4t_{pd_TG}")
More specifically, t_{hold} = "_____." (Please list out **the most fundamental sources** of hold time, in terms of each **element**; for example, "$t_{pd}(I_1)$+$t_{pd}(I_2)$+$t_{pd}(T_4)$")
The reason is _____. (It's better to describe with the help of Fig. 2.)

(c). Assume that there is no contamination delay and $t_{pd}(I_0)$=0. What will the **CLK-to-Q delay ($t_{C\text{-}Q}$)** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

Theoretically, the CLK-to-Q delay of a TG-based positive-ET DFF is "___ t_{pd_inv} + ___ t_{pd_TG}." (Please fill in a non-negative integer number into each blank; for example, "6t_{pd_inv} + 4t_{pd_TG}")
More specifically, $t_{C\text{-}Q}$ = "_____." (Please list out **the most fundamental sources** of CLK-to-Q delay, in terms of each **element**; for example, "$t_{pd}(I_1)$+$t_{pd}(I_2)$+$t_{pd}(T_4)$")
The reason is _____. (It's better to describe with the help of Fig. 2.)

(d). Using the sizes given in Table 2, build up the schematic of TG-based DFF using Composer. **Screenshot** the schematic of your TG-based DFF. Schematics inside **all blocks** (including TG,

inverter) should be provided. (1%)

(e). Similar to question 1.(f), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **setup time** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.

(e-1). For rising input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time on the waveform. (1%)

(e-2). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the setup time on the waveform. (1%)

(f). Similar to question 1.(g), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **hold time** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.

(f-1). For rising input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the hold time on the waveform. (1%)

(f-2). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q_M," "Q" signals of the DFF. **Mark** the hold time on the waveform. (1%)

(g). Similar to question 1.(h), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **CLK-to-Q delay** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.

(g-1). For rising input, **screenshot** the simulation waveform of "D," "CLK," "Q" signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (1%)

(g-2). For falling input, **screenshot** the simulation waveform of "D," "CLK," "Q" signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (1%)

(h). Use the results above to **build a performance table** to summarize the setup time, hold time, and CLK-to-Q delay performance for TG-based DFFs (for both rising input and falling input). We will use this performance table later in Q3. (1%)

3. (40%) In this question, we are going to find out the minimum and maximum allowable delay between two DFFs. This concept is called "**minimum/maximum delay failure condition**" and is very important in digital circuit design, especially for determining clock period when doing RTL synthesis.

(a). Insert some combinational logic between two DFFs to introduce delay, forming a sequential logic, as shown in Fig. 4.

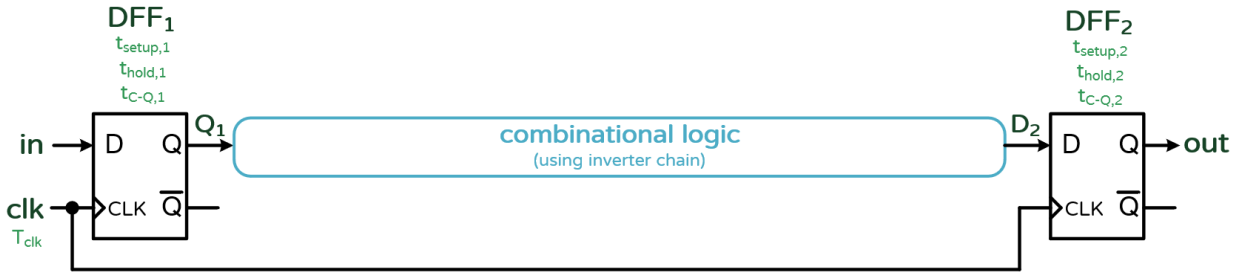


Fig. 4. Sequential logic consisting of combinational logic and DFFs

Considering the setup time (t_{setup}), hold time (t_{hold}), and CLK-to-Q delay ($t_{C\text{-}Q}$) of DFF_1 and DFF_2,

answer the following questions: (You don't need to simulate these questions with HSPICE.)

(a-1). What are the **timing requirements for the propagation delay, t_{delay}, of the combinational logic** in order to ensure proper functionality? Please express in terms of $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, and T_{clk} (the period of clk). It's better to draw some waveforms to help. (Hint: There should be one upper bound and one lower bound for t_{delay}.) (Hint: Figures in lecture note page 6-31 may give you some idea about how to draw a helpful waveform.) (2%)

(a-2). Which one does the **maximum** allowable delay of the combinational logic depend on, "setup time" or "hold time"? What if the propagation delay exceeded this maximum, what would happen? You can answer by following this format: (1%)

> *From my answer to (a-1), the maximum allowable delay of the combinational logic is _____, which depends on setup time / hold time of DFF_1 / DFF_2.*
>
> *If the propagation delay exceeded this maximum, it would have setup time violation / hold time violation at DFF_1 / DFF_2, resulting in incorrect value at Q_1 / D_2 / out.*

(a-3). Which one does the **minimum** allowable delay of the combinational logic depend on, "setup time" or "hold time"? What if the propagation delay smaller than this minimum, what would happen? You can answer by following this format: (1%)

> *From my answer to (a-1), the minimum allowable delay of the combinational logic is _____, which depends on setup time / hold time of DFF_1 / DFF_2.*
>
> *If the propagation delay smaller than this minimum, it would have setup time violation / hold time violation at DFF_1 / DFF_2, resulting in incorrect value at Q_1 / D_2 / out.*

Using NAND-based DFFs

Here we use an inverter chain (acting as combinational logic) to introduce delay. In the inverter chain, use the same size (shown in Table 3) for each stage. The number of stages in the inverter chain will be designed by yourself.

Process	0.18um technology
CLK	100MHz with t_r=t_f=50ps, duty cycle=50%
V_{DD}	1.8V
inverter size (in inverter chain)	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu m}{0.18\mu m}$; $\left(\frac{w}{L}\right)_p = \frac{1.85\mu m}{0.18\mu m}$; m=1

Table 3. Specification for Q3.

(b). **Simulation & hand-calculation of maximum delay failure condition**

(b-1). **Describe** in detail how to design/determine the number of stages in the inverter chain to get the maximum delay failure condition (maximum allowable delay of the combinational logic). (1.5%)

(b-2). Use your **NAND-based DFF** in Q1 and the above-mentioned inverter size to build up the schematic of "DFF + inverter chain" using Composer. **Screenshot** this schematic. (The

inverter chain might be long. One screenshot for hundreds of inverters is OK.) (0.5%)

With specification in Table 3, run HSPICE simulation (pre-layout simulation) **for 0.18um technology** to find the **maximum allowable delay** of the combinational logic. The input D signal needs to satisfy setup time and hold time requirements.

(b-3). For rising input (in), for **maximum allowable number of stages**, **screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (2%)

(b-4). How many inverter stages **at most** can exist in the inverter chain while keeping normal functionality? What is the maximum allowable delay? (Measure it from the waveform in (b-3).) (1%)

(b-5). Add one more stage to the inverter chain, so now we have "**maximum + 1" number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). **Which** timing requirement of **which** DFF does it violate? (1.5%)

(b-6). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate maximum delay failure condition (maximum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with t_{delay} by simulation in (b-3), and calculate the **mismatch rate** ($|\frac{\text{simulation}-\text{hand}}{\text{hand}}| \times 100\%$). If the mismatch rate exceeds 5%, then please comment on the reason. (2%)

(b-7). For falling input, for **maximum allowable number of stages**, **screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (2%)

(b-8). How many inverter stages **at most** can exist in the inverter chain while keeping normal functionality? What is the maximum allowable delay? (Measure it from the waveform in (b-7).) (1%)

(b-9). Add one more stage to the inverter chain, so now we have "**maximum + 1" number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). **Which** timing requirement of **which** DFF does it violate? (1.5%)

(b-10). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate maximum delay failure condition (maximum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with t_{delay} by simulation in (b-7), and calculate the **mismatch rate** ($|\frac{\text{simulation}-\text{hand}}{\text{hand}}| \times 100\%$). If the mismatch rate exceeds 5%, then please comment on the reason. (2%)

(c). **Simulation & hand-calculation of minimum delay failure condition**

(c-1). **Describe** in detail how to design/determine the number of stages in the inverter chain to get the minimum delay failure condition (minimum allowable delay of the combinational logic). (1.5%)

(c-2). Use your **NAND-based DFF** in Q1 and inverter size in Table 3 to build up the schematic of "DFF + inverter chain" using Composer. **Screenshot** this schematic. (0.5%)

With specification in Table 3., run HSPICE simulation (pre-layout simulation) **for 0.18um technology** to find the **minimum allowable delay** of the combinational logic. The input D signal needs to satisfy setup time and hold time requirements.

(c-3). For rising input (in), for **minimum allowable number of stages**, **screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (1%)

(c-4). What is the **smallest** number of inverter stages that can exist in the inverter chain while keeping normal functionality? What is the minimum allowable delay? (Measure it from the waveform in (c-3).) (1%)

(c-5). Remove one stage from the inverter chain, so now we have "**minimum - 1" number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). **Which** timing requirement of **which** DFF does it violate? (1%)

(c-6). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate minimum delay failure condition (minimum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with t_{delay} by simulation in (c-3), and calculate the **mismatch rate** ($|\frac{\text{simulation}-\text{hand}}{\text{hand}}| \times 100\%$). If the mismatch rate exceeds 5%, then please comment on the reason. (1%)

(c-7). For falling input, for **minimum allowable number of stages**, **screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (1%)

(c-8). What is the **smallest** number of inverter stages that can exist in the inverter chain while keeping normal functionality? What is the minimum allowable delay? (Measure it from the waveform in (c-7).) (1%)

(c-9). Remove one stage from the inverter chain, so now we have "**minimum - 1" number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of "clk," "in," "Q_1," "D_2," "out" signals. **Mark** all the related timing on the waveform (choose what

you need from $t_{setup,1}$, $t_{hold,1}$, $t_{C\text{-}Q,1}$, $t_{setup,2}$, $t_{hold,2}$, $t_{C\text{-}Q,2}$, T_{clk}, t_{delay}). **Which** timing requirement of **which** DFF does it violate? (1%)

(c-10). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate minimum delay failure condition (minimum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with t_{delay} by simulation in (c-7), and calculate the **mismatch rate** ($|\frac{\text{simulation}-\text{hand}}{\text{hand}}| \times 100\%$). If the mismatch rate exceeds 5%, then please comment on the reason. (1%)

(d). From the above simulation and hand-calculation, finish Table 4. (Don't forget to write down units.) (1%)

NAND-based	**Max. propagation delay**		**min. propagation delay**	
	simulation	hand-calculation	simulation	hand-calculation
rising input				
falling input				

Table 4. Maximum/minimum allowable propagation delay of the combinational logic between two NAND-based DFFs

Using TG-based DFFs

(e). Repeat question (b-2)~(b-10) but use **TG-based DFF** in Q2 instead. [Please title as (e-2)~(e-10).] (For question (b-6) and (b-10), use data from the performance table in question 2.(h) instead.) (4.5%)

(f). Repeat question (c-2)~(c-10) but use **TG-based DFF** in Q2 instead. [Please title as (f-2)~(f-10).] (For question (c-6) and (c-10), use data from the performance table in question 2.(h) instead.) (4.5%)

(g). From the above simulation and hand-calculation, finish Table 5. (Don't forget to write down units.) (1%)

TG-based	**Max. propagation delay**		**min. propagation delay**	
	simulation	hand-calculation	simulation	hand-calculation
rising input				
falling input				

Table 5. Maximum/minimum allowable propagation delay of the combinational logic between two TG-based DFFs