2024 EE5250 VLSI Design Homework 2

Due date: 2024/10/17 (upload to eeclass)

Note

1. Please generate report with pdf format and name report as HWX_112XXXXXX_謝 OO.pdf. At first page please add your student ID and name.
2. Please hand in the 0.18um HSPICE simulation file & netlist (.sp, .spi).
3. Try to make the information "readable". (Don't use black color in background for your screen capture figures).
4. Discussion is encouraged, but the results and comments can't be shared

Report

Please write the report according to the following format:

1. Run simulation to answer the following question, using VDD = 1.8V. (45%)

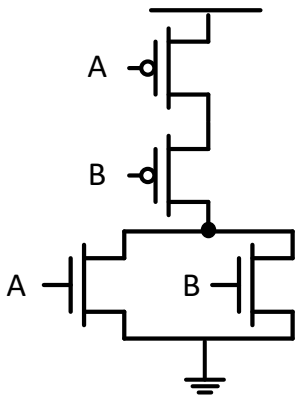

Fig. 1

(a). Please design 2-input NOR gate. Please design with $\left(\frac{w}{l}\right)_n = \frac{2um}{0.2um}$ and $\left(\frac{w}{l}\right)_p = your\ design.$

Connect the two inputs together to run the transfer curve, the transition point should be Vout = 0.5VDD@Vin = 0.5VDD (Only at TT corner). (5%)

(b). Using the 2-input NOR designed in (a) with VDD = 1.8V.
Please add a loading capacitor Cload = 2pF at the output node. Run HSPICE transient simulation of 3 cases at 3 corners and fill up the Table. 1. (10%)
The CLK signal in Table 1 is a periodic pulse signal with a frequency of 1 MHz, a rising time/falling time of 0.1 ns, and a voltage range of 1.8-0V.

Table. 1

	case 1			case 2			case 3		
Input A	CLK			0V			CLK		
Input B	0V			CLK			CLK		
Corner	TT	SS	FF	TT	SS	FF	TT	SS	FF
t_{pHL}									
t_{pLH}									
t_r									
t_f									

Note:

t_{pHL}: from input to falling output crossing 0.5VDD

t_{pLH}: from input to rising output crossing 0.5VDD

t_r: output rises from 0.1VDD to 0.9VDD

t_f: output falls from 0.9VDD to 0.1VDD

(c). Please comment on the differences. (15%)

(d). Finish the layout, DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area (μm^2). (10%)

(e). Run the post-layout simulation and compare it with the pre-sim (b). Please fill up the table.1 with post-layout simulation, too (5%)

2. Run an inverter chain with output loading 0.5pF with VDD = 1.8V, as shown in Fig 2. (The size of the first inverter has been assigned.) (The rising time and falling time of input is 0.1ns & input frequency = 5MHz). Please determine **how many stages** this inverter chain needs and the **size of each stage** to achieve **the minimum delay**. (55%)

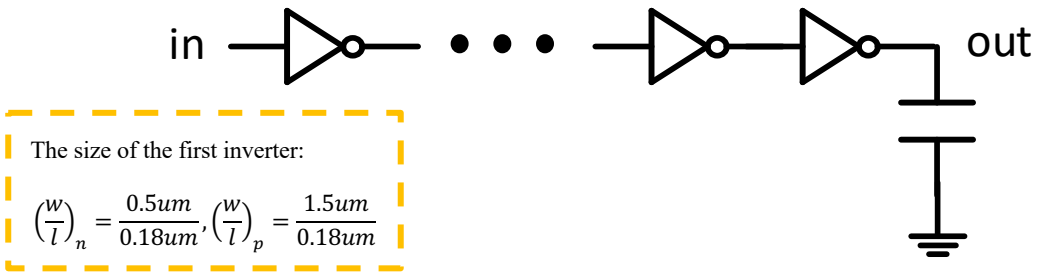

Fig. 2

(a). The logical effort (g) and the parasitic delay (p) of the first inverter is 0.968 and 1.033 respectively. Describe how you design the inverter chain to achieve minimum delay **in detail**. (25%)

(b). Provide the screenshot of input and output waveform, mark t_{pdr} and t_{pdf} and calculate t_{pd}. (5%)

(c). Finish the layout, DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area (μm^2). (15%)

(d). Run the post-layout simulation and compare it with the pre-sim (b). (10%)