2024 EE5250 VLSI Design Homework 4

Due date: 2024/12/12 (upload to eeclass)

Note

1. Please generate report with pdf format and name report as HWX_112XXXXXX_謝 OO.pdf. At first page please add your student ID and name.
2. Please hand in the 0.18um HSPICE simulation file & netlist (.sp, .spi).
3. Try to make the information “readable”. (Don’t use black color in background for your screen capture figures).
4. Make sure to mark the **titles** and **units** of x-axis and y-axis in all waveforms.
5. Please note that pin names on your layout should be marked on **metal layers**, not on diffusion or poly.
6. Discussion is encouraged, but the results and comments can’t be shared.

I. Introduction

A **Linear Feedback Shift Register (LFSR)** is a type of shift register where the input bit is determined by the XOR of specific bits from the register. In this homework, we will implement a **pseudo-random bit sequence (PRBS)** using an LFSR to generate random patterns.

An example of a 3-bit PRBS is provided below, the PRBS can generate all 2^N-1 possible patterns (excluding the all-zero sequence) when a primitive polynomial is used to derive the LFSR.

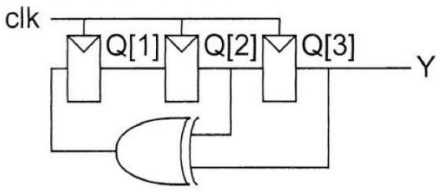

Table 10.6 LFSR sequence

Cycle	Q[1]	Q[2]	Q[3] / Y
0	1	1	1
1	0	1	1
2	0	0	1
3	1	0	0
4	0	1	0
5	1	0	1
6	1	1	0
7	1	1	1
repeats forever			

Table 10.7 Characteristic polynomials

N	Polynomial
3	$1 + x^2 + x^3$
4	$1 + x^3 + x^4$
5	$1 + x^3 + x^5$
6	$1 + x^5 + x^6$
7	$1 + x^6 + x^7$
8	$1 + x^1 + x^6 + x^7 + x^8$
9	$1 + x^5 + x^9$
15	$1 + x^{14} + x^{15}$
16	$1 + x^4 + x^{13} + x^{15} + x^{16}$
23	$1 + x^{18} + x^{23}$
24	$1 + x^{17} + x^{22} + x^{23} + x^{24}$
31	$1 + x^{28} + x^{31}$
32	$1 + x^{10} + x^{30} + x^{31} + x^{32}$

Fig. 1. 3-bit PRBS example (Chapter 7, Page 62)

In addition, the LFSR can be classified into two type: **Fibonacci LFSR** (Out-tap LFSR) and **Galois LFSR** (In-tap LFSR), an example of the type changing between out-tap and in-tap is shown below.

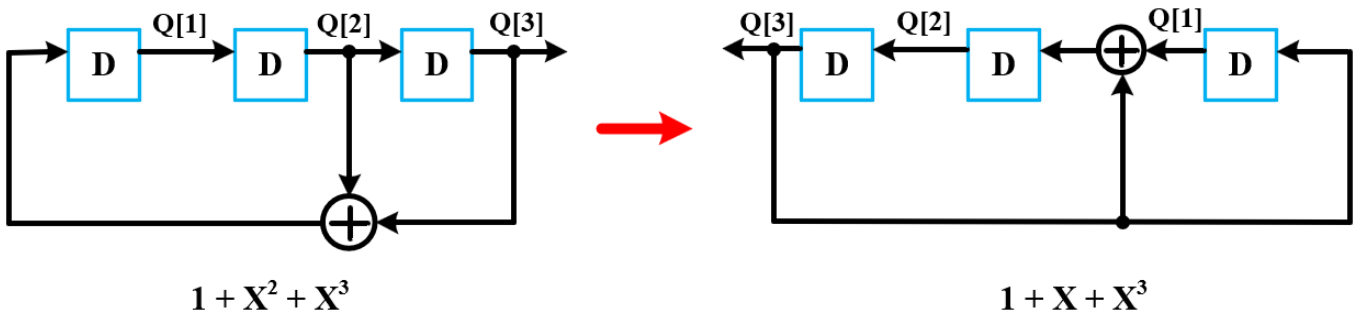

Fig. 2. 3-bit LFSR type changing example

Please design an **8-bit PRBS** for **"both"** types (Out-tap and In-tap) under the **0.18 µm** process, and ensure that your simulation follows the requirements outlined below.

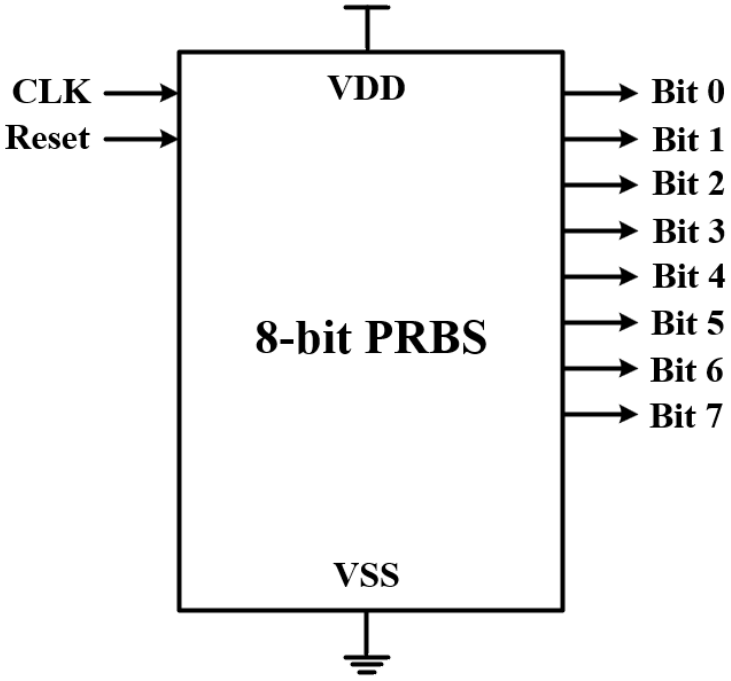

Fig. 3. 8-bit PRBS

- You are allowed only **4** input signals: Clock, Reset, VDD, and VSS. Additionally, there should be **8** output signals: Bit 0 through Bit 7.
- The rise time and fall time of the Clock should each be **10 ps**, with a **50%** duty cycle.
- Initially, all D flip-flops (DFFs) should be **reset to VDD using a negative reset signal**.
- The PRBS should generate **all 255 different patterns** (excluding the all-zero sequence).
- Please change the clock frequency with **100 MHz as the minimum step.**
- You can verify your results using the MATLAB code provided by the TA.

II. Report (70%)

Please write the report according to the following format:

1. Out-tap LFSR (30%)

(a) Please draw the block diagram of your out-tap LFSR and write down how you derived the architecture in detail. (5%)

(b) Please draw the architecture of your DFF and XOR, list all the transistors size. (5%)

(c) Please run the pre-sim at TT corner and find the maximum frequency of clock you can achieve. (5%)
(Note: Please screenshot a short time waveform and show the histogram of the output code to prove the accuracy of the result.)

(d) Please write down the reasons that limit the clock frequency in detail. (5%)

(e) Please run the pre-sim at FF, SS, FS and SF corner and find the maximum frequency of each corner. (5%)
(Note: Please show the histogram of the output code to prove the accuracy of the result.)

Corner	TT	FF	SS	FS	SF
Max. freq.					

(f) Please compare the results of (e) and provide a detailed analysis of your observations. (5%)

2. In-tap LFSR (40%)

(a) Please draw the block diagram of your in-tap LFSR and write down how you derived the architecture in detail. (5%)

(b) Please use the same size as the out-tap LFSR to run the pre-sim at TT corner and find the maximum frequency of clock you can achieve. (5%)
(Note: Please screenshot a short time waveform and show the histogram of the output code to prove the accuracy of the result.)

(c) Please compare the result with the 1(c) and provide a detailed analysis of your observations. (5%)

(d) Please run the pre-sim at FF, SS, FS and SF corner and find the maximum frequency of each corner. (5%)
(Note: Please show the histogram of the output code to prove the accuracy of the result.)

Corner	TT	FF	SS	FS	SF
Max. freq.					

(e) Please finish your layout of the in-tap LFSR

(e-1) Provide your layout screenshot with the width and length marked. Compute the area and aspect ratio of your layout. (5%)

(e-2) Show your DRC and LVS result (5%)

(f) Please run the post-sim at TT corner and find the maximum frequency of clock you can achieve. (5%) (Note: Please screenshot a short time waveform and show the histogram of the output code to prove the accuracy of the result.)

(g) Please fill the SPEC table and try your hard to meet the target (5%)

SPEC Table			
Design item	SPEC	Score	Your design
Power Supply	1.8V	0%	1.8V
Max. freq. at TT corner (Pre-sim)	$\geq$ 2.9GHz	5%	
	$\geq$ 2.5GHz	4%	
	$\geq$ 2.0GHz	3%	
	$\geq$ 1.5GHz	2%	
	$\geq$ 1.0GHz	1%	
Max. freq. at TT corner (Post-sim)	As small as possible	0%	
Layout Area	As small as possible	0%	
Layout aspect ratio	$\frac{\text{long side}}{\text{short side}} \leq 3$	0%	

III. Demo (30%)

Please design a **4-bit PRBS** for **"any"** type (Out-tap or In-tap) under the 16nm process (ADFP), and ensure that your simulation follows the requirements outlined below.

- You are allowed only **4** input signals: Clock, Reset, VDD, and VSS. Additionally, there should be **4** output signals: Bit 0 through Bit 3.
- The rise time and fall time of the Clock should each be 1 ps, with a 50% duty cycle.
- Initially, all D flip-flops (DFFs) should be **reset to VDD using a negative reset signal**.
- The PRBS should generate **all 15 different patterns** (excluding the all-zero sequence).
- You can verify your results by observing the waveform.

During the demo, please complete the following procedures:

1. Please show the waveform of pre-sim at TT, FF, SS corner and make sure the results are correct. (5%)
2. Please show the layout with the width and length marked. Compute the area and aspect ratio of your layout. (5%)
3. Please show the DRC result. (5%)
4. Please show the LVS result. (5%)
5. Please show the waveform of post-sim at TT corner and make sure the result is correct. (5%)
6. Please answer the questions from TAs. (5%)