2024 EE5250 VLSI Design Midterm Project

Due date: 2024/11/07 (upload to eeclass)

Note

1. Please generate report with pdf format and name report as VLSI_Mid_112XXXXXX_謝 OO.pdf. At first page please add your student ID and name.
2. Please hand in the SPICE netlist file (.spi) and layout file (.gds).
3. Try to make the information "readable". (Don't use black color in background for your screenshots).
4. Discussion is encouraged, but the results and comments can't be shared

I. Introduction

Thermometer code is an encoding scheme that resembles the output produced by a thermometer. In thermometer code, each symbol is a sequence of 0s followed by a sequence of 1s, and the number of 1s is the value represented by a certain symbol. As a result, for an n-bit binary code, it requires $(2^n - 1)$ bits to represent the corresponding thermometer code.

An example of a 3-bit thermometer code with the corresponding 2-bit binary code and decimal value is provided in Table 1.

Thermometer code			**Binary code**		**Decimal**
T[2]	**T[1]**	**T[0]**	**B[1]**	**B[0]**	**-**
0	0	0	0	0	0
0	0	1	0	1	1
0	1	1	1	0	2
1	1	1	1	1	3

Table 1. Example of a 3-bit thermometer code

In this project, you will design a 15-to-4 thermometer to binary converter (TBC) using combinational logic and try to minimize the propagation delay. The detail circuit implementation is free for design. However, the number of I/O pin is restricted to 15 input bits (**T[14:0]**), 4 output bits (**B[3:0]**), and power supply (**VDD** and **VSS**).

Hint: An example of 3-to-2 thermometer to binary converter (TBC)

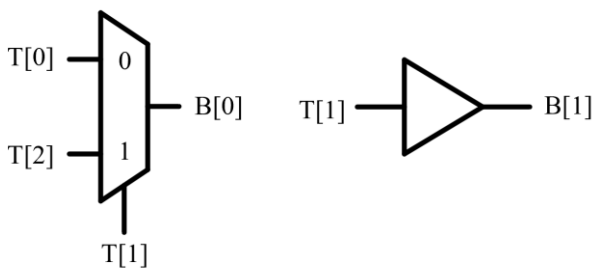

Figure 1. An example of 3-to-2 thermometer to binary converter (TBC)

II. Guidelines

In this project, SPICE code (TBC.sp & Data.txt) is provided for you to test your design. In the SPICE code, input signals, input buffers, output loadings and power supply are given as shown in Figure 2.

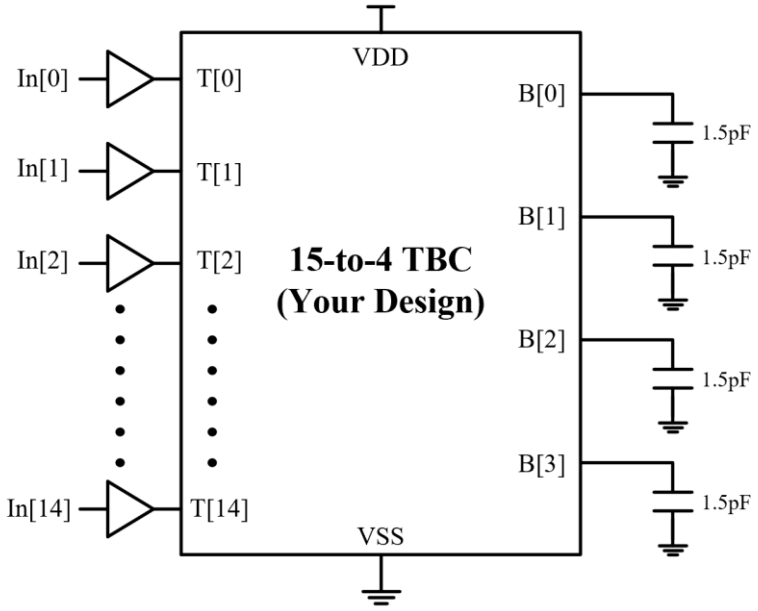

Figure 2. 15-to-4 TBC with input buffers and output loadings

In[14:0] is the 15-bit input generated by ideal voltage sources. Each bit of In connects to an input buffer and generates T[14:0], which is the actual 15-bit thermometer code input of the TBC. The input buffer is constructed by 2 inverters with the same size: $(\frac{W}{L})_p = \frac{1.5\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$, m=1 for both NMOS and PMOS. B[3:0] is the 4-bit binary output of the TBC with a 1.5pF loading at each bit.

- **Simulation**

SPICE transient analysis will be used to find out the delay and power consumption of your TBC. Initially, all 15 bits of In[14:0] are 0s. Then, the input signals change from 0 to 1 bit by bit, sequentially from In[0] to In[14] until all 15 bits become 1. After that, the input signals changes from 1 to 0 bit by bit, sequentially from In[14] to In[0] and all bits of In become 0 again at the end of the simulation.

With the input bits change as mentioned, the output sequence of TBC should be 0, 1, 2, …, 13, 14, 15, 14, 13, …, 2, 1, 0 in binary.

- **Delay and power measurement**

The delay of TBC for a certain transition is measured from the triggered bit in In[14:0] crossing $0.5V_{DD}$ to B[3:0] when the voltages of the latest transition bits crossing $0.5V_{DD}$. The power consumption of TBC for a certain transition is measured by averaging $V(V_{DD})*I(V_{DD})$ between the input trigger edge of the current transition and that of the next transition. (SPICE code for delay and power measurement are provided in TBC.sp)

- **Notifications**

TAs will check your circuit performance using TBC.sp after you submit your project. Please follow the rules below.

1. Name your sub-circuit as TBC and DO NOT include input buffers and output loadings in your sub-circuit and layout since they are included in TBC.sp. However, please note that the delays of input buffers are included while measuring the delay of your circuit.
2. Name your .spi file as TBC.spi (for pre-sim) and TBC.pex.spi (for post-sim). Also, please adjust the order of the I/O pins to fit TBC.sp.
3. Supply voltage is free for design in this project. You may adjust the supply voltage with minimum step of 0.1V.
4. **Please change the included netlist file (.spi) and supply voltage in Data.txt. TBC.sp CANNOT be modified.**
5. In transient analysis, please make sure all output bits settle to higher than (V_{DD}-1mV) for logic "1" or lower than 1mV for logic "0" before the next transition starts in both pre-sim and post-sim. You will have to adjust your design or layout if any output bit fails to meet the requirement.
6. In question 2a, 3a, and 5a, you have to provide your simulation waveforms to verify your design. You will receive -10% penalty if you don't provide the waveforms and you will receive 0 point for this project if the function of your design is wrong.

III. Design Constraints

Technology

1. CIC pseudo-0.18μm technology

Power Supply

1. $\leq$ 1.8V. You may adjust it with minimum step of 0.1V.
2. You should use the same supply voltage for all simulations.

Delay

1. Maximum delay in pre-sim $\leq$ 1.2ns at TT corner. As small as possible.
2. All output bits should settle to higher than (V_{DD} - 1mV) for logic "1" or lower than 1mV for logic "0" before the next transition starts in both pre-sim and post-sim at all 5 corners (TT, FF, SS, FS, and SF).

Layout

1. Total area is not limited. As small as possible.
2. Aspect ratio of full circuit block: long side / short side $\leq$ 3.
3. In your layout, the same node should be connected together (i.e., You can have only one VDD pin in your layout).

Figure of Merit (FoM)

1. $\text{FoM} = \sqrt{\text{Area}} \times \text{Power(Post)} \times \text{Max. Delay(Post)} \times \text{Max. Delay(Pre)}^3$
2. Area: Layout area (unit: μm^2)
3. Power (Post): Total power consumption at TT corner in post-sim (unit:mW)
4. Max. Delay (Post): Maximum delay among all transitions at TT corner in post-sim (unit: ns)
5. Max. Delay (Pre): Maximum delay among all transitions at TT corner in pre-sim (unit: ns)
6. Unit of FoM: $\mu m \times mW \times (ns)^4$

IV. Report

Please write the report according to the following format.

1. Block diagram
   a) Please draw the block diagram of your 15-to-4 Thermometer to Binary Converter and mark the critical path. (5%)
   b) Please provide the transistor size of each gate and the gate size of each stage. Describe how the gate size is decided to minimize delay. (10%)

2. Please run pre-sim of your TBC at TT corner.
   a) Show the simulation waveform and check whether the function is correct. (0%)
   b) Measure the delay of all transitions and fill the following table. Find the maximum and minimum delay among all transitions. (3%)

Transition	Delay	Transition	Delay
0 to 1		15 to 14	
1 to 2		14 to 13	
2 to 3		13 to 12	
3 to 4		12 to 11	
4 to 5		11 to 10	
5 to 6		10 to 9	
6 to 7		9 to 8	
7 to 8		8 to 7	
8 to 9		7 to 6	
9 to 10		6 to 5	
10 to 11		5 to 4	
11 to 12		4 to 3	
12 to 13		3 to 2	
13 to 14		2 to 1	
14 to 15		1 to 0	

   c) Please discuss the result of part b. (7%)

d) Measure the power consumption of all transitions and fill the following table. Find the maximum and minimum power consumption among all transitions. (3%)

Transition	Power	Transition	Power
0 to 1		15 to 14	
1 to 2		14 to 13	
2 to 3		13 to 12	
3 to 4		12 to 11	
4 to 5		11 to 10	
5 to 6		10 to 9	
6 to 7		9 to 8	
7 to 8		8 to 7	
8 to 9		7 to 6	
9 to 10		6 to 5	
10 to 11		5 to 4	
11 to 12		4 to 3	
12 to 13		3 to 2	
13 to 14		2 to 1	
14 to 15		1 to 0	
Total Power Consumption:			

e) Please discuss the result of part d. (7%)

3. Please run pre-sim of your TBC at FF, SS, FS, and SF corner.
   a) Show the simulation waveform and check whether the function is correct. (0%)
   b) Measure the delay of all transitions and fill the following table. Compare the result with TT corner. (5%)

Transition	Delay				
	TT	FF	SS	FS	SF
0 to 1					
1 to 2					
2 to 3					
3 to 4					
4 to 5					
5 to 6					
6 to 7					
7 to 8					
8 to 9					
9 to 10					
10 to 11					

11 to 12					
12 to 13					
13 to 14					
14 to 15					
15 to 14					
14 to 13					
13 to 12					
12 to 11					
11 to 10					
10 to 9					
9 to 8					
8 to 7					
7 to 6					
6 to 5					
5 to 4					
4 to 3					
3 to 2					
2 to 1					
1 to 0					

c) Measure the total power consumption and fill the following table. Compare the result with TT corner. (5%)

	TT	**FF**	**SS**	**FS**	**SF**
Total Power					

4. Please finish your layout. (10%)
   a) Provide your layout screenshot with the width and length marked. Compute the area and aspect ratio of your layout.
   b) Show your DRC and LVS result.

5. Please run post-sim of your TBC.
   a) Show the simulation waveform and check whether the function is correct at all 5 corners. (0%)
   b) Measure the delay of all transitions at TT corner and fill the following table. Compare the result with pre-sim. (5%)

Transition	Delay		Transition	Delay	
	Pre-sim	Post-sim		Pre-sim	Post-sim
0 to 1			15 to 14		
1 to 2			14 to 13		
2 to 3			13 to 12		
3 to 4			12 to 11		
4 to 5			11 to 10		
5 to 6			10 to 9		
6 to 7			9 to 8		
7 to 8			8 to 7		
8 to 9			7 to 6		
9 to 10			6 to 5		
10 to 11			5 to 4		
11 to 12			4 to 3		
12 to 13			3 to 2		
13 to 14			2 to 1		
14 to 15			1 to 0		

c) Measure the power consumption of all transitions at TT corner and fill the following table. Compare the result with TT corner. (5%)

Transition	Power		Transition	Power	
	Pre-sim	Post-sim		Pre-sim	Post-sim
0 to 1			15 to 14		
1 to 2			14 to 13		
2 to 3			13 to 12		
3 to 4			12 to 11		
4 to 5			11 to 10		
5 to 6			10 to 9		
6 to 7			9 to 8		
7 to 8			8 to 7		
8 to 9			7 to 6		
9 to 10			6 to 5		
10 to 11			5 to 4		
11 to 12			4 to 3		
12 to 13			3 to 2		
13 to 14			2 to 1		
14 to 15			1 to 0		
Total Power Consumption (Pre-sim): Total Power Consumption (Post-sim):					

6. Please fill the SPEC table and compute FoM (10%)

SPEC Table			
Design item	**SPEC**	**Score**	**Your Design**
Power Supply	$\leq$ 1.8V	0%	
Max. Delay at TT corner (Pre-sim)	$\leq$ 1.2ns	10%	
	$\leq$ 1.5ns	7.5%	
	$\leq$ 2.0ns	5%	
	$\leq$ 2.5ns	2.5%	
	$>$ 2.5ns	0%	
Max. Delay at TT corner (Post-sim)	As small as possible	0%	
Total Power consumption at TT corner (Post-sim)	As small as possible	0%	
Layout Area	As small as possible	0%	
Layout Aspect Ratio	$\frac{\text{long side}}{\text{short side}} \leq 3$	0%	
Figure of Merit (FoM)	As small as possible	0%	

Note: $\text{FoM} = \sqrt{\text{Area}} \times \text{Power(Post)} \times \text{Max. Delay(Post)} \times \text{Max. Delay(Pre)}^3$

V. Ranking of FoM

1. For students whose design meets the SPEC of power supply ≤ 1.8V, maximum delay at TT corner ≤ 1.2ns, and layout aspect ratio ≤ 3.
2. The top-performing student receives all the points in this part, the lowest-performing student receives 0 points in this part, and the remaining students are graded proportionally.

VI. Demo

1. The time and location of the demo session will be announced separately on eeclass.
2. In the demo session, you will have to describe your design to TAs and explain your design considerations. In additions, TAs might ask you some questions about your design.
3. The simulation/DRC/LVS/PEX results will be shown to TAs and TAs will record your FoM.
4. The best specification is required to be shown in the demo session. The grading of your specification depends on the result you provide in the demo session, and the data in your report should be matched to the result.

VII. Grading

1. Report
   a) Question 1 to 5: 65%
   b) SPEC Table: 10%
2. Ranking: 10%
3. Demo: 15%