

1. (47%) One type of circuit implementation of positive-edge-triggered D flip-flops (positive-ET DFFs) is based on NAND gates, as shown in Fig. 1.

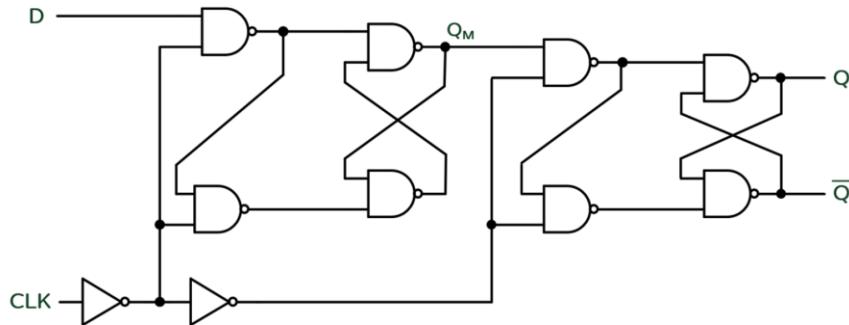


Fig. 1. NAND-based positive-ET DFF

Process	(1) 0.18um technology	(2) 16nm technology (ADFP)
CLK	100MHz with $t_r=t_f=50\text{ps}$ , duty cycle=50%	
V <sub>DD</sub>	1.8V	1V
Unit inverter size	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu m}{0.18\mu m}; \left(\frac{w}{L}\right)_p = \frac{1.85\mu m}{0.18\mu m}$	L=16nm, nfin <sub>n</sub> =2, nfin <sub>p</sub> =2

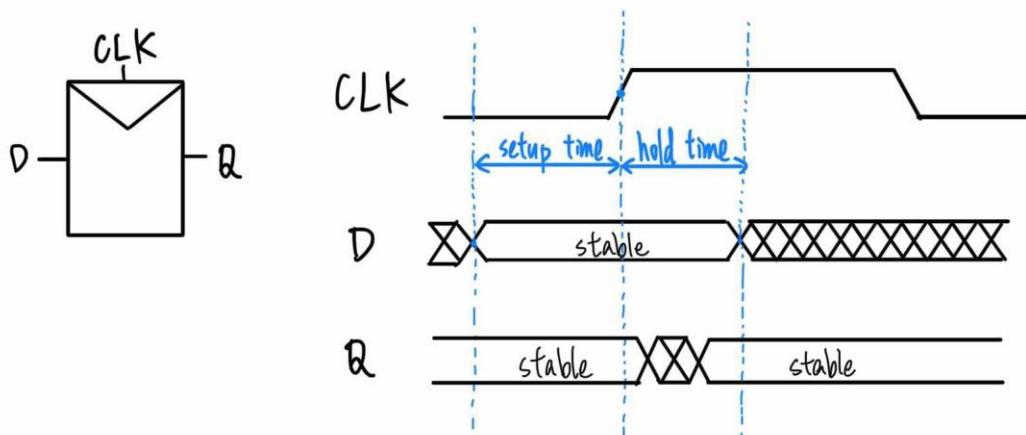
Table 1. Specification for Q1.

With the specification in Table 1, please answer the following questions:

- (a). Explain what “setup time” and “hold time” of a positive-ET DFF are. (**Multiple choice**, with only one correct answer for each \_) (2%)

**Setup time** of a positive-ET DFF means the minimum allowable time duration that the inputted data at pin D needs to be stable before CLK rising edge. On the other hand, **hold time** of a positive-ET DFF means the minimum allowable time duration that the inputted data at pin D needs to be stable after CLK rising edge.

- (b). **Draw** some waveform(s) to show the concept of “setup time” and “hold time.” In the waveform(s), there must be “D,” “CLK,” “Q” signals of a positive-ET DFF, and clearly mark “setup time” and “hold time.” (You don’t need to simulate this question with HSPICE.) (2%)



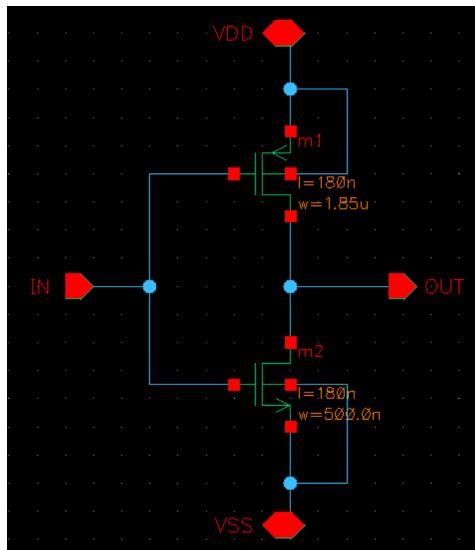
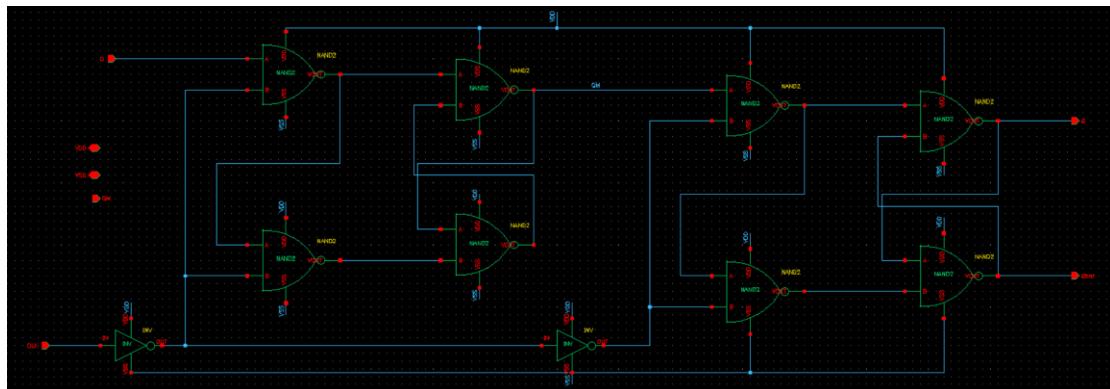
- (c). Do setup time and hold time depend on the frequency of CLK? That is, when we change CLK signal from 100MHz to 200MHz with the same  $t_r$ ,  $t_f$ , and duty cycle, do setup time and hold time remain the same? **Explain** with the reasoning. It's better to draw some figure or waveform to help. (You don't need to simulate this question with HSPICE.) (1%)

Setup time 和 hold time 理論上不會跟 CLK 的頻率有關，因為理論上 setup time 只跟 flip flop 內部節點有哪些在 CLK 訊號進來之前必須要被翻轉，以及 D 的翻轉訊號到達這些節點的 delay 有關，CLK 的頻率理論上不會影響到這些改變 setup time 的因素，而理論上 hold time 也只跟 CLK 到達時間的不確定性有關，而 CLK 的頻率理論上不會跟 sample edge 的到達時間不確定性有相關，因此綜上所述，setup time 和 hold time 理論上不會跟 CLK 的頻率有關。

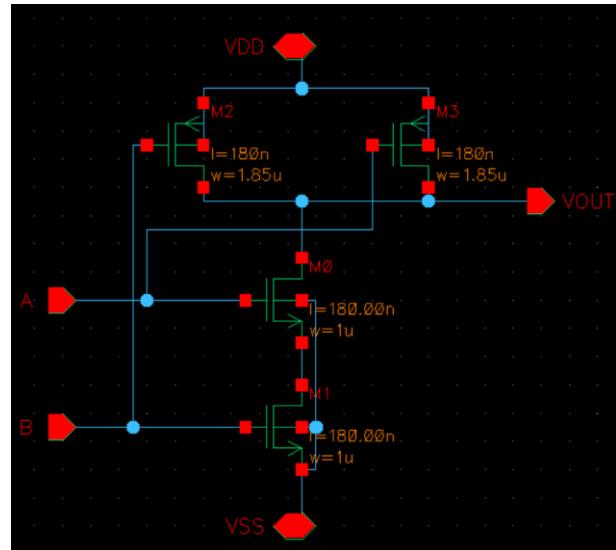
- (d). Based on the unit inverter size shown in Table 1, design the size of NAND logic gates **by hand-calculation**, with the following requirements: (You don't need to simulate this question with HSPICE.) (3%)
- The pull-up resistance of NAND should be the same as that of unit inverter.
  - The pull-down resistance of NAND should be the same as that of unit inverter.
  - Due to no output loading in this question, you can design all NAND gates with exactly the same size ( $W$ ,  $L$ ,  $m$ ).
  - [Answer this question for 0.18um technology](#)

首先我們假設在相同閘極長度  $L$  時，導通電阻  $R_{on}$  會與閘極寬度  $W$  成正比，並且令 NMOS 的尺寸為  $\left(\frac{W}{L}\right)_n \cong \frac{0.5\mu m}{0.18\mu m}$  時，導通電阻為  $R_n$ ；PMOS 的尺寸為  $\left(\frac{W}{L}\right)_p \cong \frac{1.85\mu m}{0.18\mu m}$  時，導通電阻為  $R_p$ ，因為題目給的尺寸是 unit inverter 的，因此也假設  $R_n = R_p = R$ 。負責 pull up 的是兩顆並聯的 PMOS，這使得 PMOS 的尺寸不用改變就可以滿足 pull up resistance 跟 unit inverter 一樣會是  $R$ ；負責 pull down 的是兩顆串聯的 NMOS，這使得 NMOS 的 size 需要變成在 unit inverter 中的兩倍，讓單顆 NMOS 的  $R_{on} = 0.5R$ ，串聯後的 pull down resistance 才會跟 unit inverter 一樣是  $R$ 。因此設計出的 NAND 的 MOS 尺寸分別為  $\left(\frac{W}{L}\right)_n \cong \frac{1\mu m}{0.18\mu m}$ ， $\left(\frac{W}{L}\right)_p \cong \frac{1.85\mu m}{0.18\mu m}$ 。

- (e). Using the sizes you have designed in (d), build up the schematic of DFF using Composer. **Screenshot** the schematic of your DFF. Schematics inside **all blocks** (including NAND2, inverter) should be provided. (1%)



inverter



2 input NAND gate

- (f). With specifications in Table 1, run HSPICE simulation (pre-layout simulation) to find the **setup time** of this DFF. The input D signal will be designed by yourself. **Answer the following questions for 0.18um technology.**

- (f-1). **Describe** in detail how you design the input D signal to get the **setup time** of this DFF. It is better to echo with the definition of setup time in (a). (2%)

依據(a)的定義，要找出 setup time 就相當於要找出訊號 D 最少需要提前 trigger 的 rising edge 多長的時間就要開始保持穩定，而判斷這個最少所需時間的標準就是至少要使 Q 能夠確實接收到 D 所傳遞的訊號而做出改變。因此操控 D 訊號在 CLK 訊號的 rising edge 前  $t_{su}$ (令  $t_{su}$  為 setup time)有一個 rise 或是 fall 的變化，並且 sweep 過  $t_{su}$  這個參數(step size=1ps)，看看在  $t_{su}$  是多少的時候，Q 的波形會開始正確地對於 D 的變化做出相應的變化，則此  $t_{su}$  即為 setup time。因此讓 input 是一個 pulse 訊號並且跟 CLK 有一個  $t_{su} +$  一個周期的時間差。多加一個週期是為了讓各節點的 initial condition 被洗掉。

(f-2). For rising input (D), **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

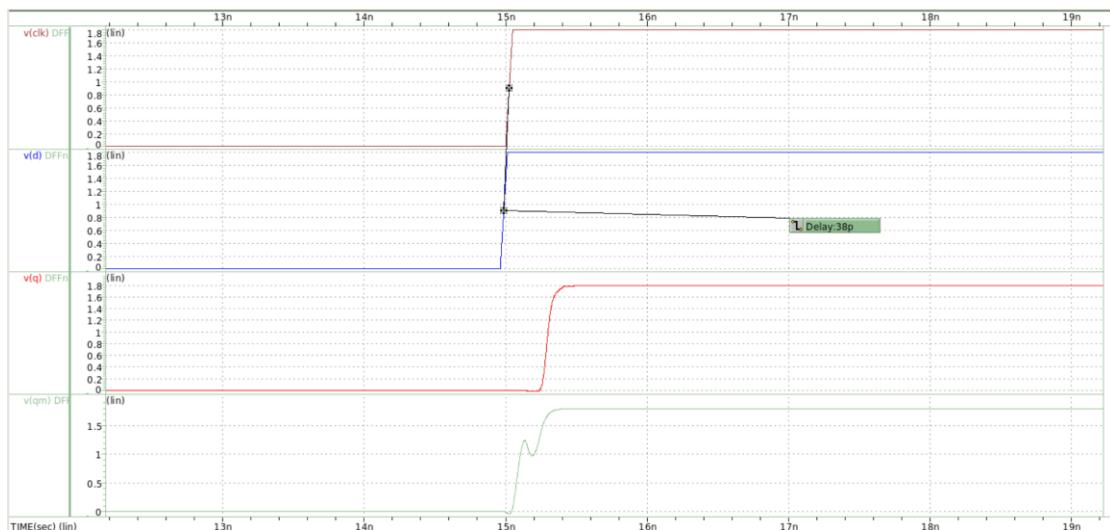
```
VCLK CLK 0 PULSE(0 VDD t 50p 50p 4.95n 10n)
```

```
VD D 0 PULSE(0 VDD t1 50p 50p 4.95n 10n)
```

Note:  $t = \text{clock}$  的第一個 rising 時間 = 5ns

$$t1 = t + \text{一個週期} - \text{setup time} = 10\text{ns} + 5\text{ns} - 38\text{ps} = 14.962\text{ns}$$

(f-3). For rising input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time on the waveform. Here we define the transition point of signals as 0.5V<sub>DD</sub>. (1%)



Setup time for rising D = 38ps(量測的點都是 V=0.9V)

(f-4). For falling input, **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

```
VCLK CLK 0 PULSE(0 VDD t 50p 50p 4.95n 10n)
```

```
VD D 0 PULSE(VDD 0 t1 50p 50p 4.95n 10n)
```

Note:  $t = \text{clock}$  的第一個 rising 時間 = 5ns

$$t1 = t + \text{一個週期} - \text{setup time} = 10\text{ns} + 5\text{ns} - 73\text{ps} = 14.927\text{ns}$$

(f-5). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time on the waveform. (1%)



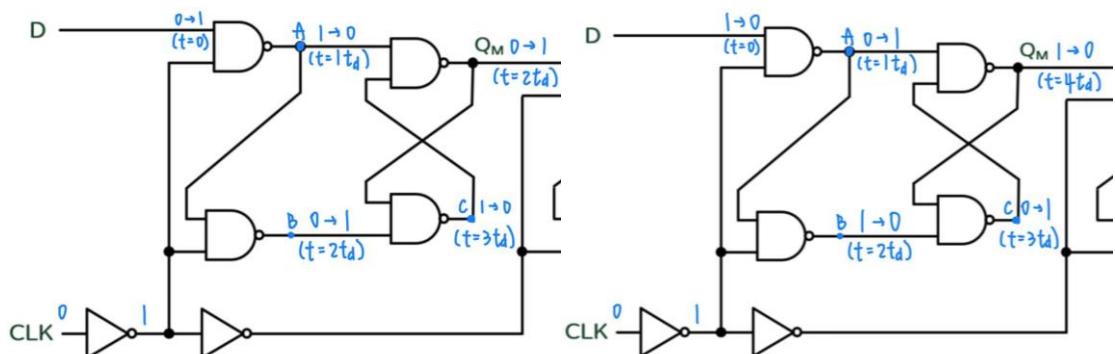
Setup time for falling D = 73ps(量測的點都是 V=0.9V)

(f-6). Compare setup time between rising input and falling input. Which one has larger setup time?

Why? It's better to explain with the circuit in Fig. 1. (1%)

Setup time (pre-sim)	
rising input D	falling input D
38ps	73ps

可以看到 falling input D 的 setup time 比 rising input D 的還要大得多，雖然說 setup time 應該是要如前面所說的看 output Q 為準，但其實只要訊號能夠從 D 傳遞到  $Q_M$ ，把訊號  $Q_M$  確實的改變，那代表訊號一定會順利傳到 output Q，而要讓  $Q_M$  確實的改變，對於 rising input，則要確保至少有將 D 與  $\overline{CLK}$  的 NAND output (如下圖的 A 點)確實的拉到邏輯 0；對於 falling input，則要確保至少有將 A 與  $\overline{CLK}$  的 NAND output (如下圖的 B 點)確實的拉到邏輯 0。可以藉由 Fig. 1 來解釋此現象，令  $t_d$  為一個 NAND gate 的 delay，trace 當  $CLK=0$  時電路中的節點訊號改變的時間點，如下圖：



左圖：rising input D

右圖：falling input D

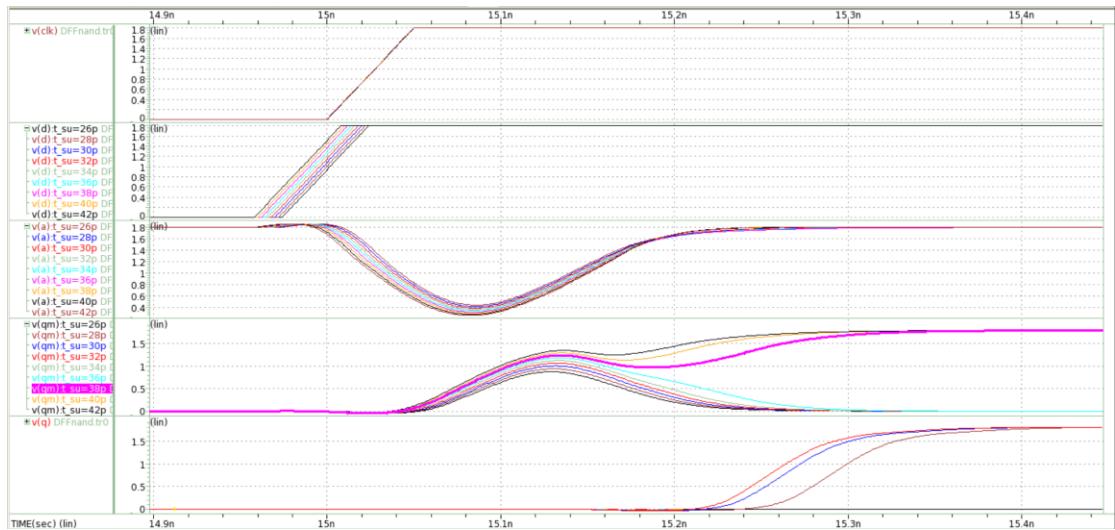
由此可見當 rising input 時，只要確實改變 A，無論 C 已經有或還沒有被改變， $Q_M$  一定會被拉到 1，而要從 input D 傳遞到 A 只需要經過 1 個 NAND gate 就可

以了；當 falling input 時，只要確實改變 B (代表 A 也一定已經改變了)，則  $Q_M$  一定會被拉到 0，而要從 input D 傳遞到 B 需要經過 2 個 NAND gate，所以 falling input 的 setup time 差不多會是 rising input 的 setup time 的兩倍，與模擬結果相符。

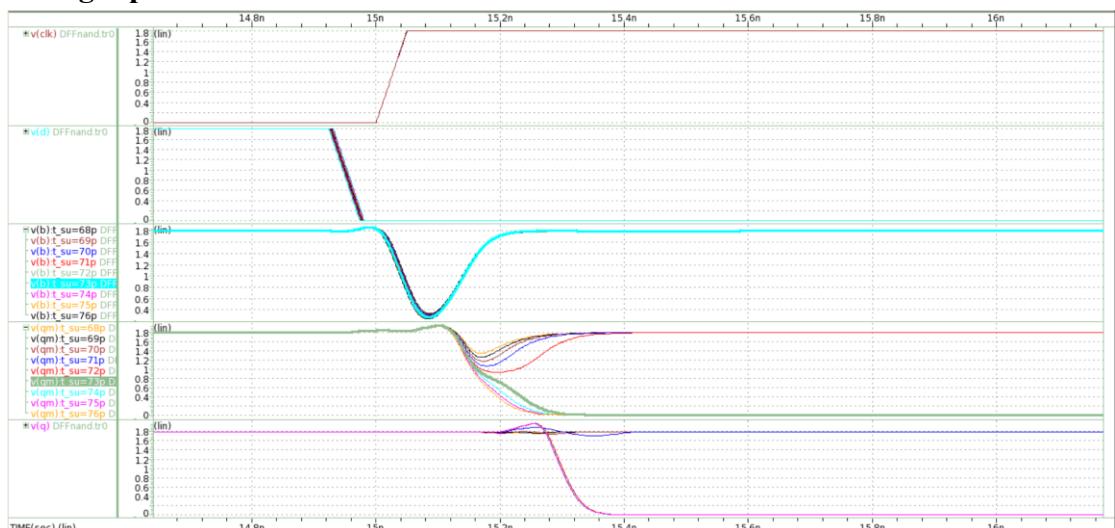
(f-7). When the setup-time constraint of this DFF is **violated**, what will happen? Please provide with some **comments** and use **simulation waveform** to verify your idea. (2%)

如果沒有在 CLK 的 positive edge 到的時間前至少間隔 setup time 改變 input D，那會導致 output Q 不會成為 input D 所變成的訊號，而會 output 出 D 原本未改變前的訊號。這是因為沒有給足夠的時間(setup time)讓節點(上一小題的 A/B)完全變成新的訊號(被拉到邏輯 0 or 1)，因此  $Q_M$  會被拉回原本(D 改變前)的訊號，output Q 也因此會是原本的訊號。可以從下兩圖的 waveform 驗證這樣的想法：

### rising input D



### falling input D



這兩張是在.tran 分析下 sweep t\_su 的 waveform，a 和 b 分別代表上一小題圖中

的 A 和 B 點，加粗的線代表的是  $t_{su}$  等於 setup time 的情況，可以看到當  $t_{su}$  小於 setup time 時， $Q_M$  雖然有被拉動，但是還沒被完全拉到 1 或 0，就會無法順利傳遞 D 的改變到 output Q 去。

- (g). With specifications in Table 1., run HSPICE simulation (pre-layout simulation) to find the **hold time** of this DFF. The input D signal will be designed by yourself. [Answer the following questions for 0.18um technology.](#)

- (g-1). **Describe** in detail how you design the input D signal to get the **hold time** of this DFF. It is better to echo with the definition of hold time in (a). (1%)

依據(a)的定義，要找出 hold time 就相當於要找出訊號 D 最少需要在 trigger 的 rising edge 之後多長的時間內保持穩定，而判斷這個最少所需時間的標準就是至少要使 Q 能夠確實接收到 D 在 CLK 訊號的 rising edge 之前所傳遞的訊號而做出改變。因此操控 D 訊號在 CLK 訊號的 rising edge 後  $t_{hold}$ (令  $t_{hold}$  為 hold time)有一個 rise 或是 fall 的變化，並且 sweep 過  $t_{hold}$  這個參數(step size=1ps)，看看在  $t_{hold}$  是多少的時候，Q 的波形會開始正確地對於 D 在 CLK 的 rising edge 之前所做出的變化做出相應的變化，則此  $t_{hold}$  即為 hold time。不過發現這個 hold time 會依 D 在 CLK 訊號的 rising edge 之前多久才做出最後的改變的時間而有所不同，因此取最嚴苛的狀況(D 在 setup time 時才做出變化)來測量，以獲得最 robust 的 hold time。

- (g-2). For rising input (D), **screenshot** the HSPICE code of voltage sources in your .sp file. (0.5%)

```
VCLK CLK 0 PULSE(0 VDD t 50p 50p 4.95n 10n)
VD D 0 PWL 0 0 t1 0 t11 VDD t3 VDD t31 0 25n 0
```

Note:  $t = \text{clock}$  的第一個 rising 時間 = 5ns

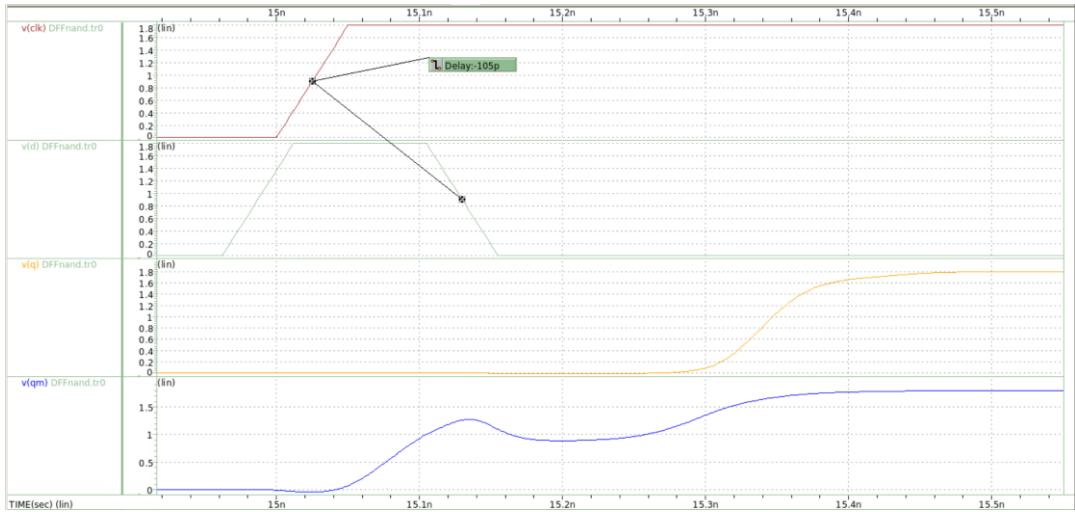
$$t1 = t + \text{一個週期} - \text{setup time} = 10\text{ns} + 5\text{ns} - 38\text{ps} = 14.962\text{ns}$$

$$t11 = t1 + \text{rising time} = 14.962\text{ns} + 50\text{ps} = 15.012\text{ns}$$

$$t3 = t + \text{一個週期} + \text{hold time} = 10\text{ns} + 5\text{ns} + 105\text{ps} = 15.105\text{ns}$$

$$t31 = t3 + \text{falling time} = 15.105\text{ns} + 50\text{ps} = 15.155\text{ns}$$

- (g-3). For rising input, **screenshot** the simulation waveform of “D,” “CLK,” “ $Q_M$ ,” “Q” signals of the DFF. **Mark** the hold time on the waveform. (1%)



Hold time for rising D = 105ps(量測的點都是 V=0.9V)

(g-4). For falling input, screenshot the HSPICE code of voltage sources in your .sp file. (0.5%)

VCLK CLK 0 PULSE(0 VDD t 50p 50p 4.95n 10n)

VD D 0 PWL 0 VDD t1 VDD t11 0 t3 0 t31 VDD 25n VDD

Note: t = clock 的第一個 rising 時間 = 5ns

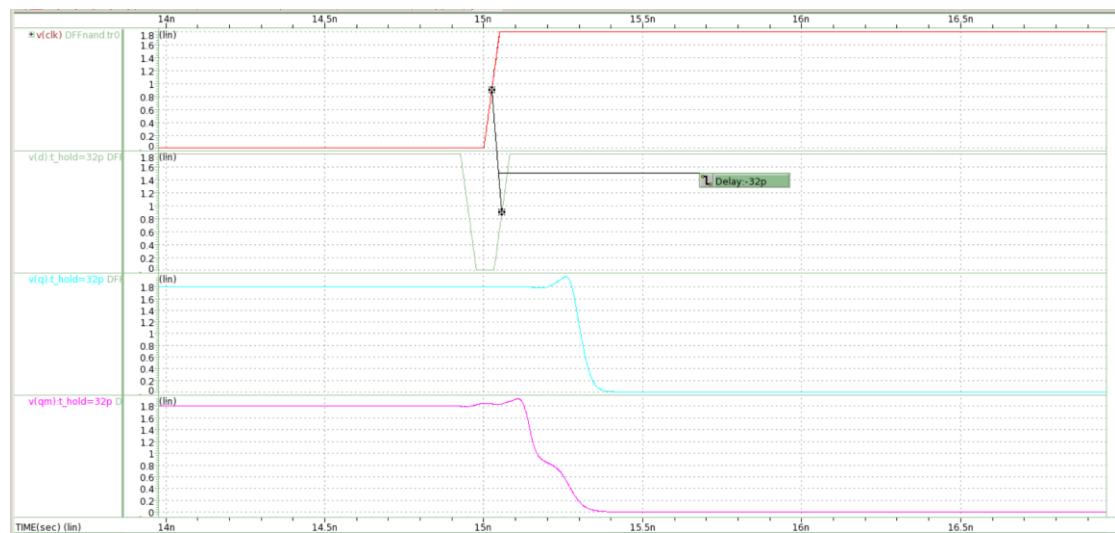
t1 = t + 一個週期 - setup time = 10ns + 5ns - 73ps = 14.927ns

t11 = t1 + rising time = 14.962ns + 50ps = 15.977ns

t3 = t + 一個週期 + hold time = 10ns + 5ns + 32ps = 15.032ns

t31 = t3 + falling time = 15.032ns + 50ps = 15.082ns

(g-5). For falling input, screenshot the simulation waveform of “D,” “CLK,” “QM,” “Q” signals of the DFF. Mark the hold time on the waveform. (1%)

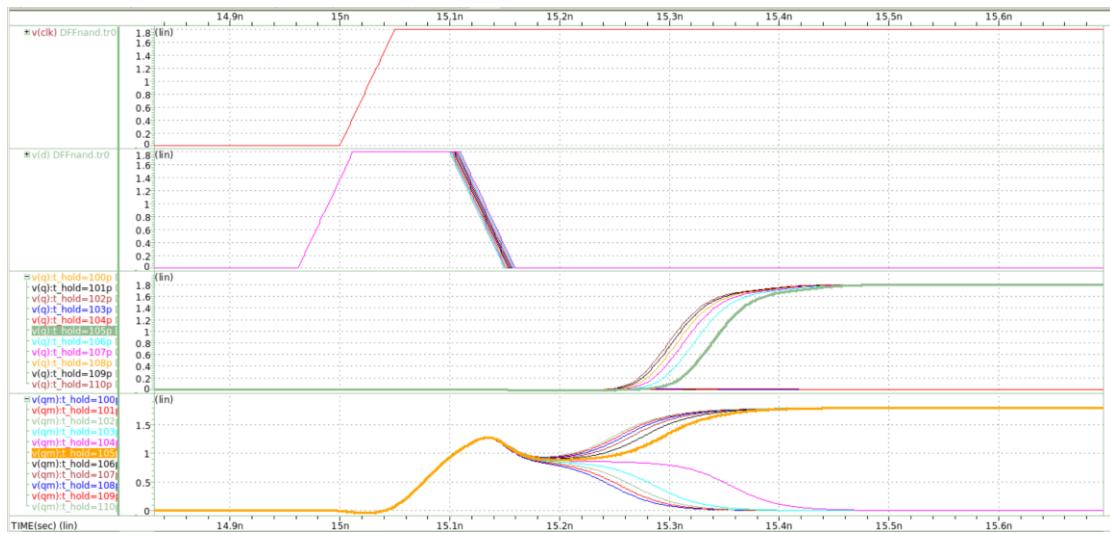


Hold time for falling D = 32ps(量測的點都是 V=0.9V)

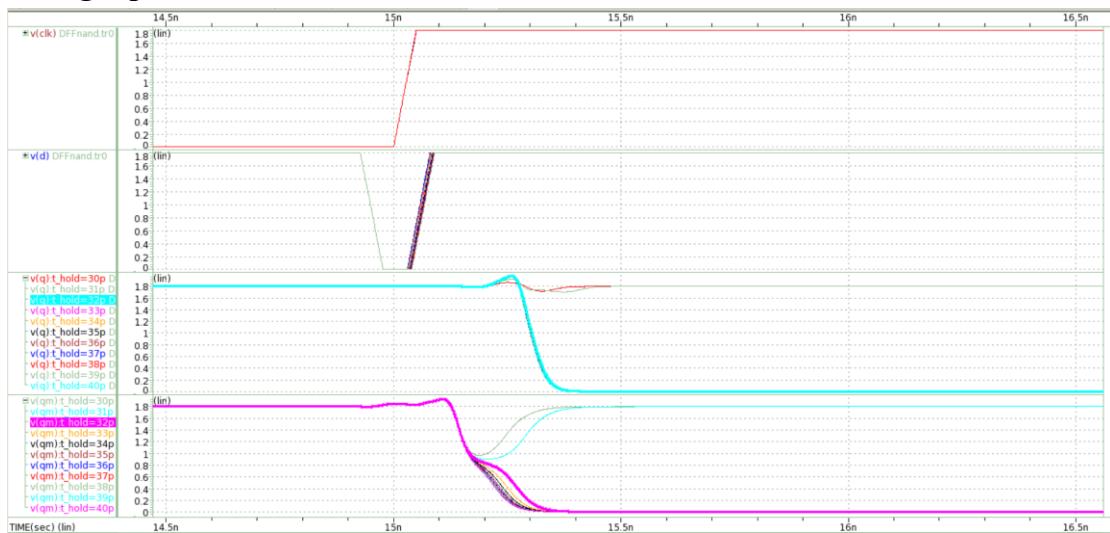
(g-6). When the hold-time constraint of this DFF is **violated**, what will happen? Please provide with some **comments** and (if the hold time of your DFF is not 0) use **simulation waveform** to verify your idea. (2%)

如果沒有讓訊號 D 在 CLK 的 trigger edge 後至少維持 hold time 的時間的話，就會造成 D 在 CLK 的 trigger edge 那個時刻的訊號無法傳遞到 output Q 去，這是因為  $Q_M$  還沒完全變成新的訊號(被拉到 0 or 1)，因此  $Q_M$  會被拉回原本(D 改變前)的訊號，output Q 也因此會是原本的訊號。可以從下兩圖的 waveform 驗證這樣的想法：

### rising input D



### falling input D



這兩張是在.tran 分析下 sweep t\_hold 的 waveform，加粗的線代表的是 t\_hold 等於 hold time 的情況，可以看到當 t\_hold 小於 hold time 時， $Q_M$  雖然有被拉動，但是還沒被完全拉到 1 或 0，就會無法順利傳遞 D 的改變到 output Q 去。

(h). With specifications in Table 1, run HSPICE simulation (pre-layout simulation) to find the **clock to Q delay (CLK-to-Q delay)** of this DFF. The input D signal will be designed by yourself. [Answer the following questions for 0.18um technology](#).

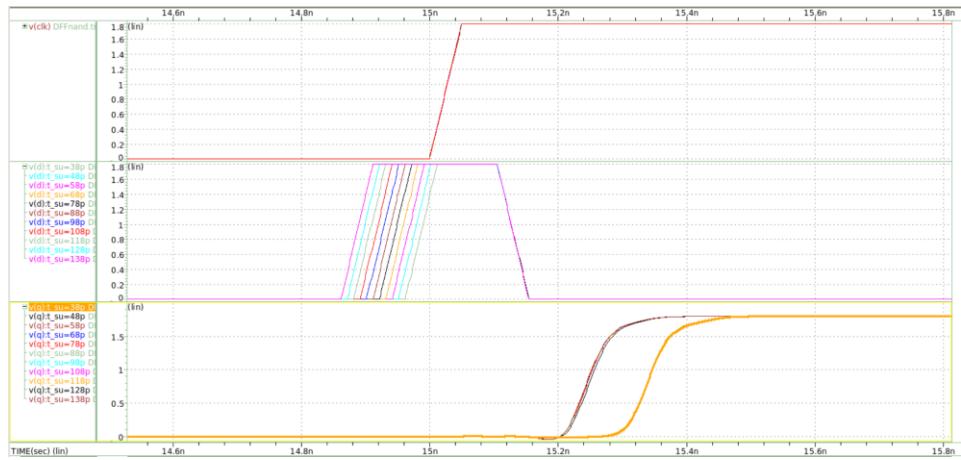
(h-1). When simulating CLK-to-Q delay, what kind of requirements does input D signal have? (1%)

Input D 所要傳遞的訊號在 CLK 的 trigger edge 前、後不同的時間開始、結束，都會造成不一樣的 CLK-to-Q delay，以下是在各種情況下模擬的 CLK、D、Q 的 waveform：

### 1. Rising input D

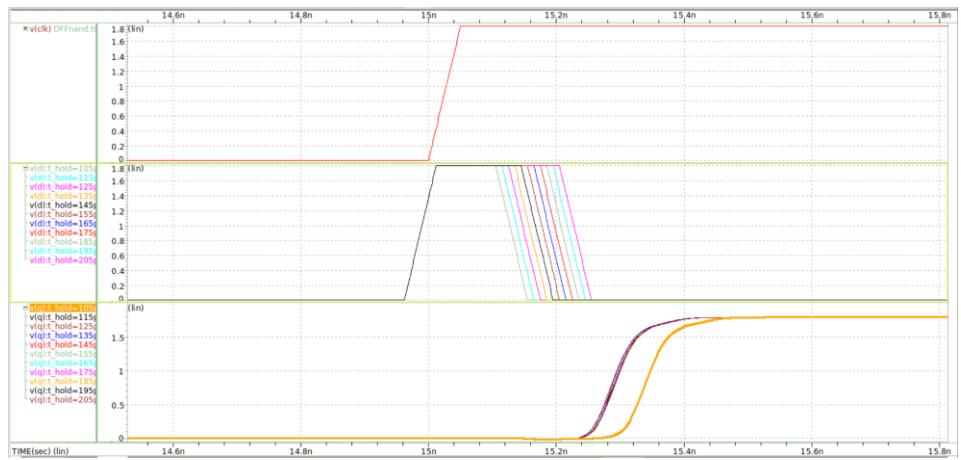
(1) 固定  $t_{hold} = hold\ time = 105ps$

Sweep  $t_{su} = 38\sim138ps$



(2) 固定  $t_{su} = setup\ time = 38ps$

Sweep  $t_{hold} = 105\sim138ps$



### 2. falling input D

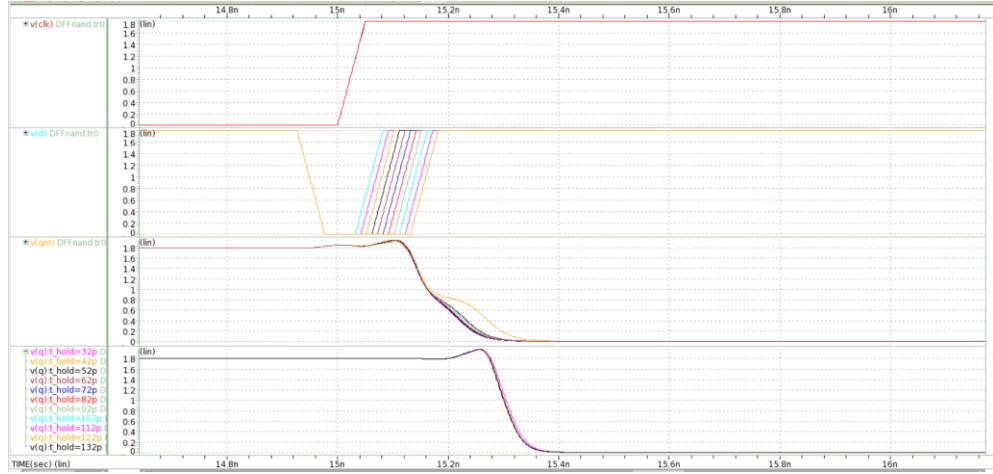
(1) 固定  $t_{hold} = hold\ time = 32ps$

Sweep  $t_{su} = 73\sim173ps$



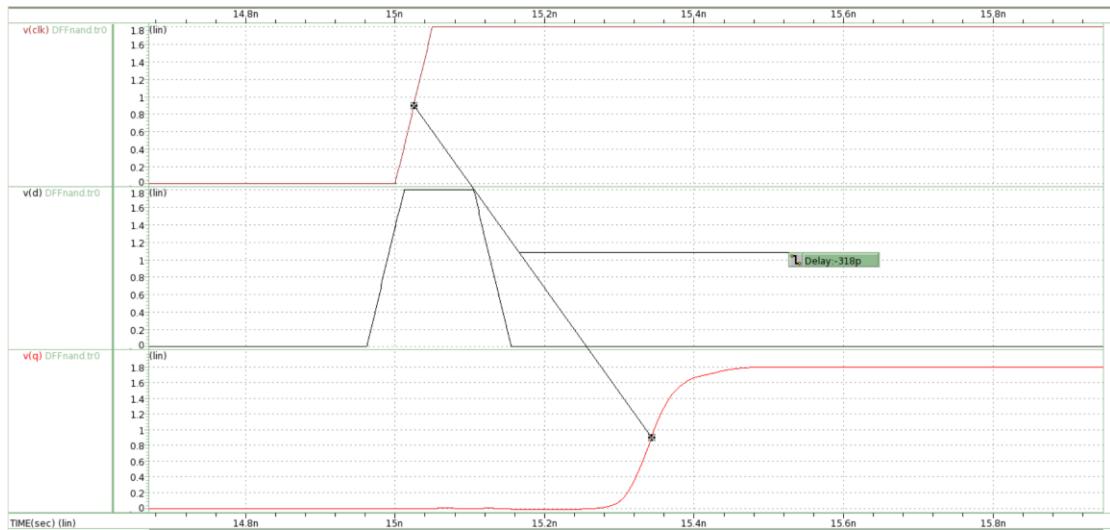
(2) 固定  $t_{su} = \text{setup time} = 73\text{ps}$

Sweep  $t_{hold} = 32\sim 132\text{ps}$



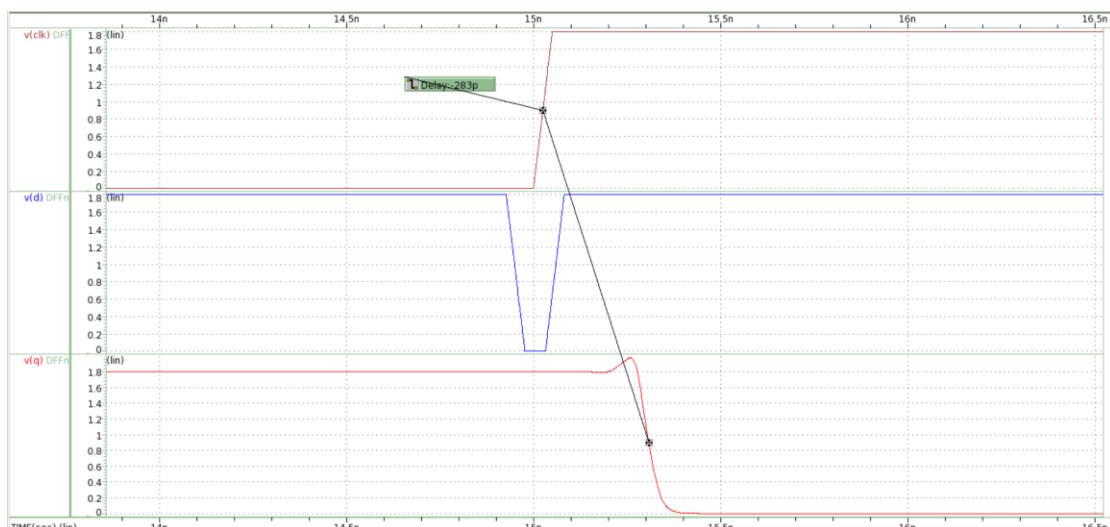
可以清楚的觀察到不管是 rising 或是 falling input 都會是在剛好滿足 setup time 與 hold time 時的狀況會有最慢的 CLK-to-Q delay，若是 D 訊號提前 trigger edge 做出最後改變的時間大於 setup time 或是在 trigger edge 後維持的時間大於 hold time，CLK-to-Q delay 的值會迅速變小並大致收斂在某個值附近(這個結論可以從前幾小題綜合這一小題的 waveform 中得到)，此題我決定使用恰好滿足 setup time 以及 hold time 的 input D，以此求得的 clock-to-Q delay 大約會是  $t_{pcq}$ 。

(h-2). For rising input (D), **screenshot** the simulation waveform of “D,” “CLK,” “Q” signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (0.5%)



CLK-to-Q delay time for falling D = 318ps(量測的點都是 V=0.9V)

- (h-3). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q” signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (0.5%)



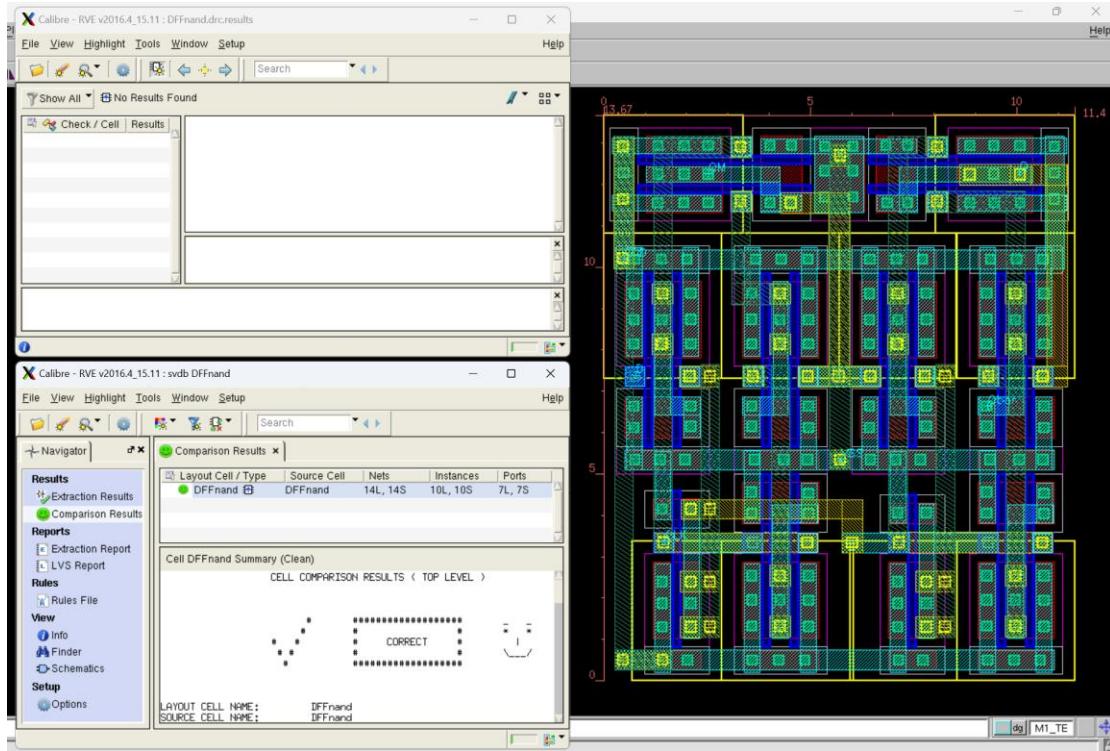
CLK-to-Q delay time for falling D = 283ps(量測的點都是 V=0.9V)

- (i). Using the sizes you have designed in (d), finish the layout of your DFF. [Answer the following questions for 0.18um technology.](#)

(i-1). There is a requirement that the layout needs to be able to be contained inside a “15um × 15um” box (which means that neither the width nor the height of your layout can be larger than 15um). Please **screenshot** your layout. **Mark** the total width and height on the layout. (5%)

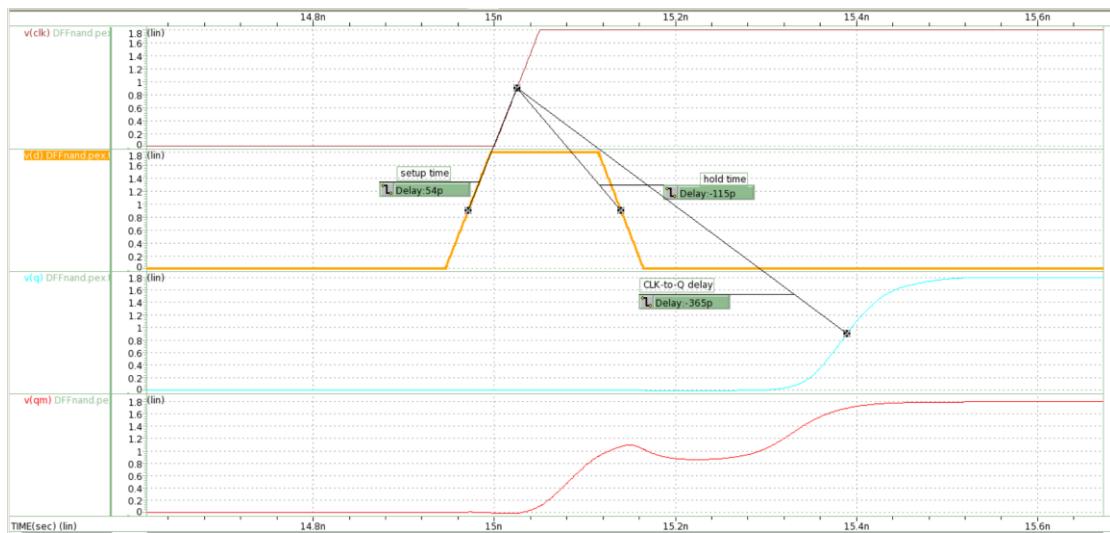
(i-2). **Screenshot** your DRC result. Make sure there is no DRC violation. (1%)

(i-3). **Screenshot** your LVS result. Make sure you get a smile \*‿\*. (1%)

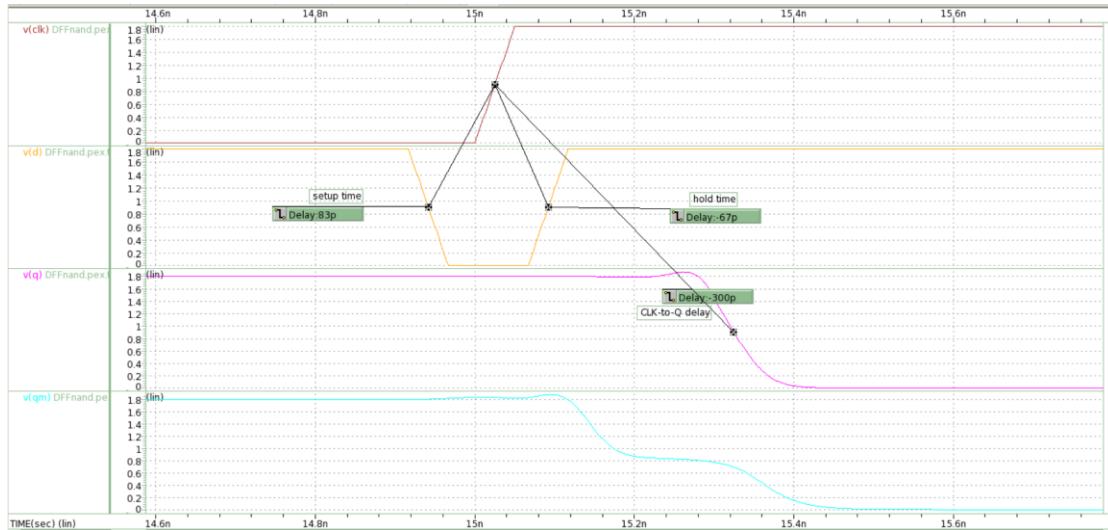


(j). Run the post-layout simulation.

(j-1). For rising input (D), **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time, hold time, and CLK-to-Q delay on the waveform. (2%)



(j-2). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time, hold time, and CLK-to-Q delay on the waveform. (2%)



(j-3). **Build a table** to compare the setup time, hold time, and CLK-to-Q delay performance between pre-sim and post-sim (for both rising input and falling input). **Where** do the differences (between pre-sim and post-sim) come from? (1.5%)

	pre-sim		post-sim	
Input D	Rising	Falling	Rising	Falling
Setup time	38ps	73ps	54ps	83ps
Hold time	105ps	32ps	115ps	67ps
CLQ-to-Q delay	318ps	283ps	365ps	300ps

可以看到每個項目都是 post-sim 略大於 pre-sim，原因是 post-sim 多考慮了實際 layout 後產生的寄生電阻與電容，使得 delay time 都往上升。

2. (14%) Another type of circuit implementation of positive-ET DFFs is based on transmission gates (TGs), as shown in Fig. 2. The circuit implementation of TG is shown in Fig. 3.

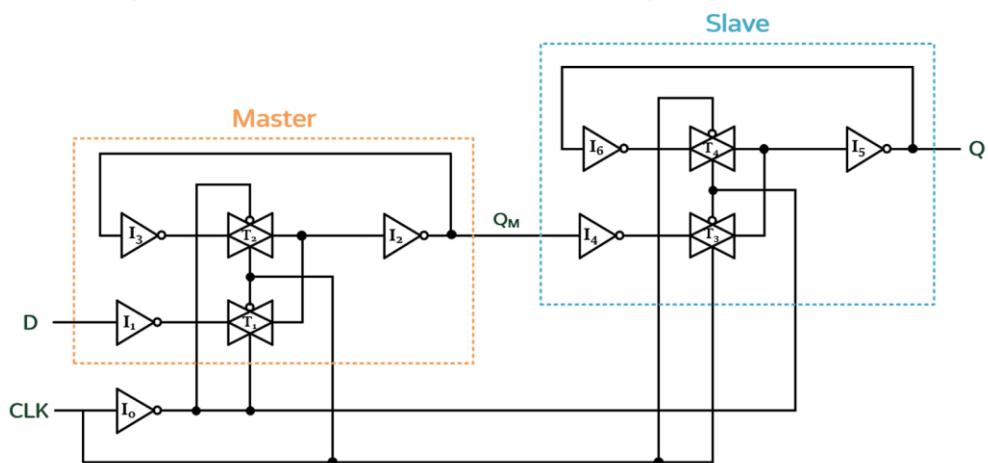


Fig. 2. TG-based positive-ET DFF

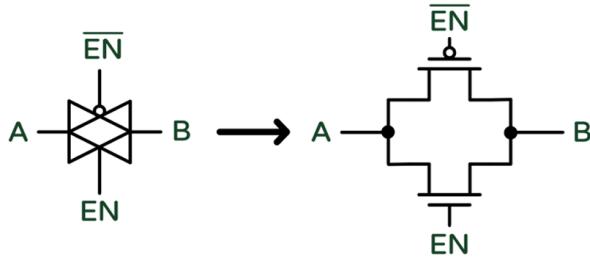


Fig. 3. Circuit implementation of TG

Process	0.18um technology
CLK	100MHz with $t_r=t_f=50\text{ps}$ , duty cycle=50%
V <sub>DD</sub>	1.8V
Unit inverter size	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu\text{m}}{0.18\mu\text{m}}, \left(\frac{w}{L}\right)_p = \frac{1.85\mu\text{m}}{0.18\mu\text{m}}$
TG size	$\left(\frac{w}{L}\right)_n = \frac{1\mu\text{m}}{0.18\mu\text{m}}, \left(\frac{w}{L}\right)_p = \frac{1\mu\text{m}}{0.18\mu\text{m}}$

Table 2. Specification for Q2.

#### Notation:

$t_{pd\_inv}$  = the propagation delay of an inverter

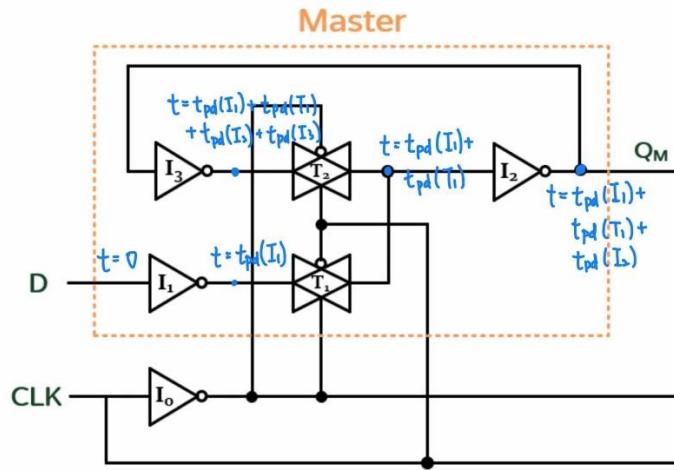
$t_{pd\_TG}$  = the propagation delay of a TG

$t_{pd}(I_{xx})$  = the propagation delay of  $I_{xx}$

$t_{pd}(T_{OO})$  = the propagation delay of  $T_{OO}$

- (a). Assume that there is no contamination delay and  $t_{pd}(I_0)=0$ . What will the **setup time ( $t_{setup}$ )** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

Theoretically, the setup time of a TG-based positive-ET DFF is “ $3 t_{pd\_inv} + 1 t_{pd\_TG}$ .” More specifically,  $t_{setup} = t_{pd}(I_1) + t_{pd}(T_1) + t_{pd}(I_2) + t_{pd}(I_3)$ .” The reason is 為了使 output Q 的訊號會確實的成為 input D 在 CLK 的 rising edge 的訊號，則要確保  $Q_M$  在 CLK 的 rising edge 將  $T_2$  導通時，可以被確實的拉成 input D 的訊號，那麼至少在 CLK 的 rising edge 將  $T_1$  截斷、 $T_2$  導通時，訊號需要從 input D 傳遞到  $I_3$  後  $T_2$  前的節點 (比較保險，不會發生 fighting，可以參考下圖的路徑)，訊號需要經過  $I_1$ ,  $T_1$ ,  $I_2$ ,  $I_3$  才會到達  $I_3$  後  $T_2$  前的節點，所以此路徑的 propagation delay 即為 setup time.

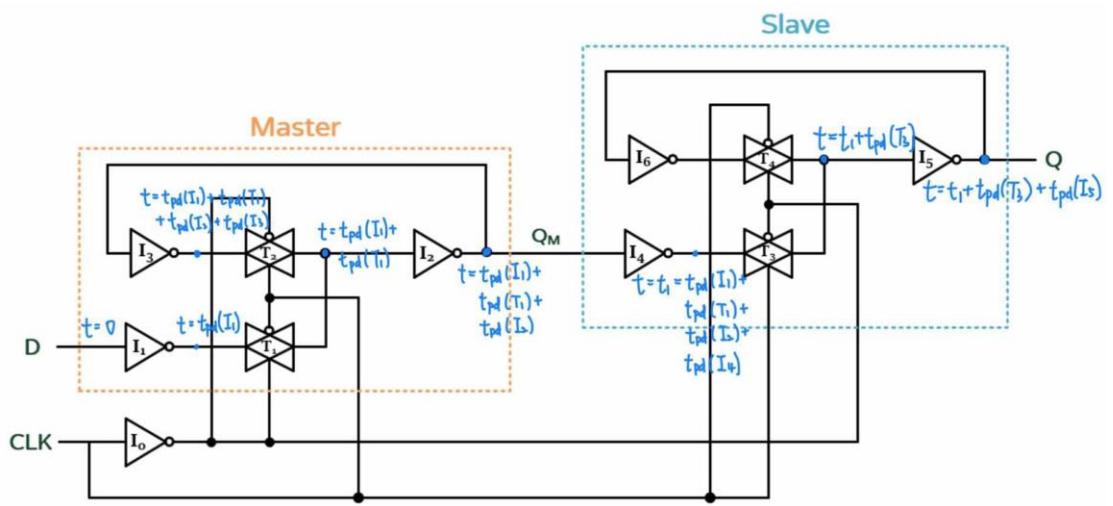


- (b). Assume that there is no contamination delay and  $t_{pd}(I_0)=0$ . What will the **hold time (t<sub>hold</sub>)** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

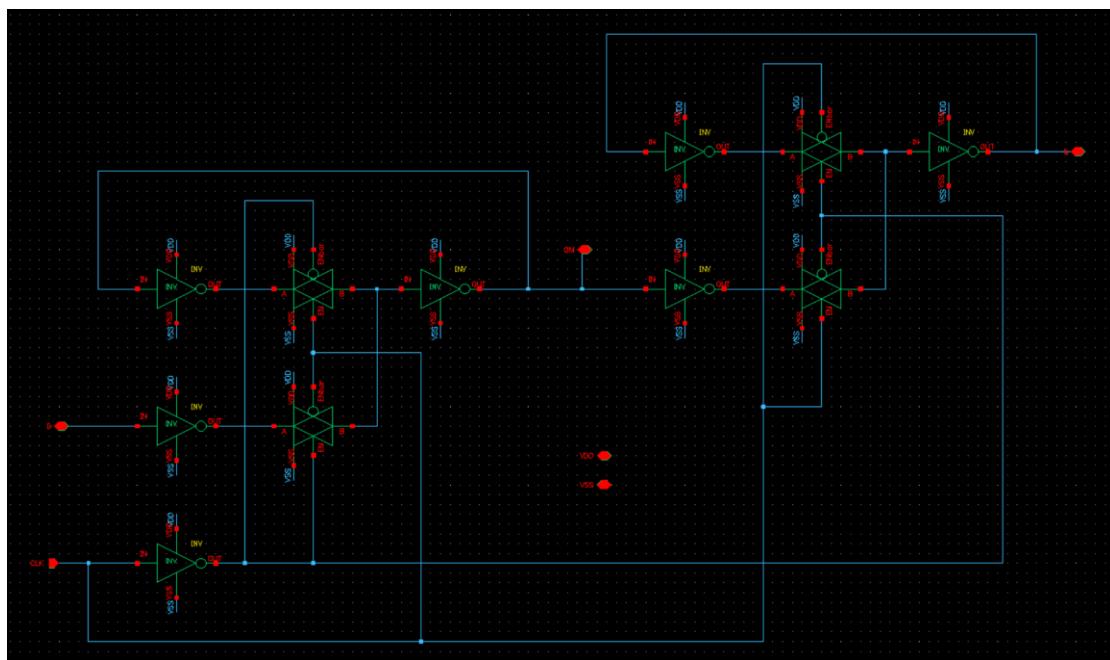
Theoretically, the hold time of a TG-based positive-ET DFF is “ $0 \ t_{pd\_inv} + 0 \ t_{pd\_TG}$ .” More specifically,  $t_{hold} = "0."$  The reason is 會有 hold time 是因為考慮到 CLK 不完美的情況下，訊號傳遞過程中可能有干擾或 delay，因此 CLK 的 sampling 的時間有不確定性，導致電路運作必須要等最慢的 CLK 訊號，但這裡假設 CLK 是理想訊號且  $t_{pd}(I_0) = 0$ ，所以並不需要 hold time.

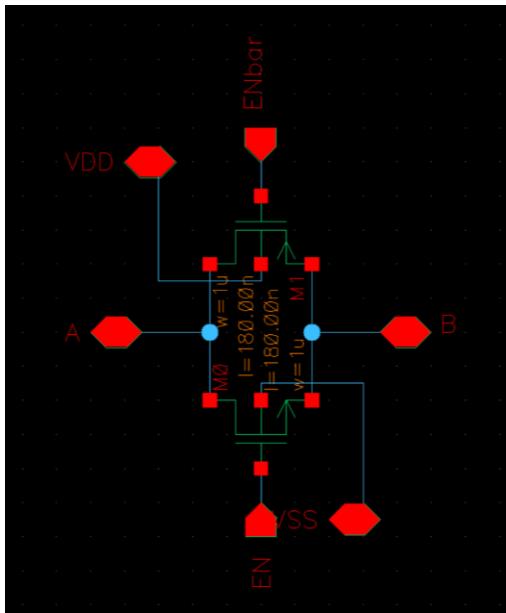
- (c). Assume that there is no contamination delay and  $t_{pd}(I_0)=0$ . What will the **CLK-to-Q delay (t<sub>c-q</sub>)** be? What's the reason behind? Please answer according to the following format. (You don't need to simulate this question with HSPICE.) (2%)

Theoretically, the CLK-to-Q delay of a TG-based positive-ET DFF is “ $1 \ t_{pd\_inv} + 1 \ t_{pd\_TG}$ .” More specifically,  $t_{c-q} = "t_{pd}(T_3) + t_{pd}(I_5)."$  The reason is 因為 input D 有比 CLK 的 rising edge 至少提前 setup time 做出最終改變，因此在 CLK 把  $T_3$  導通時，D 的訊號應該已經傳到  $I_4$  後  $T_3$  前了，因為 setup time 足夠訊號從 input D 傳過 3 個 inverter，1 個 transmission gate)，如下圖， $t_{pd}(I_1) + t_{pd}(T_1) + t_{pd}(I_2) + t_{pd}(I_3) = t_{pd}(I_1) + t_{pd}(T_1) + t_{pd}(I_2) + t_{pd}(I_4)$  所以此訊號在 CLK 將  $T_3$  導通之後，只要再經過  $T_3$  以及  $I_5$  即可到達 output Q，此路徑的 delay 即為 CLK-to-Q delay.

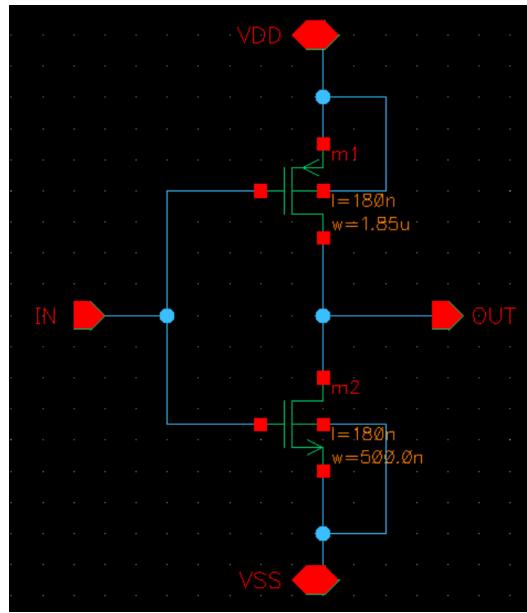


- (d). Using the sizes given in Table 2, build up the schematic of TG-based DFF using Composer. **Screenshot** the schematic of your TG-based DFF. Schematics inside **all blocks** (including TG, inverter) should be provided. (1%)



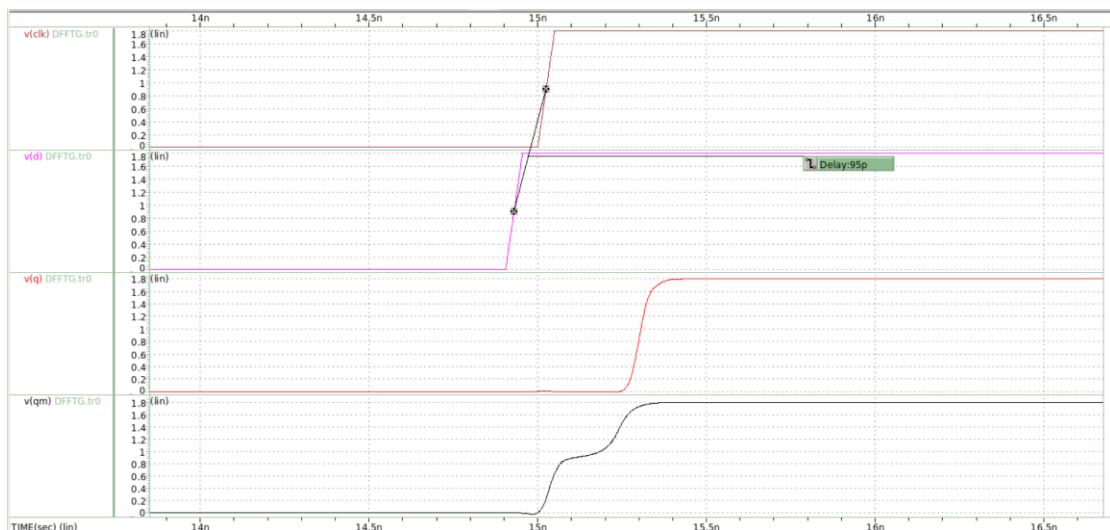


Transmission gate



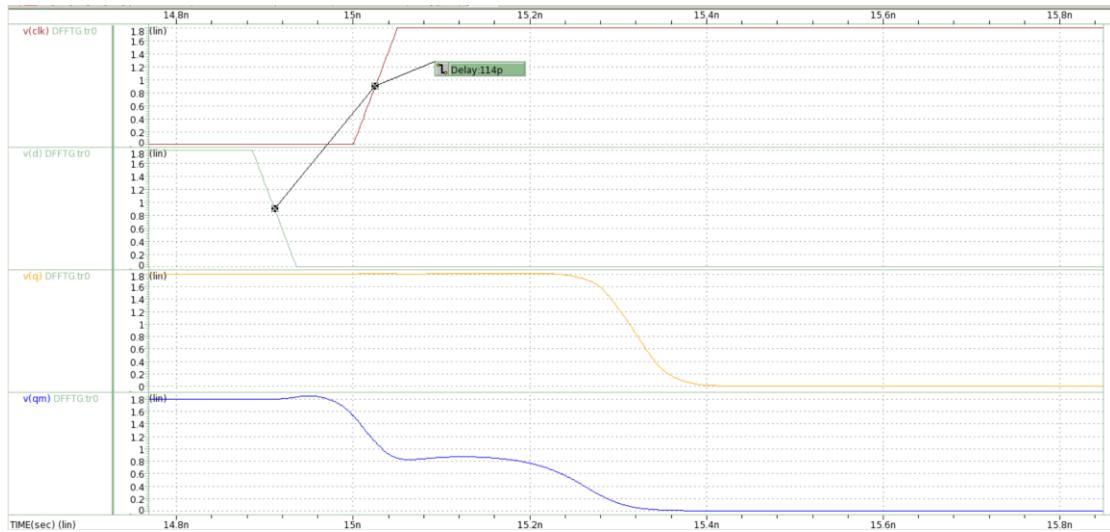
inverter

- (e). Similar to question 1.(f), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **setup time** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.
- (e-1). For rising input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time on the waveform. (1%)



Setup time for rising D = 95ps(量測的點都是 V=0.9V)

(e-2). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the setup time on the waveform. (1%)



Setup time for falling D = 114ps(量測的點都是 V=0.9V)

(f). Similar to question 1.(g), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **hold time** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.

(f-1). For rising input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the hold time on the waveform. (1%)



hold time for rising D = 39ps(量測的點都是 V=0.9V)

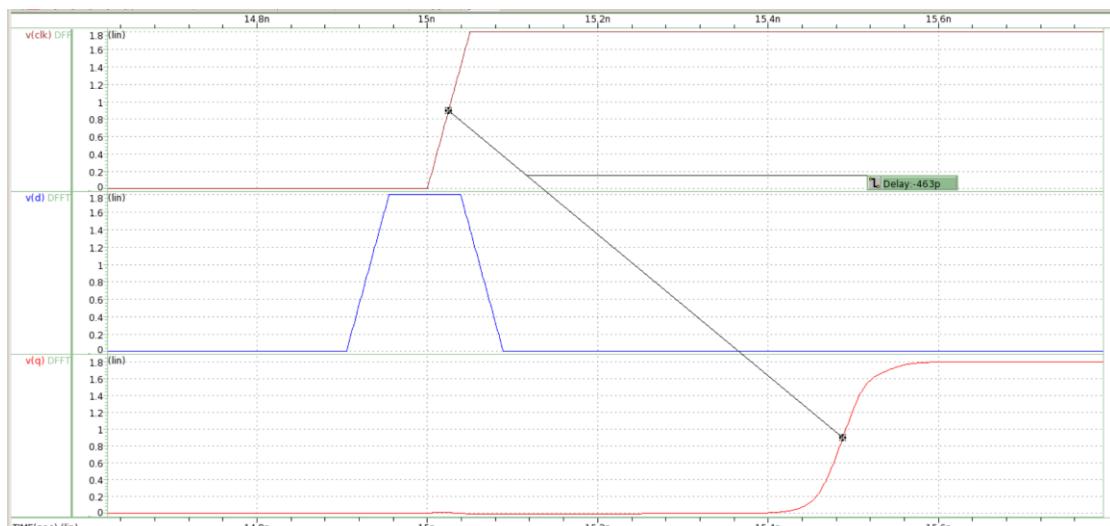
(f-2). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q<sub>M</sub>,” “Q” signals of the DFF. **Mark** the hold time on the waveform. (1%)



hold time for falling D = 0ps(量測的點都是 V=0.9V)

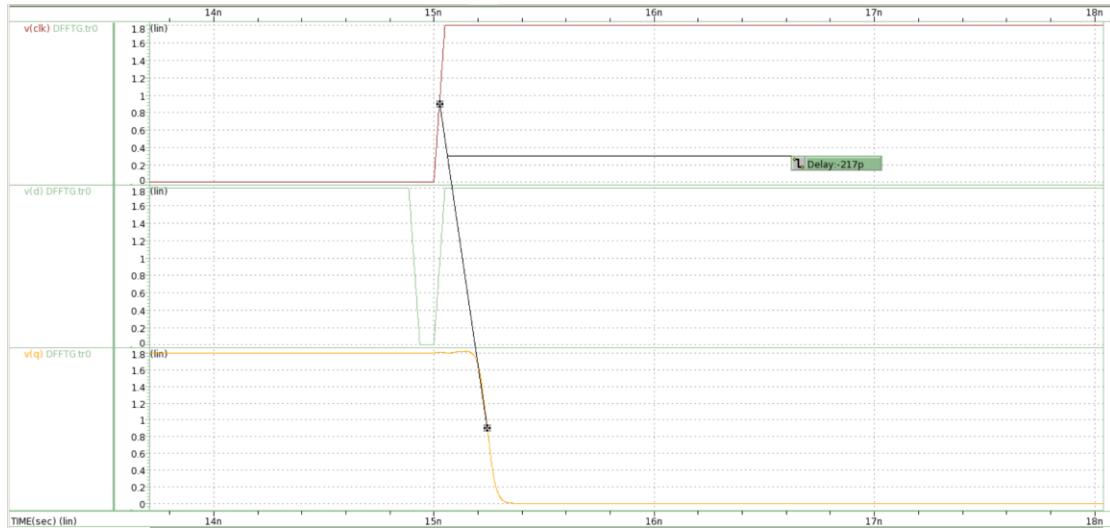
(g). Similar to question 1.(h), with specifications in Table 2., run HSPICE simulation (pre-layout simulation) to find the **CLK-to-Q delay** of TG-based DFF **for 0.18um technology**. The input D signal will be designed by yourself.

(g-1). For rising input, **screenshot** the simulation waveform of “D,” “CLK,” “Q” signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (1%)



CLQ-to-Q delay for rising D = 463ps

(g-2). For falling input, **screenshot** the simulation waveform of “D,” “CLK,” “Q” signals of the DFF. **Mark** the CLK-to-Q delay on the waveform. (1%)



CLQ-to-Q delay for falling D = 185ps

(h). Use the results above to **build a performance table** to summarize the setup time, hold time, and CLK-to-Q delay performance for TG-based DFFs (for both rising input and falling input). We will use this performance table later in Q3. (1%)

	TG-based DFF	
Input D	Rising	Falling
Setup time	95ps	114ps
Hold time	39ps	0ps
CLQ-to-Q delay	463ps	217ps

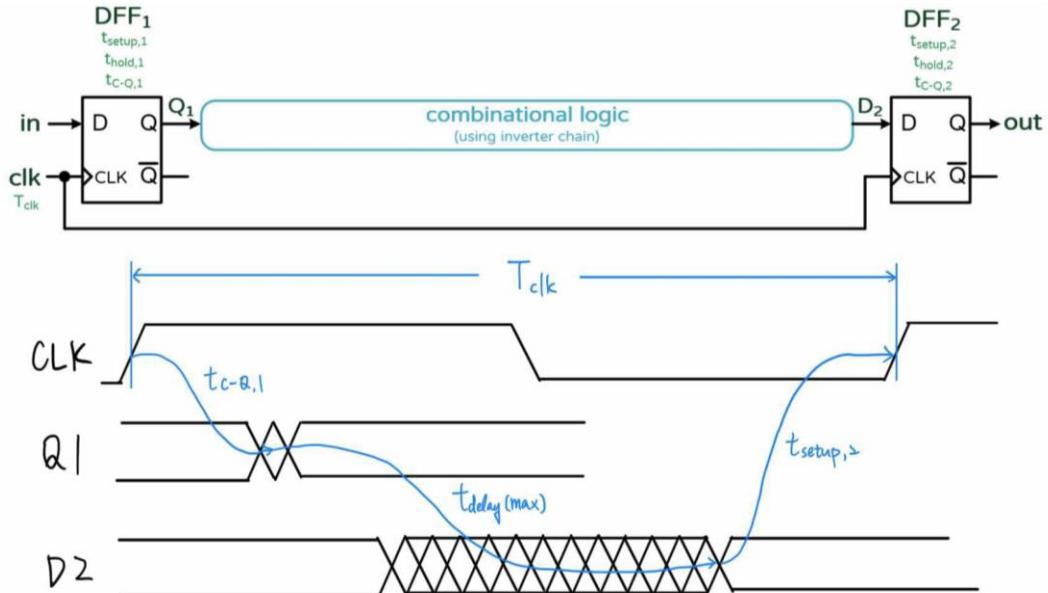
3. (40%) In this question, we are going to find out the minimum and maximum allowable delay between two DFFs. This concept is called “**minimum/maximum delay failure condition**” and is very important in digital circuit design, especially for determining clock period when doing RTL synthesis.
- (a). Insert some combinational logic between two DFFs to introduce delay, forming a sequential logic, as shown in Fig. 4.



Fig. 4. Sequential logic consisting of combinational logic and DFFs

- (a-1). What are the **timing requirements for the propagation delay,  $t_{delay}$ , of the combinational logic** in order to ensure proper functionality? Please express in terms of  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ , and  $T_{clk}$  (the period of clk). It's better to draw some waveforms to help.  
(Hint: There should be one upper bound and one lower bound for  $t_{delay}$ .)  
(Hint: Figures in lecture note page 6-31 may give you some idea about how to draw a helpful waveform.) (2%)

直接畫出 waveform 並在上面標示出  $t_{delay}$  的上下限制何在，以確保不會發生 setup time 或 hold time violation，如下面兩張圖：

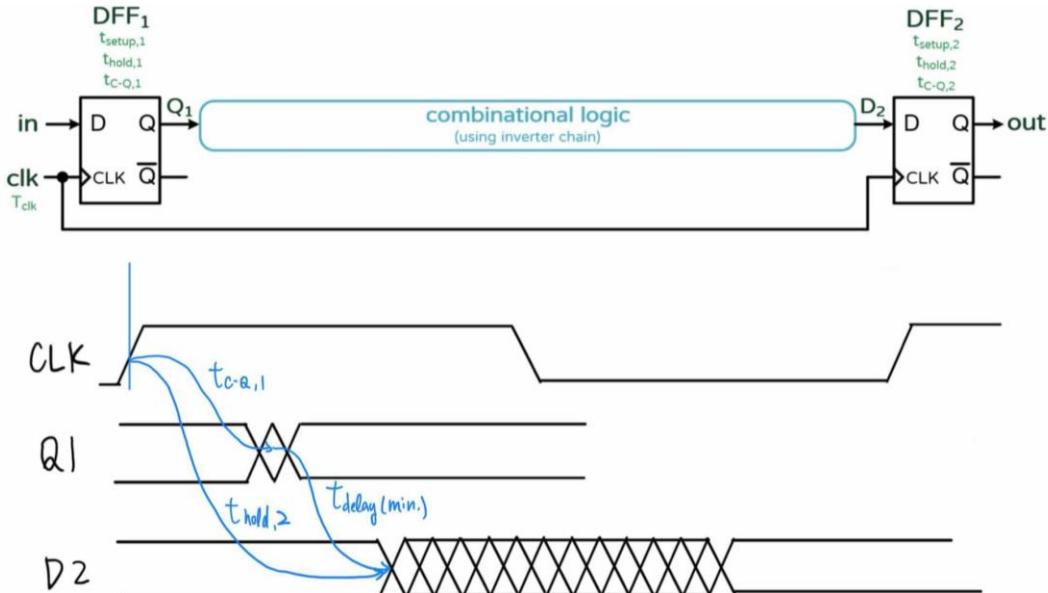


由上圖可知關係式如下：

$$T_{clk} = t_{C-Q,1} + t_{delay(max)} + t_{setup,2}$$

移項後可得

$$t_{delay(max)} = T_{clk} - (t_{C-Q,1} + t_{setup,2})$$



由上圖可知關係式如下：

$$t_{hold,2} = t_{C-Q,1} + t_{delay(min)}$$

移項後可得

$$t_{delay(min)} = t_{hold,2} - t_{C-Q,1}$$

由此得到  $t_{delay}$  的上下限如下：

$$t_{hold,2} - t_{C-Q,1} \leq t_{delay} \leq T_{clk} - (t_{C-Q,1} + t_{setup,2})$$

- (a-2). Which one does the **maximum** allowable delay of the combinational logic depend on, “setup time” or “hold time”? What if the propagation delay exceeded this maximum, what would happen? You can answer by following this format: (1%)

From my answer to (a-1), the maximum allowable delay of the combinational logic is  $T_{clk} - (t_{C-Q,1} + t_{setup,2})$ , which depends on **setup time** of **DFF<sub>2</sub>**. If the propagation delay exceeded this maximum, it would have **setup time violation** at **DFF<sub>2</sub>**, resulting in incorrect value at **out**.

- (a-3). Which one does the **minimum** allowable delay of the combinational logic depend on, “setup time” or “hold time”? What if the propagation delay smaller than this minimum, what would happen? You can answer by following this format: (1%)

From my answer to (a-1), the minimum allowable delay of the combinational logic is  $t_{hold,2} - t_{C-Q,1}$ , which depends on **hold time** of **DFF<sub>2</sub>**. If the propagation delay smaller than this minimum, it would have **hold time violation** at **DFF<sub>2</sub>**, resulting in incorrect value at **out**.

### Using NAND-based DFFs

Here we use an inverter chain (acting as combinational logic) to introduce delay. In the inverter chain, use the same size (shown in Table 3) for each stage. The number of stages in the inverter chain will be designed by yourself.

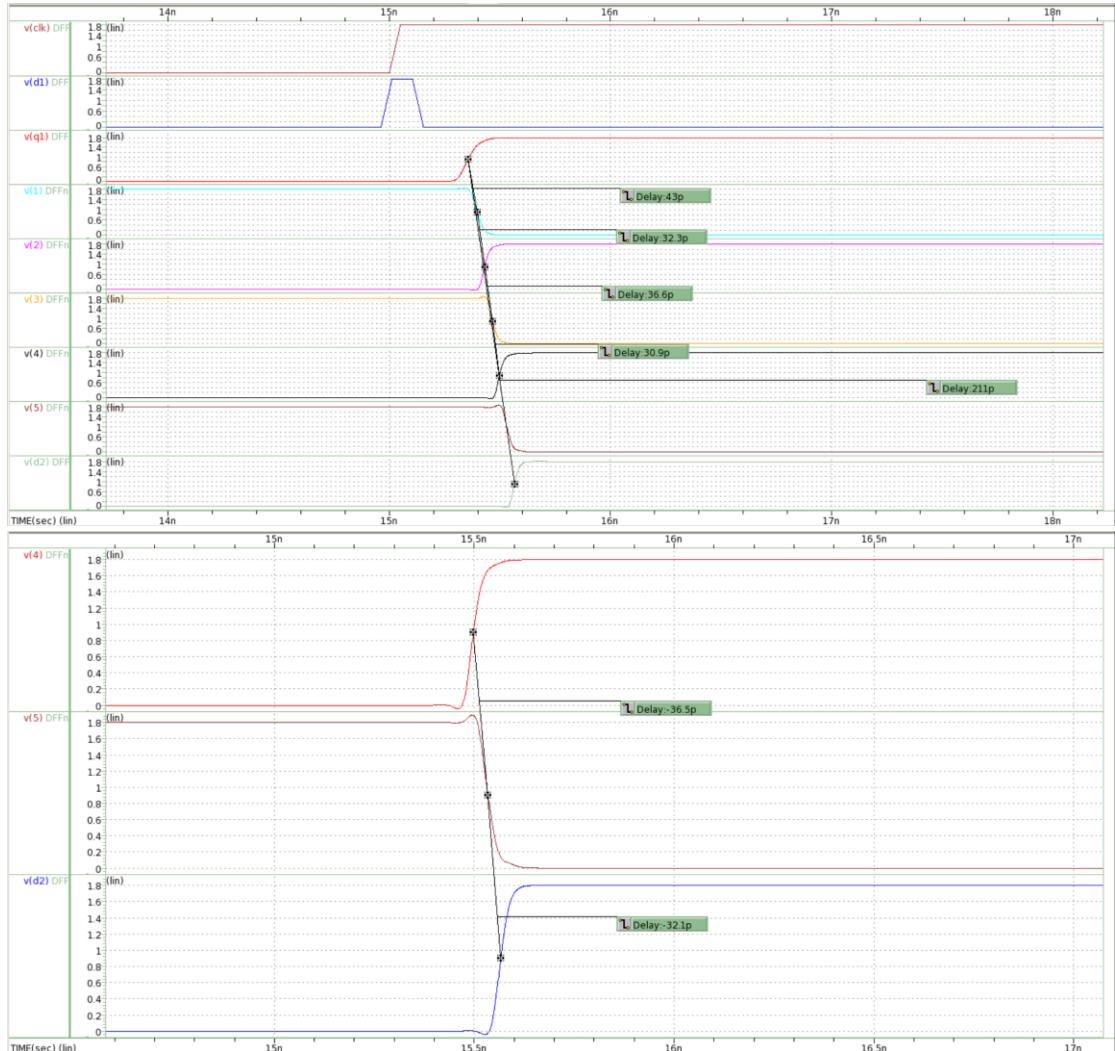
<b>Process</b>	0.18um technology
<b>CLK</b>	100MHz with $t_r=t_f=50\text{ps}$ , duty cycle=50%
<b>V<sub>DD</sub></b>	1.8V
<b>inverter size (in inverter chain)</b>	$\left(\frac{w}{L}\right)_n = \frac{0.5\mu m}{0.18\mu m}; \left(\frac{w}{L}\right)_p = \frac{1.85\mu m}{0.18\mu m}; m=1$

Table 3. Specification for Q3.

### (b). Simulation & hand-calculation of maximum delay failure condition

- (b-1). **Describe** in detail how to design/determine the number of stages in the inverter chain to get the maximum delay failure condition (maximum allowable delay of the combinational logic). (1.5%)

首先需要知道每串聯一個 inverter 平均會造成多少 delay，先在兩個 DFF 連接 6 個 inverter，並用 waveform 量測 delay，將第一個 inverter 的輸出節點設做'1'，第二個 inverter 的輸出節點設做'2'，依此類推，而 D2 會是第六個 inverter 的輸出，如下圖所示(整個過程都是使用 D1 為恰好符合 setup&hold time 的情形)：



Note: 211ps 為 Q1 到 D2 的 delay，也就是六個 inverter 的 delay

第一個 inverter 的 delay = 43ps

第二個 inverter 的 delay = 32.3ps

第三個 inverter 的 delay = 36.6ps

第四個 inverter 的 delay = 30.9ps

第五個 inverter 的 delay = 36.5ps

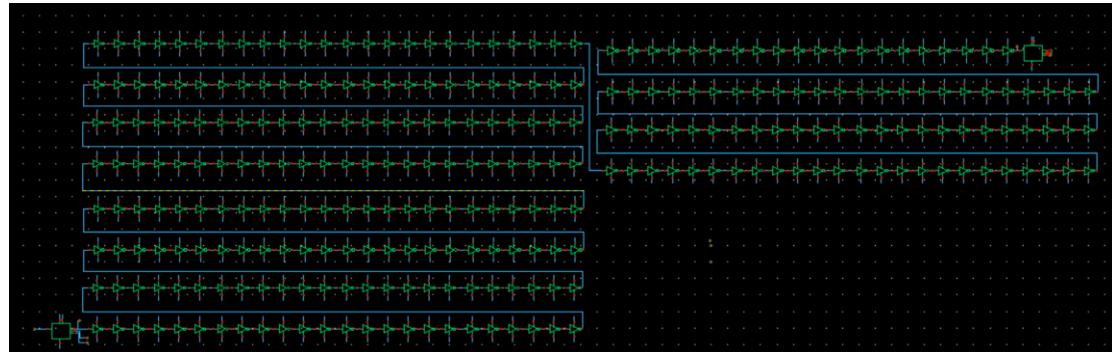
第六個 inverter 的 delay = 32.1ps

可以發現除了第一個 inverter 的 delay 略大一點，其餘的五顆 inverter 的 delay 大小都差不多，因此將後五顆的 delay 取平均等於 33.68ps，作為接下來的 inverter chain 之平均每串聯一個 inverter 的 delay。Maximum delay 的理論(手算)值會是  $T_{clk} - (t_{c-Q,1} + t_{setup,2}) = 10ns - 318ps - 73ps = 9609ps$ (假設 D1 是

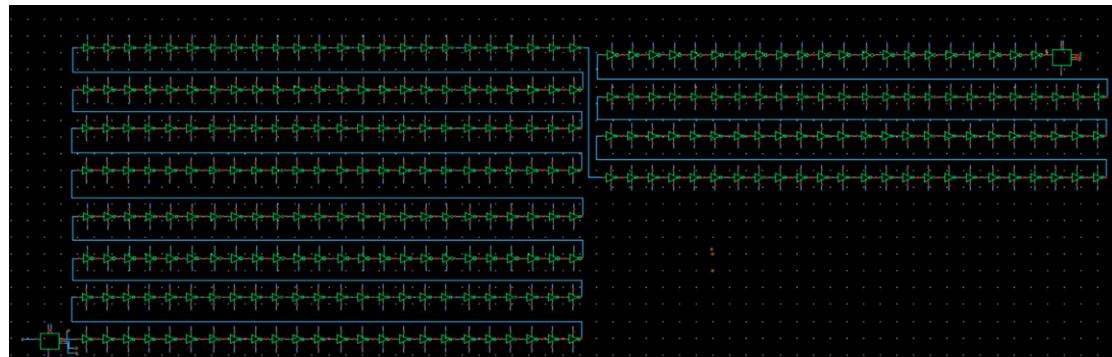
rising input，中間串聯奇數個，使 D2 是 falling 時的情況，數據使用 1.(j-3)的表格)，因此預測總級數會落在 $1 + \frac{9609-43}{33.68} \cong 285.03$ 上下，再以此為基礎調整至 Q2 恰好 fail 時，就能知道最高能放幾級 inverter 在 DFF 之間了。

- (b-2). Use your **NAND-based DFF** in Q1 and the above-mentioned inverter size to build up the schematic of “DFF + inverter chain” using Composer. **Screenshot** this schematic. (The inverter chain might be long. One screenshot for hundreds of inverters is OK.) (0.5%)

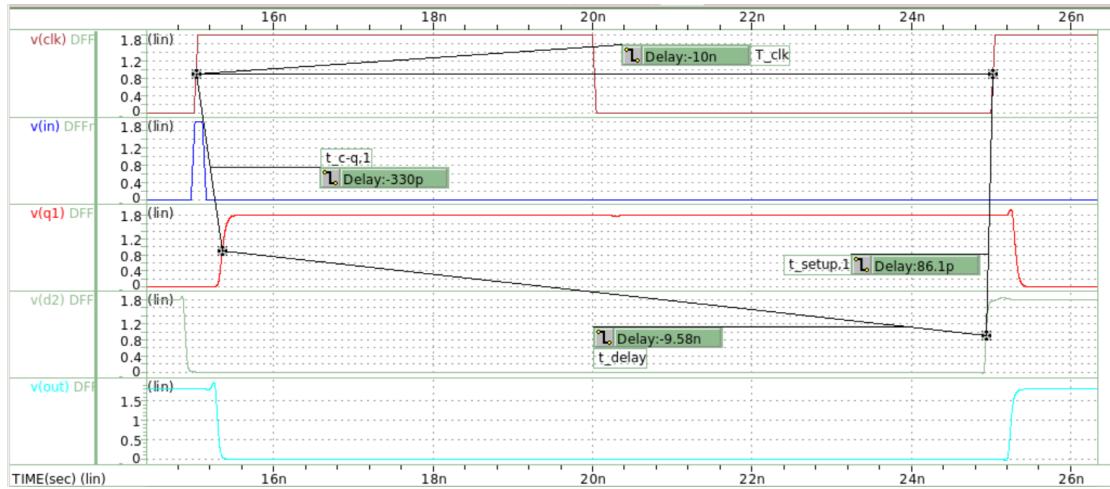
Schematic of two DFF and maximum stages (284) of inverter chain for rising input:



Schematic of two DFF and maximum stages (285) of inverter chain for falling input:



- (b-3). For rising input (**in**), for **maximum allowable number of stages**, **screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{\text{setup},1}$ ,  $t_{\text{hold},1}$ ,  $t_{\text{C-Q},1}$ ,  $t_{\text{setup},2}$ ,  $t_{\text{hold},2}$ ,  $t_{\text{C-Q},2}$ ,  $T_{\text{clk}}$ ,  $t_{\text{delay}}$ ). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (2%)

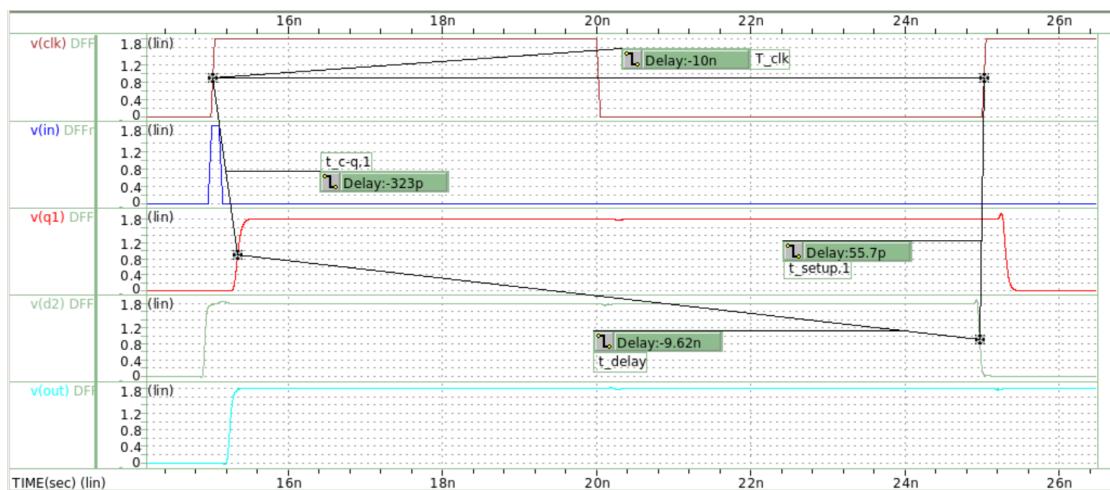


Yes, it meets all timing requirements.  $t_{setup,2}$  (86.1ps) is still longer than the setup time for rising input measured while there's no inverter chain and the second DFF (38ps). Additionally, CLQ-to-Q delay, 1 (330ps) is slightly larger than the CLQ-to-Q delay measured while there's no inverter chain and the second DFF (318ps), since there is loading capacitor at Q1 now.

- (b-4). How many inverter stages **at most** can exist in the inverter chain while keeping normal functionality? What is the maximum allowable delay? (Measure it from the waveform in (b-3).) (1%)

最多可以有 284 個 inverter 在 DFF 之間，從上一小題量到的  $t_{delay,max} = 9.58ns$

- (b-5). Add one more stage to the inverter chain, so now we have “**maximum + 1**” **number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{c-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{c-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). **Which** timing requirement of **which** DFF does it violate? (1.5%)

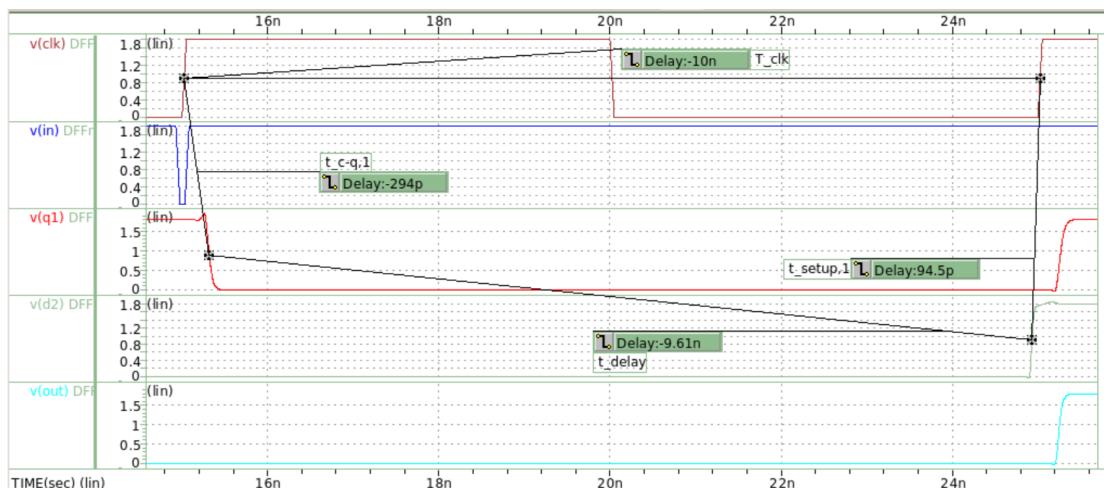


這並不滿足第二個 DFF 的 setup time requirement，因為  $t_{setup,2}$  (55.7ps) 已經小於 setup time for falling input (73ps) 了。

(b-6). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate maximum delay failure condition (maximum allowable delay of the combinational logic) by hand-calculation. Compare it with  $t_{delay}$  by simulation in (b-3), and calculate the mismatch rate ( $\left| \frac{\text{simulation-hand}}{\text{hand}} - 1 \right| \times 100\% \right)$ . If the mismatch rate exceeds 5%, then please comment on the reason. (2%)

根據(a-1)， $t_{delay,max} = T_{clk} - (t_{C-Q,1} + t_{setup,2})$ ， $t_{C-Q,1}$ 代入的是 318ps 對應到的是 1. (j-3) 的表格 pre-sim rising input 的 clock-to-Q delay，而  $t_{setup,2}$  可能是要代入 pre-sim rising 或是 falling input 的 setup time，取決於最終有幾級 inverter，因為模擬結果出來  $t_{delay,max}$  發生時的級數是 284，因此 D2 會是 rising 的，要代入的是 38ps。算得  $t_{delay,max}(\text{hand}) = 9644ps$ ，與 simulation (9.58ns) 的 mismatch rate 大約為 0.66%。

(b-7). For falling input, for maximum allowable number of stages, screenshot the simulation waveform of “clk,” “in,” “Q<sub>1</sub>,” “D<sub>2</sub>,” “out” signals. Mark all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (2%)

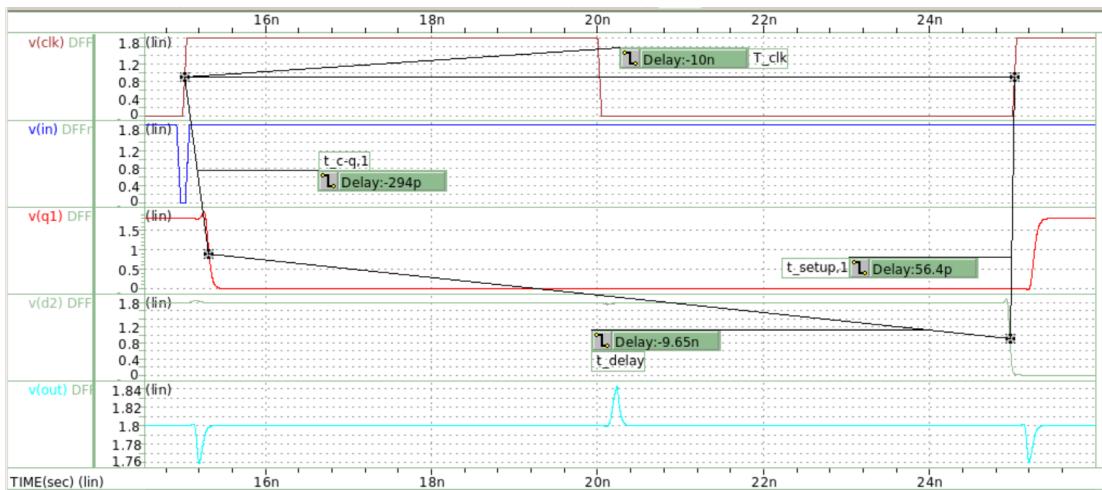


跟 1.(j-3) 的表格(只有一個 DFF 的時候)比較可以發現，這裡的 CLQ-to-Q delay,1 (294ps)稍微大於 pre-sim falling input 的 CLQ-to-Q delay (283ps)，其原因可能是因為在 Q1 多了附載電容，使得 delay 變大，而  $t_{setup,2}$  (94.5ps)仍然大於 pre-sim rising input 的 setup time (38ps)。沒有不符合任何 time requirement。

(b-8). How many inverter stages at most can exist in the inverter chain while keeping normal functionality? What is the maximum allowable delay? (Measure it from the waveform in (b-7).) (1%)

最多可以有 285 個 inverter 在 DFF 之間，從上一小題量到的  $t_{delay,max} = 9.61ns$ 。

(b-9). Add one more stage to the inverter chain, so now we have “**maximum + 1**” **number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{\text{setup},1}$ ,  $t_{\text{hold},1}$ ,  $t_{C-Q,1}$ ,  $t_{\text{setup},2}$ ,  $t_{\text{hold},2}$ ,  $t_{C-Q,2}$ ,  $T_{\text{clk}}$ ,  $t_{\text{delay}}$ ). **Which** timing requirement of **which** DFF does it violate? (1.5%)



這並不滿足第二個 DFF 的 setup time requirement，因為  $t_{\text{setup},2}$  (56.4ps) 已經小於 setup time for falling input (73ps) 了。

(b-10). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate maximum delay failure condition (maximum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with  $t_{\text{delay}}$  by simulation in (b-7), and calculate the **mismatch rate** ( $| \frac{\text{simulation-hand}}{\text{hand}} | \times 100\%$ ). If the mismatch rate exceeds 5%, then please comment on the reason. (2%)

根據(a-1)， $t_{\text{delay},\text{max}} = T_{\text{clk}} - (t_{C-Q,1} + t_{\text{setup},2})$ ， $t_{C-Q,1}$ 代入的是 283ps 對應到的是 1.(j-3)的表格 pre-sim falling input 的 clock-to-Q delay，而  $t_{\text{setup},2}$  可能是要代入 pre-sim rising 或是 falling input 的 setup time，取決於最終有幾級 inverter，因為模擬結果出來  $t_{\text{delay},\text{max}}$  發生時的級數是 285，因此 D2 會是 rising 的，要代入的是 38ps。算得  $t_{\text{delay},\text{max}}(\text{hand}) = 9679\text{ps}$ ，與 simulation (9.61ns)的 mismatch rate 大約為 0.71%。

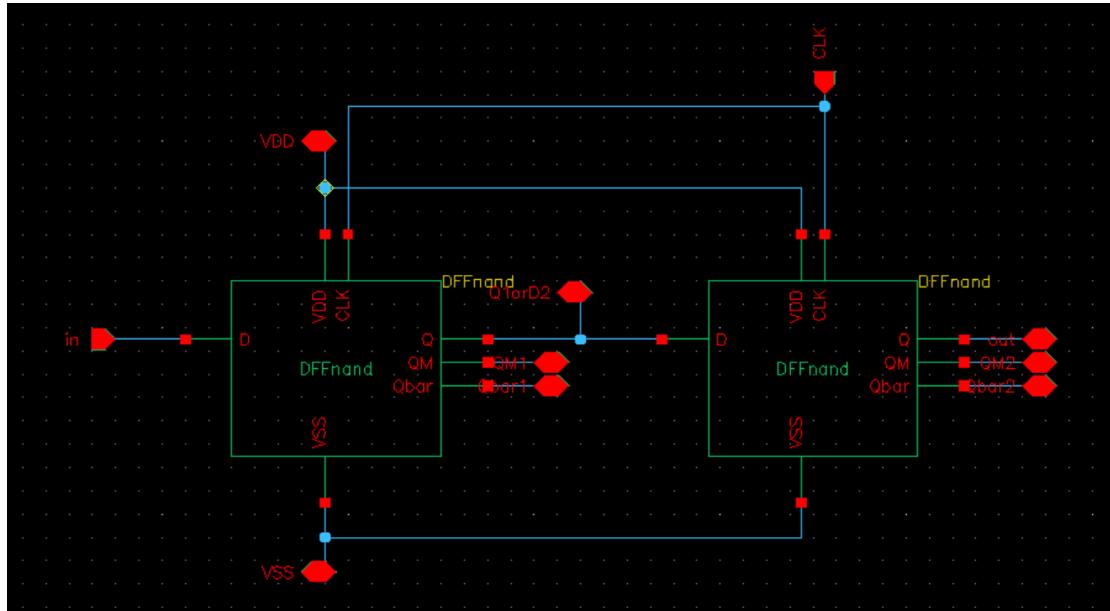
### (c). **Simulation & hand-calculation of minimum delay failure condition**

(c-1). **Describe** in detail how to design/determine the number of stages in the inverter chain to get the minimum delay failure condition (minimum allowable delay of the combinational logic). (1.5%)

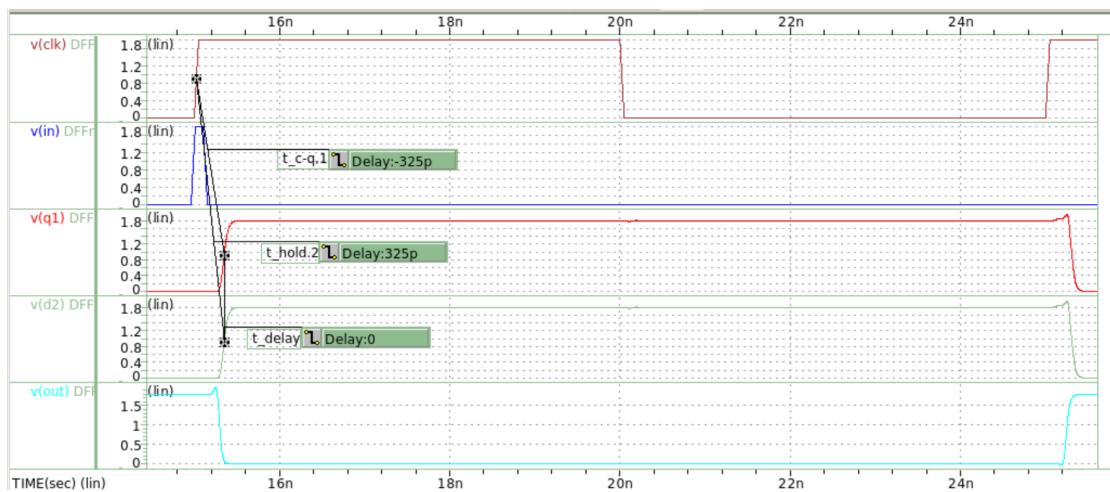
Minimum delay 的理論(手算)值會是  $t_{\text{hold},2} - t_{C-Q,1} = 105\text{ps} - 318\text{ps} = -213\text{ps}$ (假設 D1 是 rising input，中間串聯偶數個，使 D2 也是 rising 時的情況，數據使用 1.(j-3)的表格)，因此預測就算沒有 inverter 也不會有 time requirement violation，因此設定沒有 inverter 在 DFF 之間，若 0 級時卻 fail 了，

在往上一級一級加上去看 Q2 甚麼時候會有正確的輸出 D2 的訊號，此時即為 minimum allowable delay 對應的 inverter 級數。整個模擬過程的 in 也是如(b)，設成剛好滿足 setup time 和 hold time。

- (c-2). Use your **NAND-based DFF** in Q1 and inverter size in Table 3 to build up the schematic of “DFF + inverter chain” using Composer. **Screenshot** this schematic. (0.5%)



- (c-3). For rising input (**in**), for **minimum allowable number of stages**, **screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (1%)



跟 1.(j-3)的表格(只有一個 DFF 的時候)比較可以發現，這裡的 CLQ-to-Q delay (325ps)稍微大於 pre-sim rising input 的 CLQ-to-Q delay (318ps)，可能是因為多了附載電容，使得 delay 變大，而  $t_{hold,2}$  (325ps)仍然大於 pre-sim rising input 的 hold time (105ps)。沒有不符合任何 time requirement。

- (c-4). What is the **smallest** number of inverter stages that can exist in the inverter chain while keeping normal functionality? What is the minimum allowable delay? (Measure it from the waveform in (c-3).) (1%)

由上題的模擬結果可知，最少的 inverter chain 級數是 0，仍然可以具有正常運作的功能，因此如上圖所示， $t_{delay,min} = 0ps$ 。

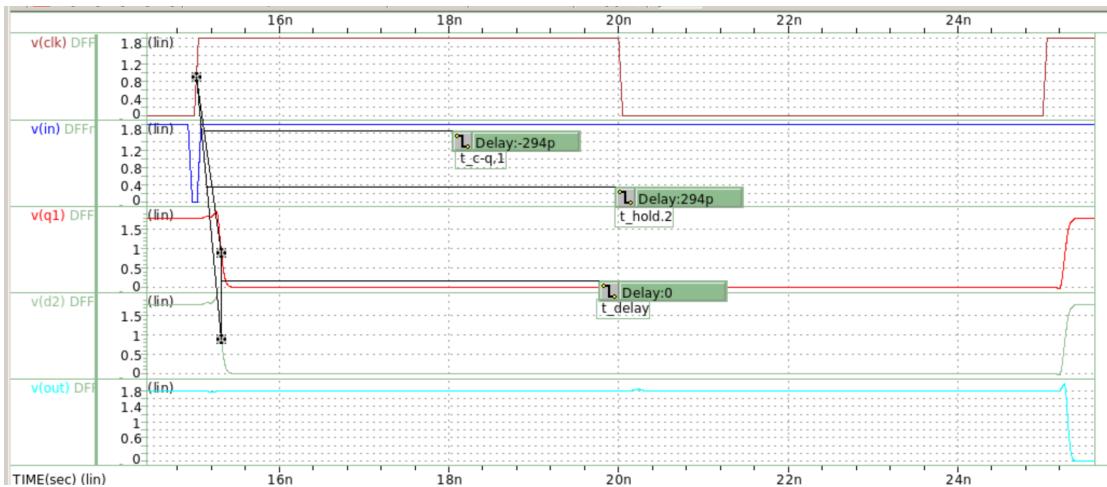
- (c-5). Remove one stage from the inverter chain, so now we have “**minimum - 1**” **number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). **Which** timing requirement of **which** DFF does it violate? (1%)

最小所需延遲為 0s，表示電路不用接任何 inverter 就能運作，不會有 fail 的情形發生。

- (c-6). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate minimum delay failure condition (minimum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with  $t_{delay}$  by simulation in (c-3), and calculate the **mismatch rate** ( $\left| \frac{simulation-hand}{hand} \right| \times 100\%$ ). If the mismatch rate exceeds 5%, then please comment on the reason. (1%)

根據(a-1)， $t_{delay,min} = t_{hold,2} - t_{C-Q,1}$ ， $t_{C-Q,1}$ 代入的是 318ps 對應到的是 1. (j-3) 的表格 pre-sim rising input 的 clock-to-Q delay，而  $t_{hold,2}$  則因為 D2 在不接 inverter 時也會是 rising 的，要代入的是 105ps。算得  $t_{delay,min} (hand) = -213ps$ ，與 simulation 的 mismatch rate 大約為 100%，為甚麼 mismatch rate 這麼高是因為手算的結果為負值，代表說  $t_{delay}$  的下限在負值，但  $t_{delay}$  做為一個 inverter chain 的 delay，其最小值只可能為 0，因此模擬最小值無法觸及到依據理論手算的最小值，所以其實模擬結果和手算結果是可以呼應的。

- (c-7). **For falling input**, for **minimum allowable number of stages**, **screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). Does it meet all the timing requirements? You can answer by comparing the timing on the waveform with the value in the performance table of question 1.(j-3) (pre-sim). (1%)



跟 1.(j-3) 的表格(只有一個 DFF 的時候)比較可以發現，這裡的 CLQ-to-Q delay,1 (294ps)稍微大於 pre-sim falling input 的 CLQ-to-Q delay (283ps)，其原因可能是因為在 Q1 多了附載電容，使得 delay 變大，而  $t_{hold,2}$  (294ps)仍然大於 pre-sim falling input 的 hold time (32ps)。沒有不符合任何 time requirement。

- (c-8). What is the **smallest** number of inverter stages that can exist in the inverter chain while keeping normal functionality? What is the minimum allowable delay? (Measure it from the waveform in (c-7).) (1%)

由上題的模擬結果可知，最少的 inverter chain 級數是 0，仍然可以具有正常運作的功能，因此如上圖所示， $t_{delay,min} = 0ps$ 。

- (c-9). Remove one stage from the inverter chain, so now we have “**minimum - 1**” **number of stages**. Then re-run HSPICE simulation. **Screenshot** the simulation waveform of “**clk**,” “**in**,” “**Q<sub>1</sub>**,” “**D<sub>2</sub>**,” “**out**” signals. **Mark** all the related timing on the waveform (choose what you need from  $t_{setup,1}$ ,  $t_{hold,1}$ ,  $t_{C-Q,1}$ ,  $t_{setup,2}$ ,  $t_{hold,2}$ ,  $t_{C-Q,2}$ ,  $T_{clk}$ ,  $t_{delay}$ ). **Which** timing requirement of **which** DFF does it violate? (1%)

最小所需延遲為 0s，表示電路不用接任何 inverter 就能運作，不會有 fail 的情形發生。

- (c-10). Use data from the performance table in question 1.(j-3) (pre-sim) to calculate minimum delay failure condition (minimum allowable delay of the combinational logic) **by hand-calculation**. **Compare** it with  $t_{delay}$  by simulation in (c-7), and calculate the **mismatch rate** ( $|\frac{simulation-hand}{hand}| \times 100\%$ ). If the mismatch rate exceeds 5%, then please comment on the reason. (1%)

根據(a-1)， $t_{delay,min} = t_{hold,2} - t_{C-Q,1}$ ， $t_{C-Q,1}$ 代入的是 283ps 對應到的是 1. (j-3) 的表格 pre-sim falling input 的 clock-to-Q delay，而  $t_{hold,2}$  則因為 D2 在不接 inverter 時也會是 falling 的，要代入的是 32ps。算得  $t_{delay,min} (hand) = -251ps$ ，與 simulation 的 mismatch rate 大約為 100%，為什麼 mismatch rate 這麼高是因為手算的結果為負值，代表說  $t_{delay}$  的下限在負值，但  $t_{delay}$  做為一個

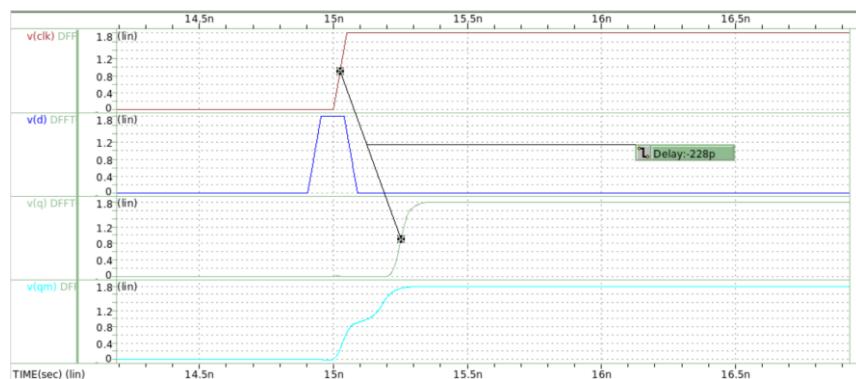
inverter chain 的 delay，其最小值只可能為 0，因此模擬最小值無法觸及到依據理論手算的最小值，所以其實模擬結果和手算結果是可以呼應的。

- (d). From the above simulation and hand-calculation, finish Table 4. (Don't forget to write down units.)  
(1%)

NAND-based	Max. Propagation Delay		Min. Propagation Delay	
	simulation	Hand-calculation	simulation	Hand-calculation
Rising input	9.58ns	9.644ns	0ps	-213ps
Falling input	9.61ns	9.679ns	0ps	-251ps

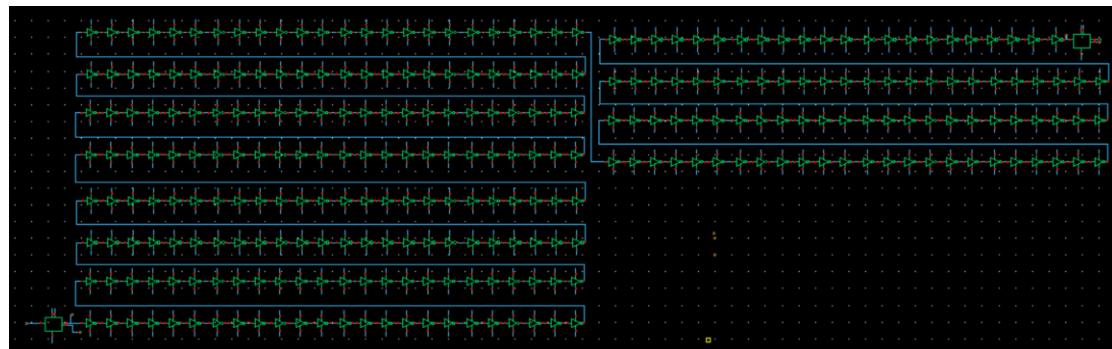
- (e). Repeat question (b-2)~(b-10) but use **TG-based DFF** in Q2 instead. [Please title as (e-2)~(e-10).]  
(For question (b-6) and (b-10), use data from the performance table in question 2.(h) instead.)  
(4.5%)

**特別注意：**在第 2 題所測得的 TG-based DFF 的 setup time 與 hold time for rising input 在這裡的串聯 200 多顆以上的 inverter 時的 case 以及直接連接下一個 DFF 時的 case 都會 fail，應該是因為這個 case 的 setup time 和 hold time 都微微的提升了一點點，所以將 setup time 與 hold time for rising input 都加 1ps (根據 2(h)的表格，setup time = (95+1)ps，hold time = (39+1)ps)，電路即可正常運作，所以這裡我讓電路的 rising input 恰滿足這組新的 setup time 與 hold time，去找到 rising input 的 max.與 min. allowable delay。也因此可以發現(e-3, e-5, f-3)中  $t_{CLK-to-Q}$  明顯比 2.(h)表中的更小許多，但若用這一題 input 所採用的值(各加 1ps)，測出來的  $t_{CLK-to-Q} = 228ps$  (如下圖所示)，則(e-3, e-5, f-3)中  $t_{CLK-to-Q}$  略大於為加附載時的  $t_{CLK-to-Q}$ ，都是合理的值。至於 falling input 沒有相關的問題，所以令 input 恰滿足 2.(h)所測得的 setup time 和 hold time 即可。

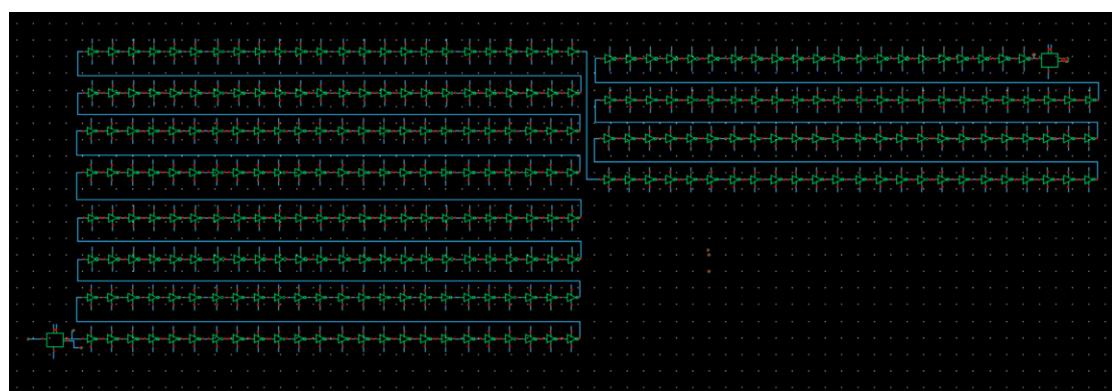


(e-2)

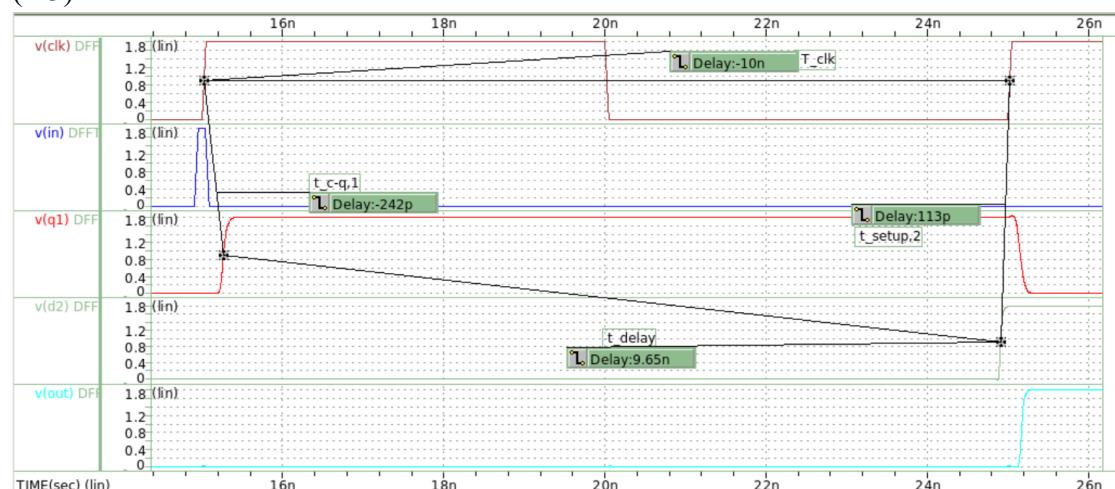
Schematic of two DFF and maximum stages (286) of inverter chain for rising input:



Schematic of two DFF and maximum stages (285) of inverter chain for falling input:



(e-3)

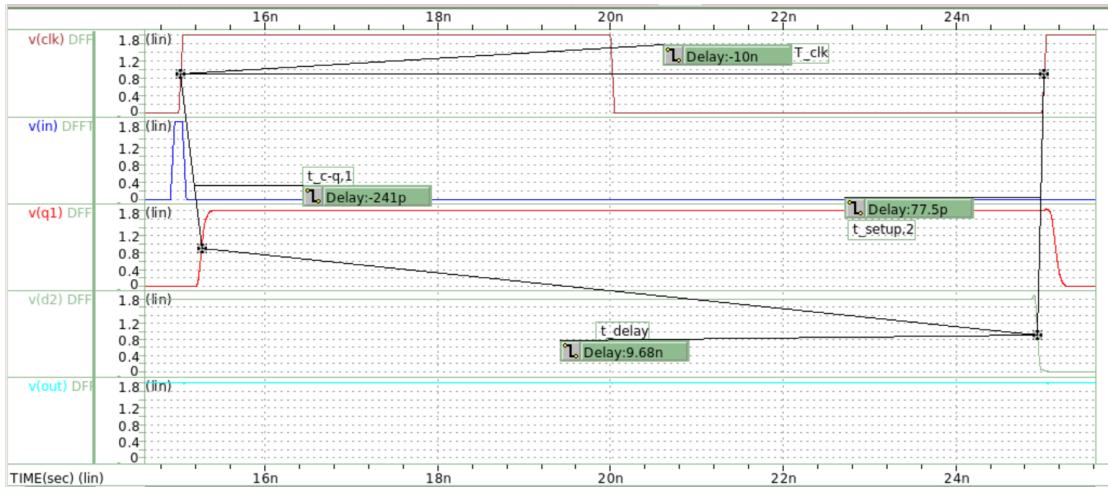


Yes, it meets all timing requirements.  $t_{setup,2}$  (113ps) is still longer than the setup time for rising input measured while there's no inverter chain and the second DFF (95ps).

(e-4)

最多可以有 286 個 inverter 在 DFF 之間，從上一小題量到的  $t_{delay,max} = 9.65ns$

(e-5)

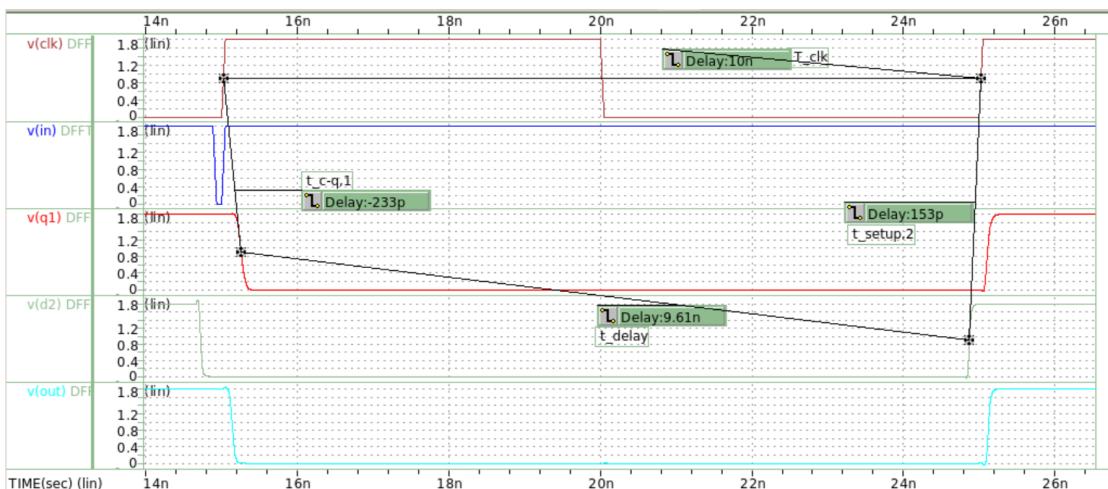


這並不滿足第二個 DFF 的 setup time requirement，因為  $t_{setup,2}$  (77.5ps) 已經小於 setup time for falling input (95ps) 了。

(e-6)

根據(a-1)， $t_{delay,max} = T_{clk} - (t_{c-Q,1} + t_{setup,2})$ ， $t_{c-Q,1}$ 代入的是 463ps 對應到的是 2.(h)的表格 pre-sim rising input 的 clock-to-Q delay，而 $t_{setup,2}$ 可能是要代入 pre-sim rising 或是 falling input 的 setup time，取決於最終有幾級 inverter，因為模擬結果出來 $t_{delay,max}$ 發生時的級數是 286，因此 D2 會是 rising 的，要代入的是 95ps。算得 $t_{delay,max} (hand) = 9442ps$ ，與 simulation (9.65ns)的 mismatch rate 大約為 2.2%。若使用(e-2)前面的”特別注意”中所新量測的對應現在 input 的  $t_{CLK-to-Q} = 228ps$ ，以及因應此題所調整的 $t_{setup} = (95 + 1)ps$ ，則會使  $t_{delay,max} (hand) = 9676ps$ ，mismatch rate 大約為 0.27%。

(e-7)



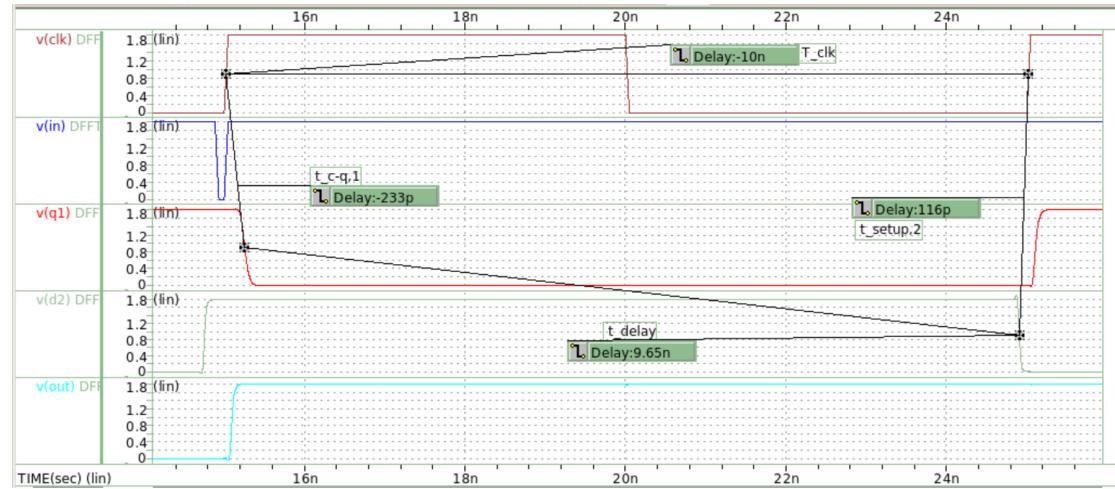
跟 2.(h)的表格(只有一個 DFF 的時候)比較可以發現，這裡的 CLQ-to-Q delay,1

(233ps)稍微大於 pre-sim falling input 的 CLQ-to-Q delay (217ps)，其原因可能是因為在 Q1 多了附載電容，使得 delay 變大，而  $t_{setup,2}$  (152ps)仍然大於 pre-sim rising input 的 setup time (95ps)。沒有不符合任何 time requirement。

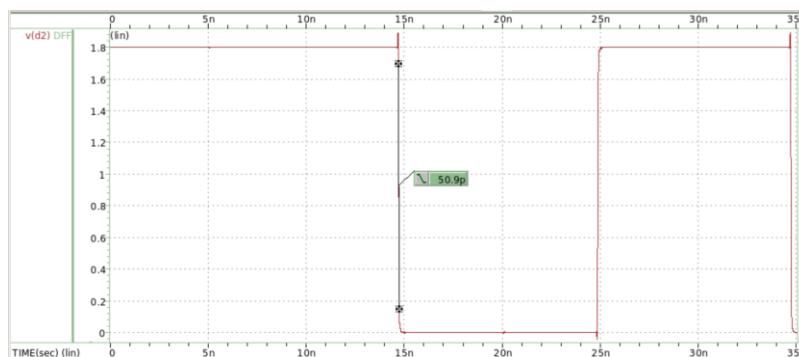
(e-8)

最多可以有 285 個 inverter 在 DFF 之間，從上一小題量到的  $t_{delay,max} = 9.61ns$ 。

(e-9)



這並不滿足第二個 DFF 的 setup time requirement，雖然  $t_{setup,2}$  (116ps)略微大於 2.(h)中的 setup time for falling input (114ps)，但是仍舊沒有能夠使 out 傳出 falling 的訊號，這可能是因為 D2 的 falling 訊號已經不再像第二題模擬時的 input 一樣是 falling time 為 50ps，變得更長了，而且還有 glitch 的發生 (如下圖所示)，這些都導致了第二題所測得的 setup time for falling input 不能如此直接的套用到現在的 case 上，會有一點小誤差是正常的。

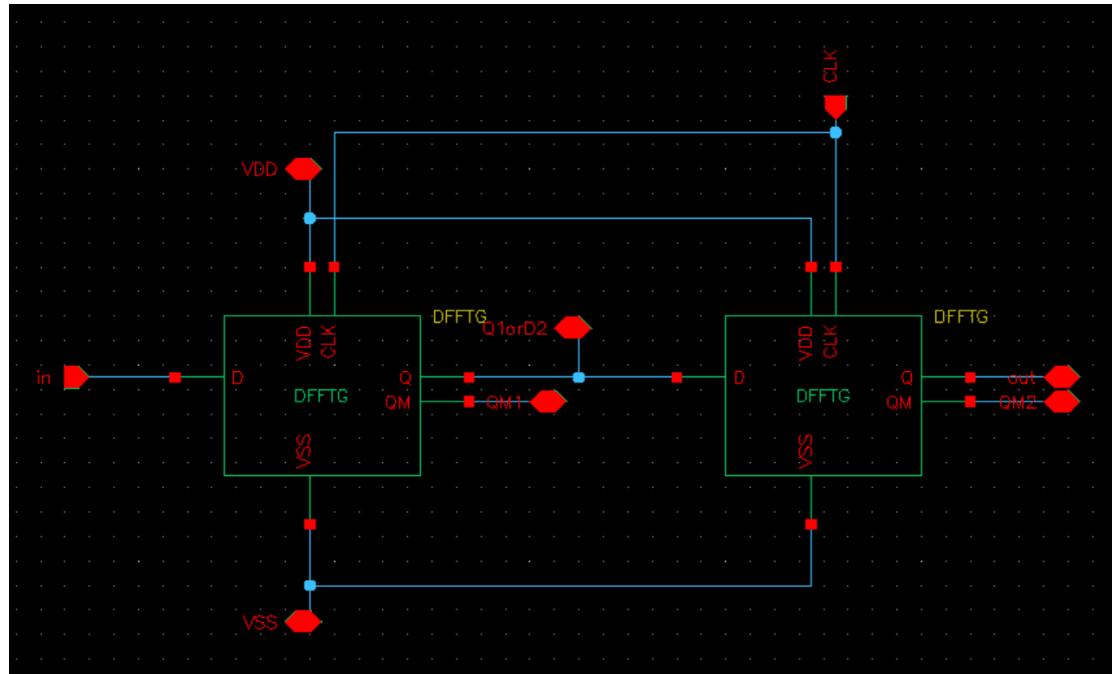


(e-10)

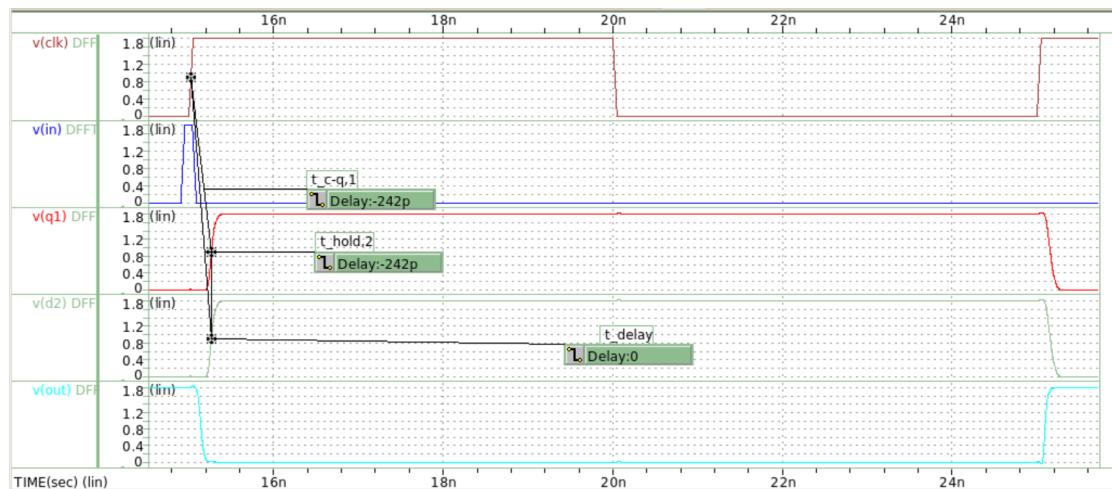
根據(a-1)， $t_{delay,max} = T_{clk} - (t_{c-q,1} + t_{setup,2})$ ， $t_{c-q,1}$ 代入的是 217ps 對應到的是 2.(h)的表格 pre-sim falling input 的 clock-to-Q delay，而  $t_{setup,2}$ 可能是要代入 pre-sim rising 或是 falling input 的 setup time，取決於最終有幾級 inverter，因

為模擬結果出來  $t_{delay,max}$  發生時的級數是 285，因此 D2 會是 rising 的，要代入的是 95ps，算得  $t_{delay,max}(\text{hand}) = 9688\text{ps}$ ，與 simulation (9.61ns) 的 mismatch rate 大約為 0.81%。

(f-2)



(f-3)



$t_{hold,2}$  (242ps) 仍然大於 2.(h) 表格中 rising input 的 hold time (39ps)。沒有不符合任何 time requirement。

(f-4)

由上題的模擬結果可知，最少的 inverter chain 級數是 0，仍然可以具有正常運作的功能，因此如上圖所示， $t_{delay,min} = 0\text{ps}$ 。

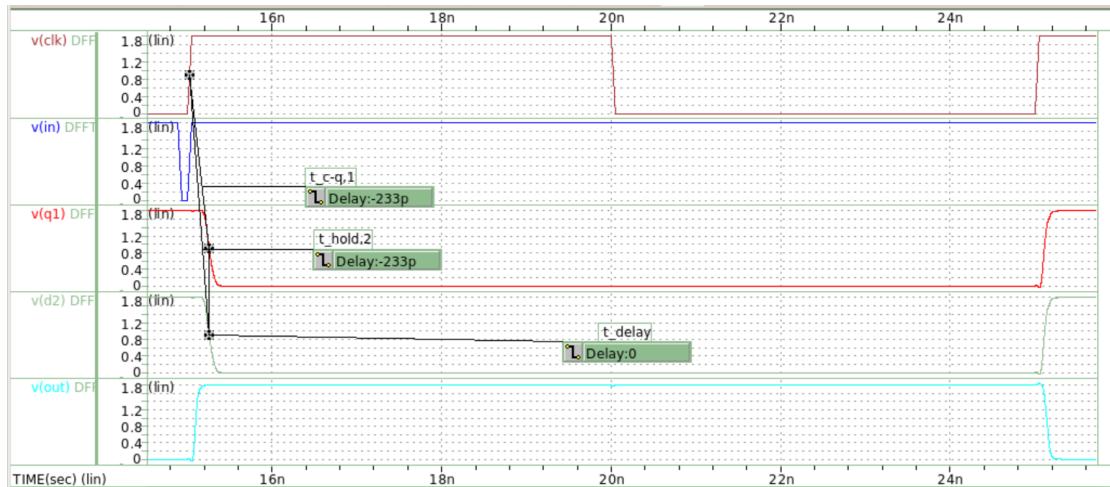
(f-5)

最小所需延遲為 0s，表示電路不用接任何 inverter 就能運作，不會有 fail 的情形發生。

(f-6)

根據(a-1)， $t_{delay,min} = t_{hold,2} - t_{C-Q,1}$ ， $t_{C-Q,1}$ 代入的是 463ps 對應到的是 2.(h) 的表格 pre-sim rising input 的 clock-to-Q delay，而 $t_{hold,2}$ 則因為 D2 在不接 inverter 時也會是 rising 的，要代入的是 39ps。算得 $t_{delay,min} (hand) = -424ps$ ，與 simulation 的 mismatch rate 為 100%，為甚麼 mismatch rate 這麼高是因為手算的結果為負值，代表說 $t_{delay}$ 的下限在負值，但 $t_{delay}$ 做為一個 inverter chain 的 delay，其最小值只可能為 0，因此模擬最小值無法觸及到依據理論手算的最小值，所以其實模擬結果和手算結果是可以呼應的。

(f-7)



跟 2.(h)的表格(只有一個 DFF 的時候)比較可以發現，這裡的 CLQ-to-Q delay,1 (233ps)稍微大於 pre-sim falling input 的 CLQ-to-Q delay (217ps)，其原因可能是因為在 Q1 多了附載電容，使得 delay 變大，而 $t_{hold,2}$  (233ps)仍然大於 pre-sim falling input 的 hold time (0ps)。沒有不符合任何 time requirement。

(f-8)

由上題的模擬結果可知，最少的 inverter chain 級數是 0，仍然可以具有正常運作的功能，因此如上圖所示， $t_{delay,min} = 0ps$ 。

(f-9)

最小所需延遲為 0s，表示電路不用接任何 inverter 就能運作，不會有 fail 的情形發生。

(f-10)

根據(a-1) ,  $t_{delay,min} = t_{hold,2} - t_{C-Q,1}$  ,  $t_{C-Q,1}$ 代入的是 217ps 對應到的是 2.(h) 的表格 pre-sim falling input 的 clock-to-Q delay , 而  $t_{hold,2}$  則因為 D2 在不接 inverter 時也會是 falling 的 , 要代入的是 0ps 。算得  $t_{delay,min} (hand) = -217ps$  , 與 simulation 的 mismatch rate 大約為 100% , 為甚麼 mismatch rate 這麼高是因為手算的結果為負值 , 代表說  $t_{delay}$  的下限在負值 , 但  $t_{delay}$  做為一個 inverter chain 的 delay , 其最小值只可能為 0 , 因此模擬最小值無法觸及到依據理論手算的最小值 , 所以其實模擬結果和手算結果是可以呼應的 。

(g). From the above simulation and hand-calculation, finish Table 5. (Don't forget to write down units.)  
(1%)

TG-based	Max. Propagation Delay		Min. Propagation Delay	
	Simulation	Hand-calculation	Simulation	Hand-calculation
Rising input	9.65ns	9.442ns	0ps	-424ps
Falling input	9.61ns	9.688ns	0ps	-217ps