2024 EE5250 VLSI Design Final Project

Due date: 2024/12/26

組別：37

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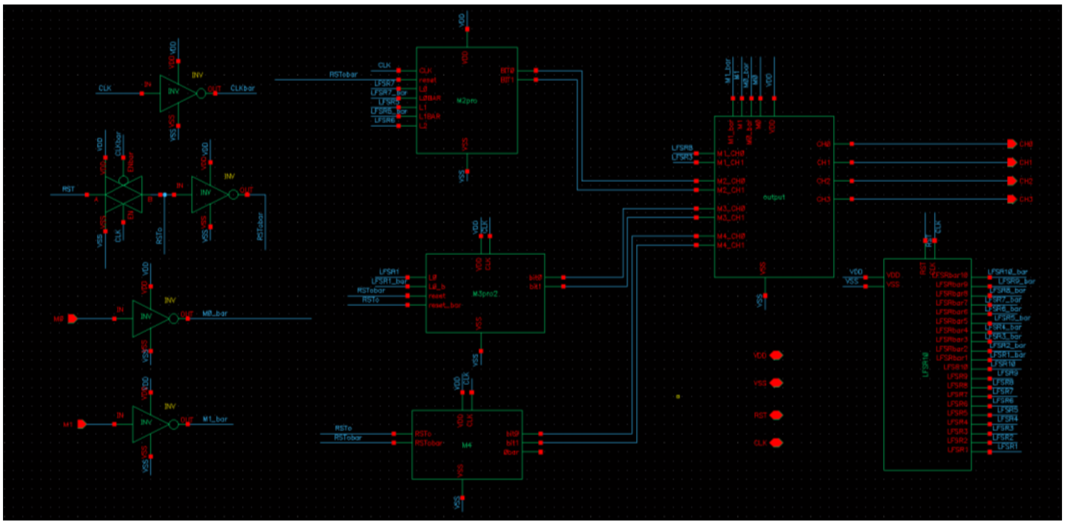
目錄

1. Top-level design

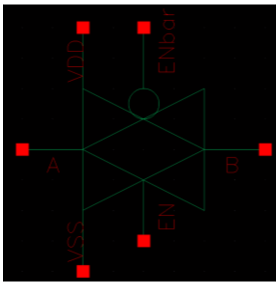
(a) Please draw the block diagram of your top-level circuit, discuss on your design.

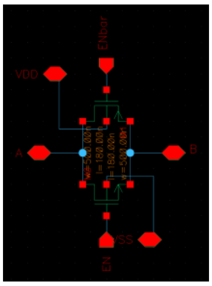


圖(一)、top-level circuit。

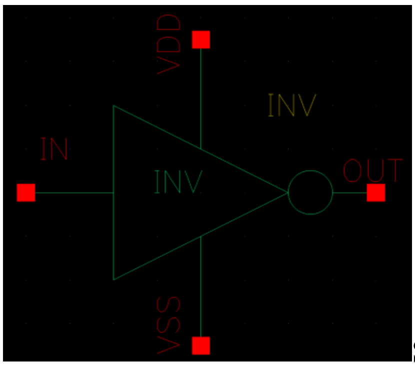
Block diagram 的 block 解釋：

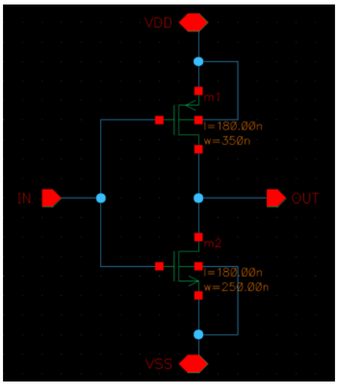
(1) Transmission gate (TG)

Symbol: 

Schematic: 

(2) Inverter (INV)

Symbol: 

Schematic: 

(3) M2pro

其中電路實現 M=2 的邏輯，詳見第 4 題。

(4) M3pro2

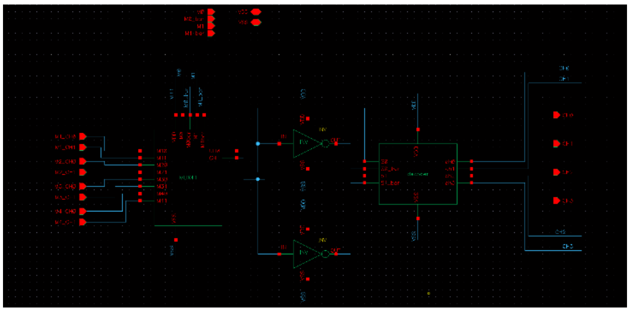
其中電路實現 M=3 的邏輯，詳見第 3 題。

(5) M4

其中電路實現 M=4 的邏輯，詳見第 2 題。

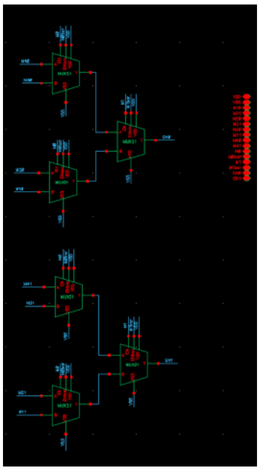
(6) Output

output 內部的 block diagram:

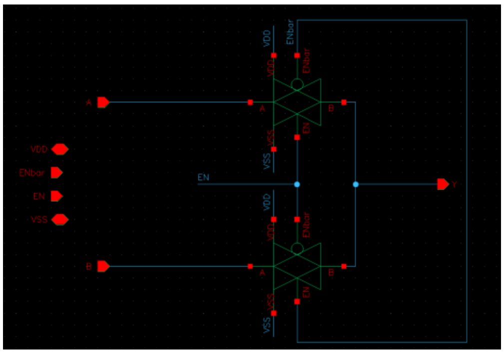


i. MUX41

MUX41 內部的 block diagram:

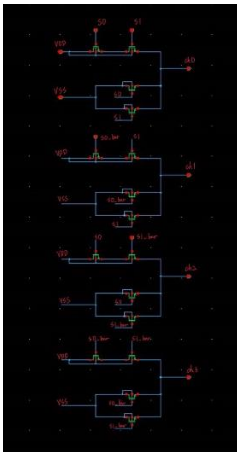


MUX21 內部的 block diagram:



ii. decoder

decoder 內部的電路:



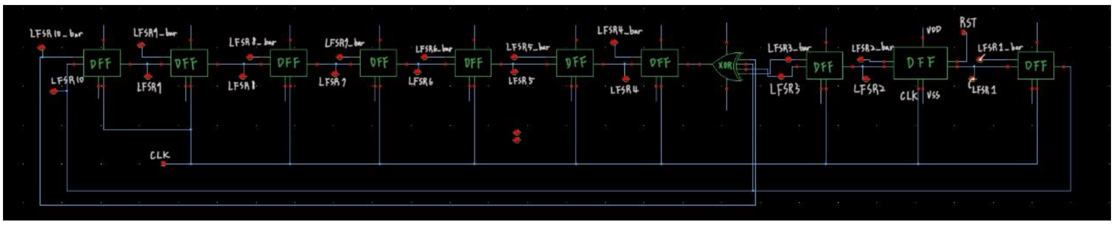
(7) LFSR10

10 bit 的 in-tap LFSR，詳見(b)。

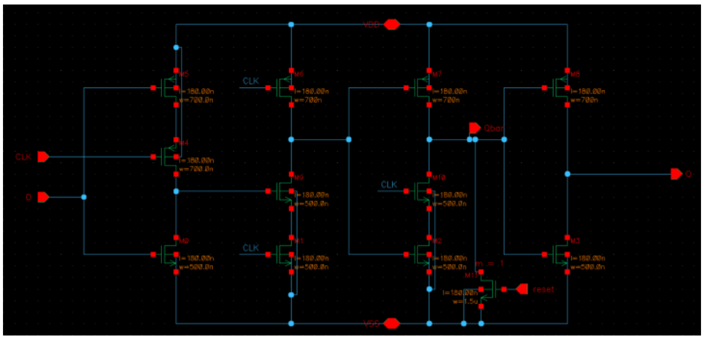
首先，我們使用 10-bit LFSR 作為 M=1, M=2, M=3, M=4(下稱 M1, M2, M3,M4)這四個 case 的輸入參數，並創建 M2 到 M4 三個 submodule 實現 M2 到 M4 的功能(M1 不需要額外電路實現，下面題目會說明)。接著將 M1 到 M4 的結果輸入 output module(如圖(二))，我們使用兩組 4 to 1 的 mux(圖中的 MUX41)，並以 M<1:0>的輸入作為控制訊號，將對應的通道選擇出來，並將輸出訊號通過 2 to 4 的 decoder，轉成我們要的 4-bit ch<3:0>。最後，為了使 DFF 實現同步 reset 功能，我們將輸入 RST 訊號通過 TG，並使用 CLK 做控制訊號，使 RST 在 CLK 為 1 時，才會將 RST 訊號傳給 DFF 並執行 reset 功能。

(b) Please draw the block diagram of your pseudo-random generator (PRG) circuit, which generates the desired probabilities for RIS method implementation, discuss on your design.

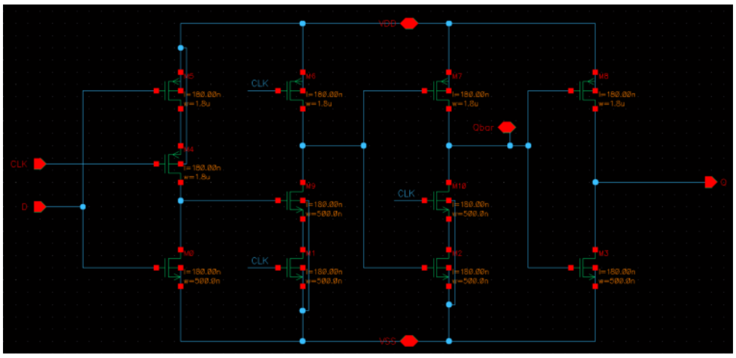
Block diagram:



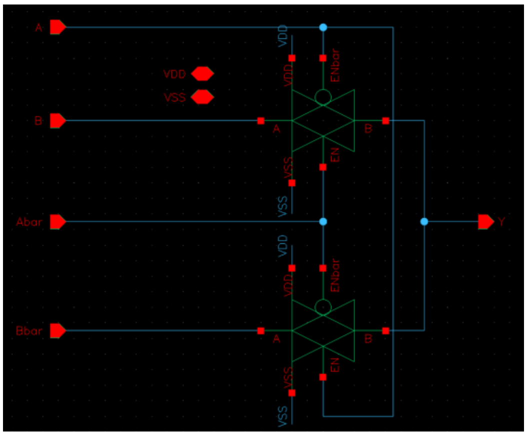
DFF 內部電路(with reset) :



DFF 內部電路(without reset):



XOR 內部電路:



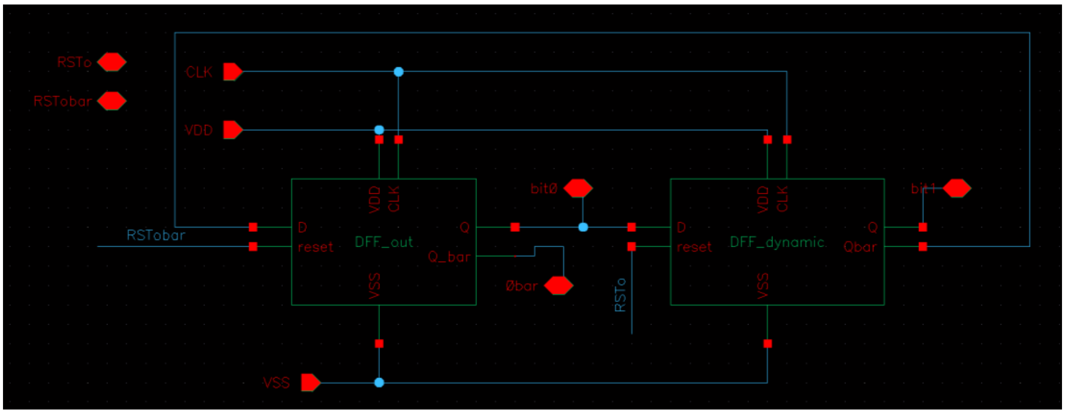
我們採用 in-tap 10-bit LFSR 來實現 PRG，根據 HW4 的經驗，in-tap LFSR 最大頻率比 out-tap 高了不少，在 FoM 側重操作頻率的情況下，比較佔優勢。另外，會使用 10-bit LFSR 而不是更少的位數，是因為測試取樣 1024 個 clock cycle，用更少的 bit 會使 1024 個 clock cycle 中序列出現的重複性增加，10bit LFSR 能使得 M1 的 case 更顯得隨機，PSD 的圖也更符合要求。

(c) Please discuss on how you optimize your design in detail. which block is the speed bottleneck?

M=2 的功能電路會是 speed bottleneck，由題目 M=2 case 的(a)小題中的圖(四)可以發現，M2 的輸出會過兩層的 mux 才會進到 output module，是所有 Mode 功能電路中，路徑最長的，故有最大到達輸出的 delay。

2. M = 4 case

(a) Please draw the block diagram of your logic in this case, discuss on your design.



圖(二)、M4 module。

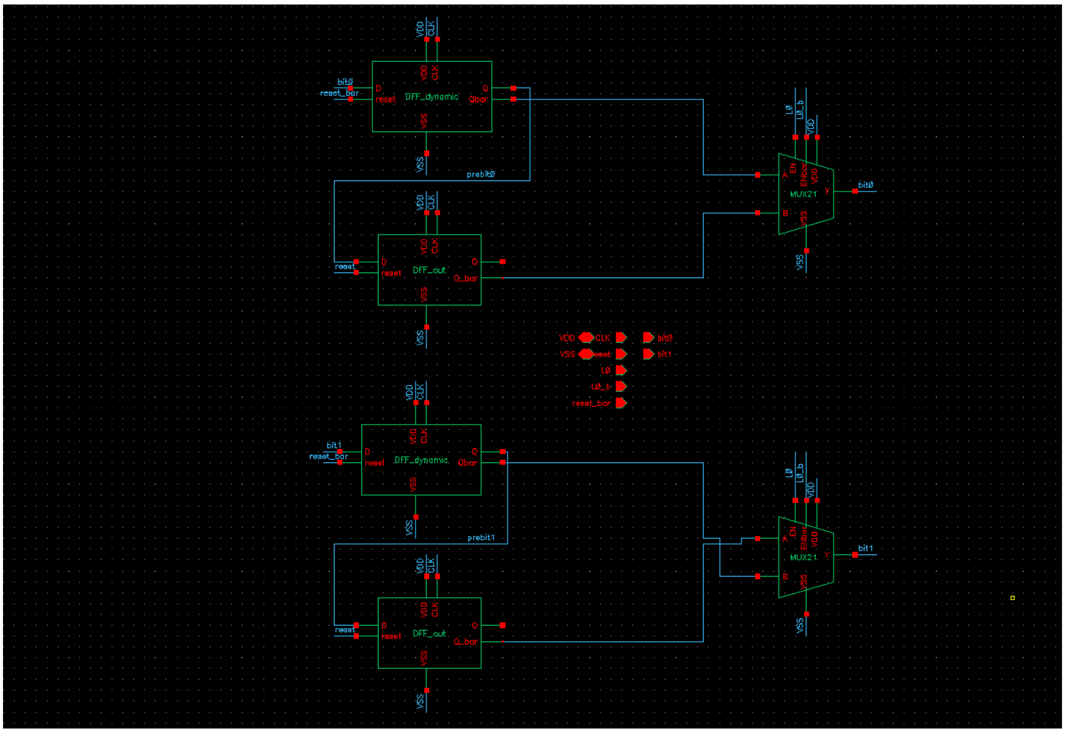
為了減少 DFF 的數量，我們計畫以兩顆 DFF 實現 M4 產生固定序列的功能，並在最後的輸出解碼成題目要求的 4-bit one-hot code。首先考慮一個循環的兩位元平行輸出移位器，由於輸入和輸出相連，最多只能產生以下三種結果，分別是一直維持 2’b00、一直維持 2’b11、或在 2’b01 及 2’b10 之間反覆。如果我們在其中一個 DFF 的輸入端加上 inverter，就可以在實現位元轉移的同時，完成四種不同輸出，該輸出順序也被稱為 Gray code，表(一)是 M4 module 的真值表，實現四個一循環的固定序列。

	Current output	Next output
Initial	2’b10	2’b00
Iteration 1	2’b00	2’b01
Iteration 2	2’b01	2’b11
Iteration 3	2’b11	2’b10
Iteration 4	2’b00	2’b01

表(一)、M4 module 的真值表。

3. M = 3 case

(a) Please draw the block diagram of your logic in this case, discuss on your design.



圖(三)、M3 module。

為了減少 DFF 的數量，我們計畫以四顆 DFF 實現 M3 的功能，並在最後的輸出解碼成題目要求的 4-bit one-hot code。從 Finite State Machine(FSM)的觀點看，我們使用兩個 DFF 共兩位元儲存 current state，並同樣使用兩個 DFF 共兩位元儲存 previous state，記住當前開啟的通道與上一個被開啟的通道，以篩選下一個應該被開啟的通道。

考慮兩位元的 binary code，並假設 PS 是 2’b00，CS 為 2’b11，由觀察可以發現，只要透過 inverter，可以藉由 PS 產生 2’b11，藉由 CS 產生 2’b00，並互換這兩個 state 的低位元，產生出新的兩組數值—2’b10、2’b01，且這兩組的值都不與 previous state 及 current state 相同，成功篩選出能夠作為 next state 的值。這種方式在 previous state 和 current state 不一樣的情況下都能運作，詳細真值表如表(二)所列。

篩選出能作為 next state 的值後，我們利用 LFSR 的偽隨機性，固定使用 LFSR 的 first bit 為 1’b0 還是 1’b1，決定以哪個篩選後剩餘的值當作下個開啟的通道。

	PS or CS(不分前後)	NS
Case 1	2’b00/2’b01	2’b10 或 2’b11
Case 2	2’b01/2’b10	2’b11 或 2’b00
Case 3	2’b10/2’b11	2’b00 或 2’b01
Case 4	2’b11/2’b00	2’b10 或 2’b01
Case 5	2’b00/2’b10	2’b01 或 2’b11
Case 6	2’b01/2’b11	2’b10 或 2’b11

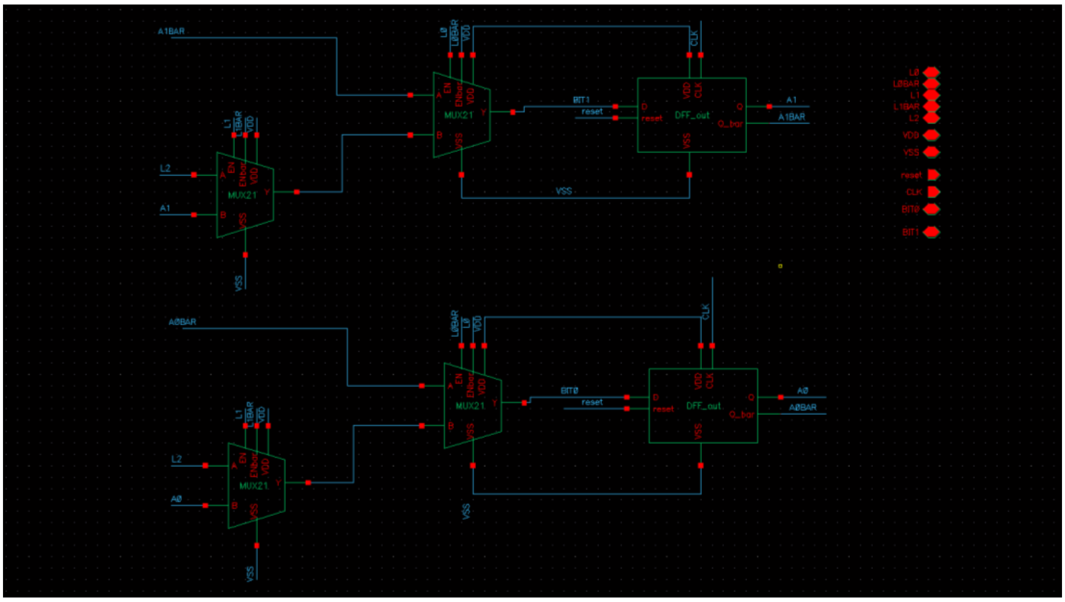
表(二)、M3 module 的真值表，PS、CS、NS 分別表示 previous、current、next state。

(b) Please discuss on how you generate the probability $\frac{1}{2}$ using the PRG.

我們採用 10-bit in-tap LFSR 的 first bit 作為決定下個啟動通道的標準，由於該電路會產生偽隨機數列，因此假設該 bit 產生 0 或 1 的機率是 1/2，故 LFSR 的 first bit 在決定 next state 時，剩下兩個通道被選到的機率都是 1/2。以 current state 為 2’b00、CS 為 2’b01 為例，next state 為 2’b11 和 2’b10 的機率，假設 LFSR first bit 為 1 選 2’b11，為 0 選 2’b10，由於 LFSR 為 0 和 1 的機率都為 50%，顯然 next state 是 2’b11 和 2’b01 的可能性都是 50%。

4. M = 2 case

(a) Please draw the block diagram of your logic in this case, discuss on your design.



圖（四）、M2 module。

為了減少 DFF 的數量，我們計畫以兩顆 DFF 實現 M2 的功能，並在最後的輸出解碼成題目要求的 4-bit one-hot code。從 Finite State Machine(FSM)的觀點看，我們使用兩個 DFF 共兩位元儲存 current state，用以篩選下一個應該被開啟的通道。

跟 M3 的想法很像，考慮兩位元的 binary code，假設 current state 為 2’b00，很容易就觀察到只要將 current state 的高位元或低位元其中一個反相，另一個隨意是 0 或 1，就能得到與 current state 完全不同的值，選擇出下一個被開啟的通道。基於上述這個理念，我們引入了 10-bit LFSR 的其中三個輸出腳位作為篩選 next state 的依據。首先，我們使用 LFSR 的 7th bit 決定 current state 要低位或高位的位元做反相，如果 LFSR 的 7th bit 是 1 選擇高位元反相，反之則是低位元被反相；其次，為了使剩餘三通道被選到的機率接近 1/3，我們額外引入兩個 LFSR 的 bit，其中一個做為控制訊號，決定 MUX 要選擇原 bit 值或是另一個 LFSR 的值。舉例來說，假設 current state 為 2’b00，LFSR 的 7th bit 選擇低位元反相，則 NS 的低位元為 1，高位元則由 LFSR 的 5th bit 控制，如果 5th bit 等於 1，選擇 LFSR 的 6th bit 當作高位元的值，反之則取原來 current state 的高位元值，表(三)為 current state 等於 2’b00 時，剩餘三個通道被選為 next state 的真值表，其他 current state 的情況可以此類推。

CS	7th bit	5th bit	6th bit	NS
2'b00	0	0	0	2'b01
2'b00	0	0	1	2'b01
2'b00	0	1	0	2'b01
2'b00	0	1	1	2'b11
2'b00	1	0	0	2'b10
2'b00	1	0	1	2'b10
2'b00	1	1	0	2'b10
2'b00	1	1	1	2'b11

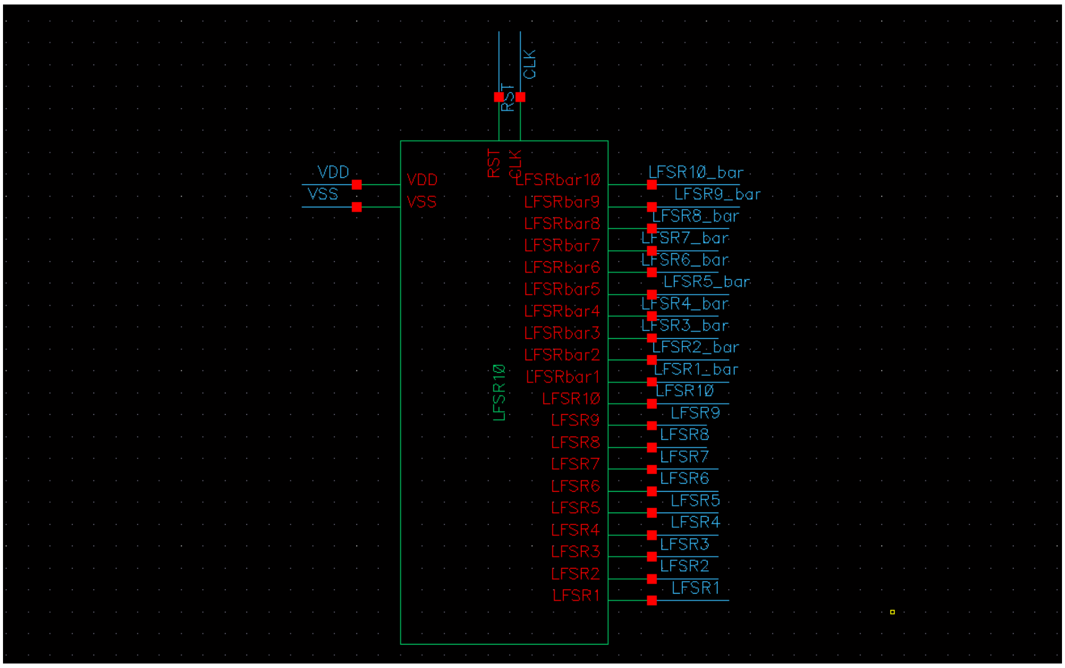
表(三)、M2 module 的真值表，CS 表示 current state。

(b) Please discuss on how you generate the probability $\frac{1}{3}$ using the PRG.

我們使用 10-bit LFSR 的 7th bit、5th bit 做為控制下一個被開啟通道的選擇依據，並使用 CS、CS 的反相以及 6th bit 產生 NS 組合的變數。根據表(四)的結果，假設 LFSR 給出的 bit 為 0 或 1 的機率是 1/2，推論表(四)中的每個狀況發生機率會是 1/8，因此我們可以得到剩餘通道被選到的機率分別是 3/8、3/8、2/8，並沒有擬合 1/3 的結果，這是因為在我們實現的邏輯中，LFSR 無論取幾位，產生的組合數都是2^n個，無法將其分割成等數量的三組去做選擇，也就無法得出真正的 1/3。經過我們的測試，雖然取 LFSR 的 4 個 bit 用不同但相似的電路架構，列出真值表後所得出能使剩餘通道被選到的機率可以是 5/16、5/16、6/16，會更接近 1/3，但這樣會使 M2 電路的面積增大、功耗增加且路徑延遲上升的風險，因此決定都嘗試 pre-sim 並且將結果給 MATLAB 測試，發現不管是取 3 bits 或 4 bits 的 LFSR 所實現的 M2，所有的 test 皆可通過且均會產生合格的 PSD 圖，故採用(a)小題所介紹的電路架構實現逼近 1/3 機率的情境。

5. M = 1 case

(a) Please draw the block diagram of your logic in this case, discuss on your design.



圖(五)、LFSR module，M1 的功能是由 LFSR 的 3rd bit 和 8th bit 產生。

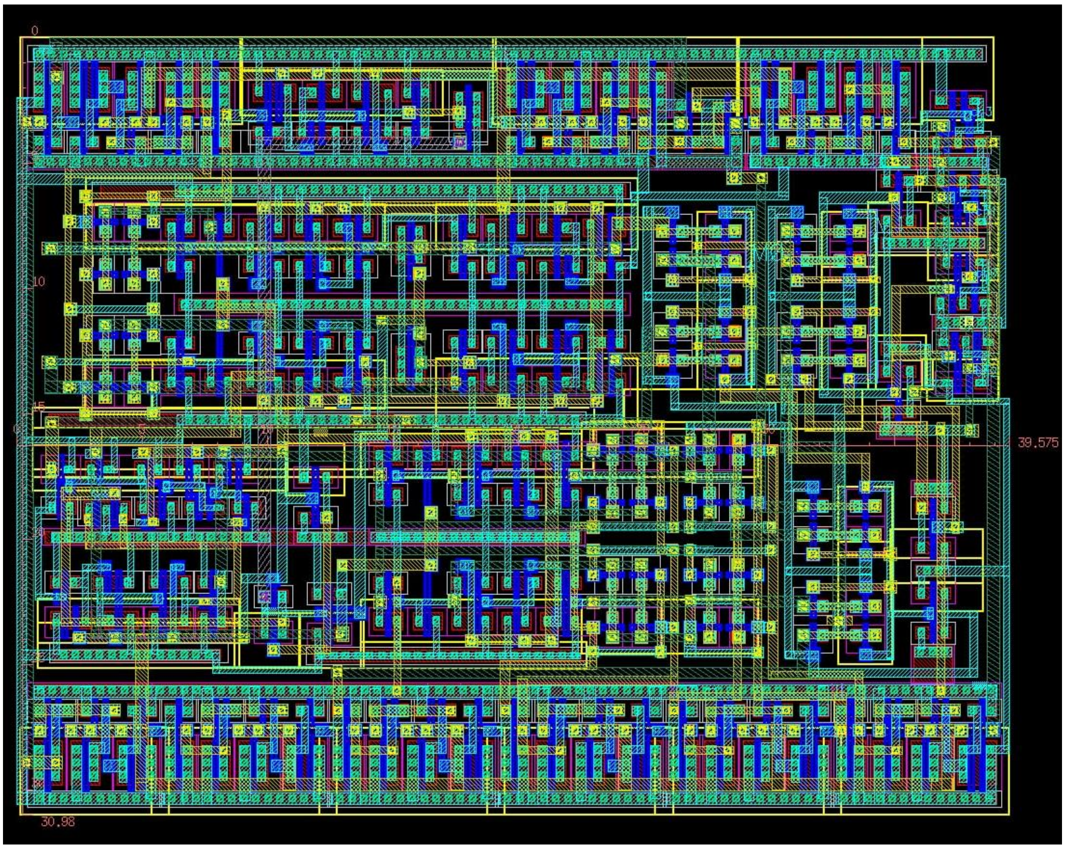
我們以 10-bit LFSR 的其中兩個 bit 作為產生 M1 要求的隨機性，所以分別選擇 LFSR 的 3rd bit 和 8th bit 成為 M=1 這個 case 的輸入訊號，並在輸出前經過 decoder 解碼成 4-bit one-hot code。

(b) Please discuss on how you generate the probability $\frac{1}{4}$ using the PRG.

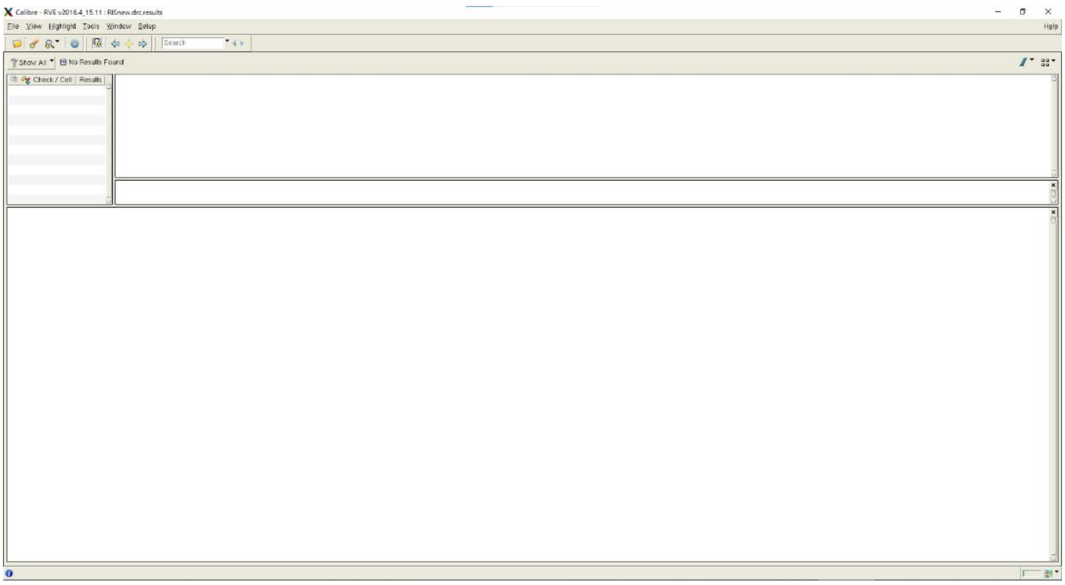
由之前的分析知，10-bit LFSR 的任一位元的輸出為 0 或 1 的機率大約會是 1/2，所以任選 10-bit LFSR 的其中兩 bit 當作 M1 產生器，出現 2’b01、2’b10、2’b11、2’b00 的機率是 1/4。

6. Simulation Result

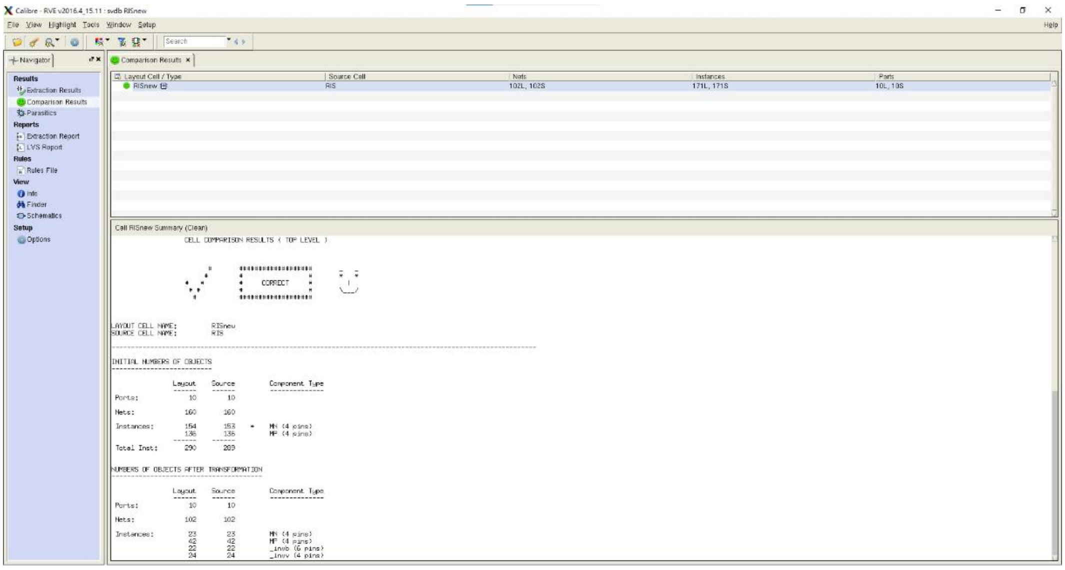
(a) Please take a screenshot of your layout (with area and aspect ratio labeled), and the DRC/LVS result.



圖(六)、Layout 面積為 30.98um×39.585um，aspect ratio=1.278。



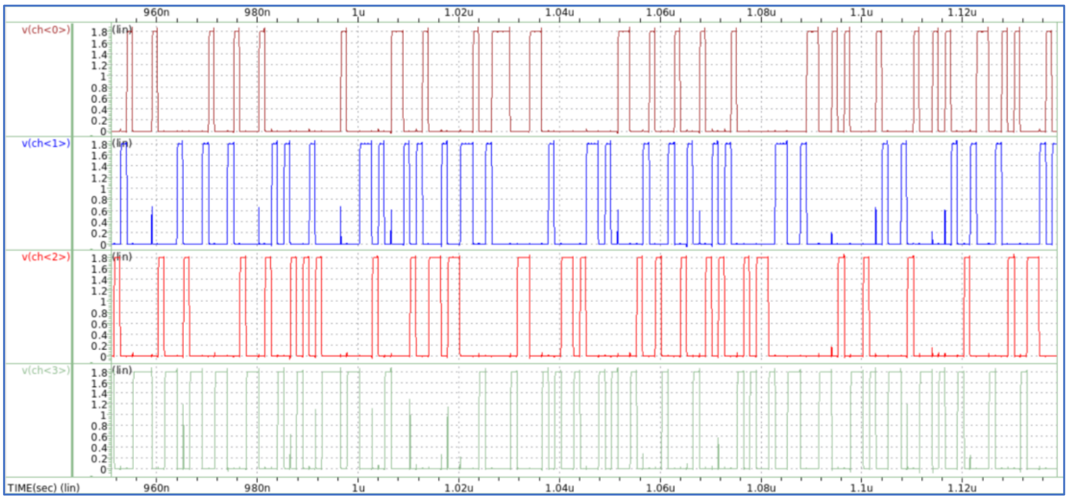
圖(七)、Layout 的 DRC 結果。



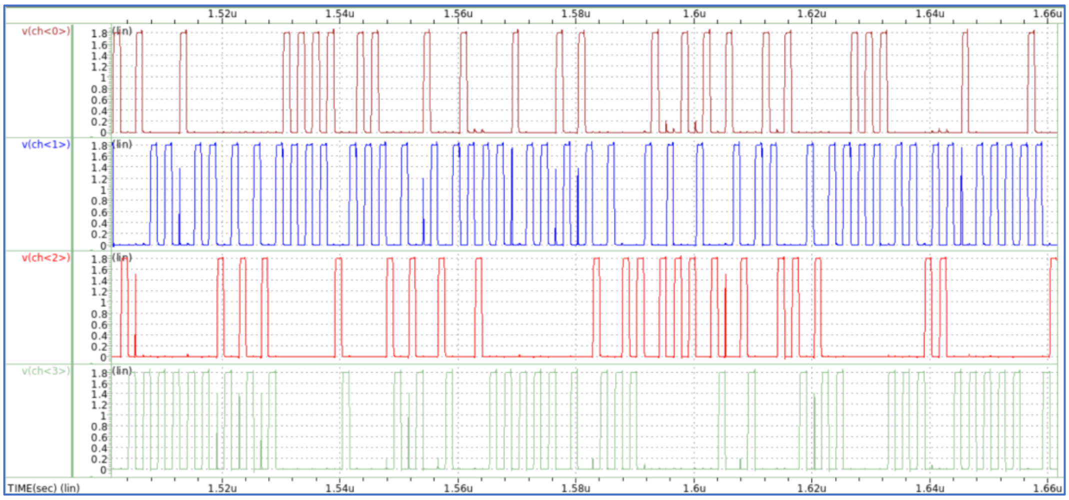
圖（八）、Layout 的 LVS 結果。

(b) Please take a screenshot of the waveform of Ch<3:0> in Waveview, the verification result of functional correctness, and the spectrum in MATLAB, for all 4 cases, 5 corners, as well as pre/post-sim. Additionally, fill the SPEC table, and provide a discussion on the results. (4 x 5 x 1%)

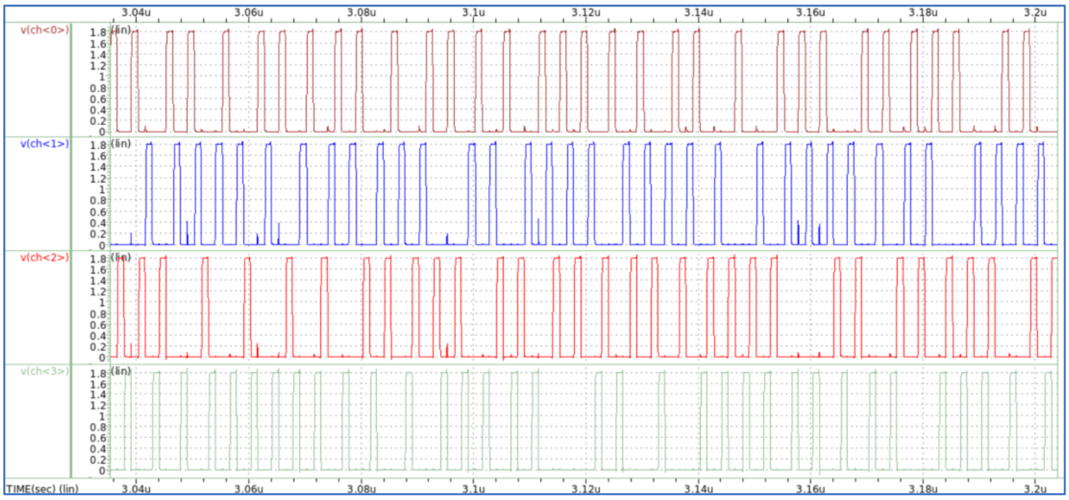
- TT presim



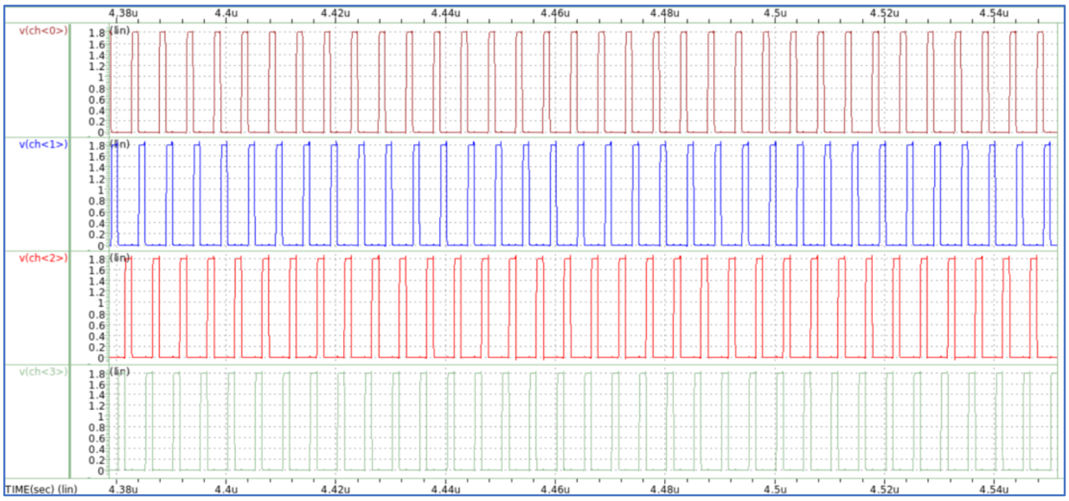
圖（九）、M1 function of TT Presim@0.8GHz。



圖(十)、M2 function of TT Presim@0.8GHz。



圖(十一)、M3 function of TT Presim@0.8GHz。



圖(十二)、M4 function of TT Presim@0.8GHz。

check the rule Concentration

```
Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.
```

check the rule Non-repetitive

```
Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.
```

Perform the QAM and calculate the PSD

QAM

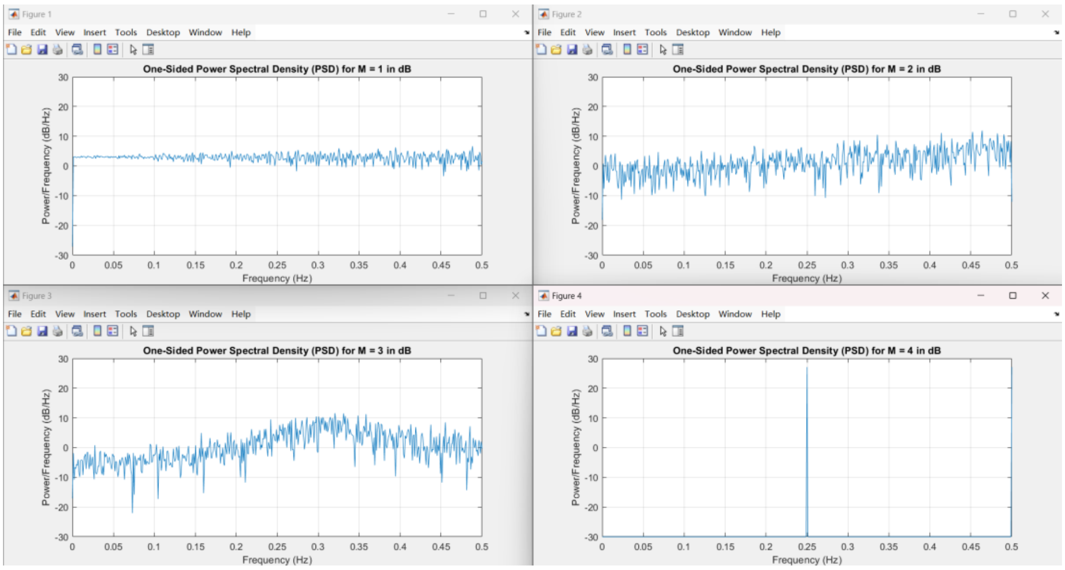
check the rule Balance

```
Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB
```

check the rule Randomness

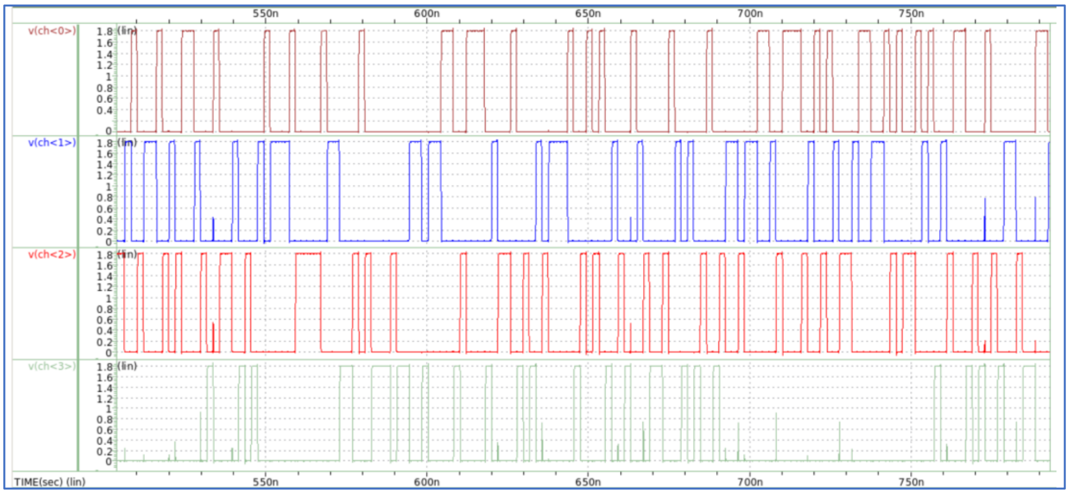
```
Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1:    6.0000dB

Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2:    8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

Ideal SNDR boost for case M = 3:    13.1330dB
```

圖(十三)、The result of functional correctness of TT Presim@0.8GHz。

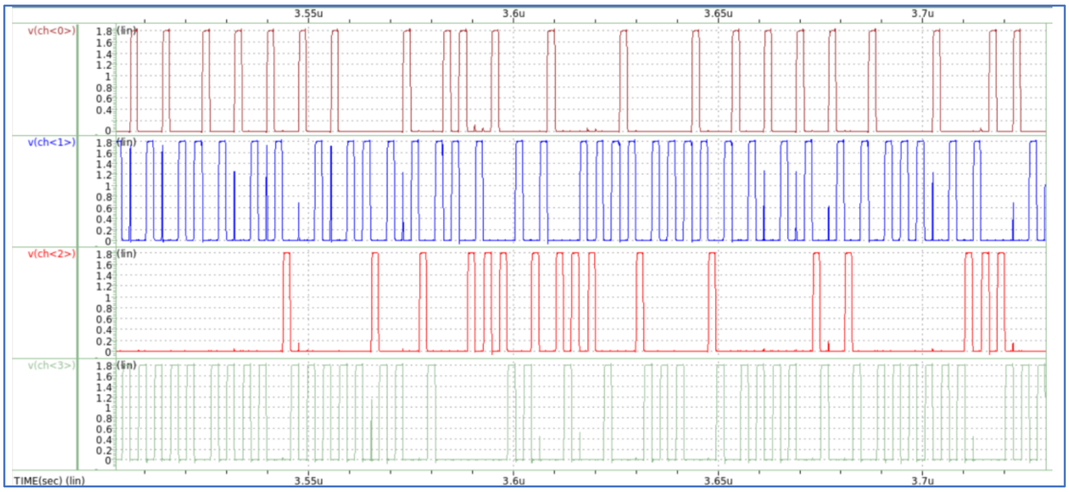


圖(十四)、The result of PSD of TT Presim@0.8GHz。

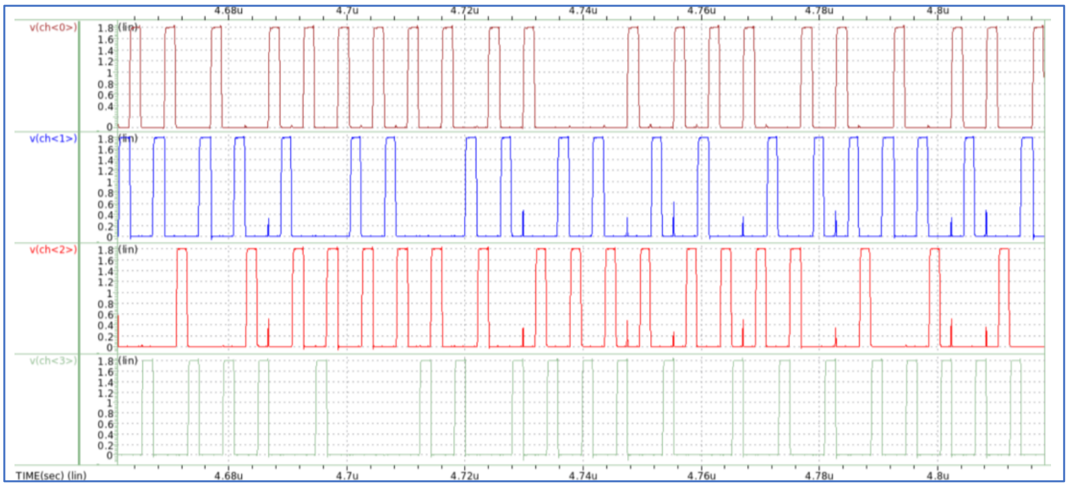
- TT postsim



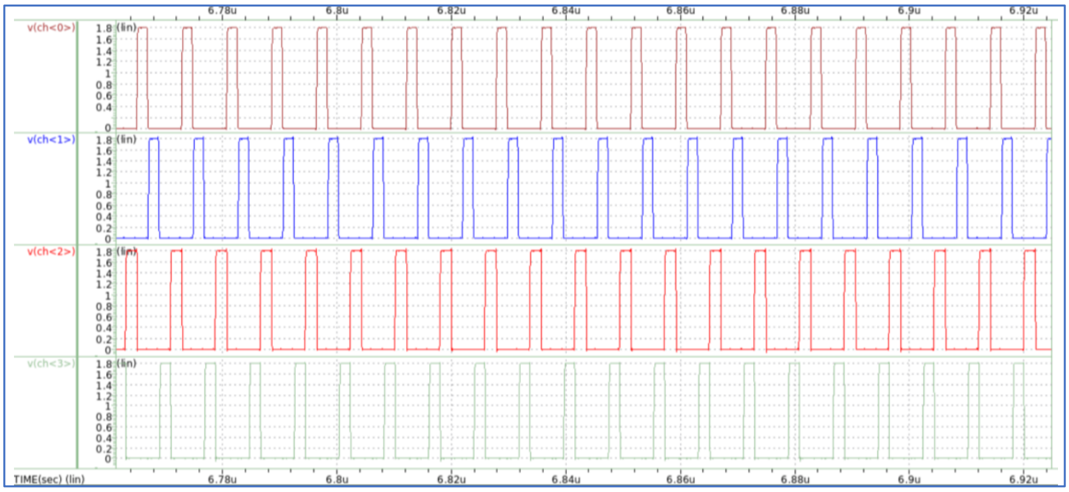
圖（十五）、M1 function of TT Postsim@0.51GHz。



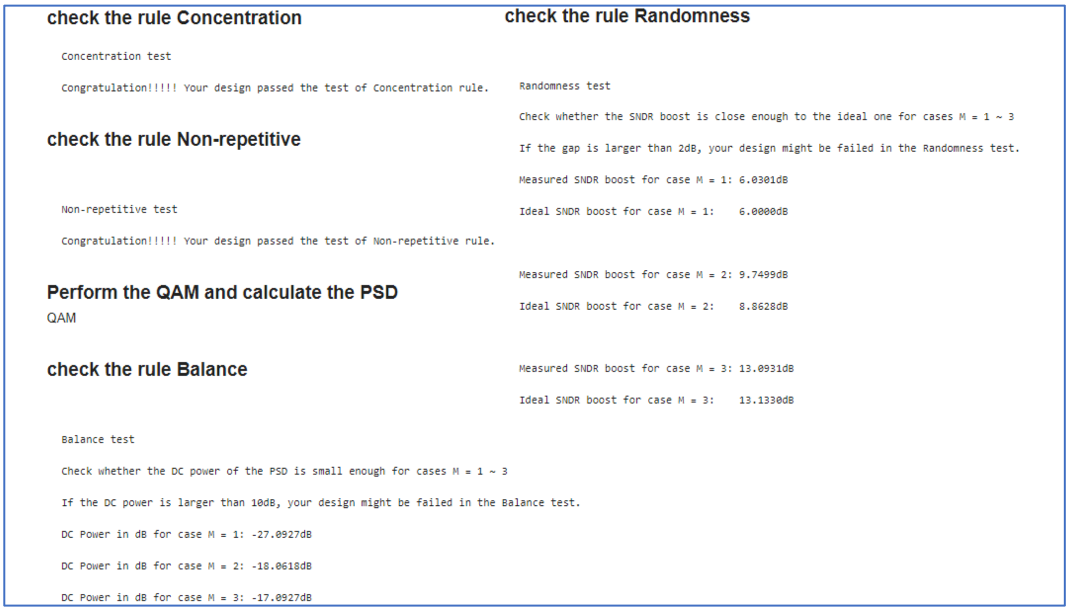
圖（十六）、M2 function of TT Postsim@0.51GHz。



圖（十七）、M3 function of TT Postsim@0.51GHz。



圖（十八）、M4 function of TT Postsim@0.51GHz。



check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1: 6.0000dB

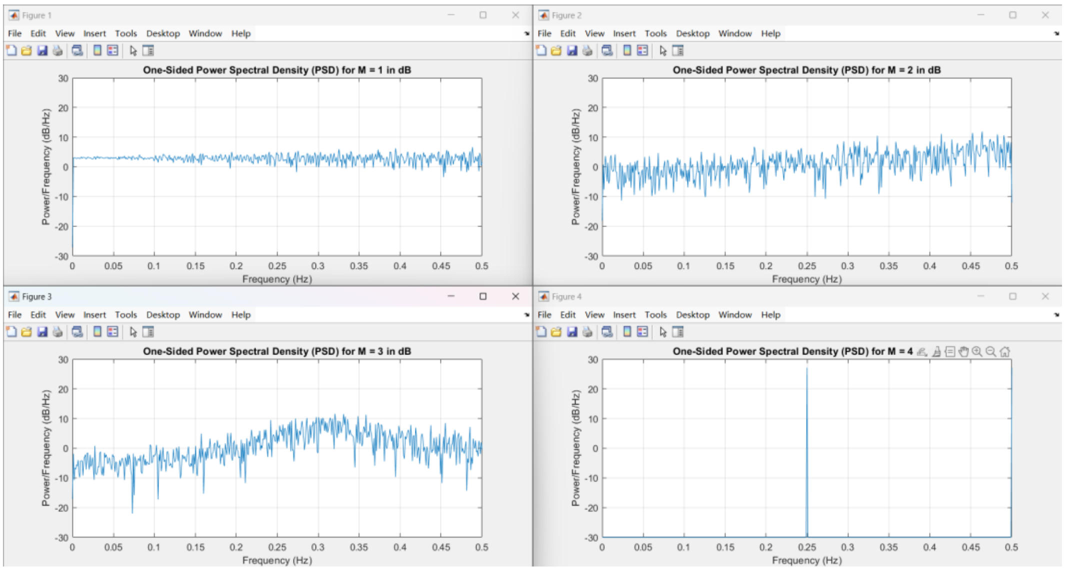
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2: 8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

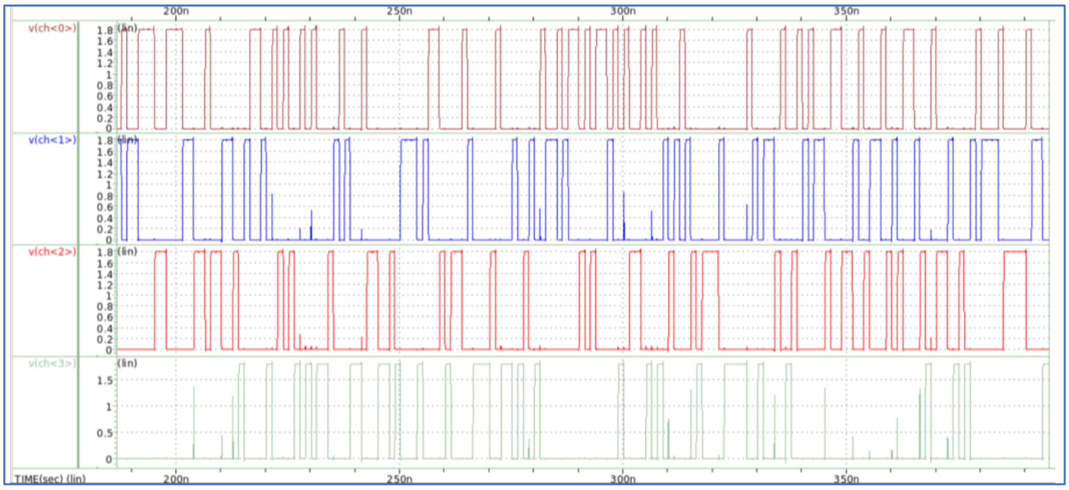
Ideal SNDR boost for case M = 3: 13.1330dB

圖（十九）、The result of PSD of TT Postsim@0.51GHz。

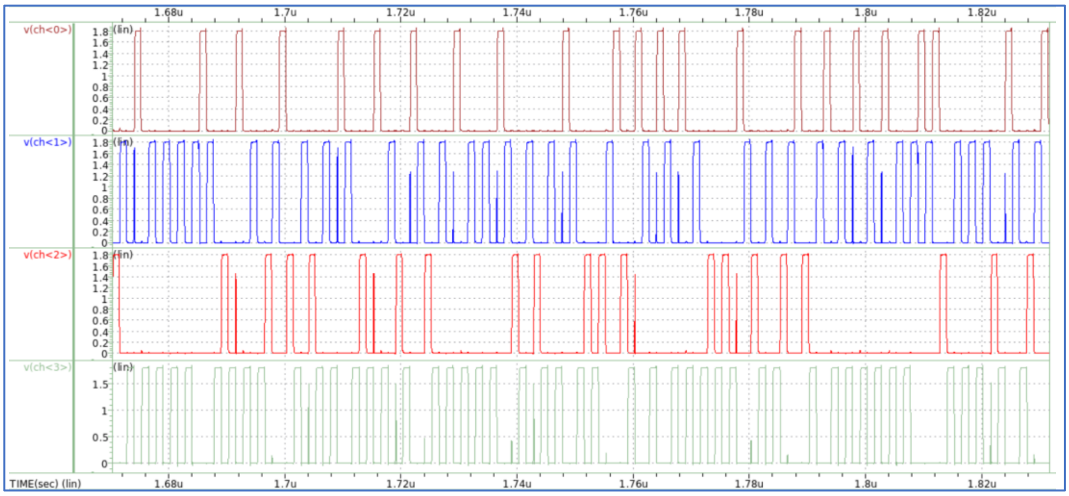


圖(二十)、The result of functional correctness of TT Postsim@0.51GHz。

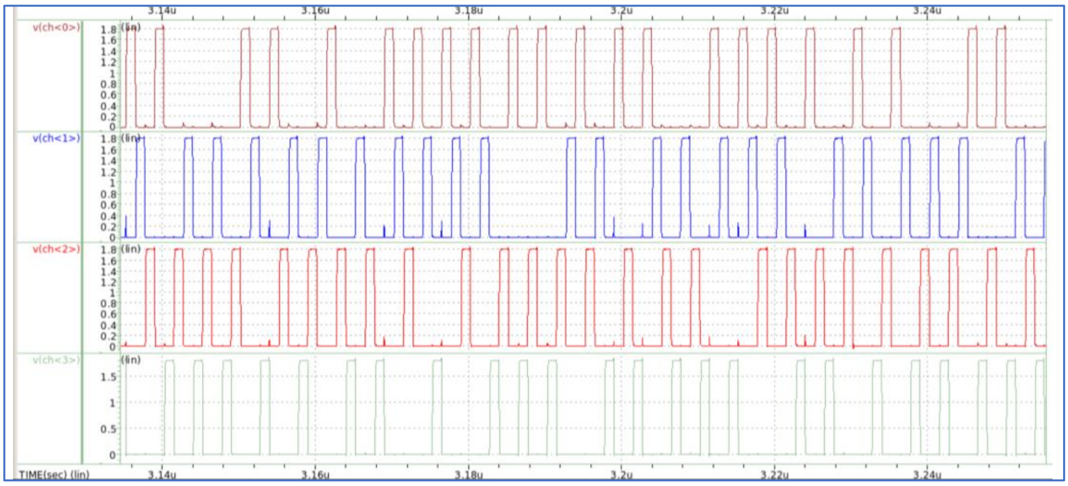
- FF presim



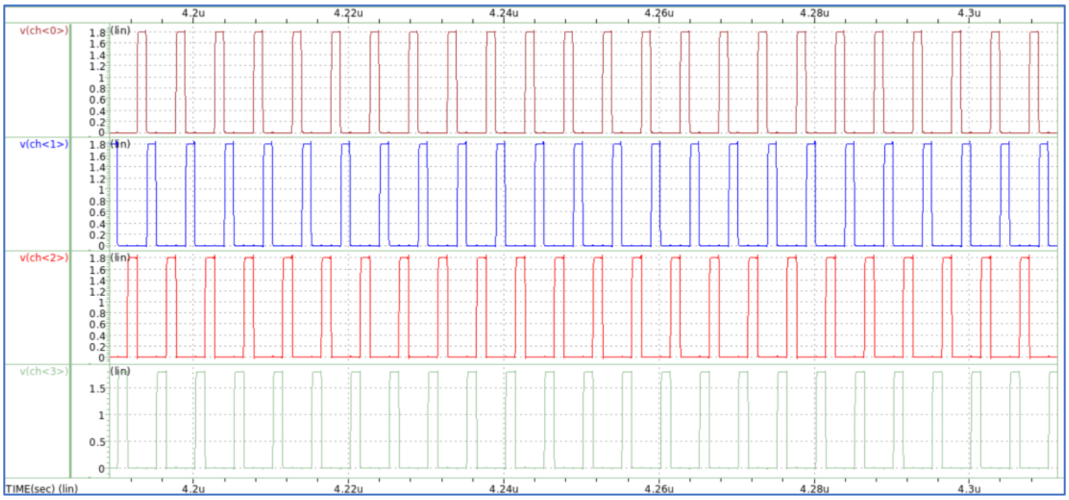
圖(二十一)、M1 function of FF Presim@0.8GHz。



圖(二十二)、M2 function of FF Presim@0.8GHz。



圖(二十三)、M3 function of FF Presim@0.8GHz。



圖(二十四)、M4 function of FF Presim@0.8GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1: 6.0000dB

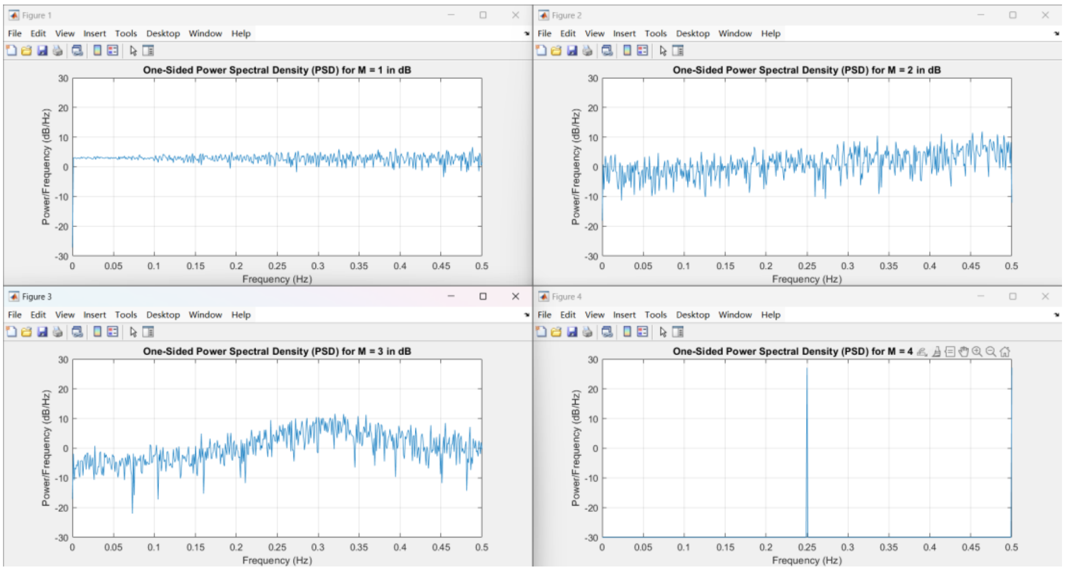
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2: 8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

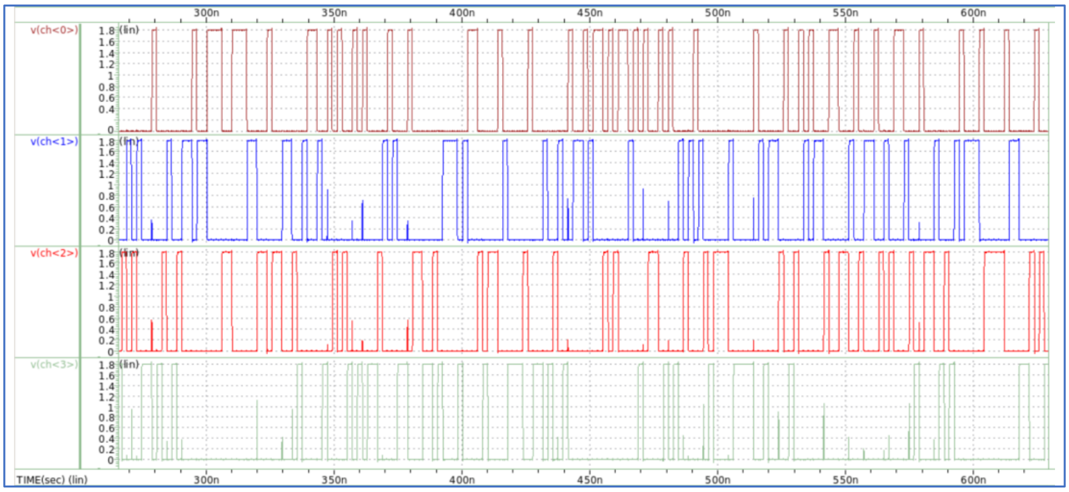
Ideal SNDR boost for case M = 3: 13.1330dB

圖(二十五)、The result of functional correctness of FF Presim@0.8GHz。



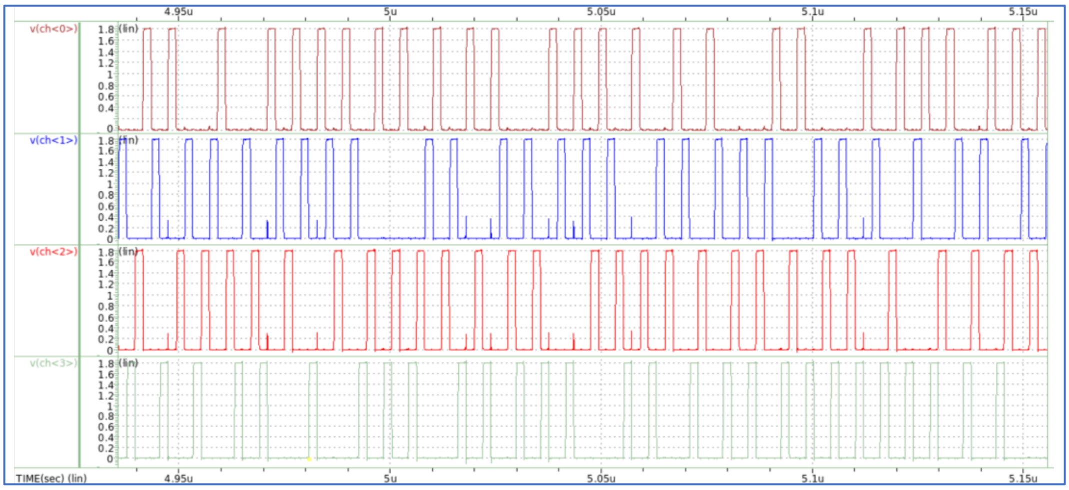
圖（二十六）、The result of functional correctness of FF Presim@0.8GHz。

● FF postsim

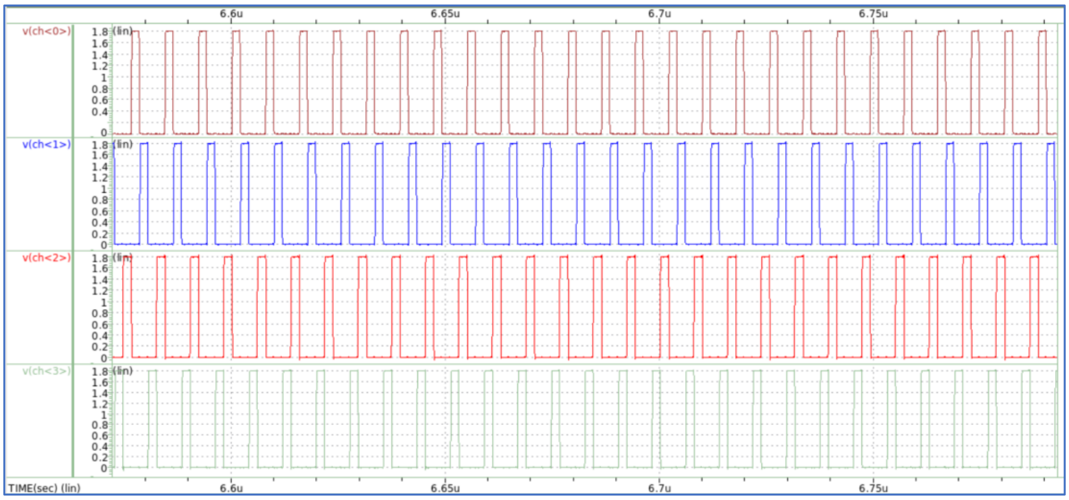


圖（二十七）、M1 function of FF Postsim@0.51GHz。

圖（二十八）、M2 function of FF Postsim@0.51GHz。



圖（二十九）、M3 function of FF Postsim@0.51GHz。



圖(三十)、M4 function of FF Postsim@0.51GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1: 6.0000dB

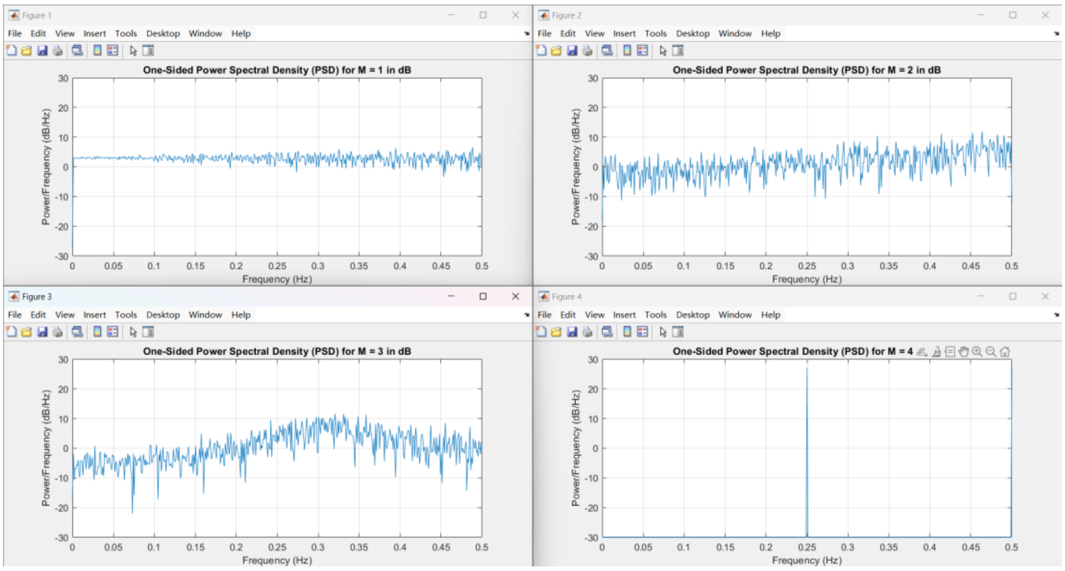
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2: 8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

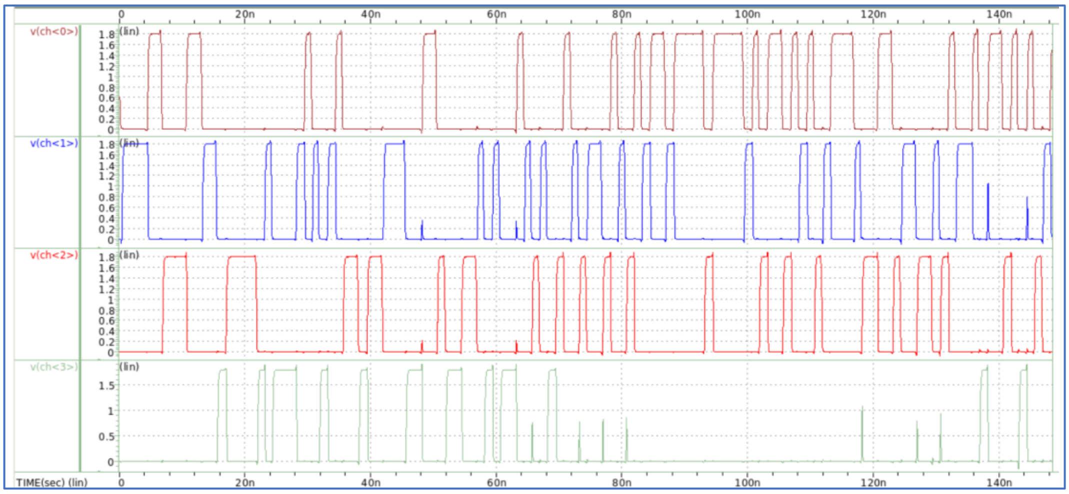
Ideal SNDR boost for case M = 3: 13.1330dB

圖(三十一)、The result of functional correctness of FF Postsim@0.51GHz。

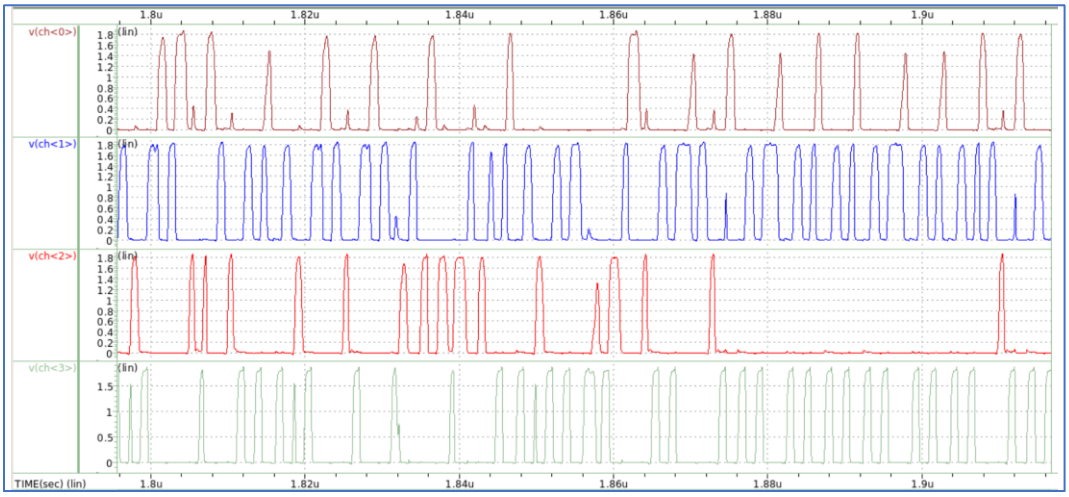


圖（三十二）、The result of functional correctness of FF Postsim@0.51GHz。

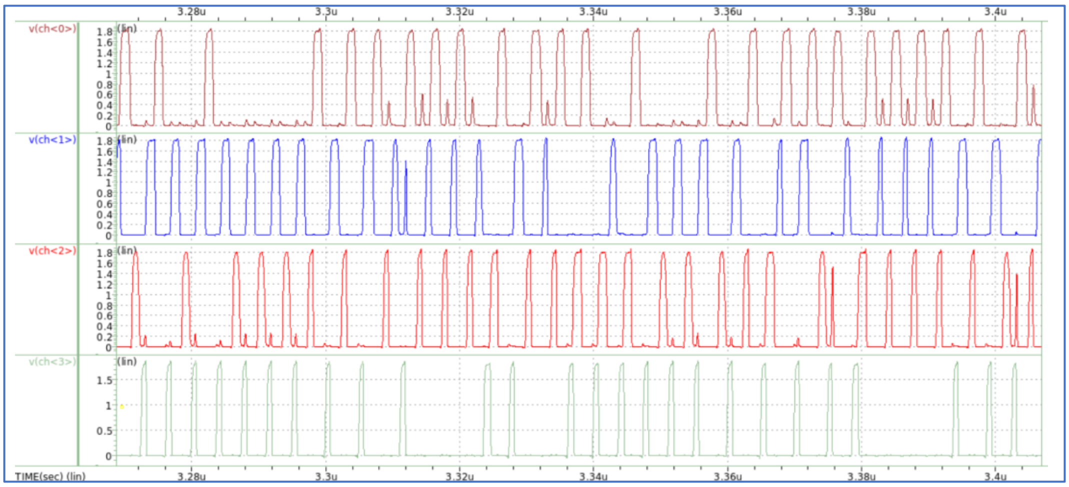
- SS presim



圖(三十三)、M1 function of SS presim@0.8GHz。

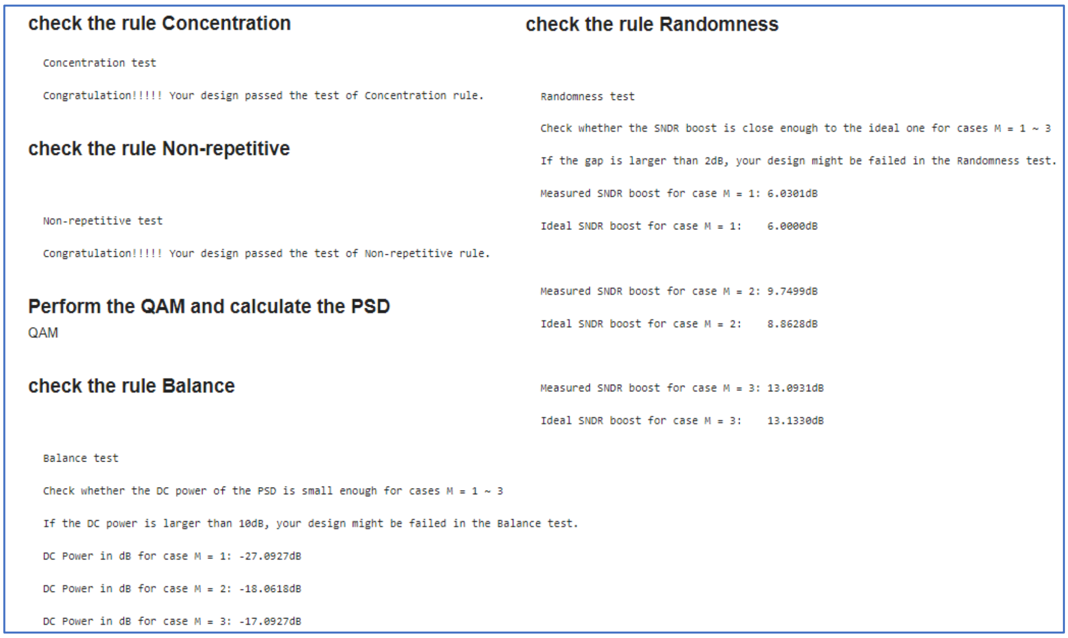


圖(三十四)、M2 function of SS presim@0.8GHz。



圖(三十五)、M3 function of SS presim@0.8GHz。

圖(三十六)、M4 function of SS presim@0.8GHz。



check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1: 6.0000dB

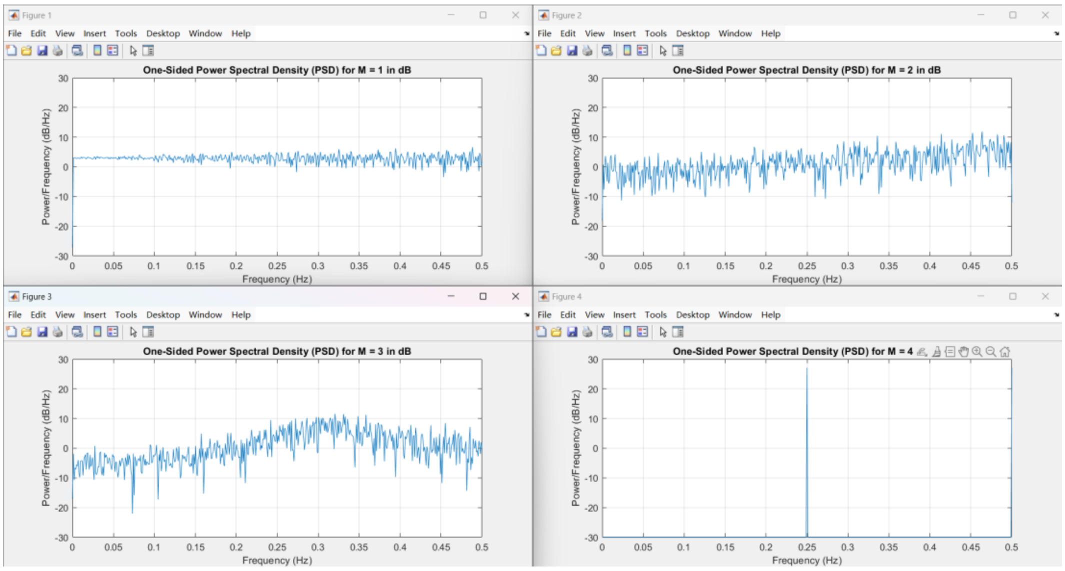
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2: 8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

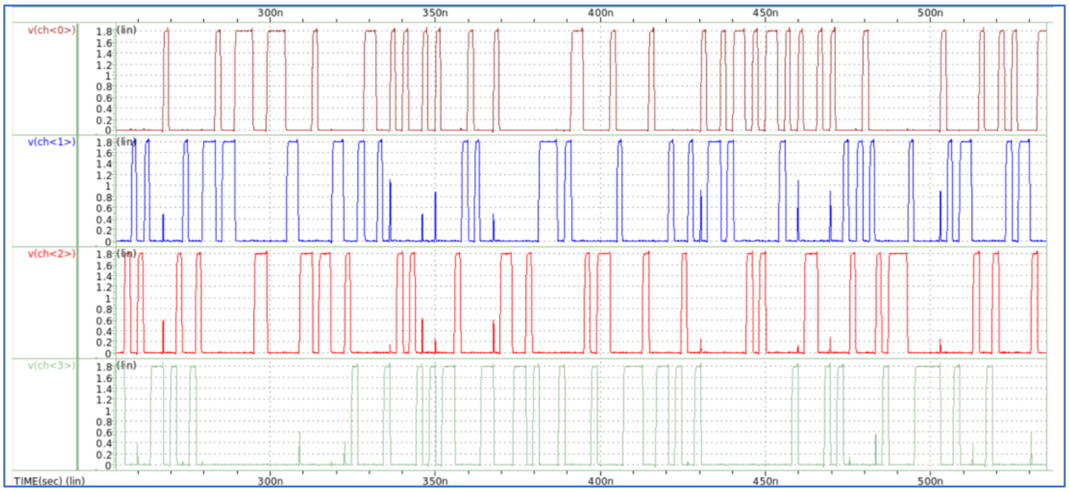
Ideal SNDR boost for case M = 3: 13.1330dB

圖(三十七)、The result of functional correctness of SS Presim@0.8GHz。

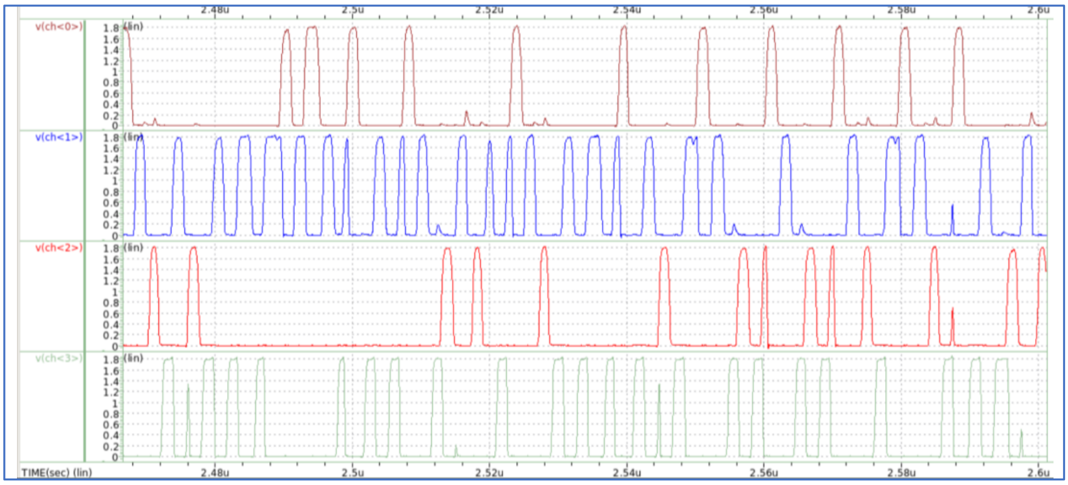


圖(三十八)、The result of functional correctness of SS Presim@0.8GHz。

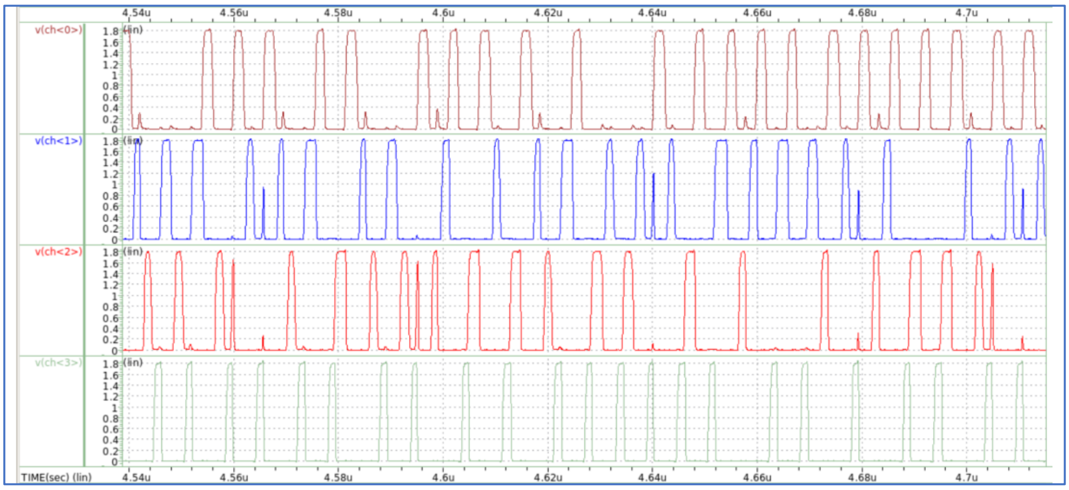
- SS postsim



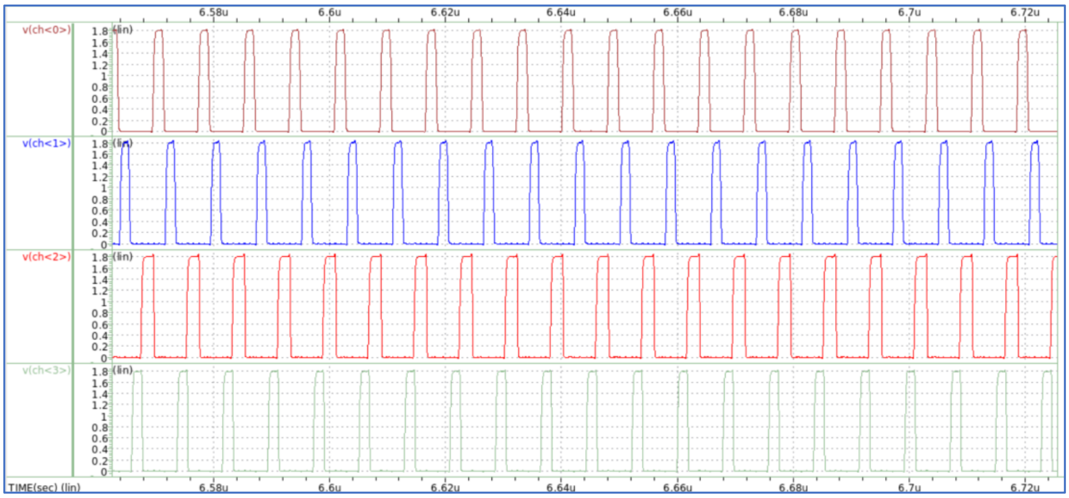
圖(三十九)、M1 function of SS postsim@0.51GHz。



圖(四十)、M2 function of SS postsim@0.51GHz。



圖(四十一)、M3 function of SS postsim@0.51GHz。



圖（四十二）、M4 function of SS postsim@0.51GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1:   6.0000dB

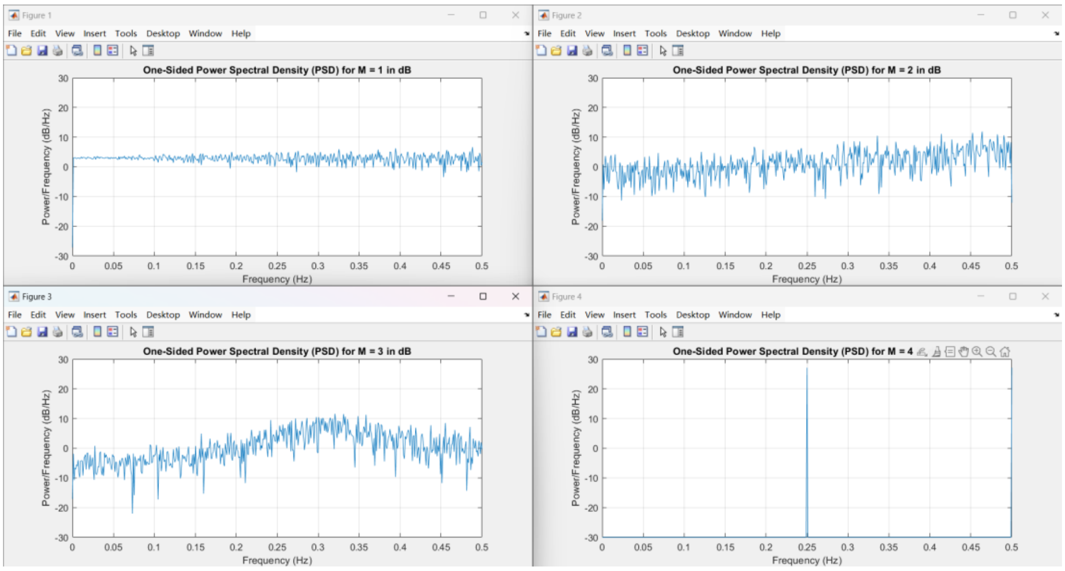
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2:   8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

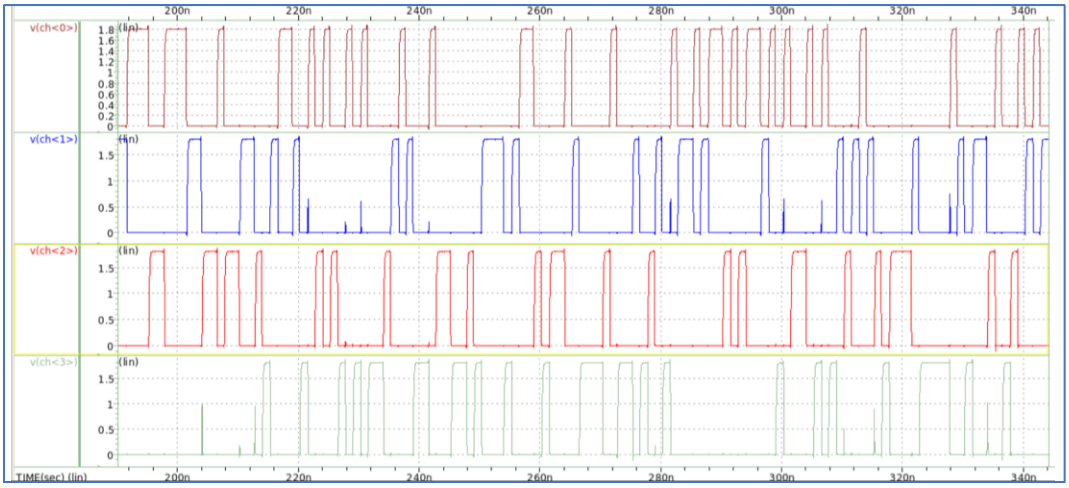
Ideal SNDR boost for case M = 3:   13.1330dB

圖（四十三）、The result of functional correctness of SS Postsim@0.51GHz。



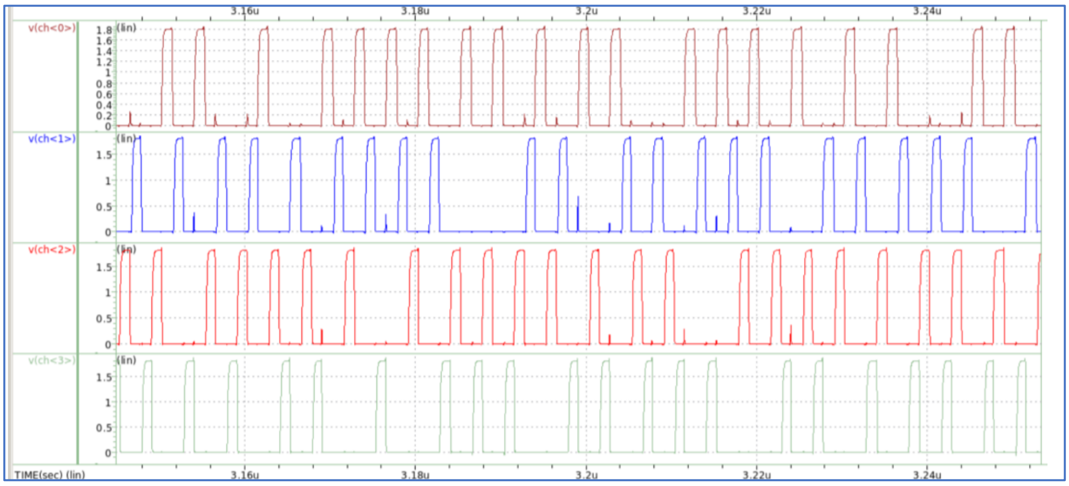
圖(四十四)、The result of functional correctness of SS Pretsim@0.51GHz。

- FS presim

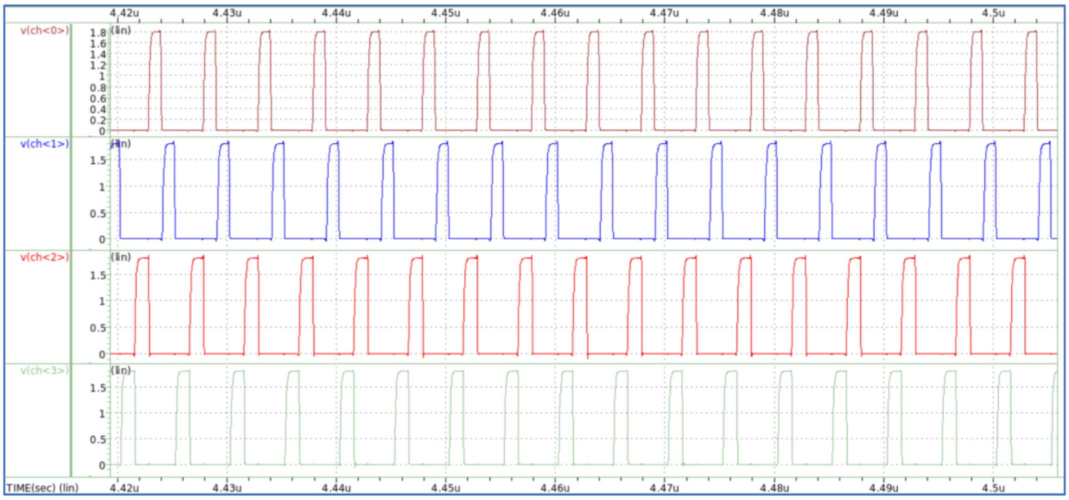


圖（四十五）、M1 function of FS presim@0.8GHz。

圖（四十六）、M2 function of FS presim@0.8GHz。



圖（四十七）、M3 function of FS presim@0.8GHz。



圖(四十八)、M4 function of FS presim@0.8GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1:   6.0000dB

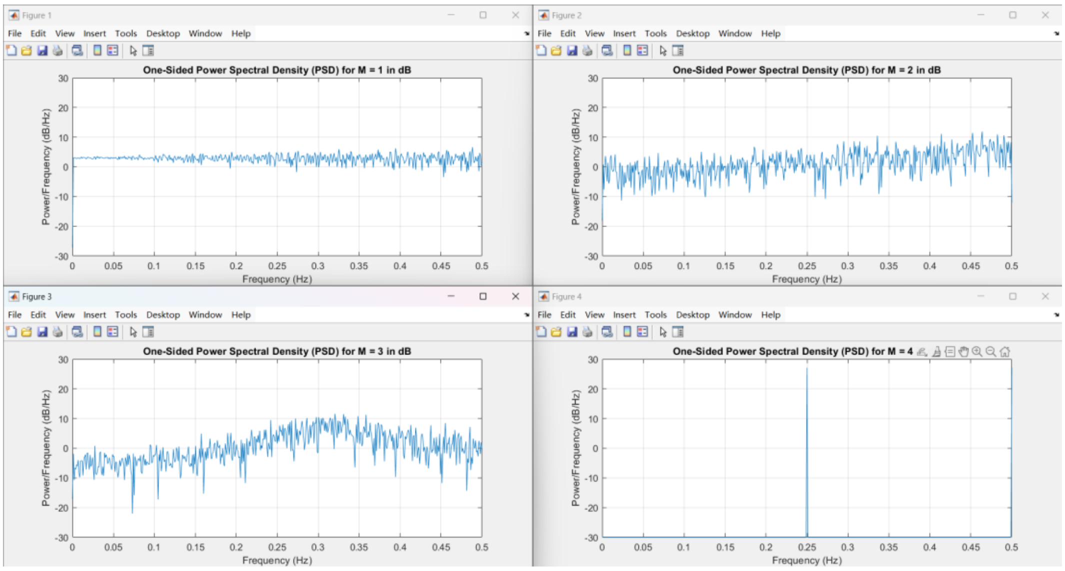
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2:   8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

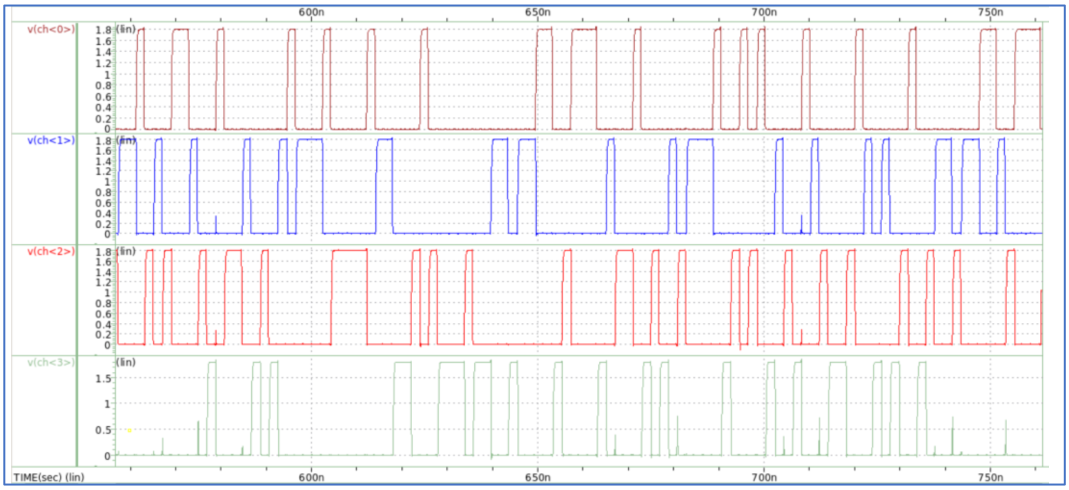
Ideal SNDR boost for case M = 3:   13.1330dB

圖(四十九)、The result of functional correctness of FS presim@0. 8GHz。

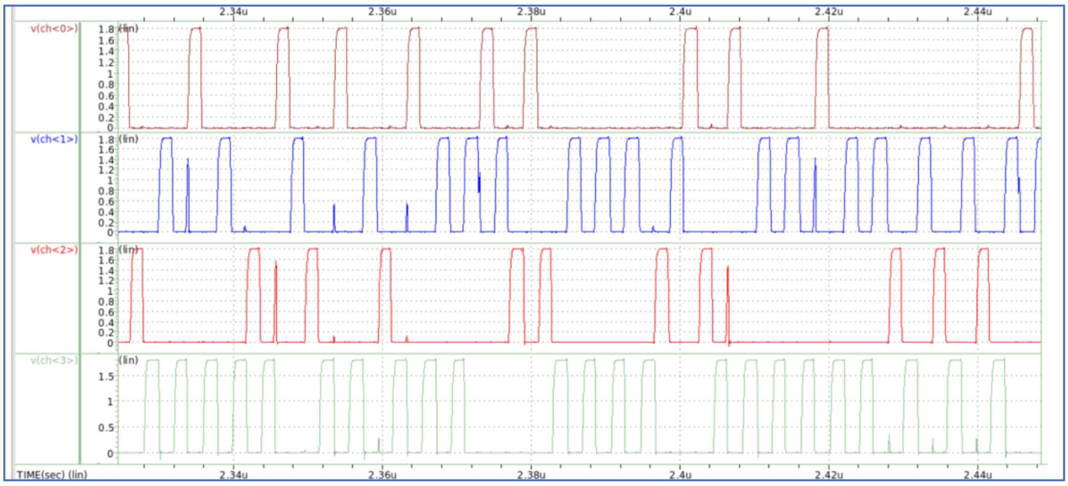


圖（五十）、The result of functional correctness of FS presim@0.8GHz。

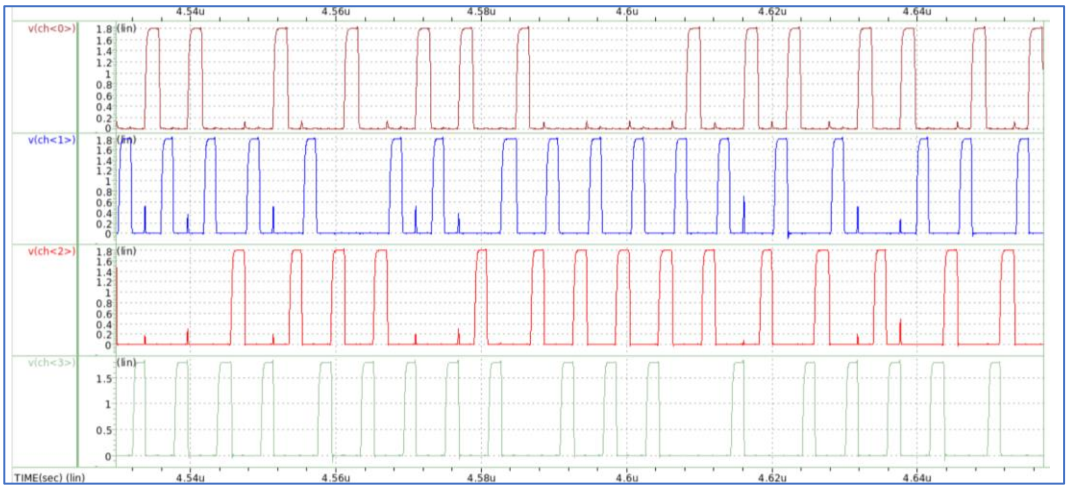
- FS postsim



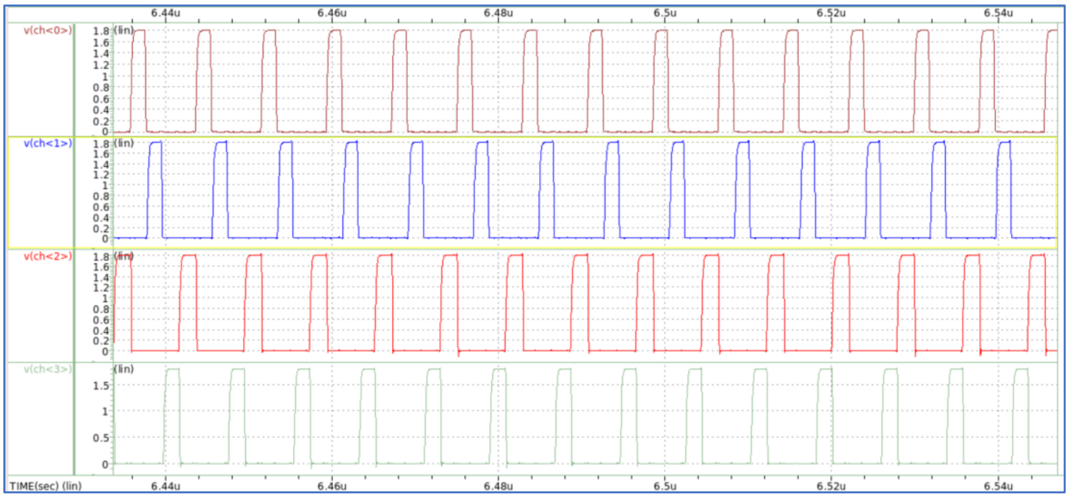
圖(五十一)、M1 function of FS postsim@0.51GHz。



圖(五十二)、M2 function of FS postsim@0.51GHz。



圖(五十三)、M3 function of FS postsim@0.51GHz。



圖(五十四)、M4 function of FS postsim@0.51GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1:   6.0000dB

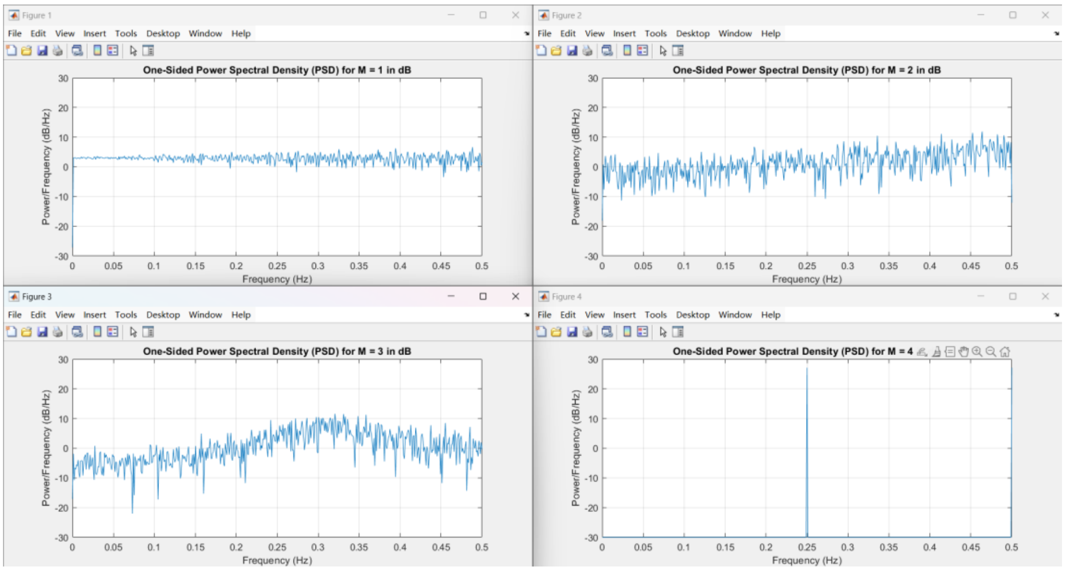
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2:   8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

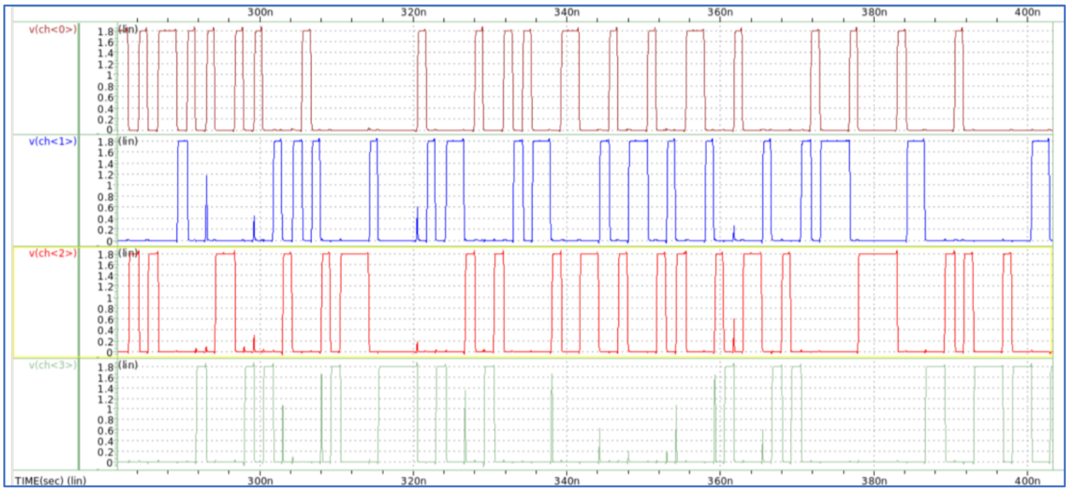
Ideal SNDR boost for case M = 3:   13.1330dB

圖(五十五)、The result of functional correctness of FS postsim@0. 51GHz。



圖(五十六)、The result of functional correctness of FS postsim@0.51GHz。

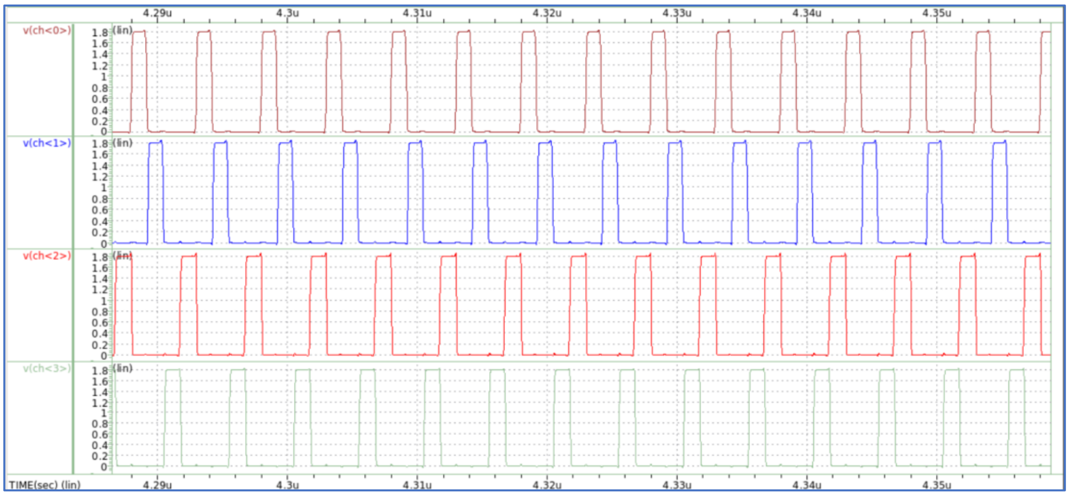
- SF presim



圖(五十七)、M1 function of SF presim@0.8GHz。

圖(五十八)、M2 function of SF presim@0.8GHz。

圖(五十九)、M3 function of SF presim@0.8GHz。



圖（六十）、M4 function of SF presim@0.8GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1:   6.0000dB

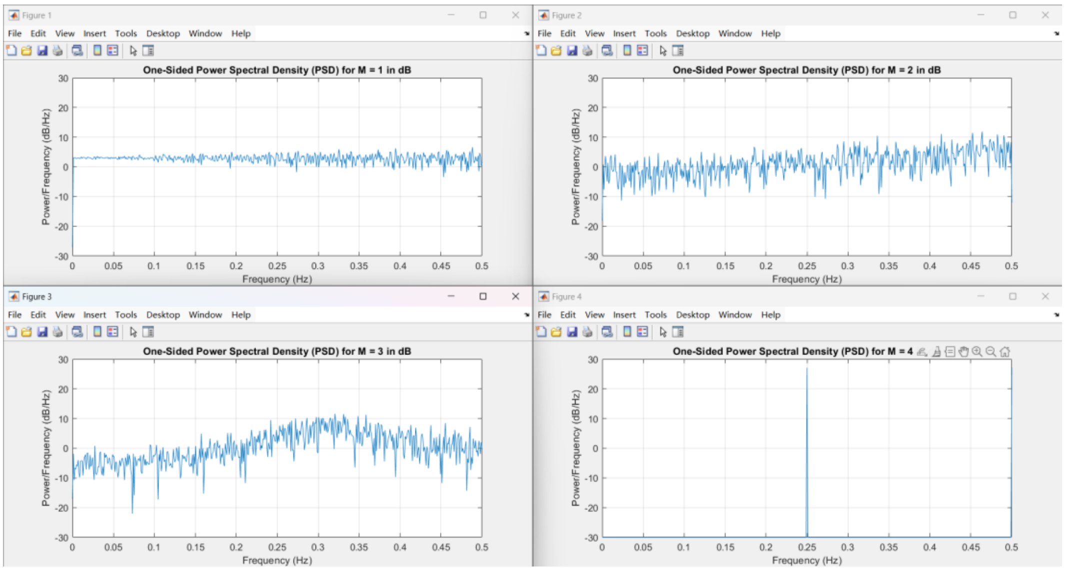
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2:   8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

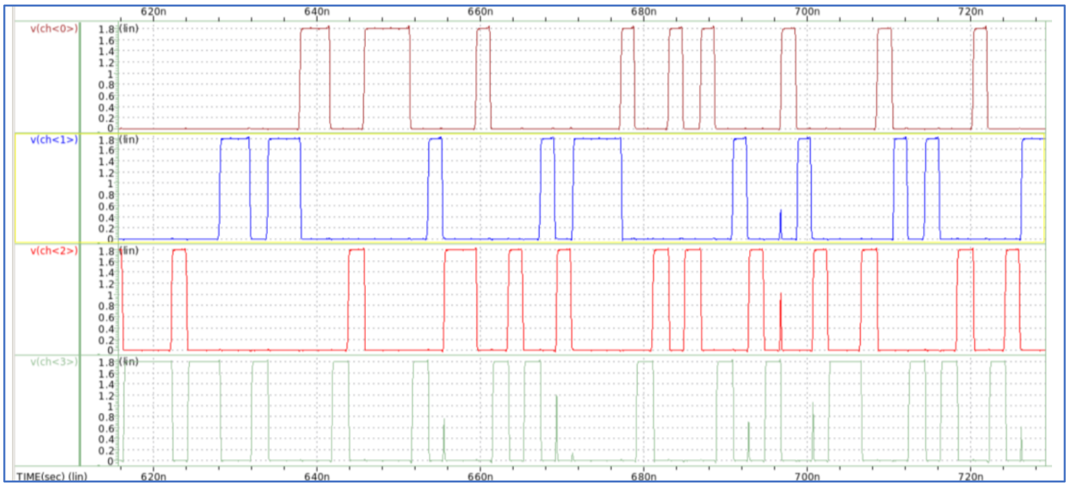
Ideal SNDR boost for case M = 3:   13.1330dB

圖（六十一）、The result of functional correctness of SF presim@0. 8GHz。



圖(六十二)、The result of functional correctness of SF presim@0.8GHz。

- SF postsim



圖（六十三）、M1 function of SF postsim@0.51GHz。

圖（六十四）、M2 function of SF postsim@0.51GHz。

圖（六十五）、M3 function of SF postsim@0.51GHz。

圖(六十六)、M4 function of SF postsim@0.51GHz。

check the rule Concentration

Concentration test

Congratulation!!!!! Your design passed the test of Concentration rule.

check the rule Non-repetitive

Non-repetitive test

Congratulation!!!!! Your design passed the test of Non-repetitive rule.

Perform the QAM and calculate the PSD

QAM

check the rule Balance

Balance test

Check whether the DC power of the PSD is small enough for cases M = 1 ~ 3

If the DC power is larger than 10dB, your design might be failed in the Balance test.

DC Power in dB for case M = 1: -27.0927dB

DC Power in dB for case M = 2: -18.0618dB

DC Power in dB for case M = 3: -17.0927dB

check the rule Randomness

Randomness test

Check whether the SNDR boost is close enough to the ideal one for cases M = 1 ~ 3

If the gap is larger than 2dB, your design might be failed in the Randomness test.

Measured SNDR boost for case M = 1: 6.0301dB

Ideal SNDR boost for case M = 1: 6.0000dB

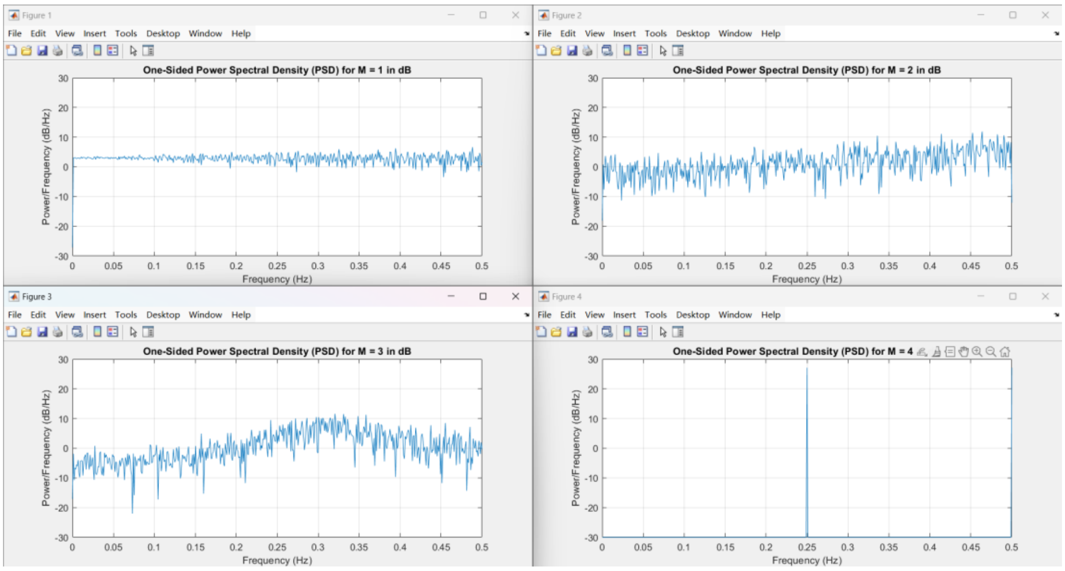
Measured SNDR boost for case M = 2: 9.7499dB

Ideal SNDR boost for case M = 2: 8.8628dB

Measured SNDR boost for case M = 3: 13.0931dB

Ideal SNDR boost for case M = 3: 13.1330dB

圖(六十七)、The result of functional correctness of SF postsim@0. 51GHz。



圖（六十八）、The result of functional correctness of SF postsim@0.51GHz。

- Spect table

SPEC Table					
Power Supply ($\leq$ 1.8) (V)	1.8V				
Layout Area (um^2)	1226.034				
Layout aspect ratio ($\leq$ 3)	1.278				
FoM = $\sqrt{\text{Area(um}^2\text{)}} \times \frac{\text{Power(uW)}}{F_{CLK}{}^2\text{(MHz}^2\text{)}}$ (post-sim, TT)	0.069				
Pre-sim	TT	FF	SS	FS	SF
Max. freq. (MHz)	800				
Power (uW)	644.283	672.521	697.704	676.325	685.378
Functional Work? (pass / M = X failed)	pass	pass	pass	pass	pass
Post-sim	TT	FF	SS	FS	SF
Max. freq. (MHz)	510				
Power (uW)	508.794	530.446	530.834	519.420	539.930
Functional Work? (pass / M = X failed)	pass	pass	pass	pass	pass

圖（六十九）、SPEC Table

- Discussion

(i)面積：

為了縮減電路面積，除了簡化電路邏輯，在 Layout 的時候也盡量以 minimum design rule 去佈線，這樣的優點是面積很小，缺點是容易使不同層的金屬層重疊，形成電容效應，使動態功耗及電路延遲上升。基於這樣的佈局，我們的電路在天梯中電路面積最小，但時鐘頻率跟功耗都不是最好。

(ii)Presim vs Postsim：

Presim 和 Postsim 的 PSD 圖和 Matlab 其他測試都會一模一樣，因為 LFSR 不是真隨機，會產生固定的序列。如果讓 Presim 和 Postsim 操作在相同的 CLK 頻率下，我們在 CLK frequency 為 0.5GHz 下，量測到 Presim 功耗大約是 0.3mW 的結果，比起 Postsim 低了不少，這可能是因為 Postsim 會考量實際電路的走線，提取電路寄生電阻跟電容，造成 Postsim 功耗上升。