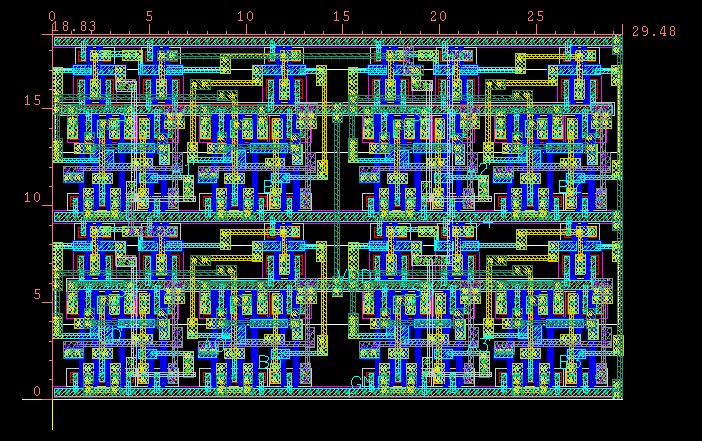
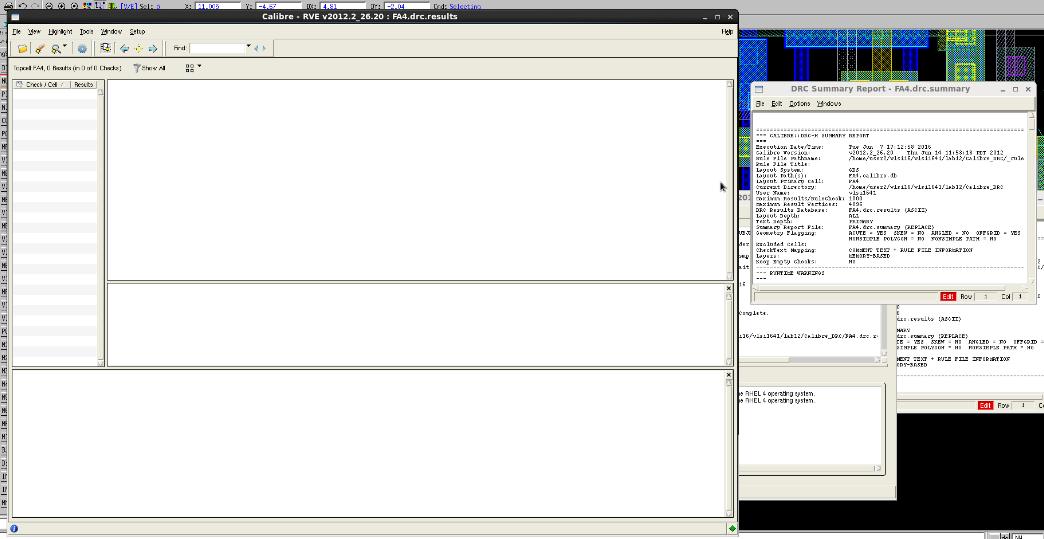
E24039122林韋儒

layout-FA4:

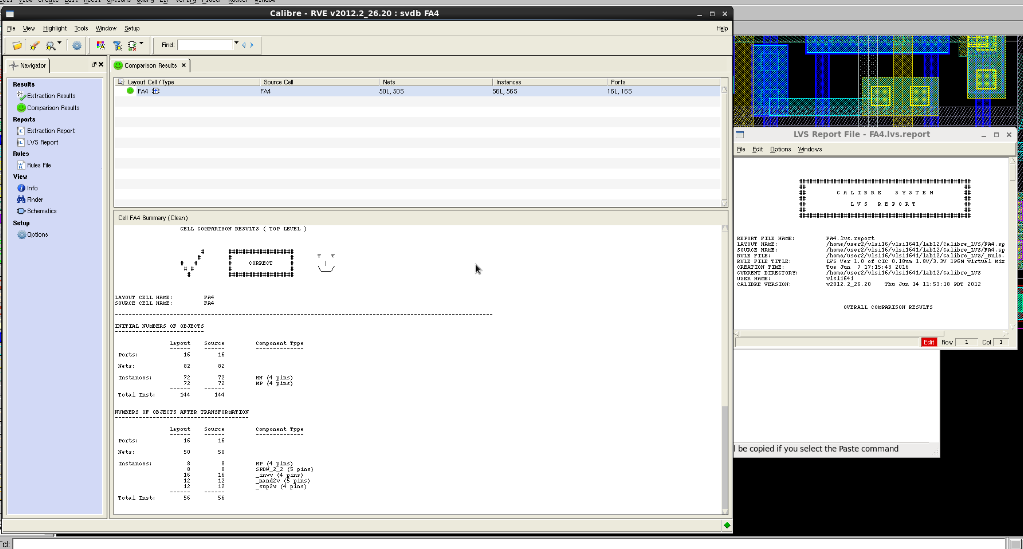


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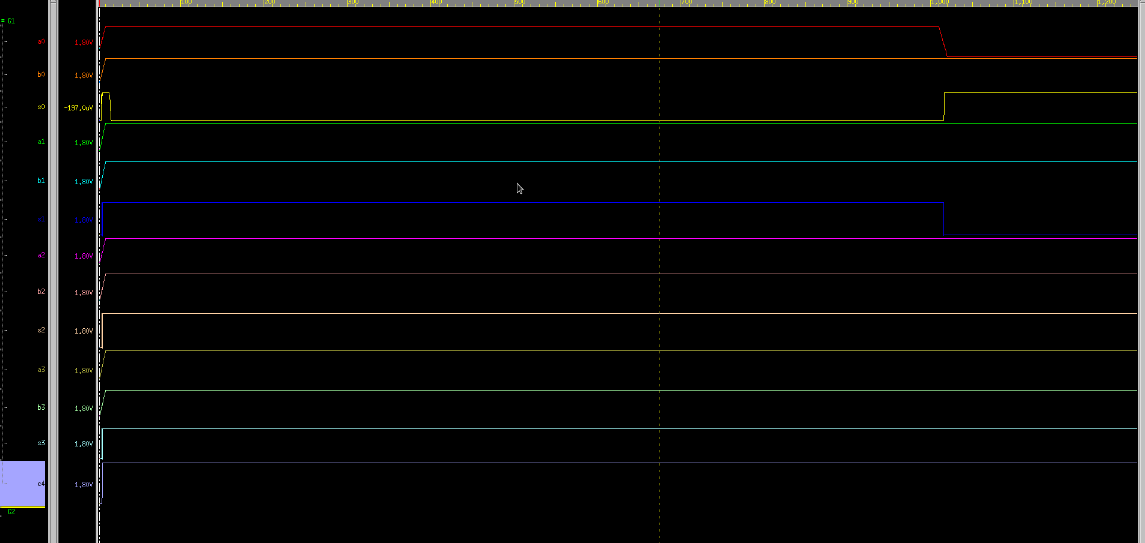
DRC- FA4

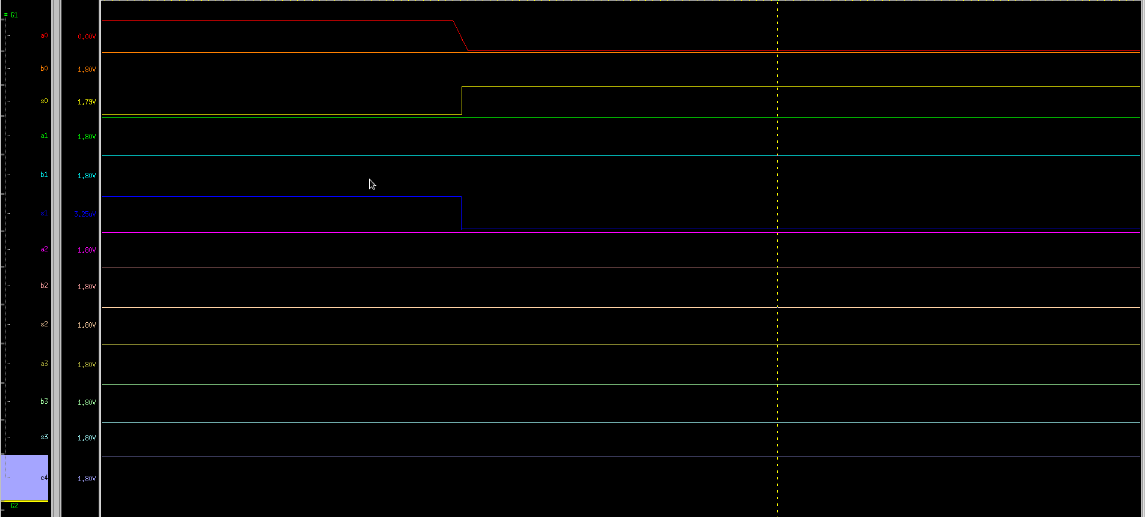
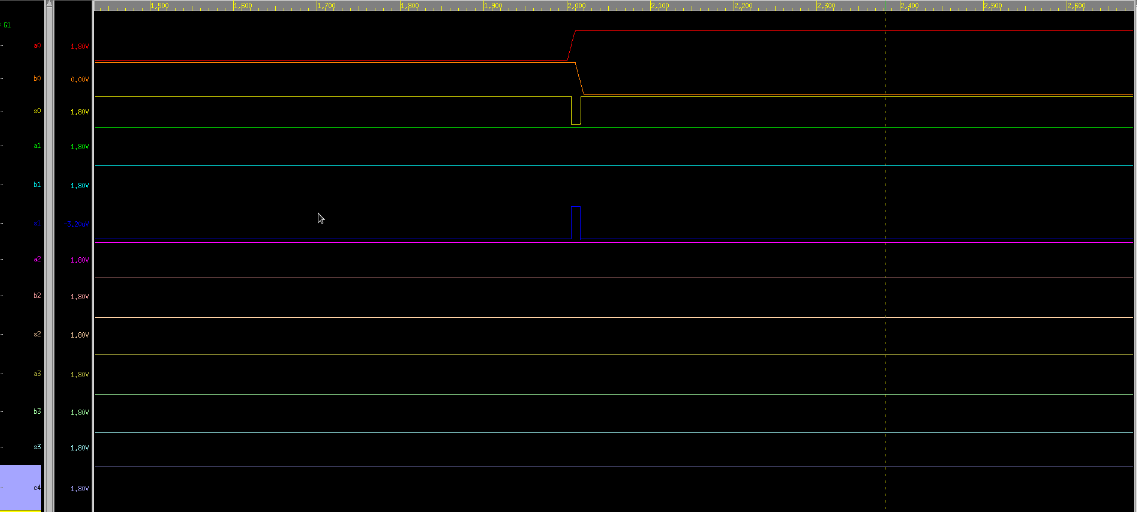
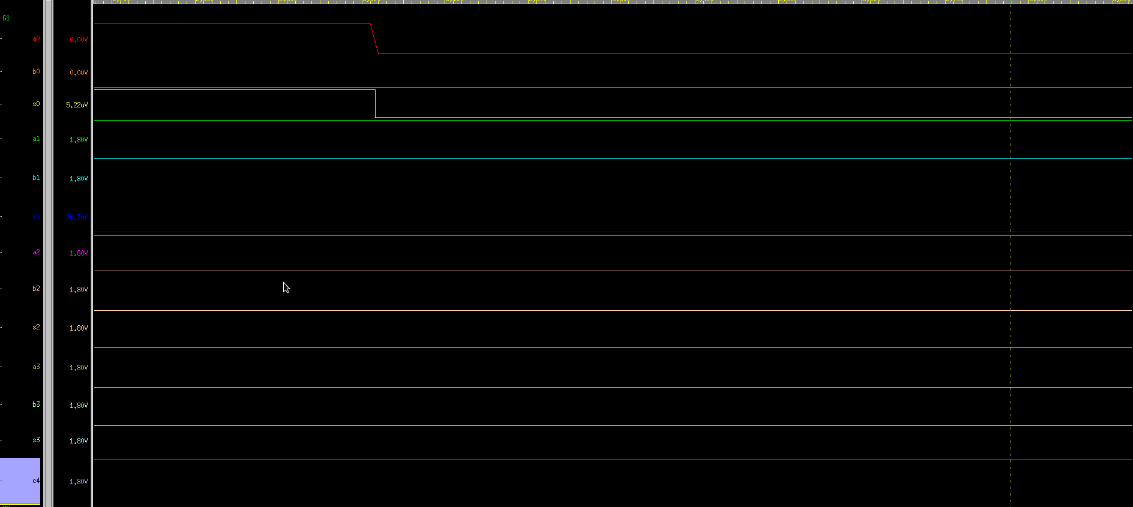
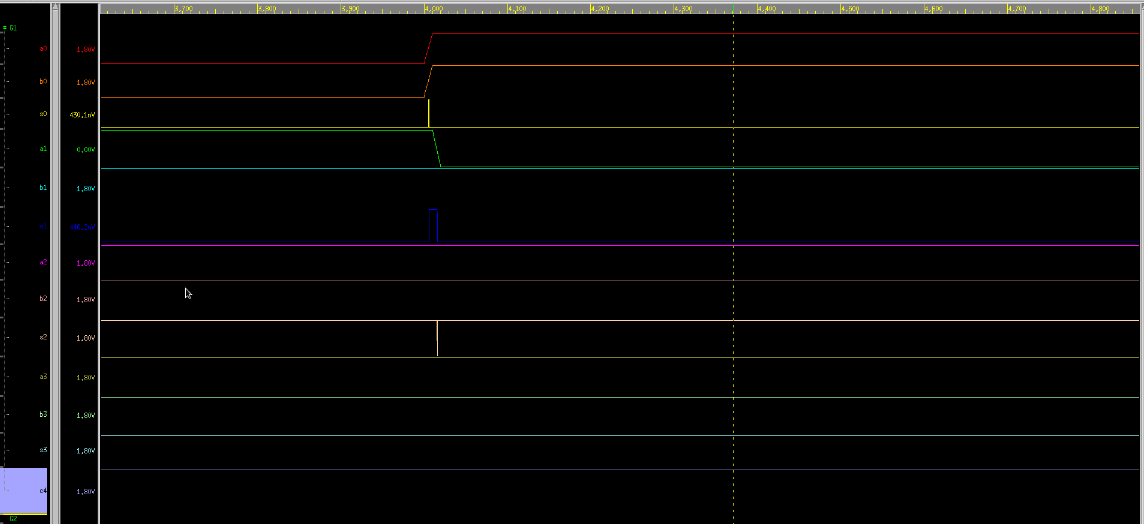
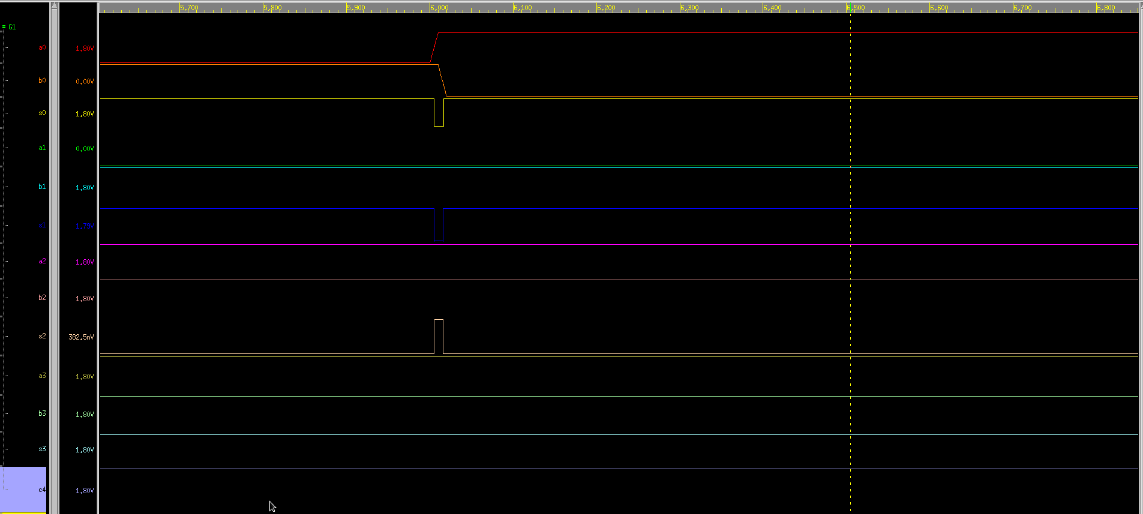
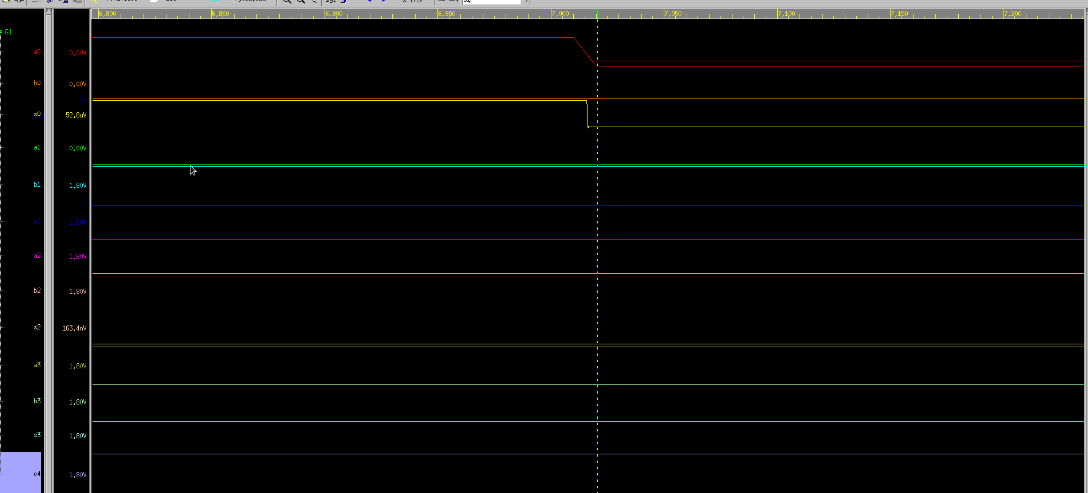
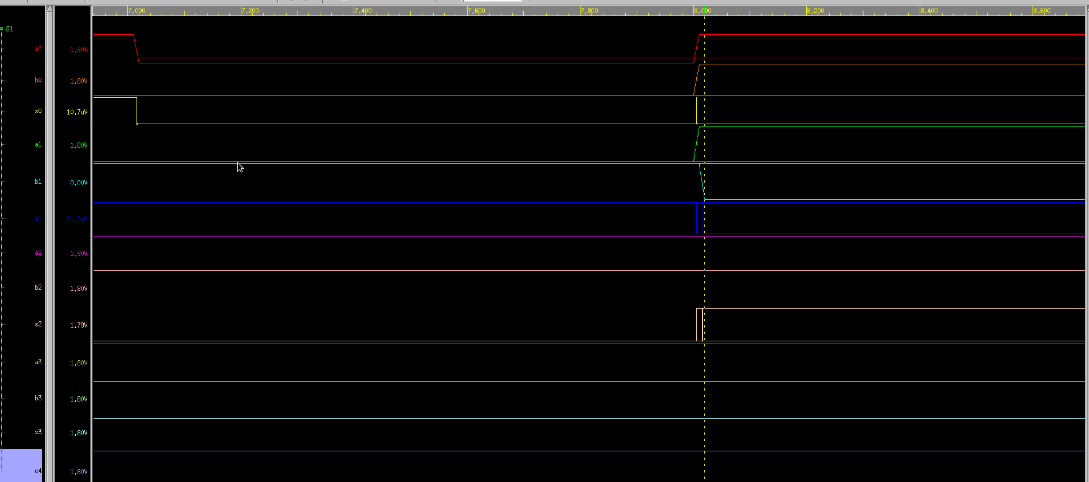
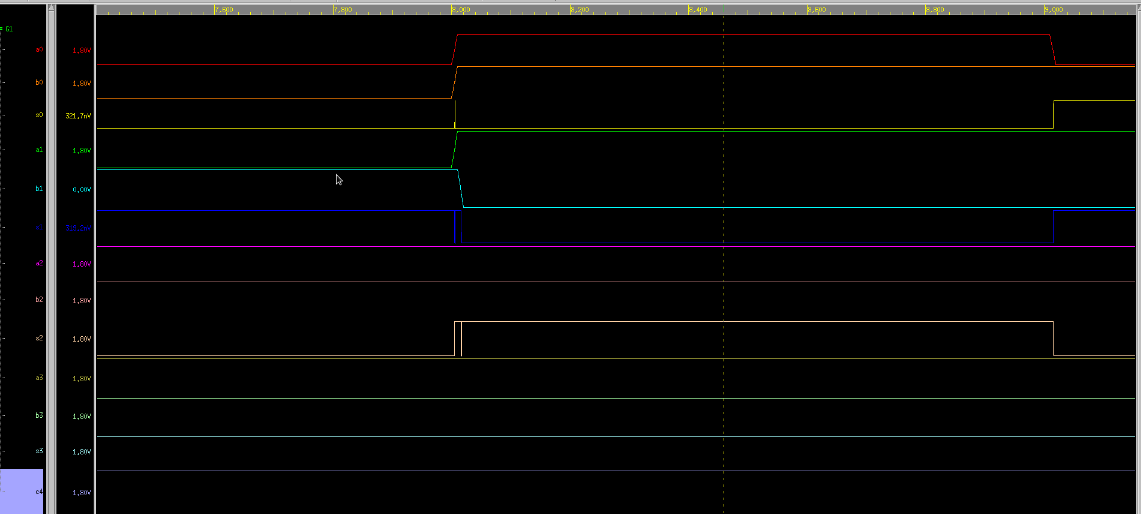
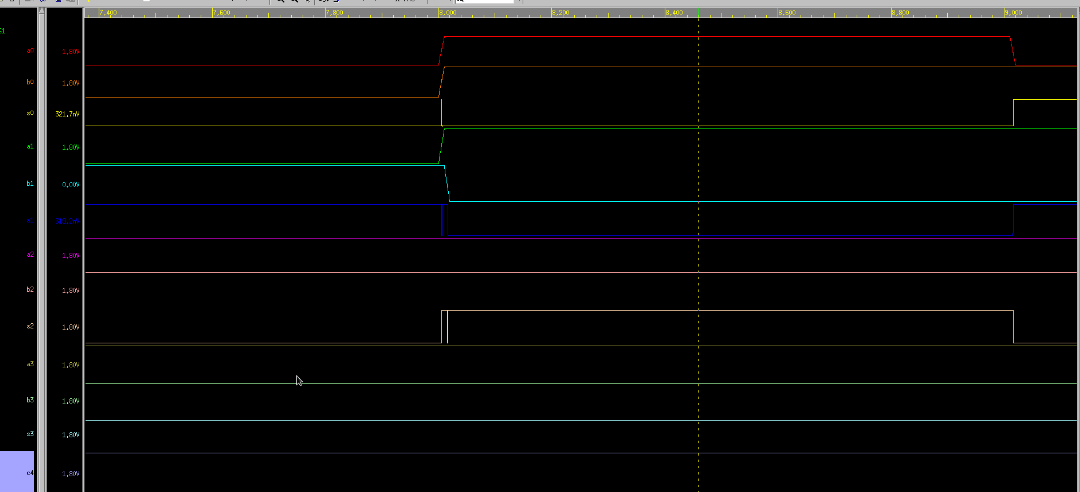
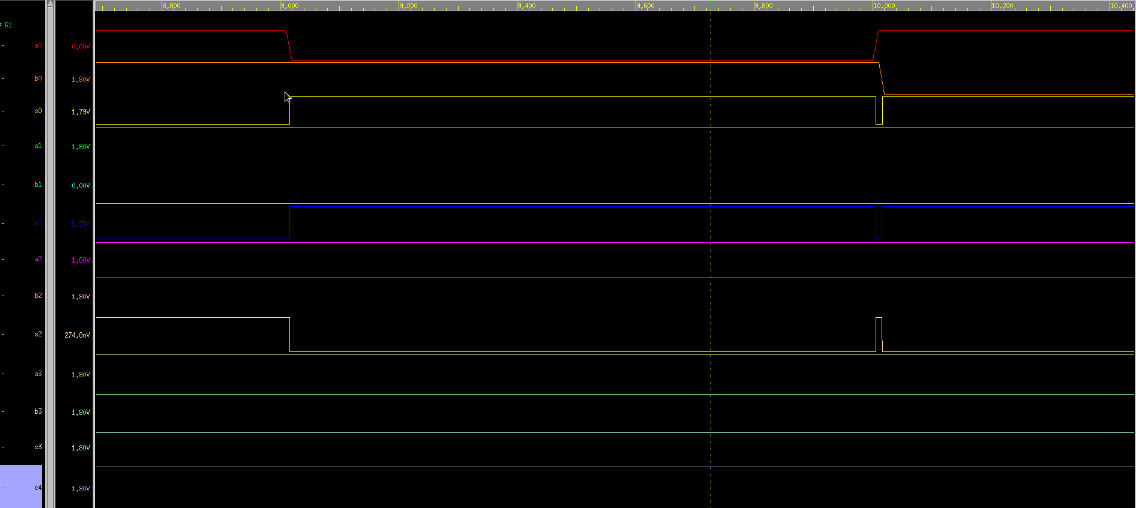


LVS-SMILE- FA4

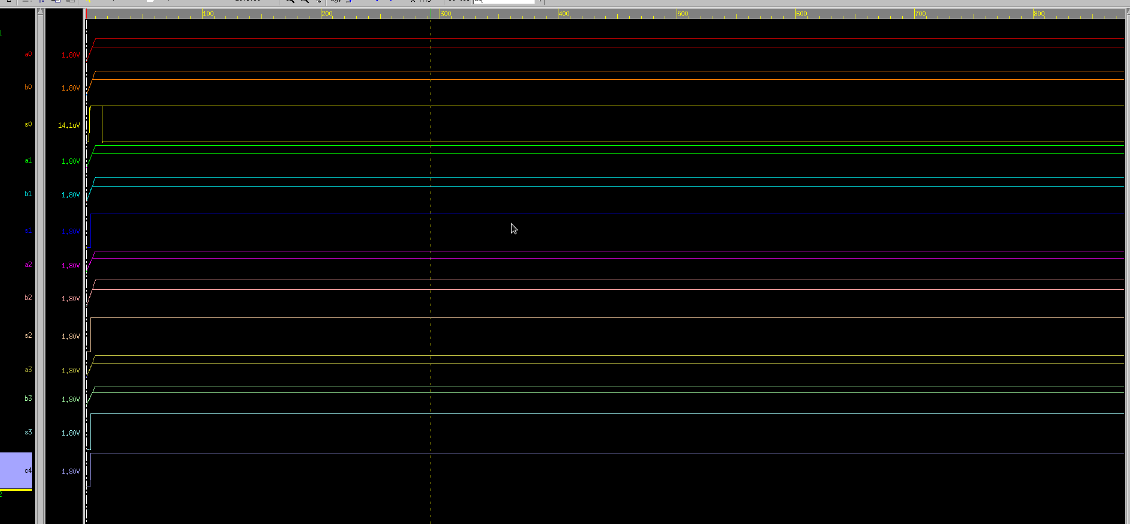
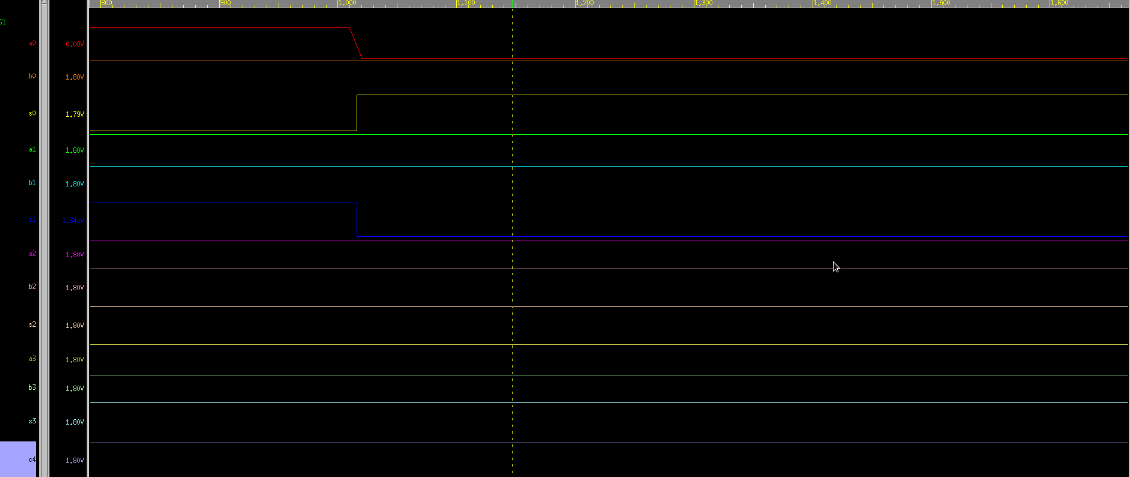
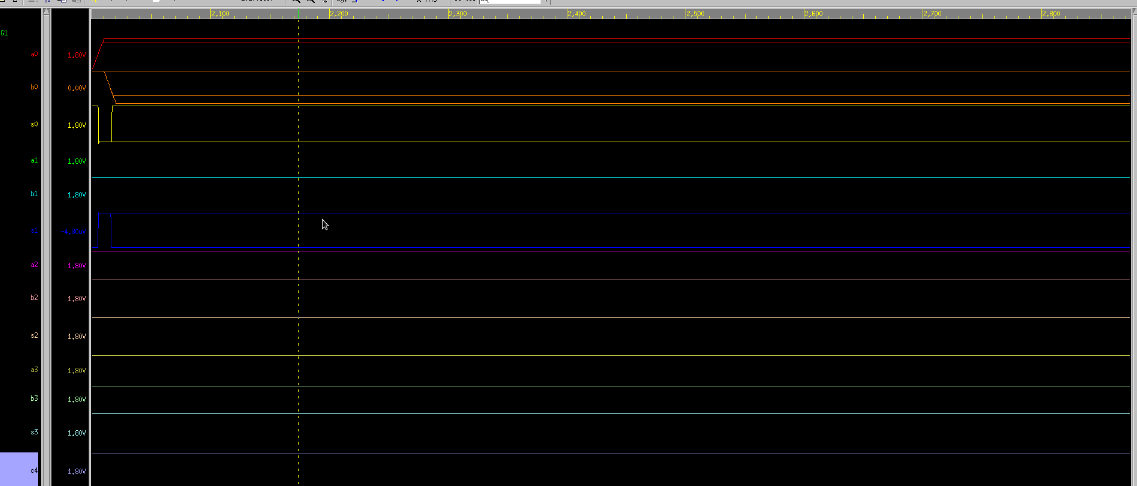
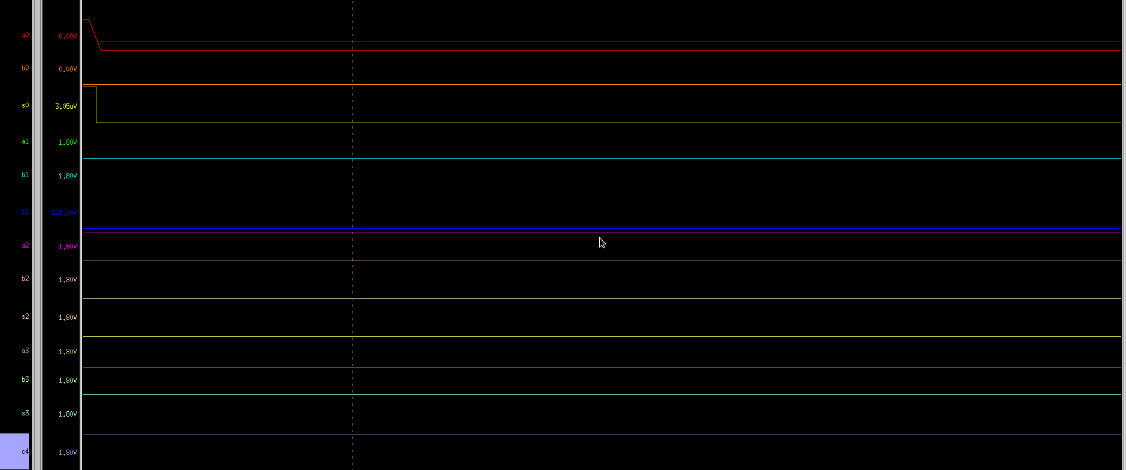
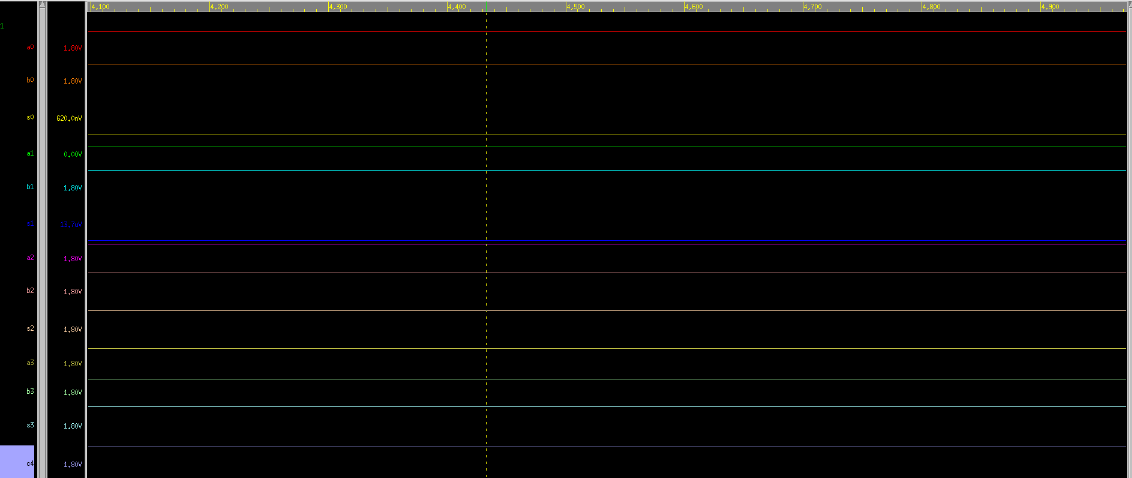
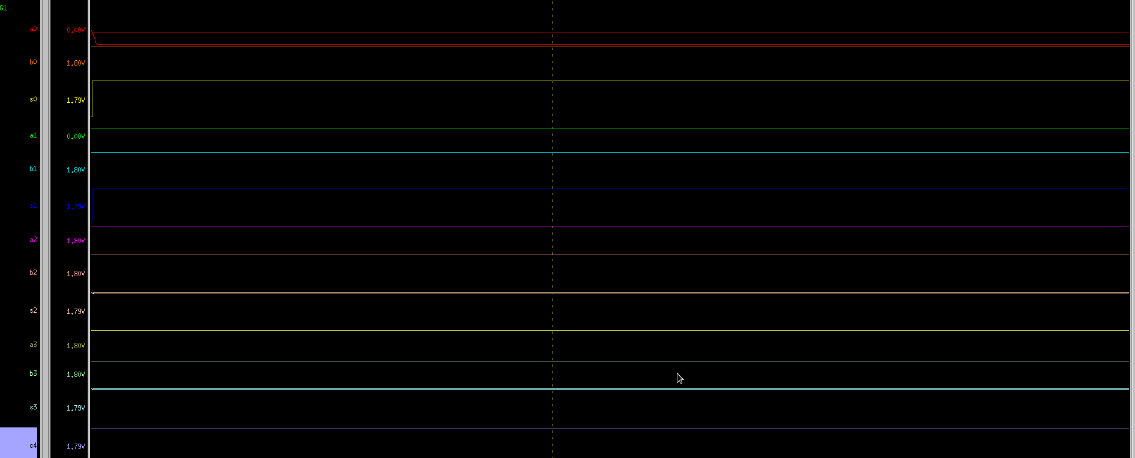
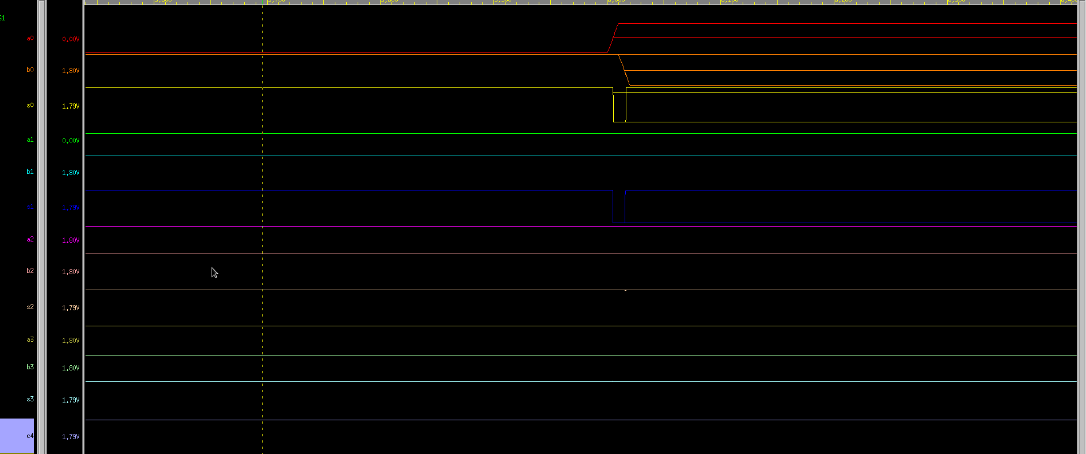
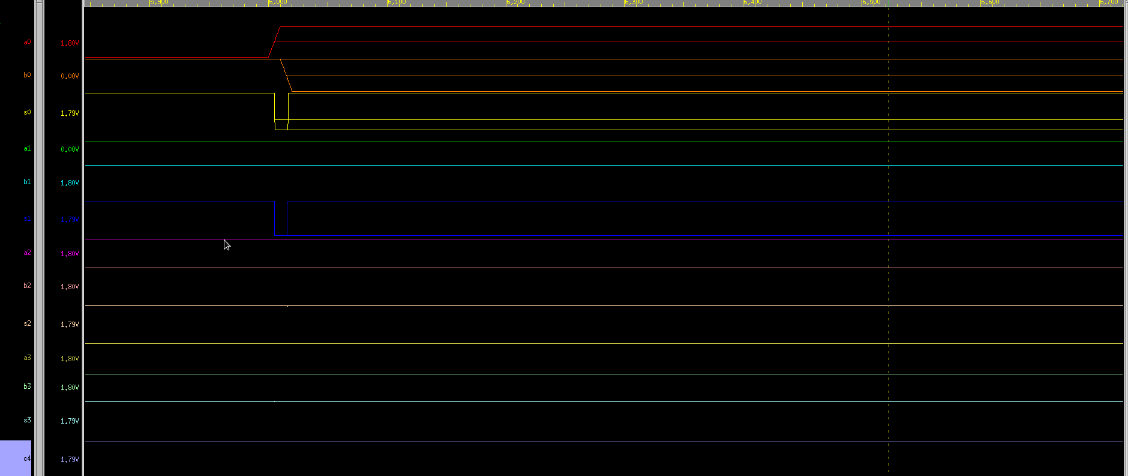
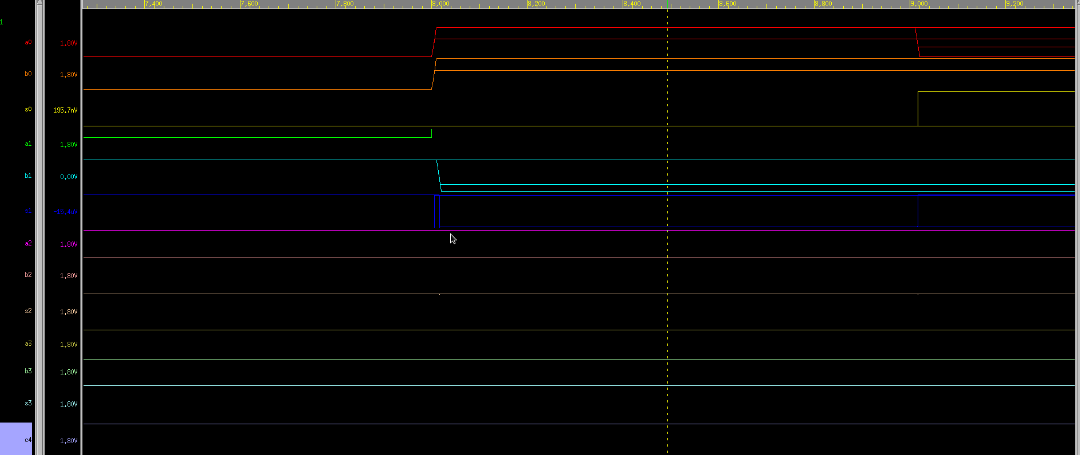
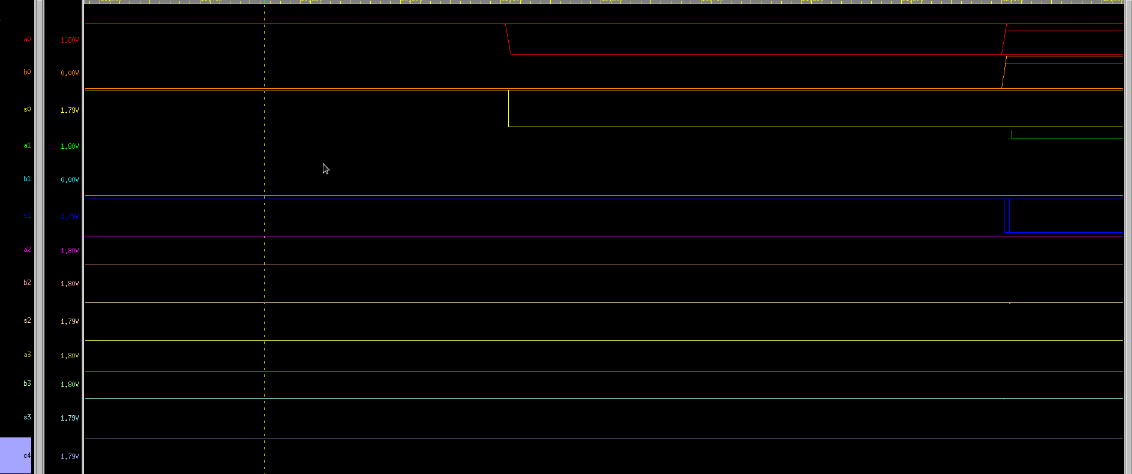
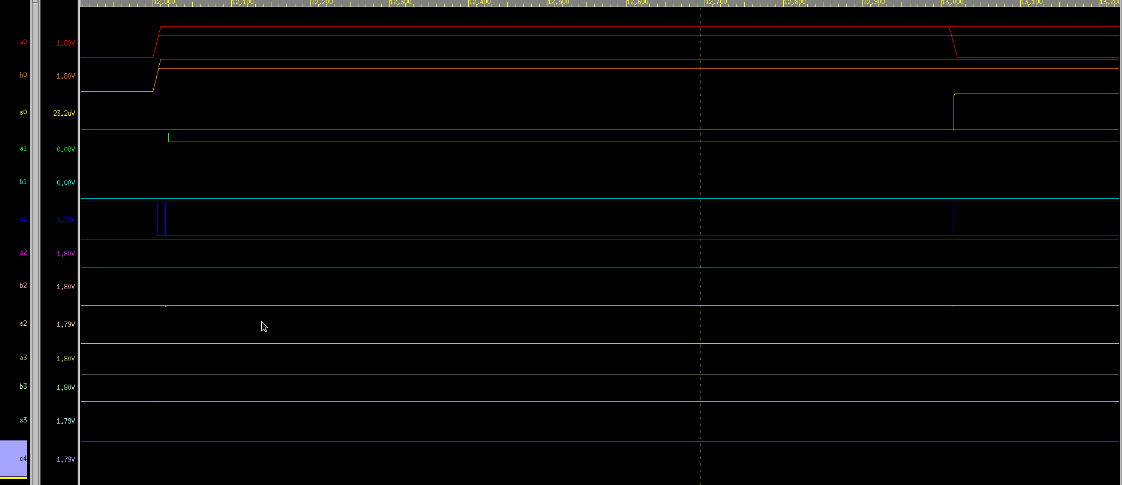
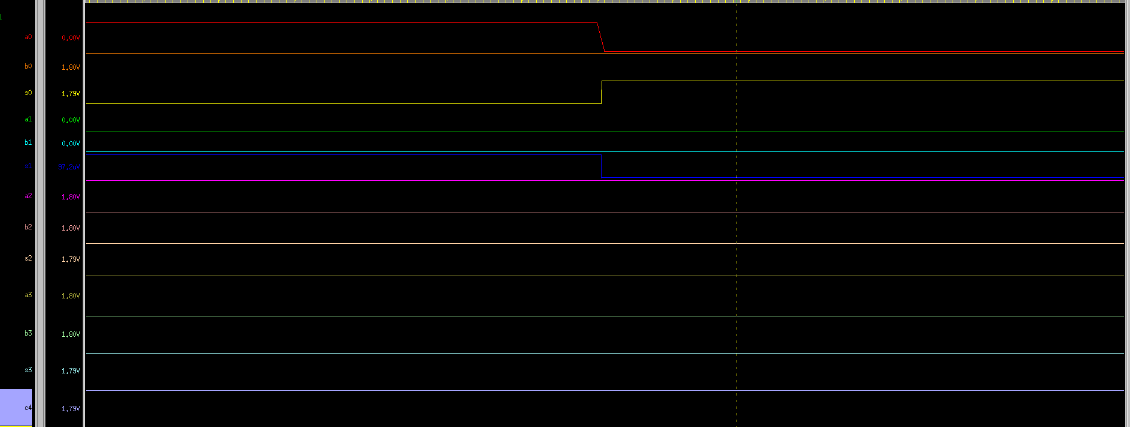
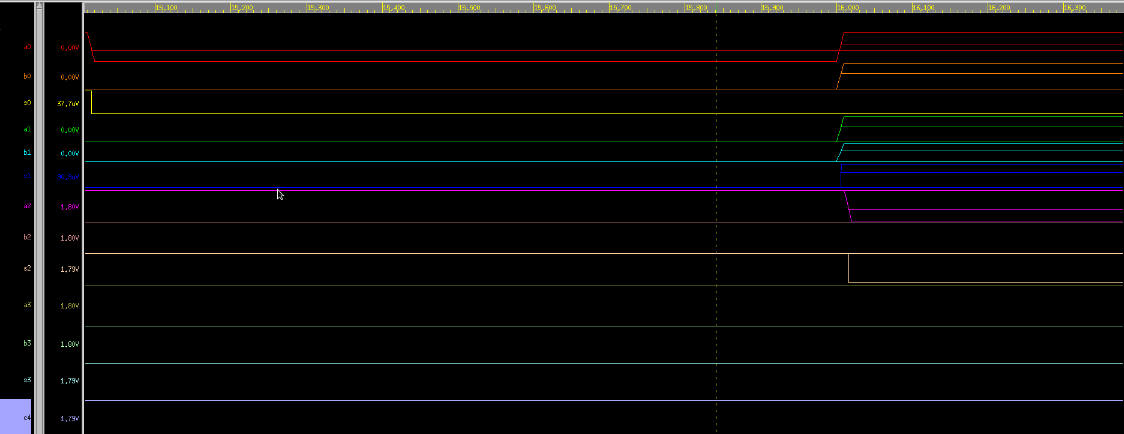


PRE - FA4



POST- FA4

PRE與POST比較起來,PRE輸出會多一根

心得:

繼上次用LAKER和HSPICE去跑模擬和畫LAYOUT,這次我覺得蠻順手的,但是要從單個邏輯閘到4-bitFULLADDER, 我覺得蠻困難的,雖然講義寫得很清楚,而且有介紹到如何畫LAYOUT和那些如何推導出圖形,但是我覺得蠻不容易拚湊出來,雖然花很多時間去熟悉這個程式,但是助教解說的蠻清楚的,讓我了解自己的缺陷,因此學到很多東西,感謝助教