**Table 15. Legend/abbreviations used in the pinout table (continued)**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in *Table 16* are: FT_f, FT_fa, FT_f, FT_fa.
2. The related I/O structures in *Table 16* are: FT_u.
3. The related I/O structures in *Table 16* are: FT_a, FT_fa, TT_a.

**Table 16. STM32L475xx pin definitions**

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 1 | PE2 | I/O | FT | - | TRACECK, TIM3_ETR, TSC_G7_IO1, FMC_A23, SAI1_MCLK_A, EVENTOUT | - |
| - | 2 | PE3 | I/O | FT | - | TRACED0, TIM3_CH1, TSC_G7_IO2, FMC_A19, SAI1_SD_B, EVENTOUT | - |
| - | 3 | PE4 | I/O | FT | - | TRACED1, TIM3_CH2, DFSDM1_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT | - |
| - | 4 | PE5 | I/O | FT | - | TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT | - |
| - | 5 | PE6 | I/O | FT | - | TRACED3, TIM3_CH4, FMC_A22, SAI1_SD_A, EVENTOUT | RTC_TAMP3/ WKUP3 |
| 1 | 6 | VBAT | S | - | - | - | - |
| 2 | 7 | PC13 | I/O | FT | (1) (2) | EVENTOUT | RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2 |
| 3 | 8 | PC14-OSC32_IN (PC14) | I/O | FT | (1) (2) | EVENTOUT | OSC32_IN |
| 4 | 9 | PC15-OSC32_OUT (PC15) | I/O | FT | (1) (2) | EVENTOUT | OSC32_OUT |
| - | 10 | VSS | S | - | - | - | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 11 | VDD | S | - | - | - | - |
| 5 | 12 | PH0-OSC_IN (PH0) | I/O | FT | - | EVENTOUT | OSC_IN |
| 6 | 13 | PH1-OSC_OUT (PH1) | I/O | FT | - | EVENTOUT | OSC_OUT |
| 7 | 14 | NRST | I/O | RST | - | - | - |
| 8 | 15 | PC0 | I/O | FT_fa | - | LPTIM1_IN1, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, LPTIM2_IN1, EVENTOUT | ADC123_IN1 |
| 9 | 16 | PC1 | I/O | FT_fa | - | LPTIM1_OUT, I2C3_SDA, DFSDM1_CKIN4, LPUART1_TX, EVENTOUT | ADC123_IN2 |
| 10 | 17 | PC2 | I/O | FT_a | - | LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, EVENTOUT | ADC123_IN3 |
| 11 | 18 | PC3 | I/O | FT_a | - | LPTIM1_ETR, SPI2_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT | ADC123_IN4 |
| - | 19 | VSSA | S | - | - | - | - |
| - | 20 | VREF- | S | - | - | - | - |
| 12 | - | VSSA/VREF- | S | - | - | - | - |
| - | 21 | VREF+ | S | - | - | - | VREFBUF_OUT |
| - | 22 | VDDA | S | - | - | - | - |
| 13 | - | VDDA/VREF+ | S | - | - | - | - |
| 14 | 23 | PA0 | I/O | FT_a | - | TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT | OPAMP1_VINP, ADC12_IN5, RTC_TAMP2/WKUP1 |
| 15 | 24 | PA1 | I/O | FT_a | - | TIM2_CH2, TIM5_CH2, USART2_RTS_DE, UART4_RX, TIM15_CH1N, EVENTOUT | OPAMP1_VINM, ADC12_IN6 |
| 16 | 25 | PA2 | I/O | FT_a | - | TIM2_CH3, TIM5_CH3, USART2_TX, SAI2_EXTCLK, TIM15_CH1, EVENTOUT | ADC12_IN7, WKUP4/LSCO |
| 17 | 26 | PA3 | I/O | TT_a | - | TIM2_CH4, TIM5_CH4, USART2_RX, TIM15_CH2, EVENTOUT | OPAMP1_ VOUT, ADC12_IN8 |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 18 | 27 | VSS | S | - | - | - | - |
| 19 | 28 | VDD | S | - | - | - | - |
| 20 | 29 | PA4 | I/O | TT_a | - | SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT | ADC12_IN9, DAC1_OUT1 |
| 21 | 30 | PA5 | I/O | TT_a | - | TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT | ADC12_IN10, DAC1_OUT2 |
| 22 | 31 | PA6 | I/O | FT_a | - | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, USART3_CTS, QUADSPI_BK1_IO3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT | OPAMP2_VINP, ADC12_IN11 |
| 23 | 32 | PA7 | I/O | FT_a | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, QUADSPI_BK1_IO2, TIM17_CH1, EVENTOUT | OPAMP2_VINM, ADC12_IN12 |
| 24 | 33 | PC4 | I/O | FT_a | - | USART3_TX, EVENTOUT | COMP1_INM, ADC12_IN13 |
| 25 | 34 | PC5 | I/O | FT_a | - | USART3_RX, EVENTOUT | COMP1_INP, ADC12_IN14, WKUP5 |
| 26 | 35 | PB0 | I/O | TT_a | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, USART3_CK, QUADSPI_BK1_IO1, COMP1_OUT, EVENTOUT | OPAMP2_ VOUT, ADC12_IN15 |
| 27 | 36 | PB1 | I/O | FT_a | - | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, QUADSPI_BK1_IO0, LPTIM2_IN1, EVENTOUT | COMP1_INM, ADC12_IN16 |
| 28 | 37 | PB2 | I/O | FT_a | - | RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, EVENTOUT | COMP1_INP |
| - | 38 | PE7 | I/O | FT | - | TIM1_ETR, DFSDM1_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT | - |
| - | 39 | PE8 | I/O | FT | - | TIM1_CH1N, DFSDM1_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 40 | PE9 | I/O | FT | - | TIM1_CH1, DFSDM1_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT | - |
| - | 41 | PE10 | I/O | FT | - | TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, FMC_D7, QUADSPI_CLK, SAI1_MCLK_B, EVENTOUT | - |
| - | 42 | PE11 | I/O | FT | - | TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, QUADSPI_NCS, FMC_D8, EVENTOUT | - |
| - | 43 | PE12 | I/O | FT | - | TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT | - |
| - | 44 | PE13 | I/O | FT | - | TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT | - |
| - | 45 | PE14 | I/O | FT | - | TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT | - |
| - | 46 | PE15 | I/O | FT | - | TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT | - |
| 29 | 47 | PB10 | I/O | FT_f | - | TIM2_CH3, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, QUADSPI_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT | - |
| 30 | 48 | PB11 | I/O | FT_f | - | TIM2_CH4, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_NCS, COMP2_OUT, EVENTOUT | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 31 | 49 | VSS | S | - | - | - | - |
| 32 | 50 | VDD | S | - | - | - | - |
| 33 | 51 | PB12 | I/O | FT | - | TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT | - |
| 34 | 52 | PB13 | I/O | FT_f | - | TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM1_CKIN1, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, SWPMI1_TX, SAI2_SCK_A, TIM15_CH1N, EVENTOUT | - |
| 35 | 53 | PB14 | I/O | FT_f | - | TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS_DE, TSC_G1_IO3, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT | - |
| 36 | 54 | PB15 | I/O | FT | - | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT | - |
| - | 55 | PD8 | I/O | FT | - | USART3_TX, FMC_D13, EVENTOUT | - |
| - | 56 | PD9 | I/O | FT | - | USART3_RX, FMC_D14, SAI2_MCLK_A, EVENTOUT | - |
| - | 57 | PD10 | I/O | FT | - | USART3_CK, TSC_G6_IO1, FMC_D15, SAI2_SCK_A, EVENTOUT | - |
| - | 58 | PD11 | I/O | FT | - | USART3_CTS, TSC_G6_IO2, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 59 | PD12 | I/O | FT | - | TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT | - |
| - | 60 | PD13 | I/O | FT | - | TIM4_CH2, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT | - |
| - | 61 | PD14 | I/O | FT | - | TIM4_CH3, FMC_D0, EVENTOUT | - |
| - | 62 | PD15 | I/O | FT | - | TIM4_CH4, FMC_D1, EVENTOUT | - |
| 37 | 63 | PC6 | I/O | FT | - | TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT | - |
| 38 | 64 | PC7 | I/O | FT | - | TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, TSC_G4_IO2, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT | - |
| 39 | 65 | PC8 | I/O | FT | - | TIM3_CH3, TIM8_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT | - |
| 40 | 66 | PC9 | I/O | FT | - | TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT | - |
| 41 | 67 | PA8 | I/O | FT | - | MCO, TIM1_CH1, USART1_CK, OTG_FS_SOF, LPTIM2_OUT, EVENTOUT | - |
| 42 | 68 | PA9 | I/O | FT_u | - | TIM1_CH2, USART1_TX, TIM15_BKIN, EVENTOUT | OTG_FS_VBUS |
| 43 | 69 | PA10 | I/O | FT_u | - | TIM1_CH3, USART1_RX, OTG_FS_ID, TIM17_BKIN, EVENTOUT | - |
| 44 | 70 | PA11 | I/O | FT_u | - | TIM1_CH4, TIM1_BKIN2, USART1_CTS, CAN1_RX, OTG_FS_DM, TIM1_BKIN2_COMP1, EVENTOUT | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 45 | 71 | PA12 | I/O | FT_u | - | TIM1_ETR, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT | - |
| 46 | 72 | PA13 (JTMS-SWDIO) | I/O | FT | (3) | JTMS-SWDIO, IR_OUT, OTG_FS_NOE, EVENTOUT | - |
| 47 | - | VSS | S | - | - | - | - |
| 48 | 73 | VDDUSB | S | - | - | - | - |
| - | 74 | VSS | S | - | - | - | - |
| - | 75 | VDD | S | - | - | - | - |
| 49 | 76 | PA14 (JTCK-SWCLK) | I/O | FT | (3) | JTCK-SWCLK, EVENTOUT | - |
| 50 | 77 | PA15 (JTDI) | I/O | FT | (3) | JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, SPI3_NSS, UART4_RTS_DE, TSC_G3_IO1, SAI2_FS_B, EVENTOUT | - |
| 51 | 78 | PC10 | I/O | FT | - | SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, SAI2_SCK_B, EVENTOUT | - |
| 52 | 79 | PC11 | I/O | FT | - | SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT | - |
| 53 | 80 | PC12 | I/O | FT | - | SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, SDMMC1_CK, SAI2_SD_B, EVENTOUT | - |
| - | 81 | PD0 | I/O | FT | - | SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, FMC_D2, EVENTOUT | - |
| - | 82 | PD1 | I/O | FT | - | SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, FMC_D3, EVENTOUT | - |
| 54 | 83 | PD2 | I/O | FT | - | TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, SDMMC1_CMD, EVENTOUT | - |

Table 16. STM32L475xx pin definitions (continued)

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| - | 84 | PD3 | I/O | FT | - | SPI2_MISO, DFSDM1_DATIN0, USART2_CTS, FMC_CLK, EVENTOUT | - |
| - | 85 | PD4 | I/O | FT | - | SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, FMC_NOE, EVENTOUT | - |
| - | 86 | PD5 | I/O | FT | - | USART2_TX, FMC_NWE, EVENTOUT | - |
| - | 87 | PD6 | I/O | FT | - | DFSDM1_DATIN1, USART2_RX, FMC_NWAIT, SAI1_SD_A, EVENTOUT | - |
| - | 88 | PD7 | I/O | FT | - | DFSDM1_CKIN1, USART2_CK, FMC_NE1, EVENTOUT | - |
| 55 | 89 | PB3 (JTDO-TRACESWO) | I/O | FT_a | (3) | JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, SAI1_SCK_B, EVENTOUT | COMP2_INM |
| 56 | 90 | PB4 (NJTRST) | I/O | FT_a | (3) | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS_DE, TSC_G2_IO1, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT | COMP2_INP |
| 57 | 91 | PB5 | I/O | FT_a | - | LPTIM1_IN1, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT | - |
| 58 | 92 | PB6 | I/O | FT_fa | - | LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, DFSDM1_DATIN5, USART1_TX, TSC_G2_IO3, TIM8_BKIN2_COMP2, SAI1_FS_B, TIM16_CH1N, EVENTOUT | COMP2_INP |

**Table 16. STM32L475xx pin definitions (continued)**

| Pin Number | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | | | | | Alternate functions | Additional functions |
| 59 | 93 | PB7 | I/O | FT_fa | - | LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, DFSDM1_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, FMC_NL, TIM8_BKIN_COMP1, TIM17_CH1N, EVENTOUT | COMP2_INM, PVD_IN |
| 60 | 94 | BOOT0 | I | - | - | - | - |
| 61 | 95 | PB8 | I/O | FT_f | - | TIM4_CH3, I2C1_SCL, DFSDM1_DATIN6, CAN1_RX, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT | - |
| 62 | 96 | PB9 | I/O | FT_f | - | IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM1_CKIN6, CAN1_TX, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT | - |
| - | 97 | PE0 | I/O | FT | - | TIM4_ETR, FMC_NBL0, TIM16_CH1, EVENTOUT | - |
| - | 98 | PE1 | I/O | FT | - | FMC_NBL1, TIM17_CH1, EVENTOUT | - |
| 63 | 99 | VSS | S | - | - | - | - |
| 64 | 100 | VDD | S | - | - | - | - |

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0351 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.