EEL2020 Digital Design Lab Report
Sem II AY 2023-24

Experiment No.	:	**01**
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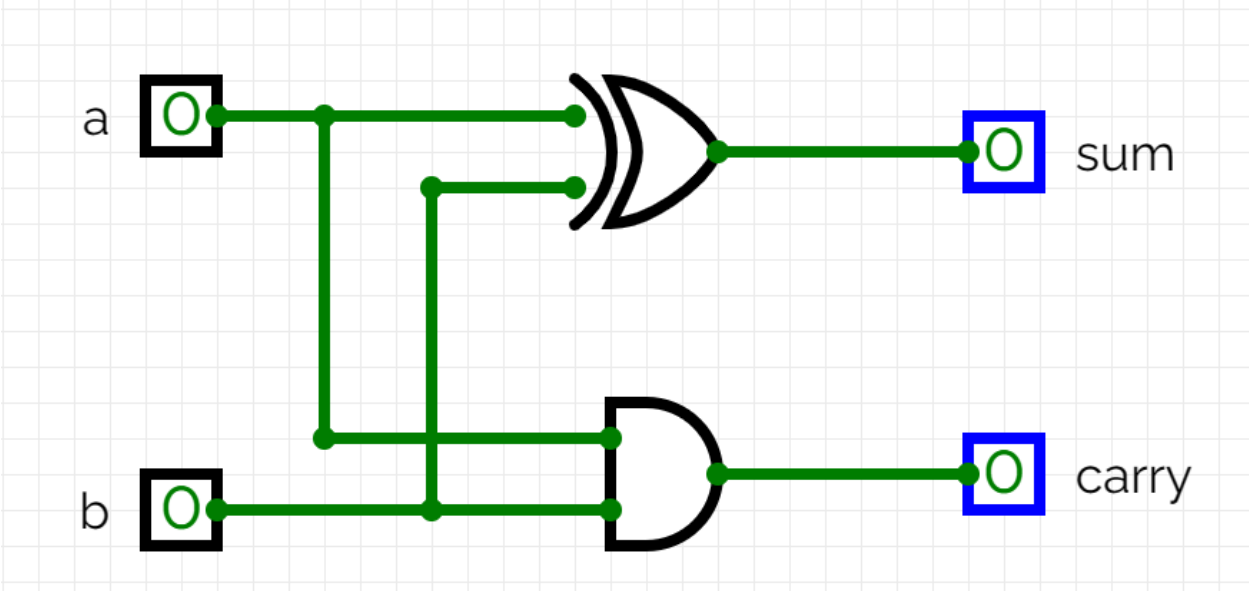
Objective

Implement a half-adder on the PYNQ Z2 FPGA board using Verilog through the Vivado Design Suite.

Logic Design



Made using circuitverse.org

Source Description

- Design source

The source file is a half_adder module that generates an output carry and sum from inputs a, b.

- Constraint file

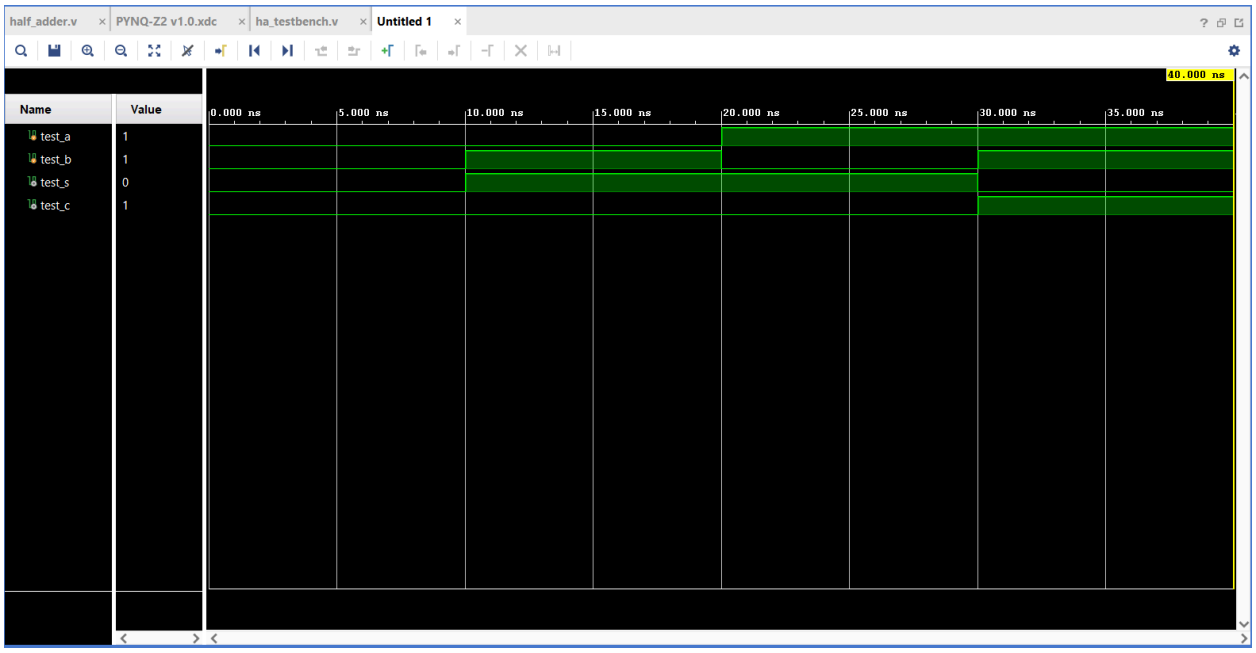
The XDC file was updated with the following changes:

Ports (from Verilog module)	**Designation** (Input/Output)	PYNQ Component Type (Button/LED/Switch etc. along with number, eg. LD01, BTN2, etc.)	Pin Configuration (from the PYNQ User Manual)
a	Input	SW1	M19
b	Input	SW0	M20
s	Output	LED0	R14
c	Output	LED1	P14

- Simulation source

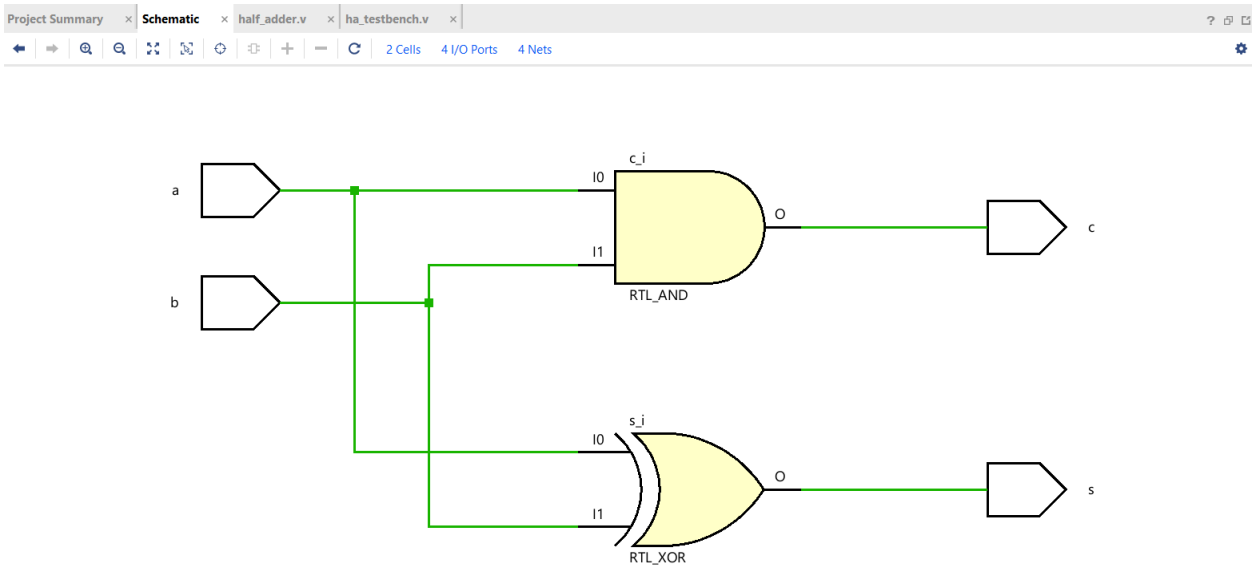
We have used a test bench for the input cases 00, 01, 10, 11 each that runs for 10 ns.

Simulation Results (Timing diagram)



Expected Truth Table				From the Timing Diagram			
a	***b***	***c***	***s***	***a***	***b***	***c***	***s***
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**
1	**0**	**0**	**1**	**1**	**0**	**0**	**1**
1	**1**	**1**	**0**	**1**	**1**	**1**	**0**

Elaborated Design



The circuit diagram created by vivado matches the expected circuit diagram.

PYNQ Working Video

🗀 Lab 01

This is the link to the Google Drive where all relevant documents are uploaded, including the codes folder, the working video, this report, and the images attached in this report.

List of Attachments

The following files are included in the zipped folder submitted along with this report in GC:-

1) half_adder.v – the half adder module
2) ha_testbench.v – the test bench
3) Constraints file