Yongru Pan

261001758

Chenyi Xu

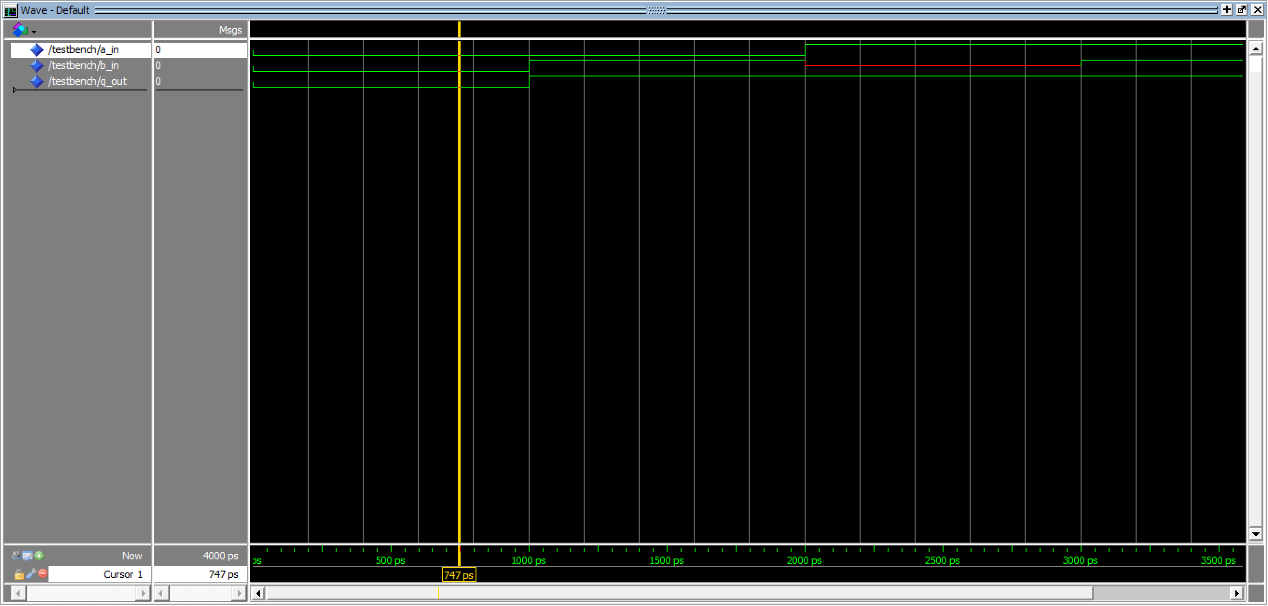
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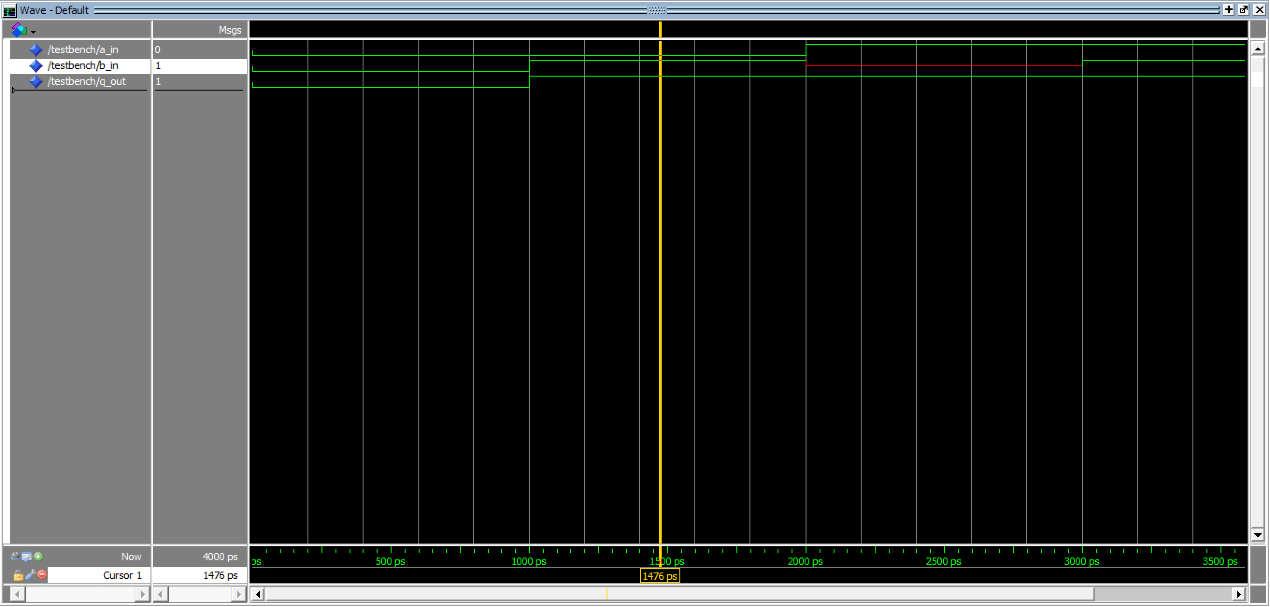
**VHDL 1 lab report**

**Executive Summary**

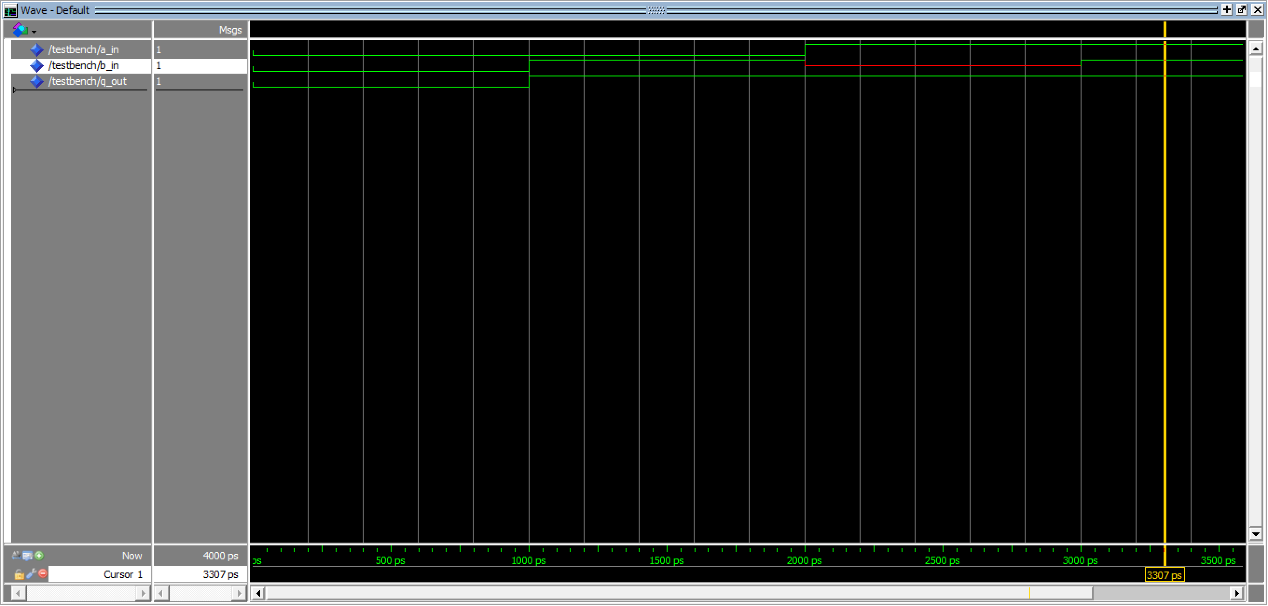
The simulation was designed to compile the or gate and the testbench code to produce the simulation of a simple OR gate and test it using the testbench code. There are two inputs to be a and b respectively and an output of q. Testbench is used to test whether the simulation is an or gate. When the inputs are both 0, output should be 0. When any one of the two inputs are 1, output is 1. When the inputs are both 1, output should be 1. When the above conditions are satisfied, the simulation is confirmed to be the OR gate and will be displayed on the window by using the RTL viewer.

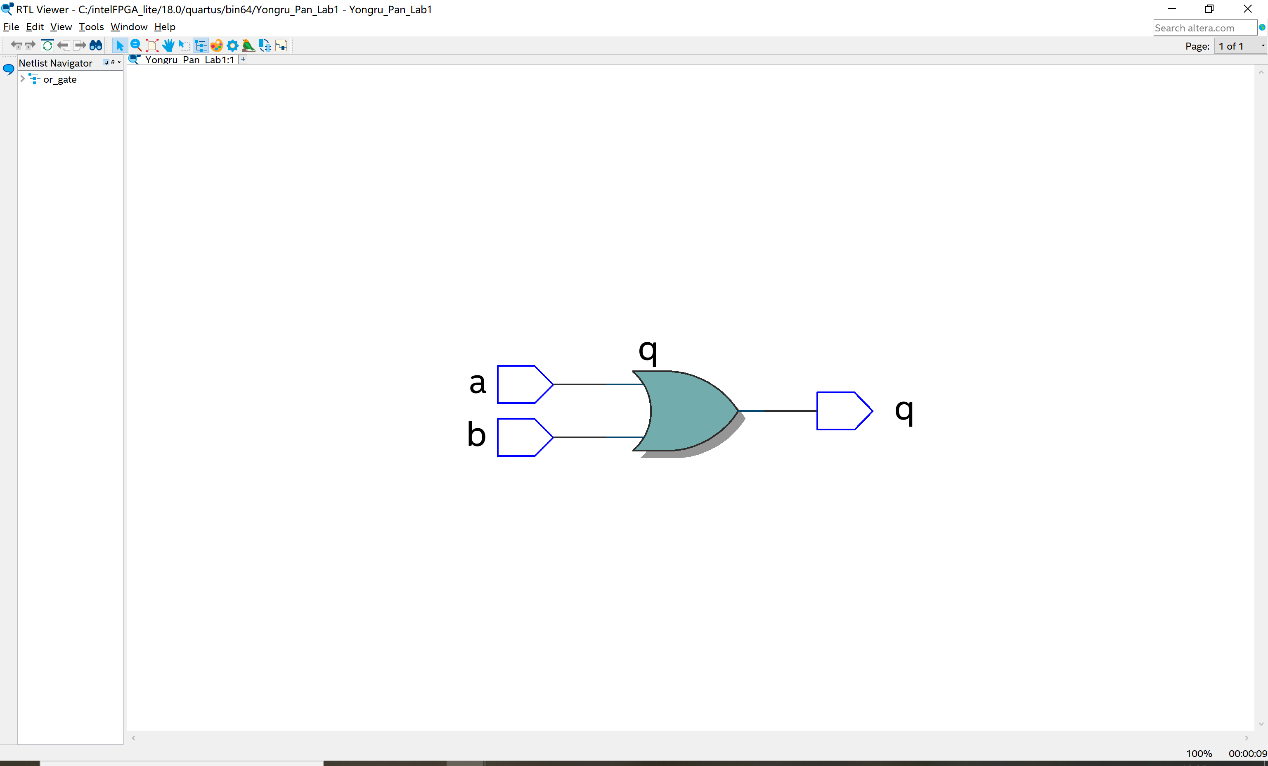
**Legible Figures**











**Explanation of the Results Obtained in the Assignments**

The result matches the conditions of an OR gate. An OR gate is successfully produced. Based on the testbench, when a and b are both 0, q is 0. When a is zero and b is 1, q is 1. When a is 1 and b is X, q is 1. When a is 1 and b is 1, q is 1. When a is 0 and b is 0, q is 0.

**Conclusions**

The simulation code is an OR gate simulation and prove by the testbench code.