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**Executive Summary**

For the first part of the VHDL assignment, we drew a 4-bit comparator circuit. It has 4-bit inputs and a single 1-bit output. Since ModelSim does not understand the schematic diagrams we designed, Quartus was used to convert it to a VHDL description file. A template of the testbench file was attained from Quartus and replaced the always part with the code provided. Run the simulations in ModelSim and add the for-loop code provided in order to run through all 256 cases. In the second part of the assignment, both a structural and behavioral design of 2-1 MUX are written with a testbench respectively to simulate plots in ModelSim.

**Response to answers**

1: Explanation for Code

*Part1*

Code for part 1 is autogenerated from the schematic file. Parts of testbench is generated with the testbench writer in Quartus and the other parts are given by instruction

*Part2*

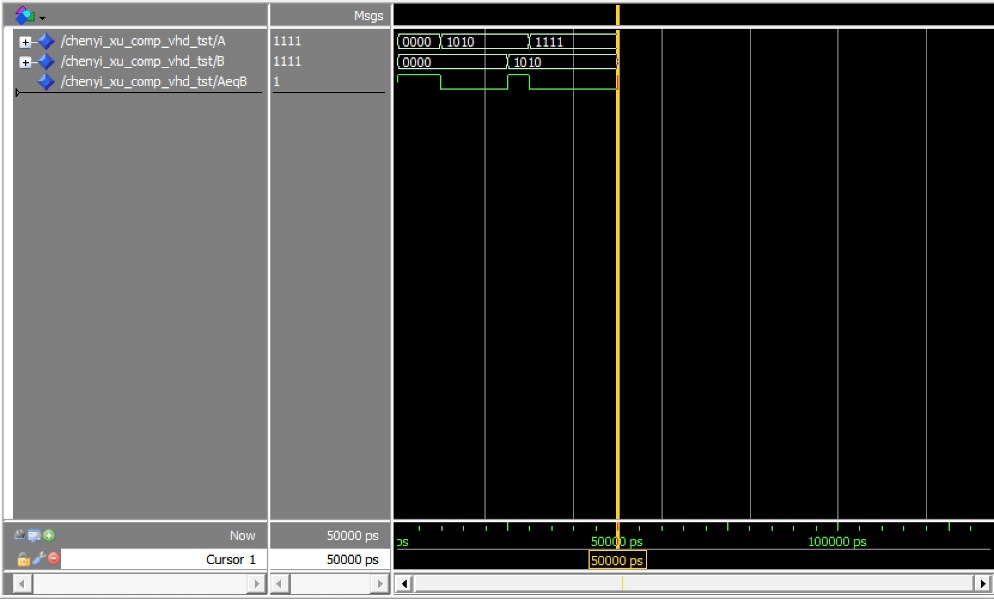
A digital system can be represented behaviorally and structurally. Behavioral describes the interconnection between each component while a structural describes the relationship between input and output. Import library we need at the start of each file. VHDL code always starts with entity declaration and follows by the architecture part that describes the functionality of it. Each design file has a testbench file which contains its instantiation of its top-level design entity and simulate input and output vectors

Followed by the step of part 1, the structural code of 2 to 1 mux is created from the schematic form and the testbench is autogenerated by Quartus. Then the always process is replaced by a newly written part to suit the need of the structural design. All the possible combinations are included in the testbench. Compile both the structural design file and the testbench file in ModelSim to generate the simulation plot. The behavioral design is written with the instruction on the assignment handout. The conditional signal assignment/ the “when/else” statement is used to describe the concurrent signal in the behavioral code of 2 to 1 MUX. Options include when s equals 1. y equals B and when S equals 0, y equals A. The testbench file for behavioral bench is similar to the one for structural. The entity, architecture name are both edited to correspond to the name “behavioral”. Both files are compiled in ModelSim to generate the simulation plots.

2: Report the number of pins and logic modules

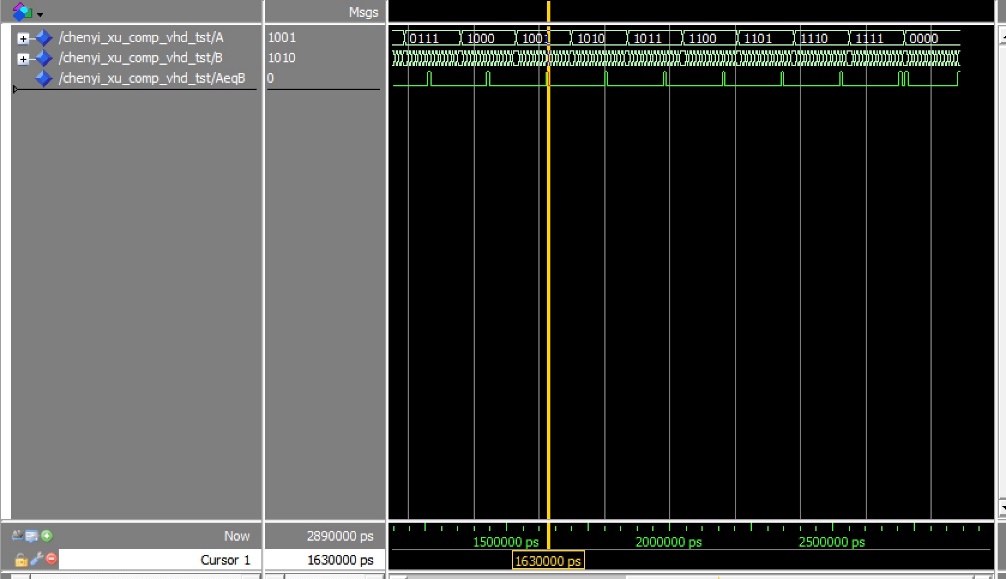
|  |  |  |  |
| --- | --- | --- | --- |
|  | AqeB | 2-to-1 MUX | |
|  | schematic | Structural | Behavioral |
| Logic Utilization (in ALMs) | 2 | 2 | 1 |
| Total pins | 9 | 5 | 4 |

3: representative simulation plot for the introductory testing

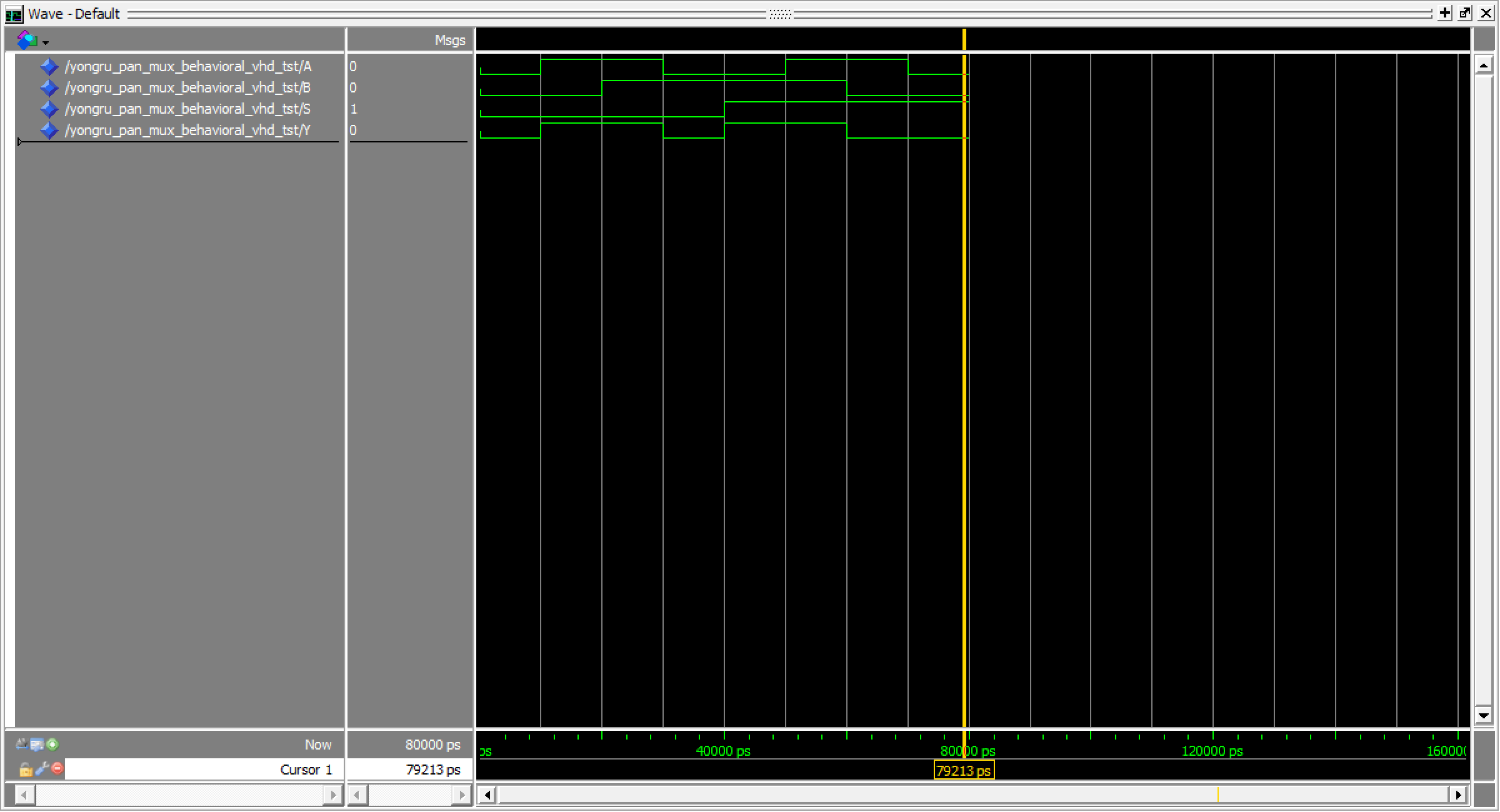


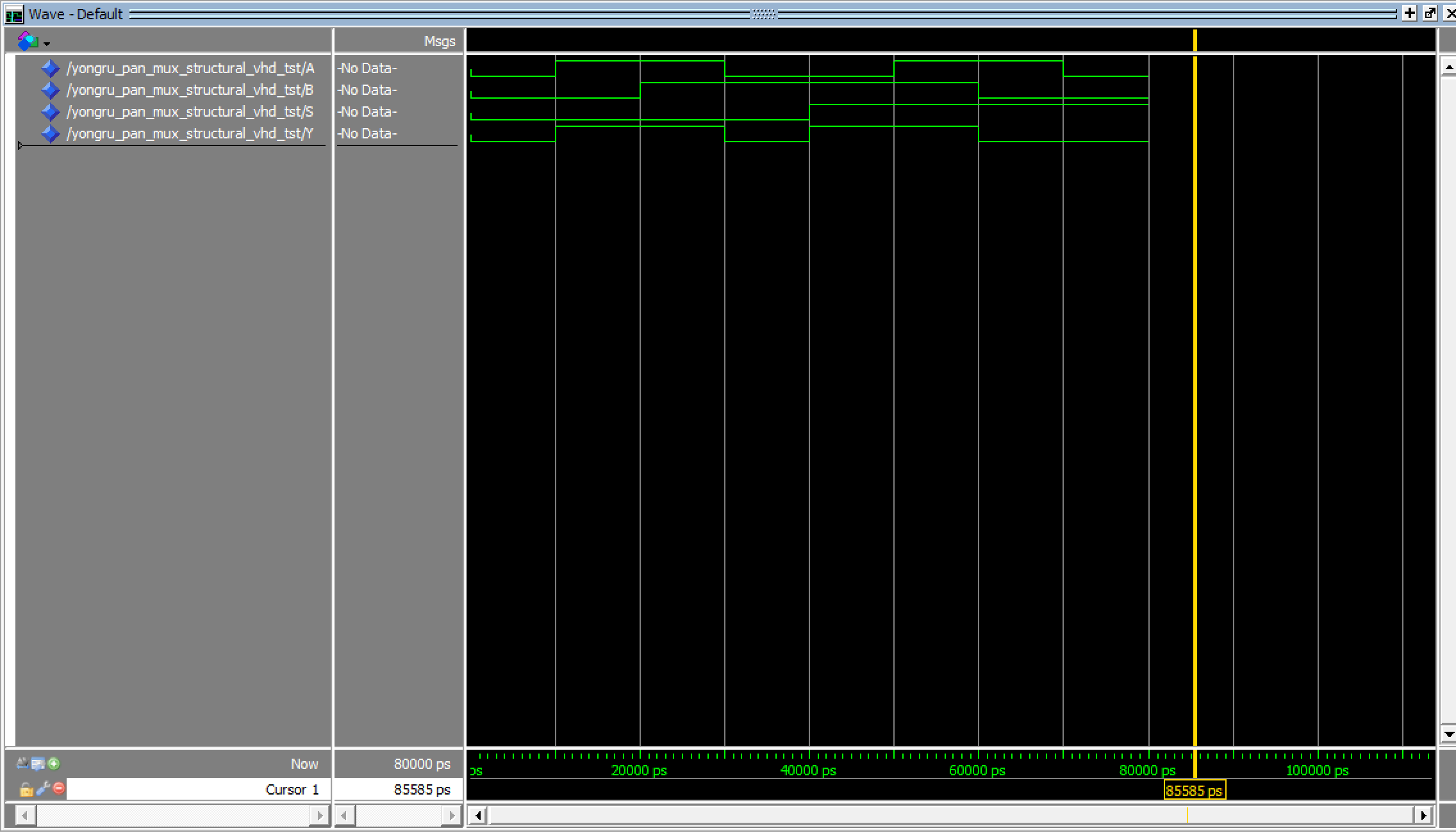
4: representative simulation plots for the exhaustive test





5: representative simulation plots of the 2-to-1 MUX





**Explanation for Result**

*Part 1*

When the 4-bit input A is 0000 and the 4-bit input B is 0000, the 1-bit output is to be 1;

When the 4-bit input A is 1010 and the 4-bit input B is 0000, the 1-bit output is to be 0;

When the 4-bit input A is 1010 and the 4-bit input B is 1010, the 1-bit output is to be 1;

When the 4-bit input A is 1111 and the 4-bit input B is 1010, the 1-bit output is to be 0;

*Part 2*

When A, B, S equal 0, output Y is 0;

When A is 1, B is 0, S is 0, output Y is 1.

When A is 1, B is 1, S is 0, output Y is 1;

When A is 0, B is 1, S is 0, output Y is 0;

When A is 0, B is 1, S is 1, output Y is 1;

When A is 1, B is 1, S is 1, output Y is 1;

When A is 1, B is 0, S is 1, output Y is 0;

When A is 0, B is 0, S is 1, output Y is 0.

The simulated output matches the truth table

**Conclusion**

Simulations for 4-bit comparator circuit and 2-1 MUX are successfully created.