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**VHDL 4 Report**

**Executive Summary**

A wrapper design circuit made with BCD adder code and seven segment decoder is made. The critical path of it is found. The circuit was then being tested on the Altera DE1\_SoC board.

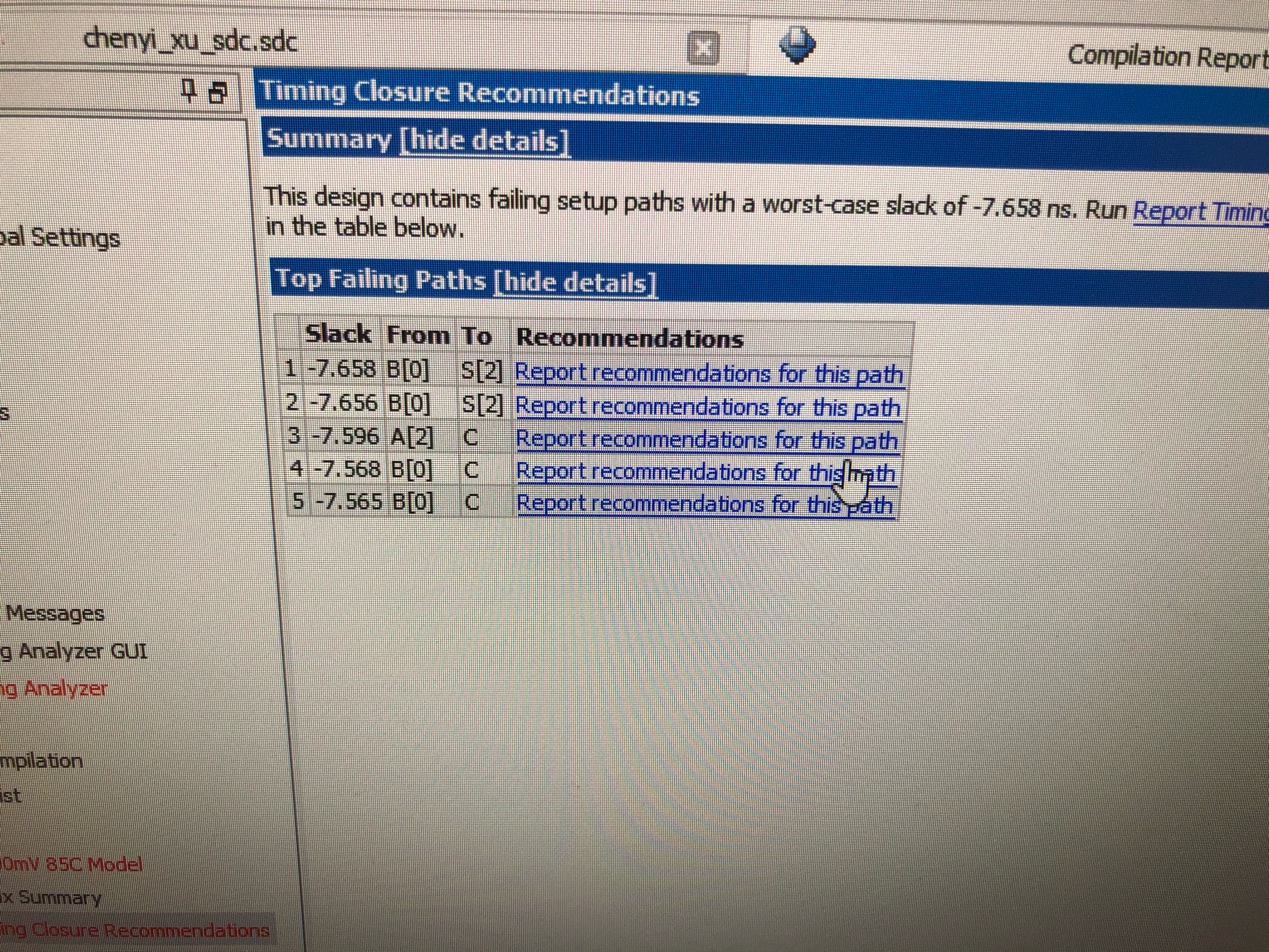
**VHDL Code Explain**

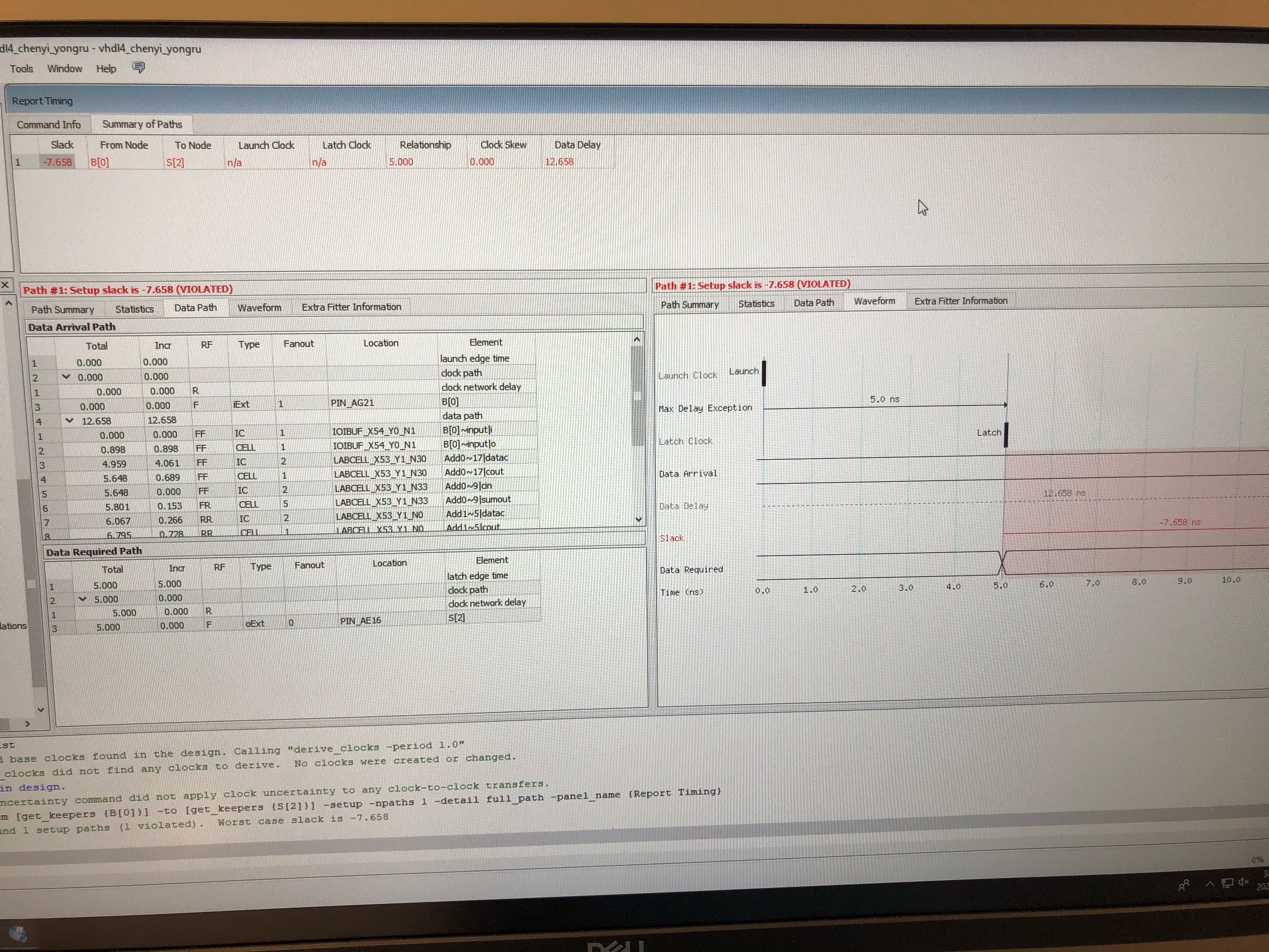
In the wrapper design, a BCD behavioral code and a 7-segment decoder code is implemented. In the wrapper design, a BCD behavioral code and a 7-segment decoder code is implemented.

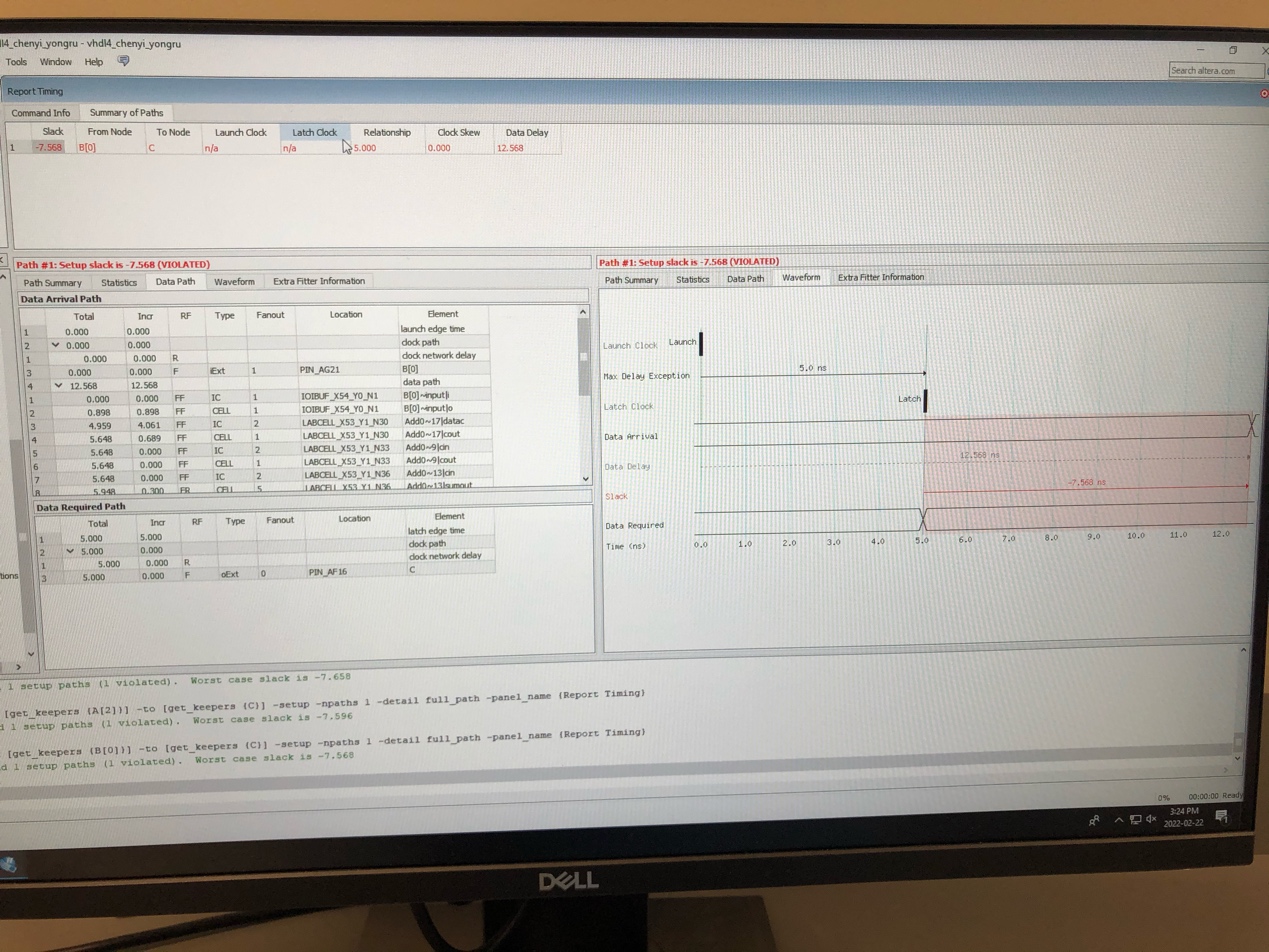
The BCD behavioral code is the same as the one in the VHDL 3 assignment. The reasoning behind it is when the intermediate carry out is less than or equal to 9, no action is needed; when the intermediate carry out is more than 9, 6 is added to the result to get a carry out.

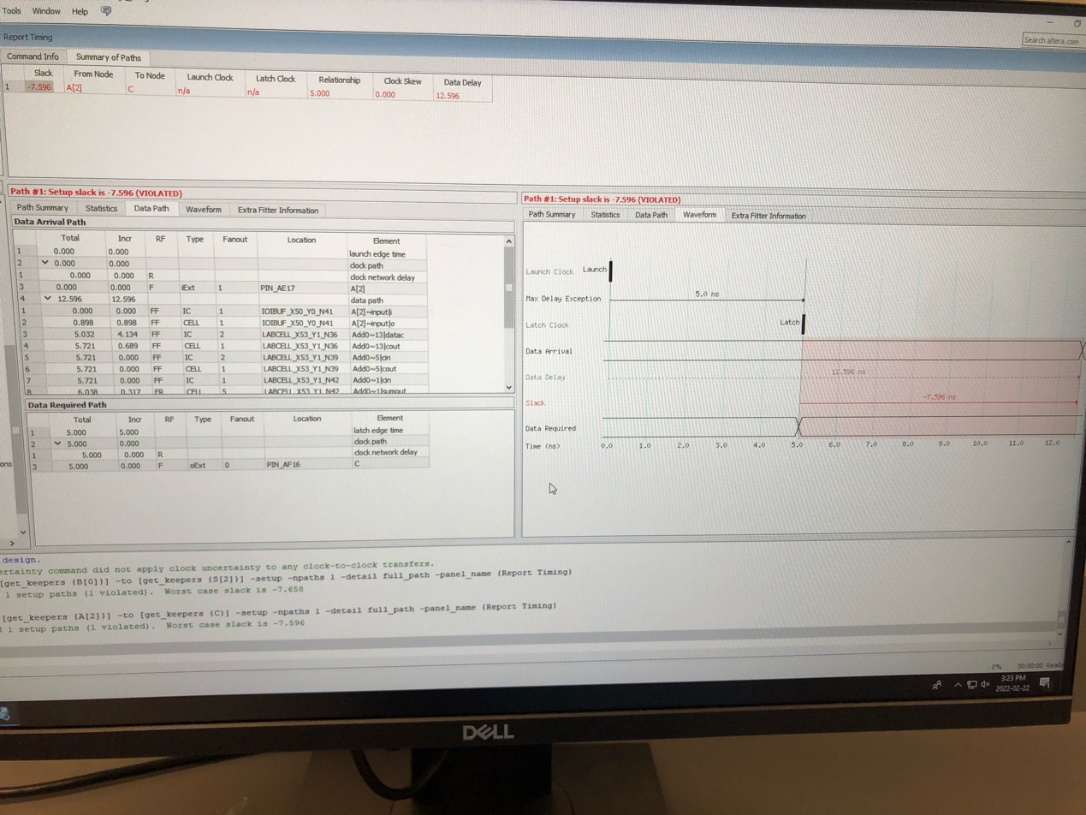
The 7-segment decoder is given in the VHDL 4 handout.

**Obtained Time Waveform**









Critical path: B[0] - S[2]

**FPGA photos and Switch Explain**

Switches from right to left: A[0], A[1], A[2], A[3], B[0], B[1], B[2], B[3]

LED segments from right to left:

Right most LED: bit 0 == decoded\_A[0]

bit 1 == decoded\_A[1]

bit 0 == decoded\_A[2]

bit 0 == decoded\_A[3]

bit 0 == decoded\_A[4]

bit 0 == decoded\_A[5]

bit 0 == decoded\_A[6]

Right second LED: bit 0 == decoded\_B[0]

bit 1 == decoded\_B[1]

bit 2 == decoded\_B[2]

bit 3 == decoded\_B[3]

bit 4 == decoded\_B[4]

bit 5 == decoded\_B[5]

bit 6 == decoded\_B[6]

Right fourth LED: bit 0 == decoded\_AplusB[0]

bit 1 == decoded\_AplusB[1]

bit 2 == decoded\_AplusB[2]

bit 3 == decoded\_AplusB[3]

bit 4 == decoded\_AplusB[4]

bit 5 == decoded\_AplusB[5]

bit 6 == decoded\_AplusB[6]

Right third LED: bit 0 == decoded\_AplusB[7]

bit 1 == decoded\_AplusB[8]

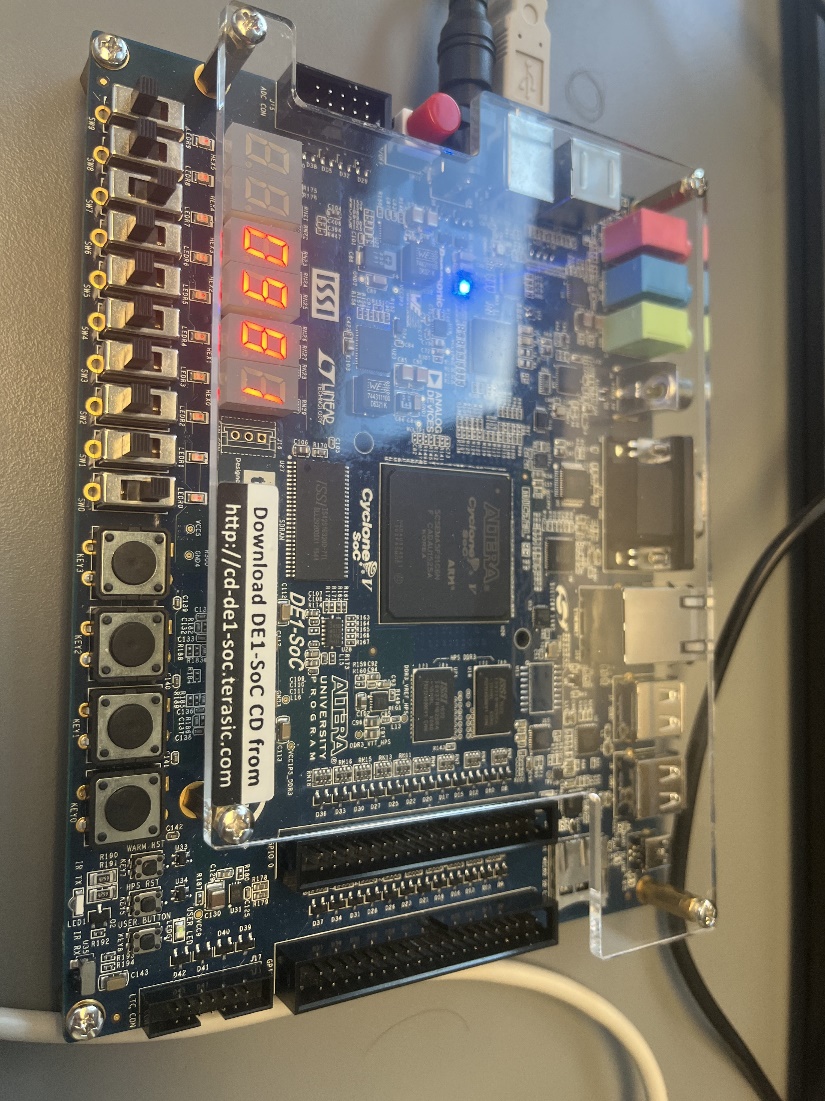
bit 2 == decoded\_AplusB[9]

bit 3 == decoded\_AplusB[10]

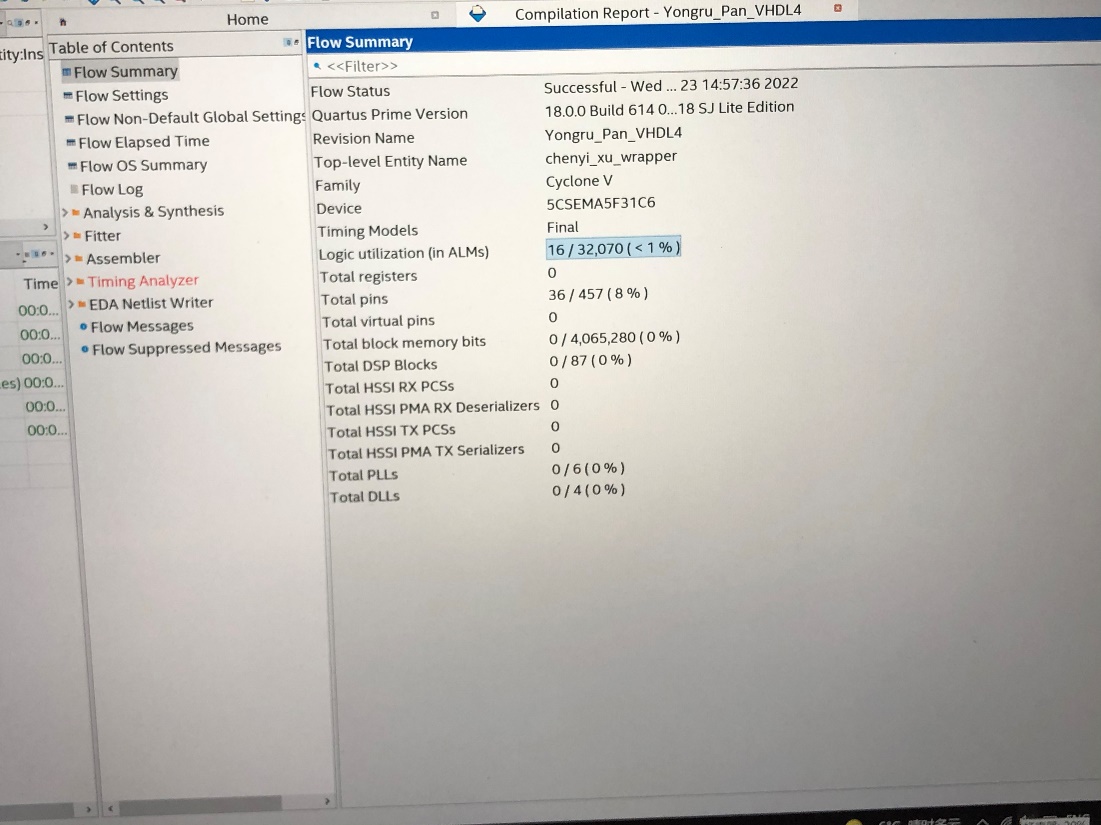
bit 4 == decoded\_AplusB[11]

bit 5 == decoded\_AplusB[12]

bit 6 == decoded\_AplusB[13]



**Number of pins and Logic Modules**



**Result**

The result obtained is aligned with the expectation where the right two LEDs indicate the two inputs A and B, and the left two LEDs together indicate the sum of A and B.

**Conclusion**

The lab is completed successfully as indicated in the instructions.

In part 4, we have successfully found the critical path of the Slow 1100mv 85C Model. The critical path of the Fast 1100mv 85C Model is not found because there is no violation occurred. The critical path in this section is found to be from B[0] to S[2] since this path has the longest propagation time.

In part 5, the 7-segment LED decoder is successfully created following the instruction in handout.

In part 6, the wrapper design is created with BCD behavioral and 7-segment LED decoder and compiled successfully.

In part 7, the test is done and passed as expected. Only that the placement of the LED is inverse from what is expected due to the inverse assignment of pins. Once pins are reversely assigned, the LED will be displayed as expected.

Overall, the VHDL lab is successful.