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**Lab report for VHDL 6**

**Executive summary:**

During this assignment, a sequence detector, a sequence counter and a wrapper circuit were designed. A template of the testbench file was attained from Quartus and replaced the always part in order to run through all the possible cases. The code is then tested, and waveforms are generated on ModelSim.

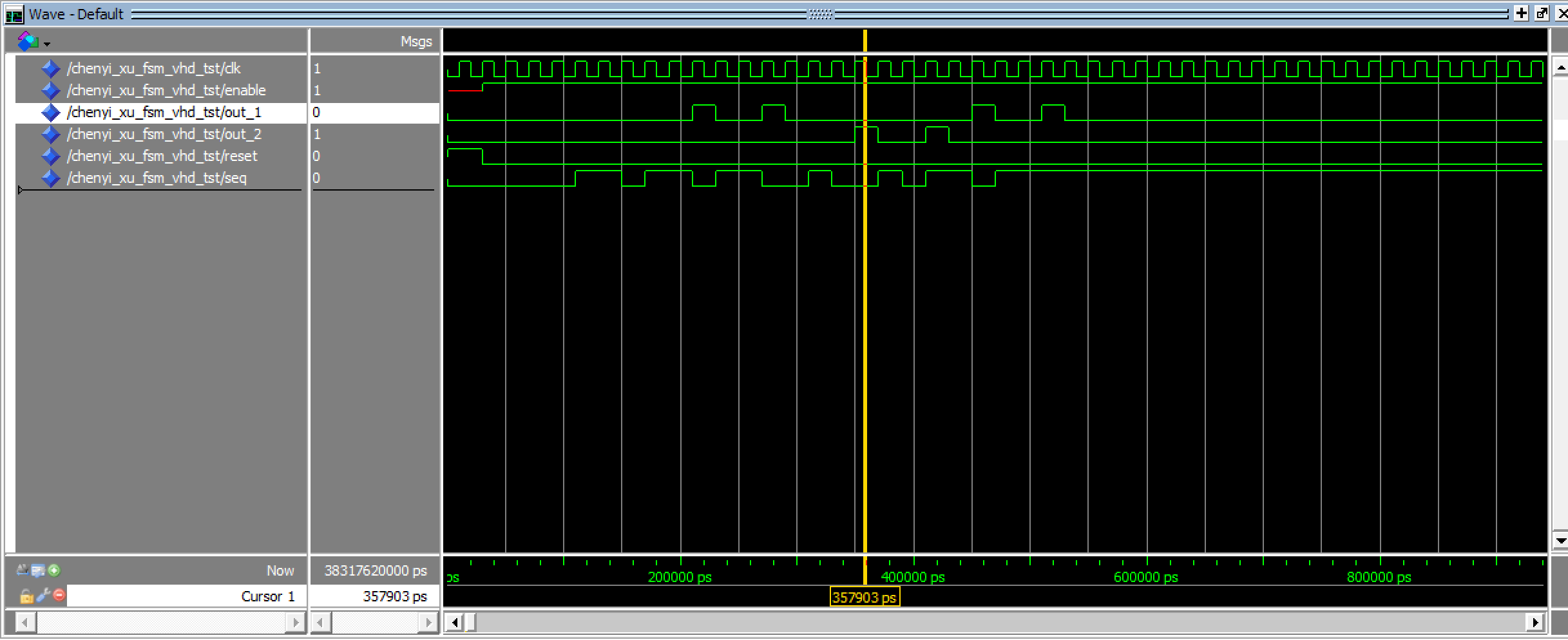
**1: Why is it better to use 2 finite-state-machine than one?**

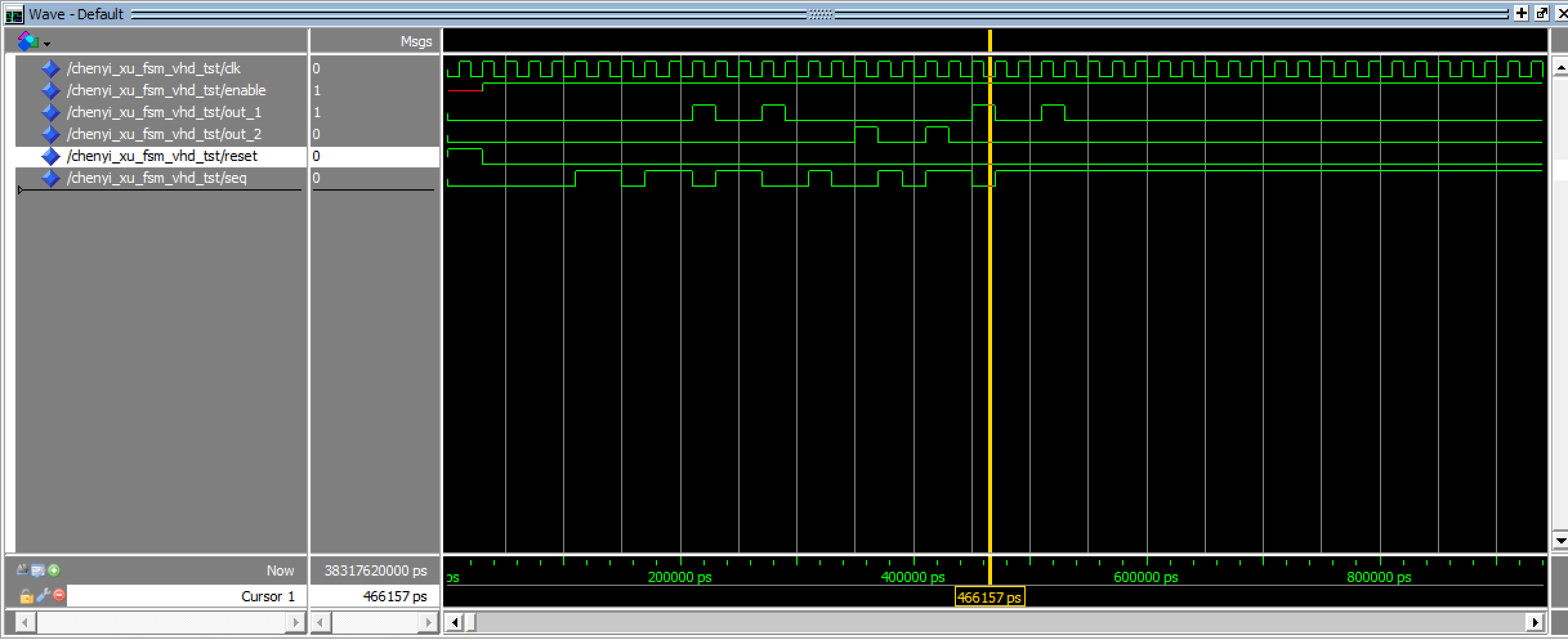
Because there are two distinct patterns to be detected. With two FSM, it is also clearer in terms of its logic. Also state machine only has one state at a time.

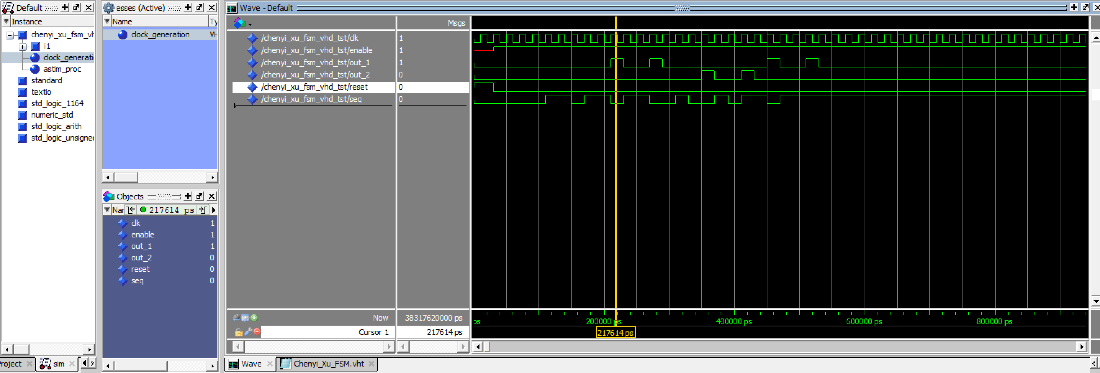
**2: Code explanation:**

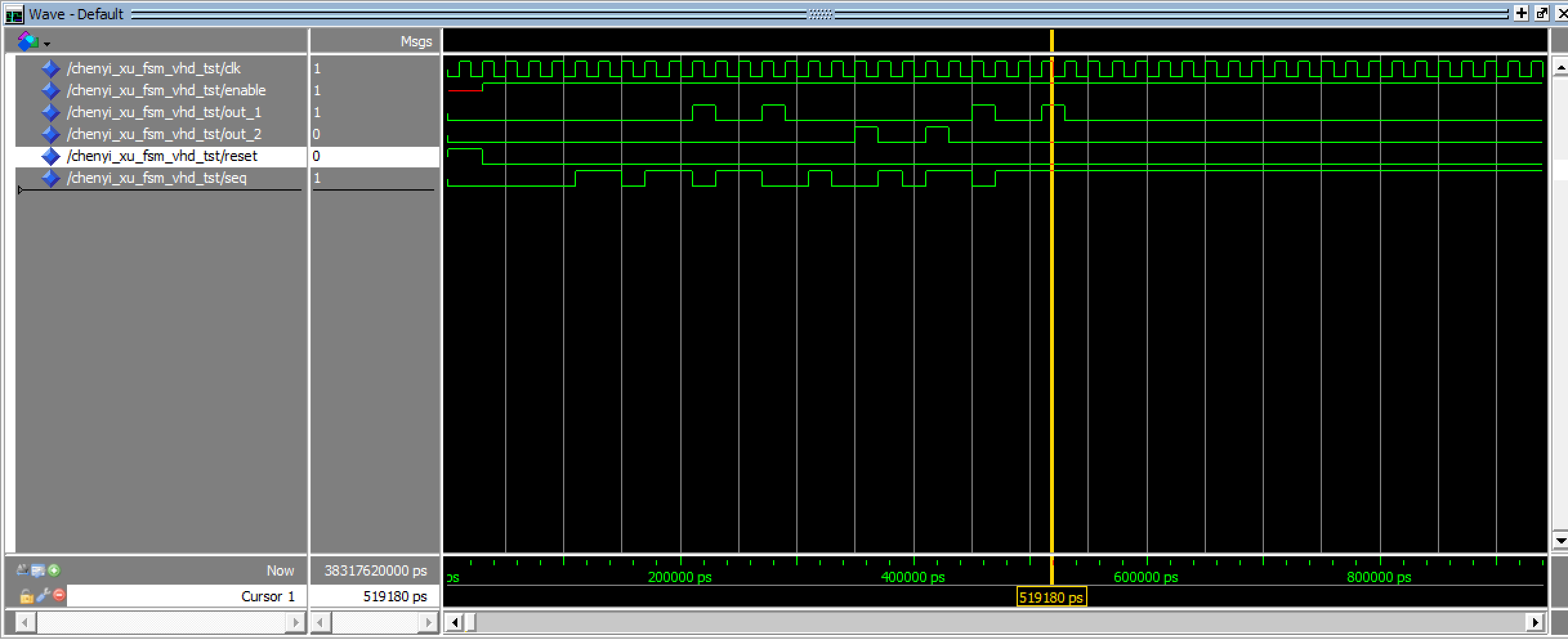
***Sequence detector***

For the first part of the experiment, a sequence detector that takes a sequence as its input and can detect two different patterns is successfully simulated. The output out\_1 will be one when pattern 1011 exists. The output out\_2 will be one when pattern 0010 exists. Two outputs will be 0 for all the other conditions



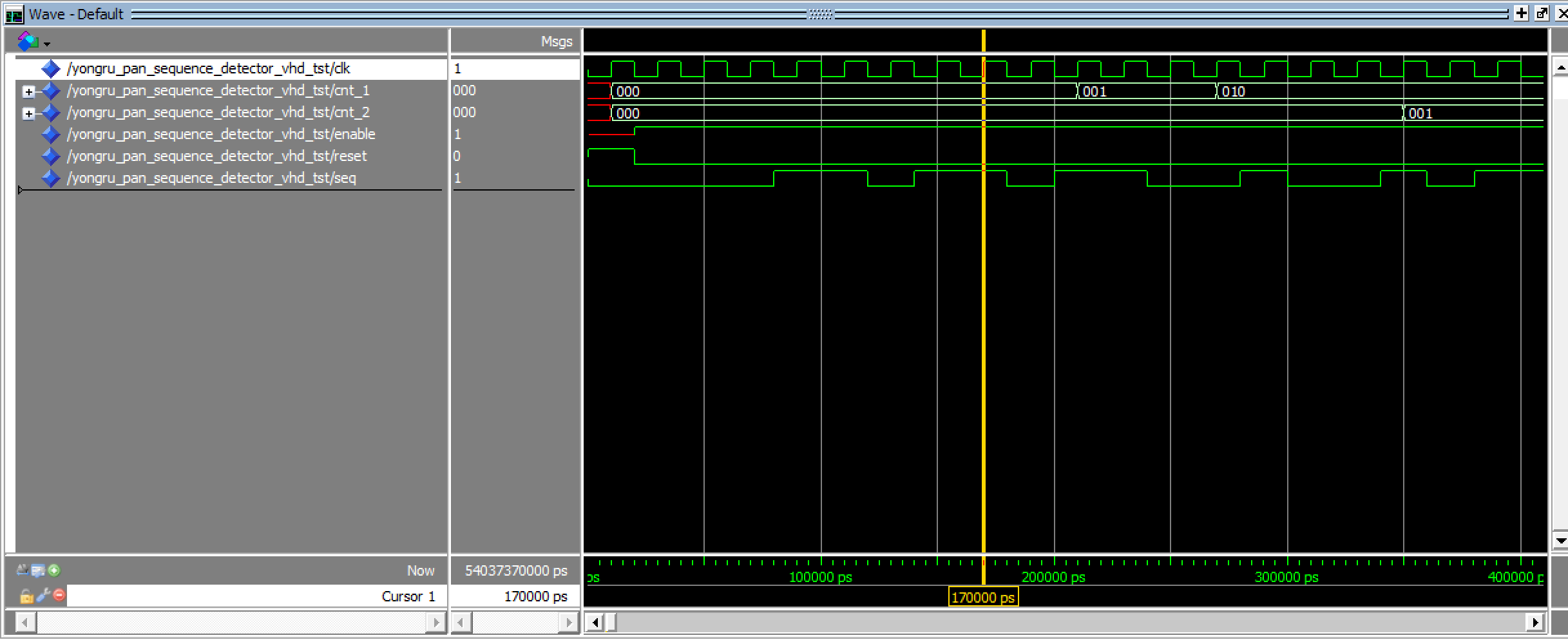


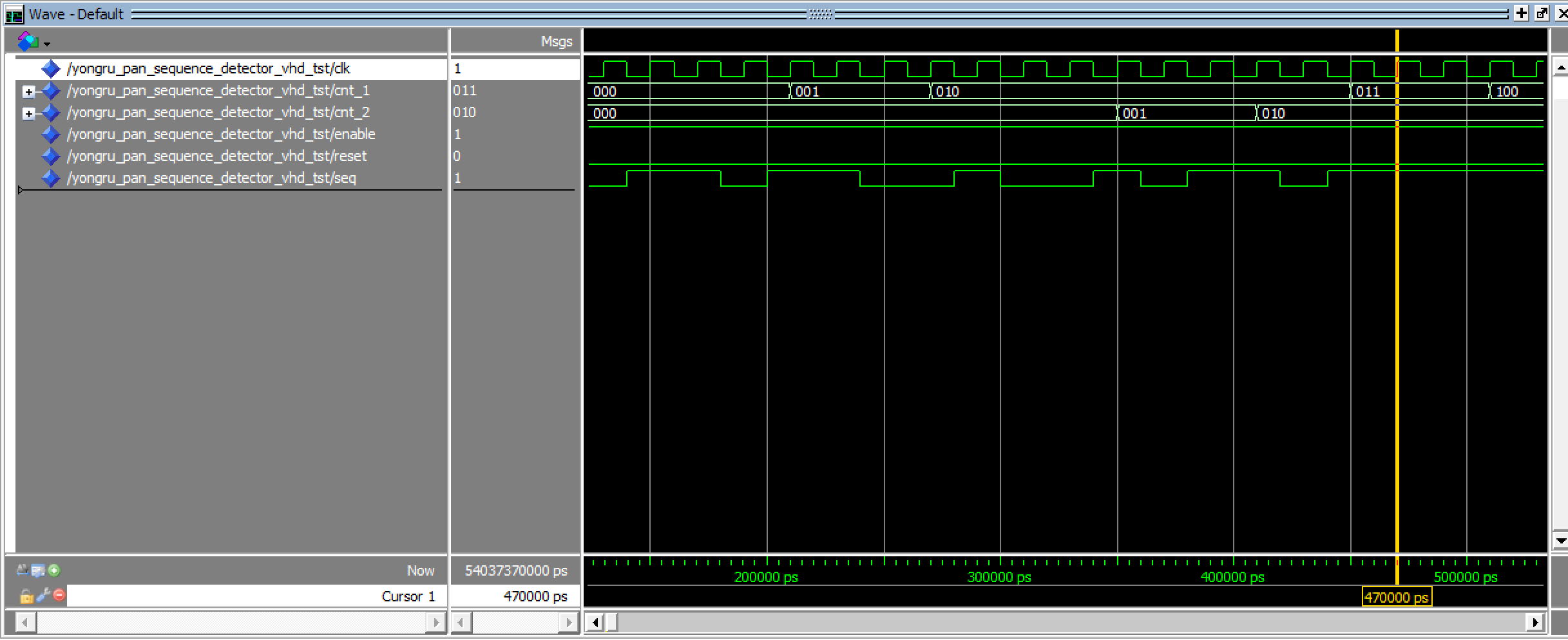


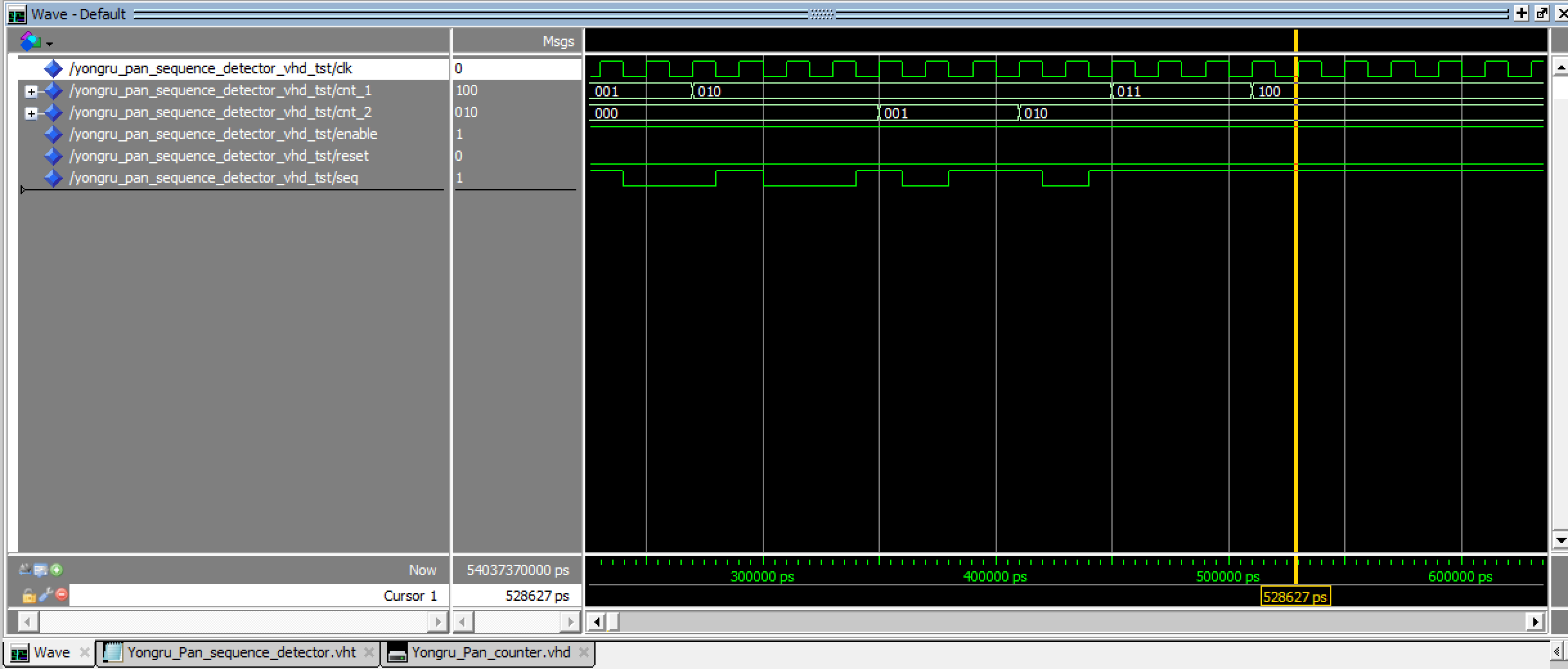


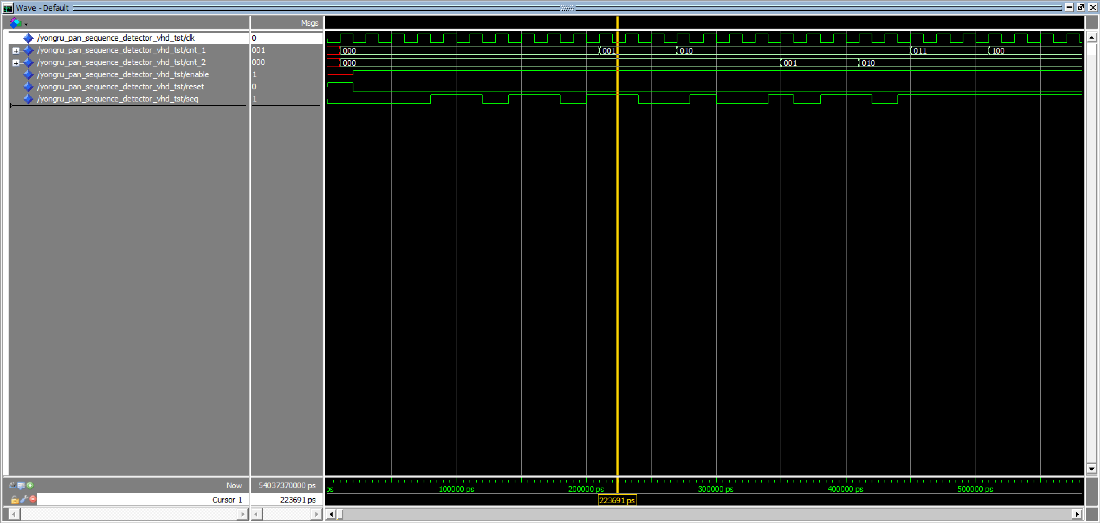
***Sequence Counter***

The sequence detector from the previous section and the 3bit up counter from Assignment 5 are used to simulate the sequence counter circuit with an asynchronous reset and enable signals. The output cnt\_1 will increase by one when there is an occurrence of the pattern 1011. The output cnt\_2 will increase by one when there is an occurrence of the pattern 0010.



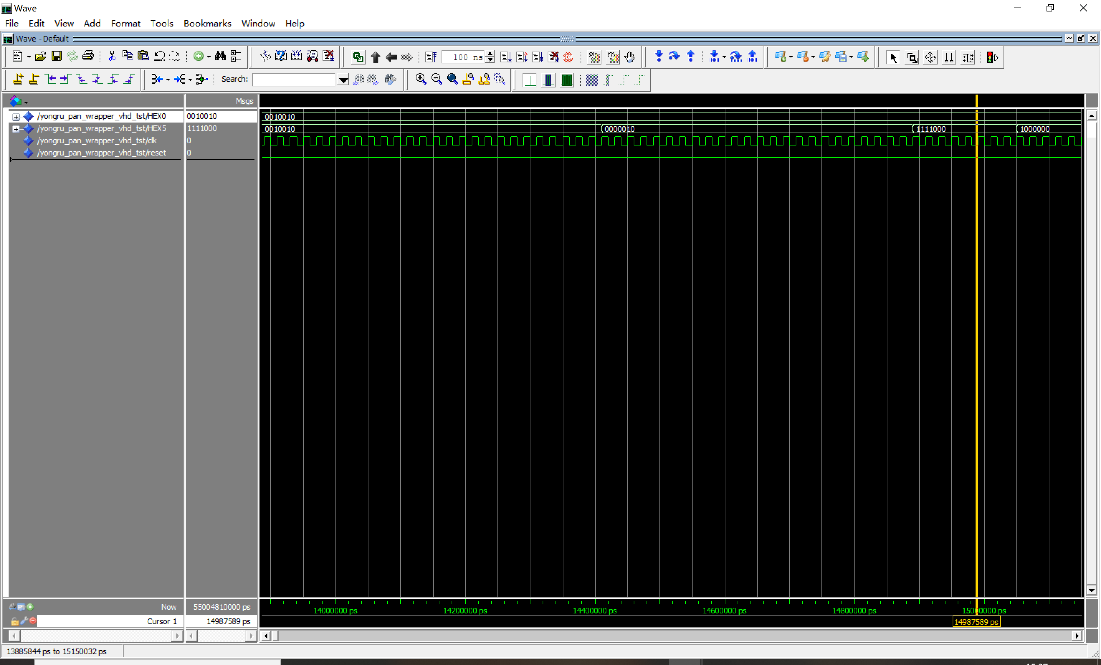


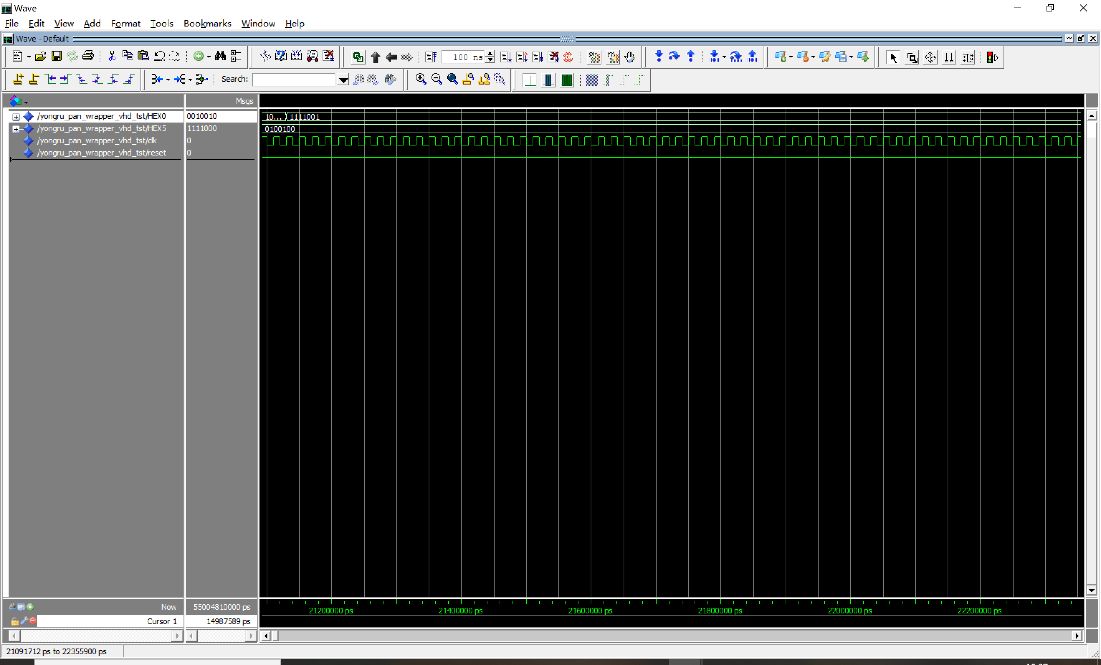


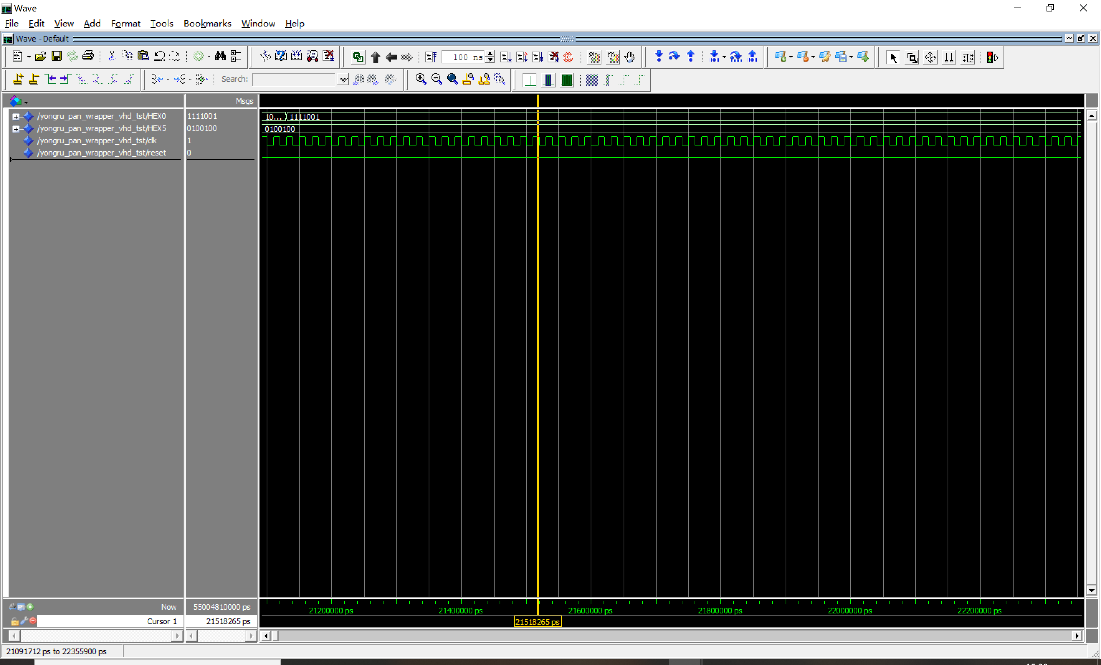


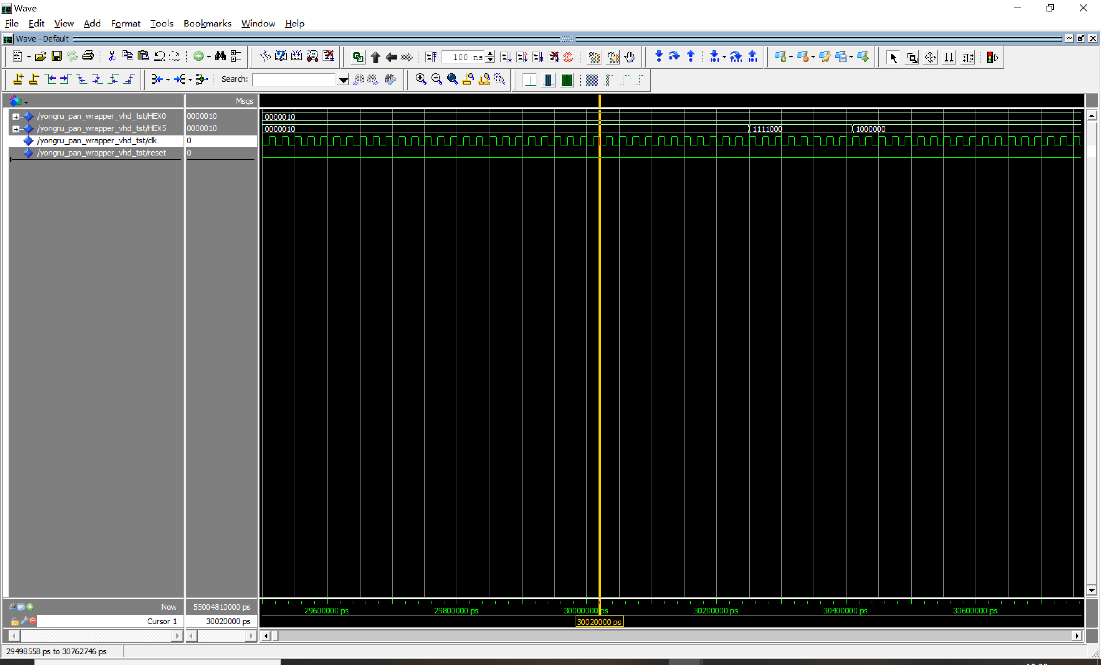
***Wrapper***

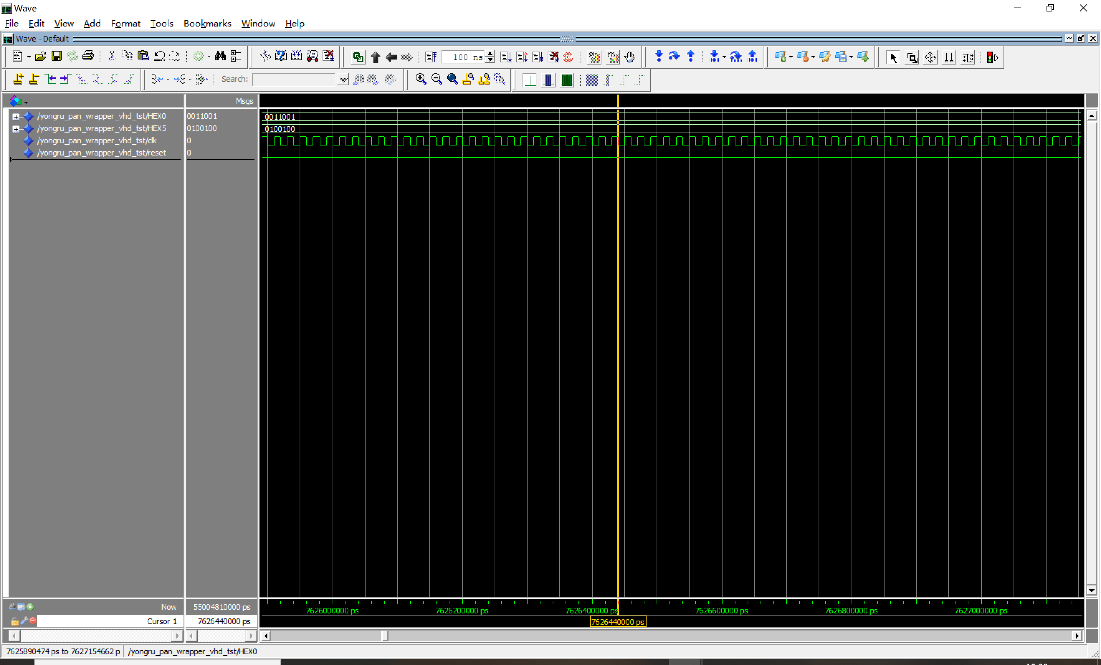
The number of occurrences of each pattern is displayed on the hex displays in order to demonstrate the functionality of the circuit created. Components ROM, clock divider, sequence counter, 7-segment decoder are used.







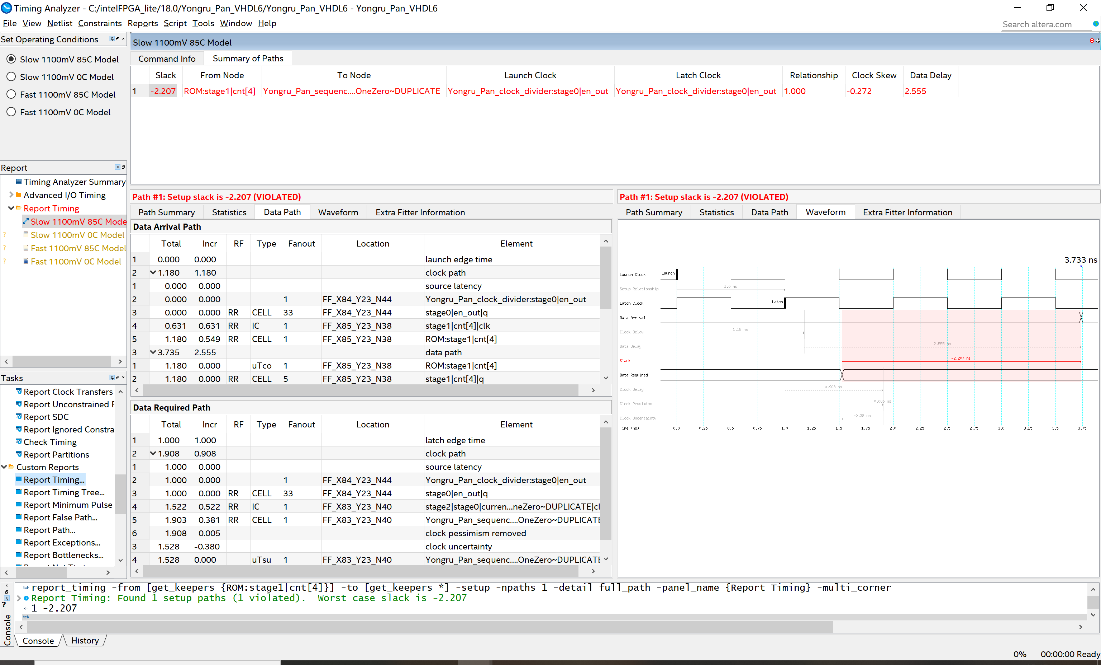


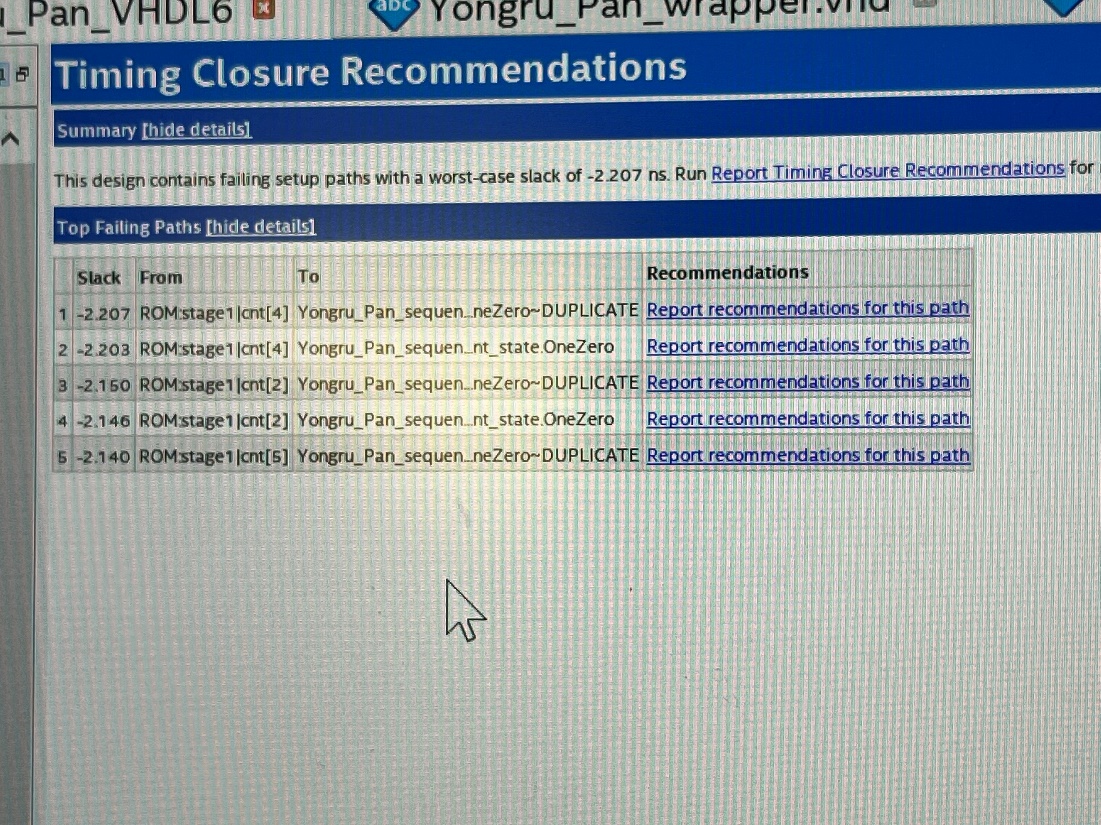


***4: Timing Analysis:***

Critical path

The delay is 2.207 seconds.





***5: Number of pins and logic modules:***

Total pins 16

Logic utilization 26

**Conclusion:**

All sections of the experiments were successfully generated. For the first section, when the input pattern is 1011, output\_1 is 1; when the input pattern is 0010, output\_2 is 1; both outputs are 0 for all other cases. For the sequence counter, the output cnt\_1 will increase when the pattern 1011 occurs while the output cnt\_2 will increase by 1 when the pattern 0010 occurs. The wrapper is then demonstrated on the FPGA board.