MS7210
Digital in to HDMI
Register Map

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Note: MS7210 registers not in the following list should not be written.

I2C Read/Write slave address

SA	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	0	1	1	0
1	1	0	1	1	0	0	1	0

Top MISC					
BASE Address：0x0000					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x04	audio_clk_en	[0]	audio clock enable	R/W	0x0
0x08	tx_audio_clk_inv	[2]	tx audio clock invert	R/W	0x0
	tx_audio_clk_sel	[1..0]	tx audio clock select 00: select i2s clock 01: reserve 10: reserve 11: select spdif clock	R/W	0x0
0x0c	aupll_sel	[3..2]	audio pll select : 00 : use AUDIO PLL 01: use AUDIO DLL + AUDIO PLL 10: use AUDIO DLL 11: use AUDIO PLL(XTAL input)	R/W	0x0
0x1e	pclk_freq	[7..0]	pclk_freq result pclk_freq*(xtal/10000)/4096	RO	/
0x19	freq_clk_sel	[2..1]	11: pclk clock others: reserve	R/W	0x0
	freq_enable	[0]	frequency meter enable	R/W	0x0
0xc1	tx_sclk_sel	[7..6]	00: no divide 01: divide 2 10: divide 4 11: divide 8	R/W	0x0
0xa5	spdif_cdr	[4]	i2s_sd3 input data use to tx spdif(data and clock)	R/W	0x0
	spdif_from_i2sd3	[3]	i2s_sd3 input data use to tx spdif(data)	R/W	0x0
0x79	dig_pd	[5]	digital pads pull down enable,active high	R/W	0x0
	dig_pu	[4]	digital pads pull up enable,active high	R/W	0x1
0x09	dvin_sw_rstb	[0]	digital video input module reset 0:reset	R/W	0x0
0x16	dvin_en	[2]	digital video input enable 0:disable 1:enable	R/W	0x0

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Top MISC					
BASE Address：0x0000					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0xC0	dvin_clk2tx_sel	[1]	0:pclk to tx and dvin_lat_clk to tx pixel clk 1:pclk div2 to txpll and dvin_lat_clk div2 to tx pixel clk example:dvin 8-bit sdr need set it to 1	R/W	0x0
	dvin_lat_clk_sel	[0]	0:dvin_lat_clk from PA 1:dvin_lat_clk from txpll example: dvin 16-bit ddr mode set it to 1	R/W	0x0
0x08	tx_pll_clk_en1	[4]	1:HDMI tx pll calibration clock enable	R/W	0x0
0x06	tx_audio_clk_en	[4]	1:TX audio clock enable	R/W	0x0
	tx_clk_en	[0]	1:TX pixel and tmds clock enable	R/W	0x0
0x0a	tx_pll_cal_sw_rstb	[4]	TX pll calibration reset 0:reset	R/W	0x0
	spdif_cdr_sw_rstb	[1]	spdif cdr logic reset 0:reset	R/W	0x0
0x0b	audio_sw_rstb	[4]	0:TX audio reset	R/W	0x0
	video_sw_rstb	[0]	0:TX video reset	R/W	0x0
0x12	ddc_disable	[0]	set to 1 disable HDMI DDC	R/W	0x1

DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x00	dvin_sync_fmt	[3..2]	Digital Video Input Sync information format 00: Sync information include HS, VS; 01: Sync information include HS, VS, DE; 10: Sync information include VS, DE; 11: Embedded sync (such as 656,1120..).	R/W	0x1
0x01	dvin_data_swap	[7]	digital video input data MSB/LSB swap D[0..23]->D[23..0]	R/W	0x0

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DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
	dvin_data_sel	[6..4]	24 bit digital in pin map 000: dvin y/g mapping to din[15..8] dvin u/b mapping to din[7..0] dvin v/r mapping to din[23..16] 001: dvin y/g mapping to din[15..8] dvin u/b mapping to din[23..16] dvin v/r mapping to din[7..0] 010: dvin y/g mapping to din[23..16] dvin u/b mapping to din[15..8] dvin v/r mapping to din[7..0] 011: dvin y/g mapping to din[23..16] dvin u/b mapping to din[7..0] dvin v/r mapping to din[15..8] 100 dvin y/g mapping to din[7..0] dvin u/b mapping to din[15..8] dvin v/r mapping to din[23..16] 101 dvin y/g mapping to din[7..0] dvin u/b mapping to din[23..16] dvin v/r mapping to din[15..8]	R/W	0x0

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DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
	dvin_data_sel	[6..4]	16 bit digital in pin map 000: dvin y mapping to din[15..8] dvin uv mapping to din[7..0] 001: dvin y mapping to din[7..0] dvin uv mapping to din[15..8] 010: dvin y mapping to din[23..6] dvin uv mapping to din[15..8] 011: dvin y mapping to din[15..8] dvin uv mapping to din[23..16] 100: dvin y mapping to din[23..16] dvin uv mapping to din[7..0] 101: dvin y mapping to din[7..0] dvin uv mapping to din[23..16]	R/W	0x0
	dvin_data_sel	[6..4]	8 bit digital in pin map 000: dvin yuv mapping to din[23..16] 001: dvin yuv mapping to din[15..8] 010: dvin yuv mapping to din[7..0]	R/W	0x0
	dvin_data_sync_swap	[3]	digital video input sync and data swap 1:d[0..23],hysnc,vsync,de->de,vsync,hysnc,d[0..23]	R/W	0x0

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DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x02	dvin_sync_swap	[2..0]	000: DEIN mapping to DE HSIN mapping to HSYNC VSIN mapping to VSYNC 001: DEIN mapping to DE HSIN mapping to VSYNC VSIN mapping to HSYNC 010: DEIN mapping to HSYNC HSIN mapping to DE VSIN mapping to VSYNC 011: DEIN mapping to HSYNC HSIN mapping to VSYNC VSIN mapping to DE 100: DEIN mapping to VSYNC HSIN mapping to HSYNC VSIN mapping to DE 101: DEIN mapping to VSYNC HSIN mapping to DE VSIN mapping to HSYNC	R/W	0x0
	dvin_embedded_sync	[7]	SAV/EAV data cut in embedded sync input	R/W	0x0
	dvin_2xembedded_mode	[6]	digital video input in embedded,EAV and SAV double	R/W	0x0
	dvin_embedded_mode	[5]	digital video input in embedded EAV and SAV	R/W	0x0
	dvin_ddr_edge_inv	[4]	First pixel in DDR video mode fetched by clock falling edge or rising edge 0: by clock rising edge 1: by clock falling edge	R/W	0x0
	dvin_ddr_mode	[3]	Digital video input in DDR mode 0: SDR mode video 1: DDR mode video	R/W	0x0

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DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
	dvin_mode_sel	[2..0]	Digital video input mode for bus width 000: 24-bit 444 mode 001: 16-bit yuv 422 mode 010: 20-bit yuv 422 mode 011: 24-bit yuv 422 mode 100: 8-bit yuv 422 mode 101: 10-bit yuv 422 mode 110: 12-bit yuv 422 mode 111: 8-bit yuv 422 mode	R/W	0x0
0x06	dvin_dein_flip	[2]	DVIN DE input polarity flip	R/W	0x0
		[1]	DVIN VSYNC input polarity flip	R/W	0x0
		[0]	DVIN HSYNC input polarity flip	R/W	0x0
0x07	dvin_hvdet_sel	[6..4]	DVIN H/V detected information selection. 0x0: Horizontal total detection counted by pixel clock 001: Vertical total detection counted by pixel clock 010: Horizontal active pixel number 011: Horizontal active start position 100: Vertical active start position	R/W	/
	dvin_hvdet_clr	[1]	DVIN H/V detection status clear	R/W	0x0
	dvin_hvdet_en	[0]	DVIN H/V detection enable, active high	R/W	0x0
0x08	dvin_hvdet_rd0	[7..0]	dvin_rd_hvdet_status[7..0]	R/W	/
0x09	dvin_hvdet_rd1	[7..0]	dvin_rd_hvdet_status[15..8]	R/W	/
0x0A	dvin_hvdet_rd2	[7..0]	dvin_rd_hvdet_status[23..16]	R/W	/
0x0B	dvin_fldout_flip	[6]	DVIN output field polariity flip	R/W	0x0
	dvin_vsout_flip	[5]	DVIN output VS polarity flip, active high.	R/W	0x0
	dvin_hsout_flip	[4]	DVIN output HS polarity flip, active high	R/W	0x0
	dvin_prgs_in	[2]	DVIN input timing is progressive. 0: interlace input 1: progressive	R/W	0x0
0x0C	dvin_htotal_l	[7..0]	DVIN horizontal total pixel number[7..0]	R/W	0x5a
0x0D	dvin_htotal_h	[4..0]	DVIN horizontal total pixel number[12..8]	R/W	0x3
0x0E	dvin_vtotal_l	[7..0]	DVIN vertical total line number[7..0]	R/W	0xd
0x0F	dvin_vtotal_h	[3..0]	DVIN vertical total line number[11..8]	R/W	0x2
0x10	dvin_pxl_shift_l	[7..0]	dvin_pixel_shift[7:0]	R/W	0x0
0x11	dvin_pxl_shift_h	[4..0]	dvin_pixel_shift[12:8]	R/W	0x0
0x12	dvin_line_shift_l	[7..0]	dvin_line_shift[7..0]	R/W	0x0
0x13	dvin_line_shift_l	[3..0]	dvin_line_shift[11..8]	R/W	0x0
0x14	dvin_hsw_l	[7..0]	dvin_hs_width[7..0]	R/W	0x40

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DVIN					
BASE Address：0x1200					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x15	dvin_hsw_h	[3..0]	dvin_hs_width[11..8]	R/W	0x0
0x16	dvin_vsw_l	[7..0]	dvin_vs_width[7..0]	R/W	0x6
0x17	dvin_vsw_h	[3..0]	dvin_vs_width[11..8]	R/W	0x0
0x18	dvin_hde_st_l	[7..0]	dvin_hde_st[7..0]	R/W	0x7c
0x19	dvin_hde_st_h	[4..0]	dvin_hde_st[12..8]	R/W	0x0
0x1A	dvin_hde_sp_l	[7..0]	dvin_hde_sp[7..0]	R/W	0x4c
0x1B	dvin_hde_sp_h	[4..0]	dvin_hde_sp[12..8]	R/W	0x3
0x1C	dvin_vde_ost_l	[7..0]	dvin_vde_odd_st[7..0]	R/W	0x2a
0x1D	dvin_vde_ost_h	[3..0]	dvin_vde_odd_st[11..8]	R/W	0x0
0x1E	dvin_vde_osp_l	[7..0]	dvin_vde_odd_sp[7..0]	R/W	0xa
0x1F	dvin_vde_osp_h	[3..0]	dvin_vde_odd_sp[11..8]	R/W	0x2
0x20	dvin_vde_est_l	[7..0]	dvin_vde_even_st[7..0]	R/W	0x2a
0x21	dvin_vde_est_h	[3..0]	dvin_vde_even_st[11..8]	R/W	0x0
0x22	dvin_vde_esp_l	[7..0]	dvin_vde_even_sp[7..0]	R/W	0xa
0x23	dvin_vde_esp_h	[3..0]	dvin_vde_even_sp[11..8]	R/W	0x2
0x24	dvin_uv_swap	[1]	dvin U/V index swap	R/W	0x0
	dvin_yc_swap	[0]	dvin Y/C index swap	R/W	0x0
0x37	dvin_rd_trig	[0]	DVIN trigger enable for timing registers. in RO: it is the status of write 1: means write done 0: means write not finished	WO/ RO	/
0x62	dvin_bt1004_mode	[0]	16-bit BTA1004 enalbe,active high	R/W	0x0
0x63	dvin_12b444	[0]	12 bit RGB/YUV444 ddr mode enable,active high	R/W	0x0
0x64	dvin_yuv422_uvflip	[1]	YUV422 digital input YC flip enable 1:enable	R/W	0x0
0x65	de_only_mode	[0]	digital input DE only mode enable	R/W	0x0

CSC					
BASE Address：0x80					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x00	dst_csc	[3..2]	output color space for color space conversion 01: YUV444 10: YUV422	R/W	0x0
	src_csc	[1..0]	input color space for color space conversion: 00 : RGB 01: YUV444 10: YUV422	R/W	0x0

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CSC					
BASE Address：0x80					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x01	csc_yuv2rgb_hd_sel	[5]	YCbCr 709 color space select in YCbCr to RGB color space conversion 0: 601 1: 709	R/W	0x0
	csc_yuv2rgb_range	[4]	range select in YCbCr to RGB color space conversion 1: RGB output is 0-255 for 8 bit 0: RGB output is 16-235 for 8 bit	R/W	0x0
	csc_rgb2yuv_hd_sel	[1]	YCbCr 709 color space select in RGB to YCbCr color space conversion 0: 601 1: 709	R/W	0x0
	csc_rgb2yuv_range_press_sel	[0]	range select in RGB to YCbCr color space conversion 1: RGB input is 0-255 for 8 bit 0: RGB output is 16-235 for 8 bit	R/W	0x0
0x02	csc_yuv444to422_filter	[5]	U and V filter bypass in 444to422 conversion. 1: filter bypass 0: filter enable	R/W	0x1
	csc_yuv444to422_uv_flip	[4]	U and V swap in 422to444 or 444to422 conversion. 0: UVUV; 1: VUVU	R/W	0x0
	csc_yuv422to444_filt_bypass	[1]	U and V filter bypass in 422to444 conversion. 1: filter bypass 0: filter enable	R/W	0x1
	csc_yuv422to444_uv_flip	[0]	U and V swap in 422to444 conversion. 0: UVUV 1: VUVU	R/W	0x0

PA					
BASE Address：0x1280					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x01	pa_s	[2]	1:clock invert	R/W	0x00

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	pa_s	[1..0]	phase control bits : 01:1ns 10:2ns 11:3ns		

HDMI TX					
BASE Address：0x0900					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x20	tx_bias_pd	[5]	TX bias current power down 0: normal work 1: power down	R/W	0x1
	tx_div5_rstb	[4]	TX DIV5 reset 0: reset 1: normal work	R/W	0x1
	tclk_p2s_pwdz	[3]	P2S power down 0: power down 1: normal work	R/W	0x0
	tclk_drv_dwdz	[2]	Clock channel driver power down 0: power down 1: normal work	R/W	0x0
	data_p2s_pwdz	[1]	P2S power down 0: power down 1: normal work	R/W	0x0
0x23	tx_idrv_6m_en	[4]	TX data drive enhance 1:enable	R/W	0x0
	rg_post_pre2_en	[2]	CH2 pre-emphasis pre-driver enable 0: disable 1: enable	R/W	0x0
	rg_post_pre1_en	[1]	CH1 pre-emphasis pre-driver enable 0: disable 1: enable	R/W	0x0
	rg_post_pre0_en	[0]	CH0 pre-emphasis pre-driver enable 0: disable 1: enable	R/W	0x0
0x24	main_pre1	[6..4]	CH1 pre-driver control 100: 3Gbps 010: 1.5Gbps 001: 750Mbps 000: <750Mbps	R/W	0x4

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HDMI TX					
BASE Address：0x0900					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
	main_pre0	[2..0]	CH0 pre-driver control 100: 3Gbps 010: 1.5Gbps 001: 750Mbps 000: <750Mbps	R/W	0x4
0x25	main_prec	[6..4]	Clock channel pre-driver control	R/W	0x0
	main_pre2	[2..0]	CH2 pre-driver control 100: 3Gbps 010: 1.5Gbps 001: 750Mbps 000: <750Mbps	R/W	0x4
0x26	main_po1	[7..4]	CH1 Driver current control 8mA+4.5mA*bit3+2mA*bit2+2mA*bit1+1mA*bit0	R/W	0x2
	main_po0	[3..0]	CH0 Driver current control 8mA+4.5mA*bit3+2mA*bit2+2mA*bit1+1mA*bit0	R/W	0x2
0x27	main_poc	[7..4]	clock CH Driver current control 8mA+4.5mA*bit3+2mA*bit2+2mA*bit1+1mA*bit0	R/W	0x2
	main_po2	[3..0]	CH2 Driver current control 8mA+4.5mA*bit3+2mA*bit2+2mA*bit1+ 1mA*bit0	R/W	0x2
0x28	post_po1	[7..4]	CH1 pre-emphasis driver current control 2mA*bit3+1mA*bit2+0.5mA*bit1+ 0.25mA*bit0	R/W	0x0
	post_po0	[3..0]	CH0 pre-emphasis driver current control 2mA*bit3+1mA*bit2+0.5mA*bit1+ 0.25mA*bit0	R/W	0x0
0x29	post_po2	[3..0]	CH2 pre-emphasis driver current control 2mA*bit3+1mA*bit2+0.5mA*bit1+ 0.25mA*bit0	R/W	0x0
0x2A	txpll_prediv2_en	[6]	TXPLL prediv2 enable 0:disable 1:enable	R/W	0x0
	txpll_afte_fbdiv2_en	[2]	TXPLL after fbdiv2 enable 0:disable 1:enable	R/W	0x0

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HDMI Controller					
BASE Address：0x0500					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x02	hpd_status	[0]	HPD detect,active high	RO	0x0
0x03	dvi_en	[0]	DVI mode enable 1:DVI mode 0:HDMI mode	R/W	0x0
0x06	soft_rst_clk_pll	[2]	tmds clock domain soft reset,active high	R/W	0x0
	soft_rst_aud_clk	[1]	audio clock soft reset, active high	R/W	0x0
0x07	audio_mute	[2]	audio mute 1:mute 0:normal work	R/W	0x1
	video_mute	[1]	video mute 1:mute 0:normal work	R/W	0x1
0x08	color_space	[7..6]	00:RGB 01:YUV422 10:YUV444	R/W	0x0
	num_rept	[5..4]	00:no repeater 01:2x repeat 10:3x repeat 11:4xrepeat	R/W	0x0

HDMI TX Audio					
BASE Address：0x0530					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
0x0	cfg_iis_spdif	[0]	audio data selection 0:I2S 1:SPDIF	R/W	0x0
0x1	audio_enable	[7]	when audio is ready, write this register, and the HW will calculate the values of N/CTS.	R/W	0x0
	sample_32k	[6]	when audio sample rate is 32 KHz, set this register to1	R/W	0x0
	sample_441k	[5]	when audio sample rate is 44.1 KHz, set this register to1	R/W	0x0
	sample_882k	[4]	when audio sample rate is 88.2 KHz, set this register to1	R/W	0x0
	sample_176k	[3]	when audio sample rate is 176.4 KHz, set this register to1	R/W	0x0
	sample_48k	[2]	when audio sample rate is 48 KHz, set this register to1	R/W	0x1
	sample_96k	[1]	when audio sample rate is 96 KHz, set this register to1	R/W	0x0

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HDMI TX Audio					
BASE Address：0x0530					
Offset	**Register name**	**BIT**	**Description**	**Type**	**Default value**
	sample_192k	[0]	when audio sample rate is 192 KHz, set this register to1	R/W	0x0
0x2	audio_ch_en	[3..0]	when audio is I2S, the registers are used to set the channel number: When I2S is 2-channel, it is set to 4'b0001 When I2S is 8-channel, it is set to 4'b1111	R/W	0x1
0x5	audio_length	[5..4]	I2S data length 01:16-bit otherwise:24-bit	R/W	0x0
	i2s_data_inv	[3]	I2S data invert	R/W	0x0
	i2s_lrclk_inv	[2]	I2S lrclk invert	R/W	0x0
	i2s_mode	[1..0]	00:left justified,0T delay 01:right mode 10:left justified,1T delay	R/W	0x2

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