Digital Circuit and System
Lab05 Pattern

20240418

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SystemVerilog

- SystemVerilog is widely used in design and verification
- SystemVerilog uses the logic type as a general-purpose variable
  - logic w; // can be used in both assignment and procedure
  - logic in SystemVerilog = reg & wire in Verilog
- Almost all syntax of Verilog can be used in SystemVerilog.

Lab - Pattern

- In this lab, you need to write a pattern to verify the design we write, identify if there is any error.
- The only file you need to write is **pattern.sv** in 00_TESTBED folder.
- lab05.sv and lab05_X.sv (X = 1~5) are designs. lab05.sv is the correct design, while lab05_X.sv is the design with the SPEC-x error.
- You are not allowed to modify lab05.sv and lab05_X.sv.
- You are not allowed to modify PATNUM = 100 in pattern.sv.
- You can refer to the pattern of HW2.

Lab - Pattern

- Input and output signals:

Signal	I/O	Bit Width	Description
clk	I	1	Clock signal (Posedge design)
rst_n	I	1	Reset signal for active high asynchronous
in_number	I	4	Range (-8,7), pattern will give 4 numbers continuously
mode	I	1	Corresponding to four operation modes.
in_valid	I	1	Set high when giving in_number
out_result	O	7	Output data port
out_valid	O	1	Valid output signal (High for 1 cycle)

Lab - Pattern

- mode:
  - First, the four input values (in_1 to in_4) need to be sorted in ascending order. Assuming after sorting, sort_1 is the smallest, and sort_4 is the largest.

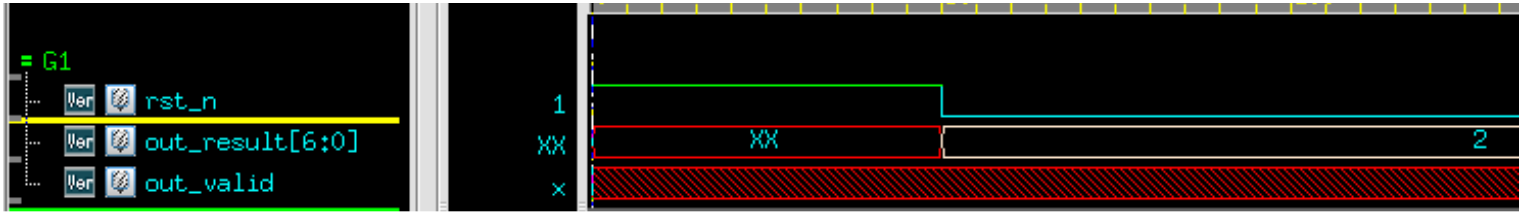
mode	Description
0	out_result = sort_1 + sort_2
1	out_result = sort_2 - sort_1
2	out_result = sort_4 - sort_3
3	out_result = sort_1 - sort_4

SPEC

- Spec1 : All output signals should be reset after the reset signal is asserted.
- Spec2 : The out_valid must be high for exact 1 cycles during output.
- Spec3 : The out_valid cannot overlap with in_valid at any time.
- Spec4 : The execution latency is limited in 100 cycles. The latency is the clock cycles between the falling edge of the in_valid and the rising edge of the out_valid.
- Spec5 : The out_result should correct when out_valid is high.

Output & Waveform

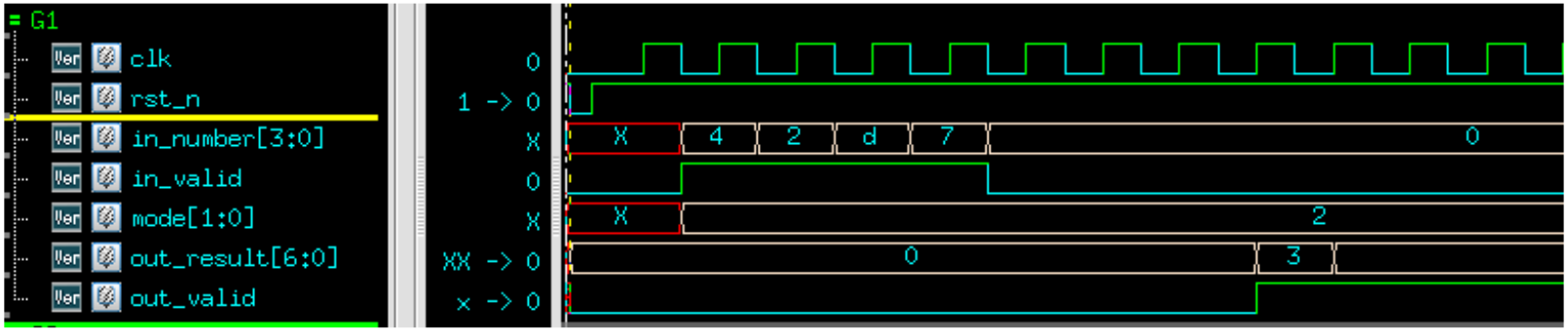
- SPEC1 error
  - All output signals should be reset after the reset signal is asserted.




```
SPEC1!
Reset
```

Output & Waveform

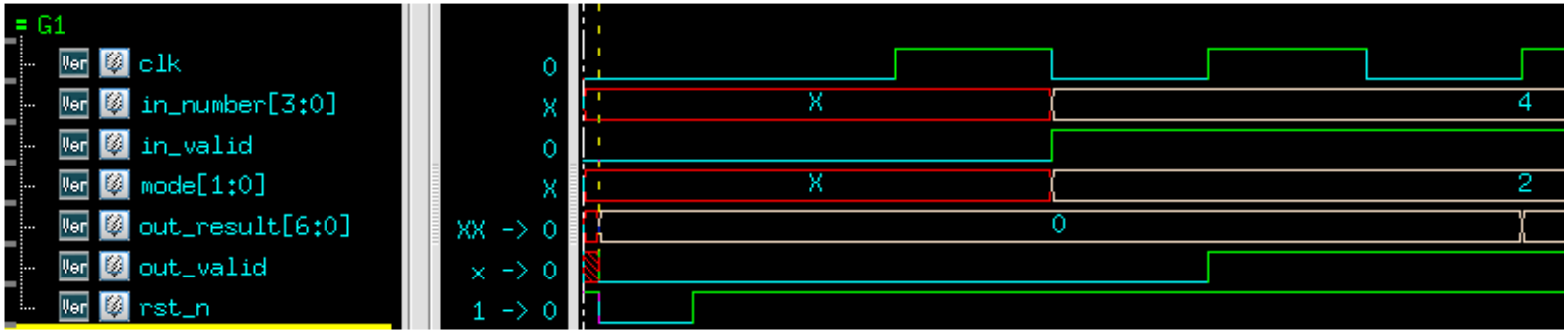
- SPEC2 error
  - The out_valid must be high for exact 1 cycles during output




```
SPEC2!
Output should be zero after check
```

Output & Waveform

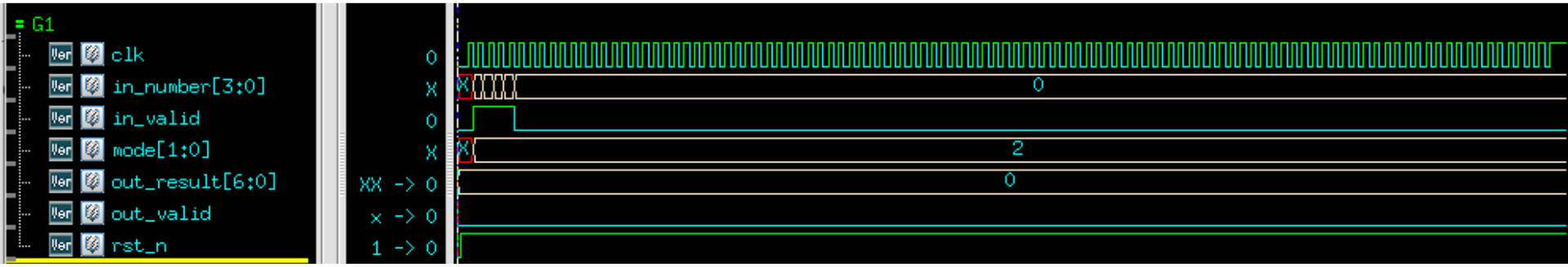
- SPEC3 error
  - The out_valid cannot overlap with in_valid at any time.




```
--------------------------------------------------------------
                          SPEC3!
    Outvalid should be zero before give data finish
--------------------------------------------------------------
```

Output & Waveform

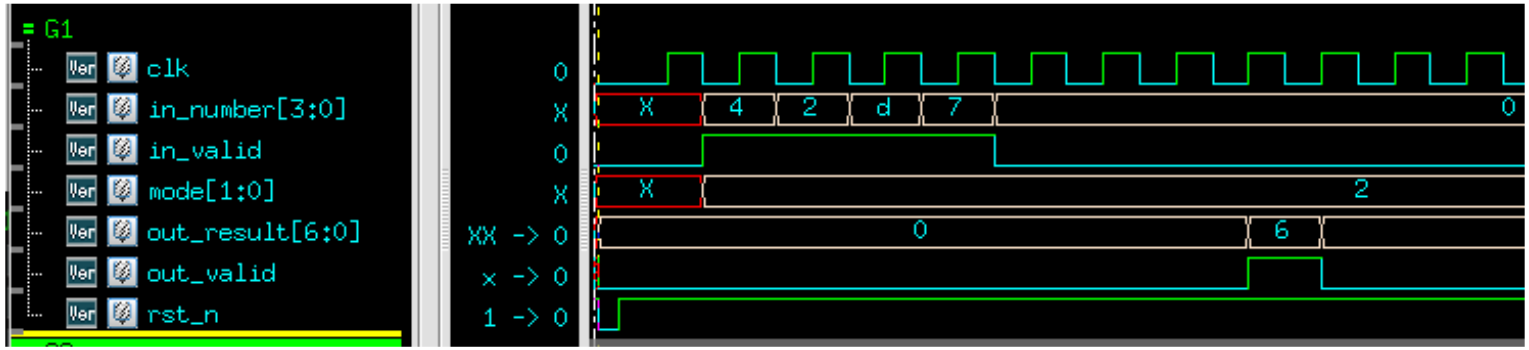
- SPEC4 error
  - The execution latency is limited in 100 cycles. The latency is the clock cycles between the falling edge of the in_valid and the rising edge of the out_valid.




```
--------------------------------------------------------
                      SPEC4!
   The execution latency are over 100  cycles
--------------------------------------------------------
```

Output & Waveform

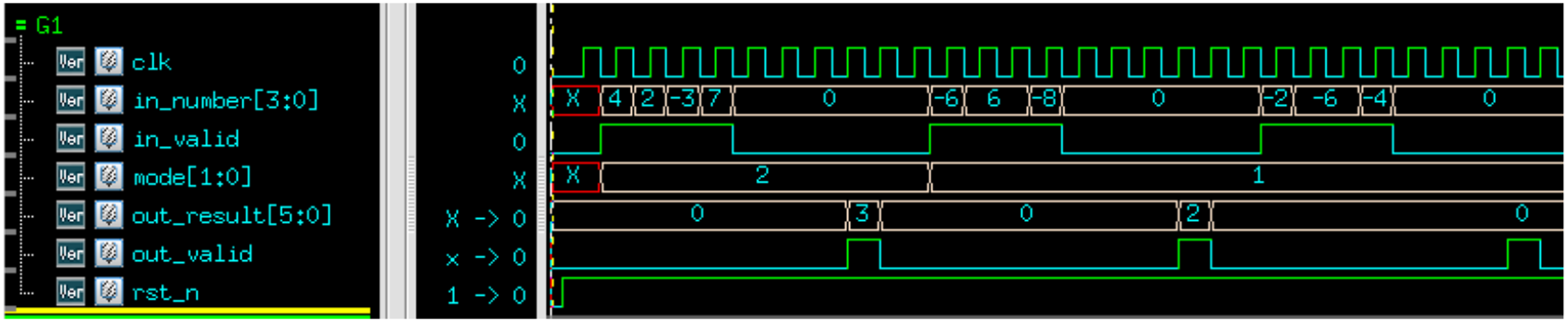
- SPEC5 error
  - The out_result should be correct when out_valid is high.
  - golden means the proper answer.




```
--------------------------------------------------------
                          SPEC5!
        YOUR:    6
        GOLDEN:    3
--------------------------------------------------------
```

Output & Waveform

- PASS
  - All the output_result should be correct and you can't violate any SPEC




```
----------------------------------------
        Congratulations!
You have passed all patterns!
        time:  1001500 ns
----------------------------------------
```

Output & Waveform

- ./07_check_pattern
  - Run the 6 commands.

```
14:43 DCS150@ee24[~/Lab05/01_RTL]$ ./07_check_pattern
**************************************************************************
* Please make sure you include the encrypted design in your TESTBED.v *
**************************************************************************
--- CORRECT DESING check Pass ---
--- SPEC 1 check Pass ---
--- SPEC 2 check Pass ---
--- SPEC 3 check Pass ---
--- SPEC 4 check Pass ---
--- SPEC 5 check Pass ---
--- PATTERN PASS !!! ---
14:46 DCS150@ee24[~/Lab05/01_RTL]$
```

```
14:43 DCS150@ee24[~/Lab05/01_RTL]$ ./07_check_pattern
**********************************************************
************
* Please make sure you include the encrypted design in your
 TESTBED.v *
**********************************************************
************
--- CORRECT DESING check Pass ---
--- SPEC 1 check Fail ---
```

Score

- Finish this Lab:
  - Today: 100 points
  - On Friday: 100 points
  - On Saturday: 80 points
  - On Sunday: 60 points
  - On Monday: 40 points
  - On Tuseday: 20 points
  - After Monday: 0 points

Command List

- Extract files from TA's directory (home directory): (It will be valid at 16:30 p.m.)
  - **tar -xvf ~DCSTA01/Lab05.tar**
- Verilog RTL simulation (01_RTL/):
  - **./01_run_spec1 : run for check spec1(should display SPEC1 Fail)**
  - **./01_run_spec2 : run for check spec2(should display SPEC2 Fail)**
  - **./01_run_spec3 : run for check spec3(should display SPEC3 Fail)**
  - **./01_run_spec4 : run for check spec3(should display SPEC4 Fail)**
  - **./01_run_spec5 : run for check spec4(should display SPEC5 Fail)**
  - **./01_run : run for right design(should display Congratulation)**
  - **./07_check_pattern : run the 6 commands above continuously.**
- Observe waveform to debug
  - **nWave &**
  - find *.fsdb
  - shift + L for reload fsdb file

Command List

- Submit your Lab:
  - **cd 09_SUBMIT**
  - **./00_tar 10**
    - 10 means the cycle time in this design. Don’t modify in this Lab.
  - **./01_submit**
  - **./02_check**