

NYCU-DCS-2024

HW1

Design: Central Processing Unit (CPU) - ALU & ID unit

Data Preparation

1. Extract test data from TA's directory:

```
% tar xvf ~DCSTA01/HW01.tar
```

Design Description

A Central processing unit (CPU) plays a crucial role in a computer. It is the primary component responsible for executing the instructions of a computer program. This includes performing arithmetic and logic operations, managing control, and handling I/O tasks.

In this homework, you have to design an ALU (Arithmetic Logic Unit) and an ID (Instruction Decoder) unit of a 16-bits CPU with 16 registers. Each instruction will carry out different operations based on ISA. Finally, the result of your operations will be stored in a certain memory location. The instruction format involved in this homework is shown below:

- Instruction Format - (16-bits)			
MSB			LSB
opcode (3-bits)	rs (4-bits)	rt (4-bits)	immediate (5-bits)

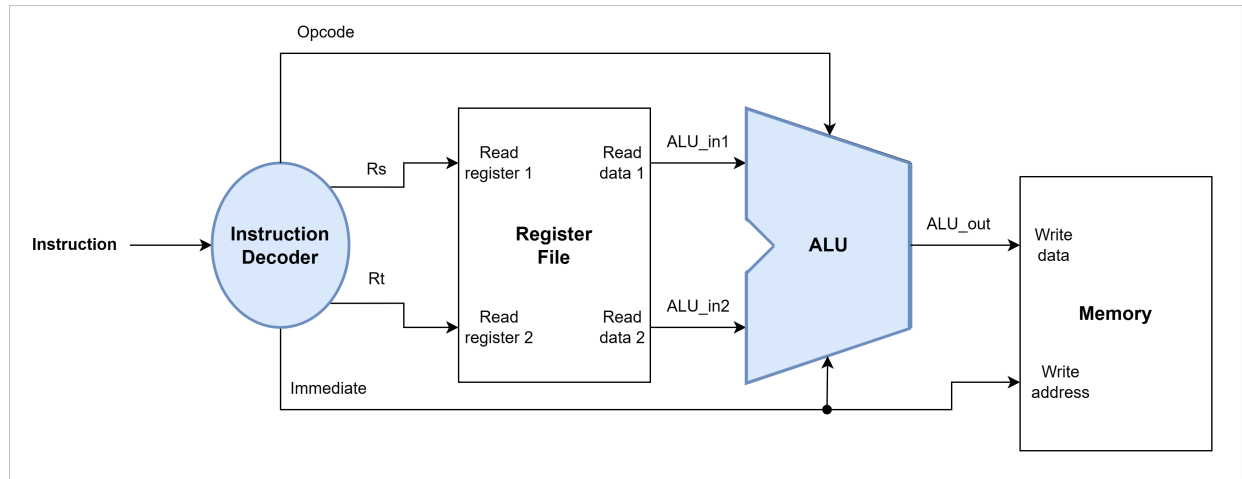
Rs and Rt signify the addresses of specific registers. With 4-bit register addresses, there are 16 available registers. Each of these registers can hold 16 bits of data. The instruction decoder (ID) unit must assign the relevant bits to the register file, enabling the arithmetic logic unit (ALU) to access the necessary data for its operations.

Immediate refers to a memory address. A 5-bit immediate value indicates that there are 32 distinct memory blocks available. In your architecture, the ID unit needs to assign the relevant bits to this memory, which allows the ALU to direct its results to the correct memory location.

Opcode indicates which function ALU will execute; details are as shown below:

Function Name	Operation	op code
Add	Out = R[rs] + R[rt]	3'b000
Mult	Out = R[rs] x R[rt]	3'b001
And	Out = R[rs] & R[rt]	3'b010
Inverse	Out = ~R[rs]	3'b011
Absolute Value	Out = R[rs]	3'b100
Minimum	Out = min(R[rs], R[rt])	3'b101
Left Shift	Out = R[rs] << unsigned(Imm)	3'b110
Addi	Out = R[rs] + sign extended(Imm)	3'b111

Block Diagram



Input

Signal	Number of bit	Description
Instruction	16 bits	After Instruction Decoder gets the Instruction, you should separate the Instruction into "opcode" 、"rs" 、"rt" 、"immediate", then send the specific part of Instruction to Register, ALU, and Memory.

Output

Signal	Number of bit	Description
ALU_out	16 bits	ALU would receive data from Register File, then do the function corresponding to the opcode send by Controller. After ALU operation, you should save calculate result to the Memory, and we will check data in the Memory to verify your design.

Homework Upload

1. Use the command we provided to tar whole file into HW1 folder.
2. Upload the tar file and your report file to the new E3.
3. Your report file should be followed the naming rule: report_DCSxxx.pdf.
4. Upload your file before 3/28 (Thu) 15:00.

Grading Policy

1. Pass all the pattern we provided. 70%
2. Report 30%

Report

Your report must contain:

1. A Screenshot of output result, the figure must contain **your server account** information, as shown in the figure below.
2. The problem encountered in this homework and how the problem was solved.
3. Any suggestions about previous Labs and homework.

```
0      0      19      19      PASS
0      0      31      31      PASS
-32256 -32256  9       9       PASS
9011   9011   26      26      PASS
8894   8894   6       6       PASS
268    268    18      18      PASS
3333   3333   13      13      PASS
0      0      23      23      PASS
0      0      17      17      PASS
4569   4569   24      24      PASS
17636  17636  3       3       PASS
0      0      26      26      PASS
0      0      5       5       PASS
5678   5678   29      29      PASS
3333   3333   5       5       PASS
0      0      23      23      PASS
4545   4545   24      24      PASS
168    168    9       9       PASS
4545   4545   30      30      PASS
1111   1111   20      20      PASS
8888   8888   11      11      PASS
1111   1111   18      18      PASS
-24576 -24576  13      13      PASS
5      5      6       6       PASS
-6667  -6667  27      27      PASS
10000  10000  20      20      PASS
13185  13185  20      20      PASS

Info: /OSCI/SystemC: Simulation stopped by user.
Number of pass cases: 53
Congratulation! Your design is correct!
14:42 DCSTA05@ee21[~/HW01]$
```

Command List

1. Compile & Run SystemC source code.
./01_systemc
2. Clean SystemC executable file.
./09_clean
3. Compress the files to be submitted.
./10_tar