CS M152A Project 1 Report

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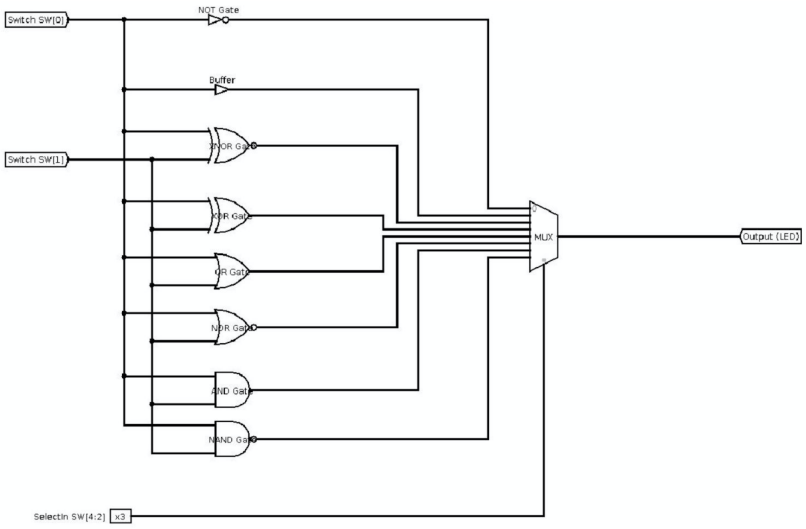
1 Introduction and Requirement

The focus of this lab is for students to get used to basics of Verilog as a hardware description language and to get more familiar with the Xilinx ISE as our simulation and synthesis tool. For the first part of the project, we built a combination circuit from a diagram provided in the project specification with various gates and multiplexers. In the second part of the project, we moved on to sequential circuits and built small modules revolving around counters. We implemented 4-bit Counter in two ways, one fully based on schematics provided and one with a higher level of abstraction. For the last part, we used counters to build a simple clock divider that can be used to flash LED signal at a frequency of $1Hz$ based on a $10kHz$ clock.

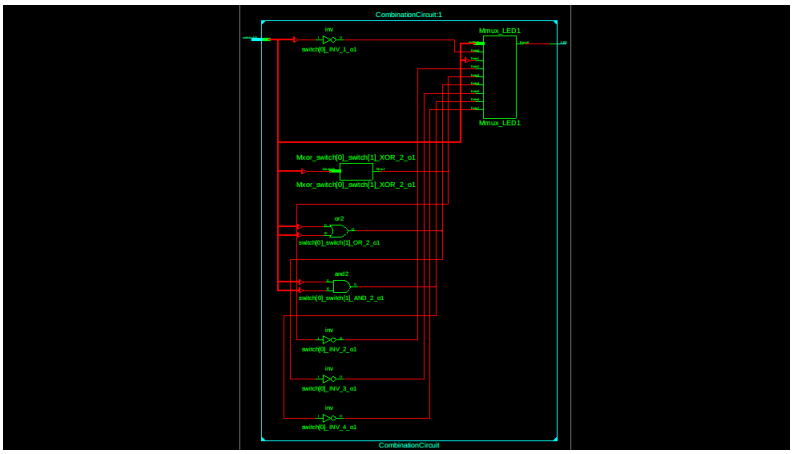
2 Design Description

a. **Combination Circuit**
For this part of the project, we implemented the combination circuit below:



Schematic of Combination Circuit provided in Project Guidelines

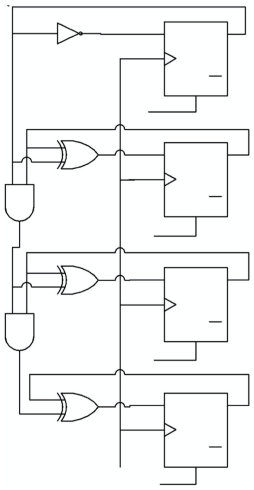
I designed one module named `CombinationCircuit` that takes in a 5-bit input `switch`, and outputs a one bit output `LED`. I used a switch statement based on `switch[4:2]` with 8 cases to implement the multiplexer. The select signal for the multiplexer comes from `switch[4:2]`. Each input into the multiplexer depends on the value of `switch[1:0]` and the operation from the circuit diagram. For example, if the select signal is `3'b111`, then we assign to `LED` the value of $\sim$`(switch[0]switch[1])` as corresponding to select signal `3'b111` is a nand gate in the diagram above.



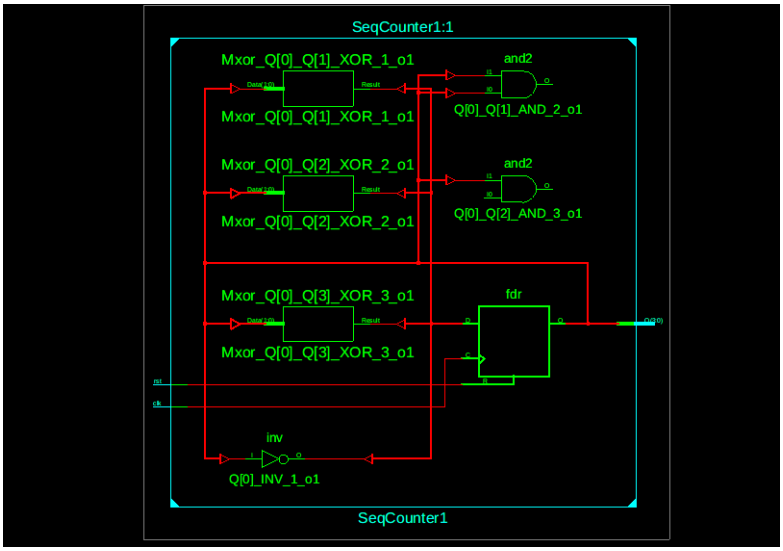
RTL Schematic for Combination Circuit

From the RTL schematic generated by the Xilinx ISE shown above, we can see that the hardware components in the diagram is very similar to the circuit diagram provided by the project guidelines. In the RTL schematic, different gates are used for different inputs into the multiplexer in order for different output to be computed based on the select signal.

b. **4-Bit Counter: Translating the Schematics**
For this part of the project, we designed a 4-bit counter with D flip-flops using gate-level hardware description based on the schematic below:


Schematic of 4-Bit Counter provided by Project Guidelines

I designed one module named `SeqCounter1` that takes in two 1-bit inputs `clk` and `rst`, and outputs a 4-bit output `Q` that represents the current value of the counter. Since the design of a counter is based on sequential circuits, I designed my module to have an `always` block that is triggered by `posedge clk`. Inside the `always` block, if `rst` is high, it will cause value of Q to be reset to 0. If `rst` is low, since we're translating the schematics, I map each gate to an operator and each flip-flop to a line inside the always block to execute the increment part of the counter. Thus, every time the `posedge clk` occurs, my `SeqCounter1` will increment the value of `Q` by 1 using the exact same gates and flipflops as the schematic above.



RTL Schematic for 4-Bit Counter based on Schematics

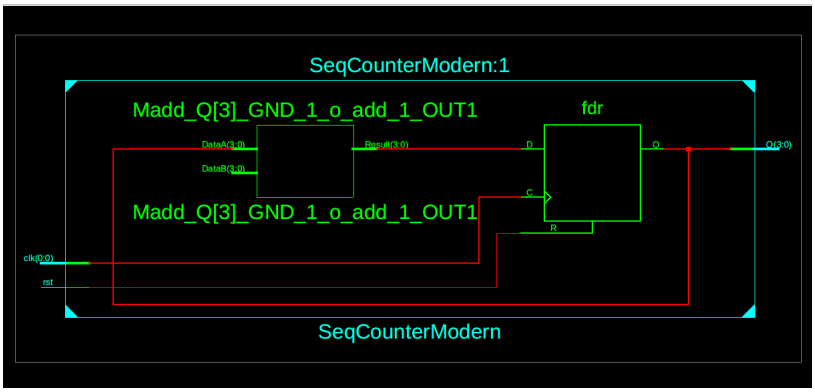
From the RTL schematic generated by the Xilinx ISE above, we can see that the hardware components used do not exactly match what is provided in the schematic in the project guidelines. Nevertheless, there are many similarities in the flip flop being used and gates being used. The two schematics are not identical even though they both accomplish the same task which is probably because Xilinx ISE tried to optimize our code for the specific FPGA we chose.

c. **4-Bit Counter: Modern Version**

For this part of the project, we created the same 4-bit counter but instead of basing the implementation directly on a schematic, we use higher level abstraction provided by Verilog HDL.

I designed one module named `SeqCounterModern` that takes in two 1-bit inputs `clk` and `rst`, and outputs a 4-bit output `Q` that represents the current value of the counter. This module takes in the exact same input and output the same values as `SeqCounter1`, but the implementation varies in that instead of using gates and 4 flipflops, we use the addition operator provided by Verilog. The line `Q <= Q + 1'b1` works the same way as the gates and flipflops in the schematic for `SeqCounter1`. Similar to `SeqCounter1`, the `rst` signal with an `if` statement takes care of resetting value of `Q` to 0.

The modern implementation of the 4-bit Counter appears much simpler than the Schematics version, but it is important for us to be aware of the hardware underlying our Verilog code.



RTL Schematic for Modern 4-Bit Counter

From the RTL schematic generated by Xilinx ISE above, we can observe an adder connected to a flip flop as major hardware components. This matches our design as the `SeqCounterModern` module

simply uses the `+` operator to increment output `Q` on every `posedge clk`. The `+` operator corresponds to the adder and flip flop(register) stores value of `Q` until next `posedge clk`.

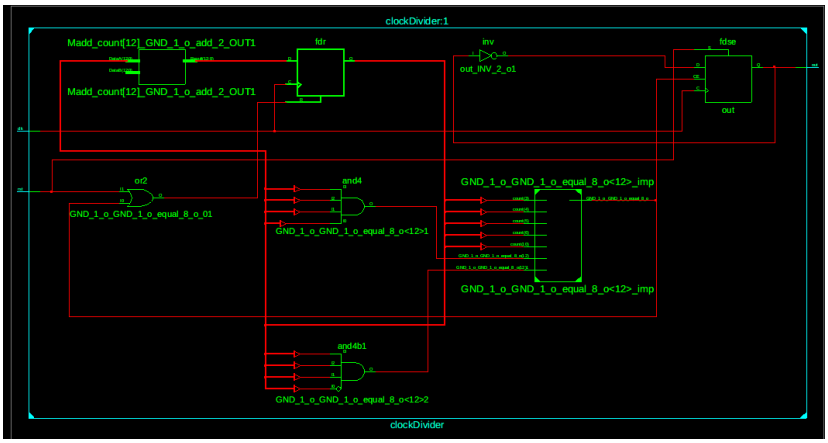
d. **Clock Divider: Counter in Action**

In this part of the project, I designed and implemented clock dividers using the concept of counters. The project specified us to build a flashing LED with a frequency of $1Hz$ and in the test bench we should design and use a $10kHz$ clock.

To build the divider, I created a module `clockDivider` that takes in two 1-bit signals `clk` and `rst` as inputs and outputs a 1-bit signal `out`, which should be high every 1 second. In order to keep track how much time has passed we use the `clk` signal, a 13-bit register `count`, and a local parameter `constNumber = 5000`. `constNumber` represents the value our counter will count until, it is set to 5000 as we have a $10kHz$ clock and we want the LED to flash at $1Hz$ i.e. flash every one second. Since clock is at a 10000x higher frequency than our LED flash frequency, we want signal `out` to be high every time clock hits 10000 iterations(reaches `posedge` 10000 times). We use register `count` to keep track of number of iterations clock has had a `posedge`, when `count` is 5000, this means that signal of `flash` needs to flip in order for LED to flash(`out` to be switched to high) every 1 second. Thus, our register `count` needs to be 13 bits as the highest value `count` will store is 5000 and $\log_2(5000) = 13$.

In my module, I have two `always` blocks. The first `always` block takes care of incrementing `count` and resetting `count` when `count` hits 5000 or when `rst` is high. The second `always` block takes care of flipping signal of `out` when `count` hits 5000 and keeping the signal of `out` the same at all other times or 1 when `rst` is high.

With the above implementation, the `out` signal will flash(turn on) at a frequency of $1Hz$ if a clock signal of $10kHz$ is passed in as the `clk` parameter.



RTL Schematic for Clock Divider

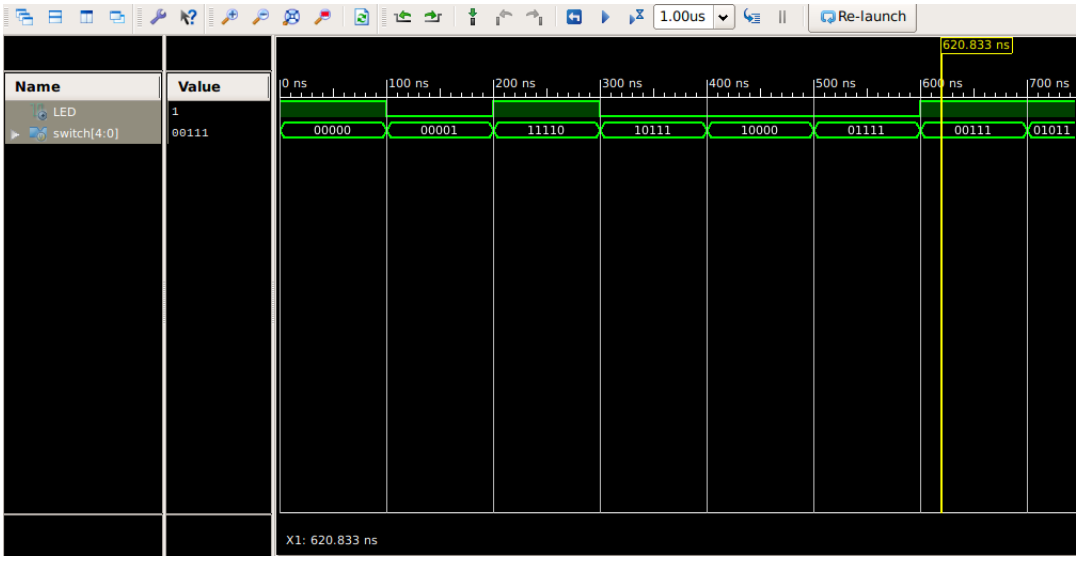
From the RTL schematic generated by the Xilinx ISE above, we can see that our `clockDivider` module is more complicated than our previous three modules. We can observe registers being used to store values of `count` and output value, adder being used to increment `count`, and comparators being used to compare values of `count` and local parameter`constNumber`.

3 Simulation Documentation

a. **Combination Circuit**

For the Combination Circuit Module, in my test bench I tested different values of `switch [4:0]` and observed how they change the value of output `LED`. For example, when `switch [4:0] = 5'b00000`, according to the schematic, the output LED should be the invert `switch[0]`, which should be 1. As shown in the first 100ns of the simulation waveform, when `switch [4:0] = 5'b00000`, LED = 1. In the next 100ns, the input `switch [4:0] = 5'b00001`, thus the output LED should be the

invert `switch[0]`, which should be 0 and it is 0 in the simulation waveform. At 200ns, `switch [4:0] = 5'b11110`, so according to the schematics, the nand operation should be done on `switch[0]`, `switch[1]` and should result in LED = 1, which matches output in waveform below.

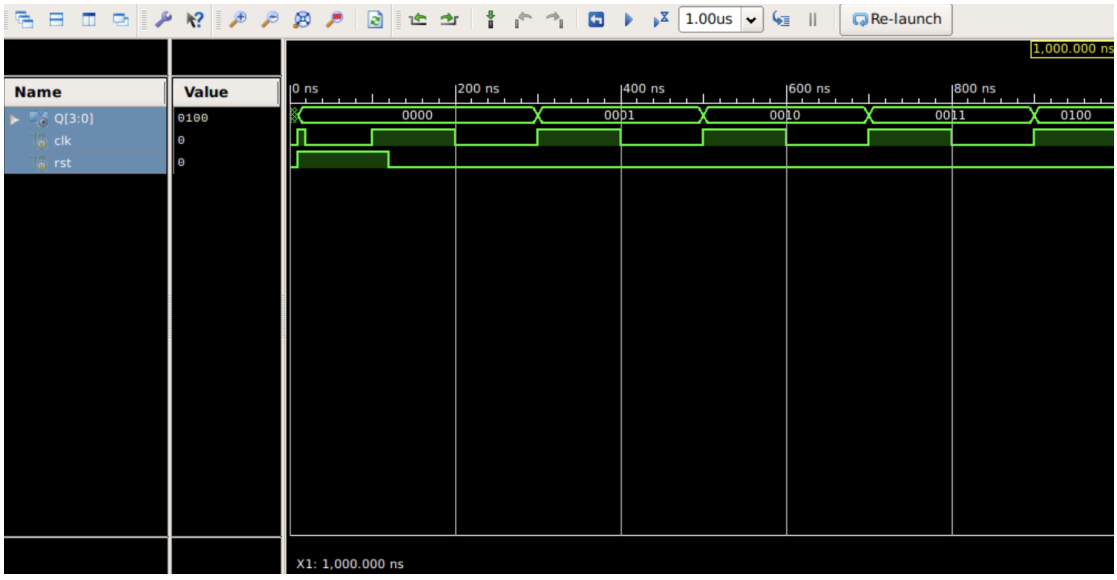


Simulation Waveform for Combination Circuit

Synthesis and Implementation Report included at end of document.

b. **4-Bit Counter: Translating the Schematics**

For this part of the project, my test bench flips the clock signal in order to trigger the `always` block to increment our 4-bit counter. A correct 4-bit counter should increment its output by 1 each time a `posedge clk` occurs. Below is the output waveform of my test bench:



Simulation Waveform for 4-Bit Counter(Schematics)

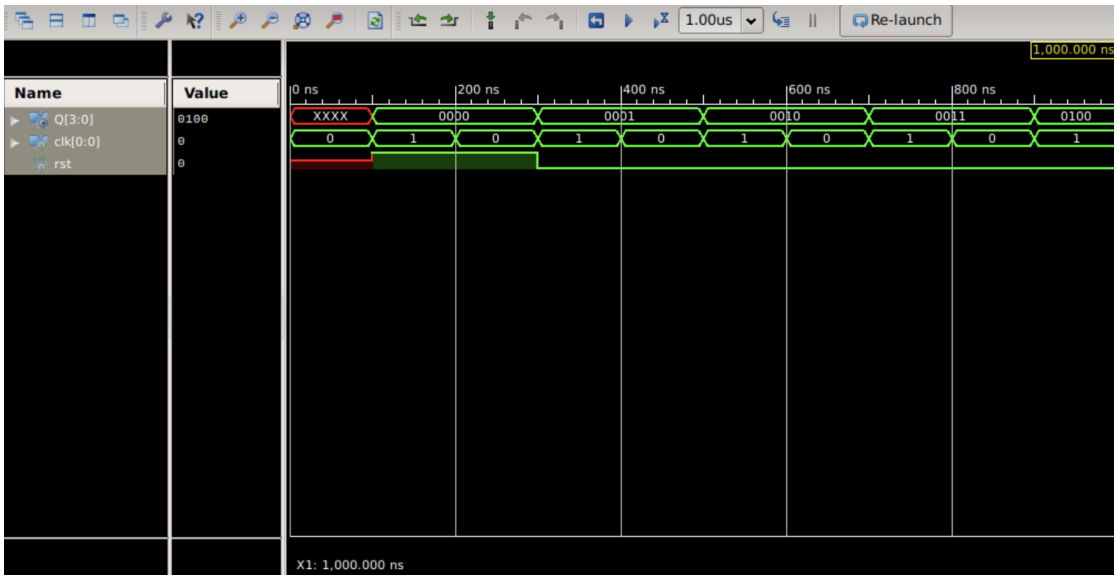
From the waveform diagram above, we can see that when `rst` is high and `clk` has a `posedge`, the output `Q` is set to 0. When `rst` is low and `clk` has a `posedge`, the output `Q` increments by 1 at every `posedge`. The waveform from my test bench highlights that the 4-bit counter implemented based on the schematics works as stated by the specifications.

As I implemented the `SeqCounter1` module, my test bench and wave form helped me realized that early on I had a bug where my output `Q` was always `xxxx`. I realized that the reason for this error was in the start of my test bench when I set `rst` to high, it was not detected by my `always` block as I switched `rst` back to low prior to occurrence of `posedge clk`.

Synthesis and Implementation Report included at end of document.

c. **4-Bit Counter: Modern Version**

My test bench for this part of the project is the same as my test bench for the schematics version of 4-Bit Counter as different implementation of 4-bit counter should receive the same outputs given the same inputs. Below is the output wave form of my test bench:



Simulation Waveform for 4-Bit Counter(Modern)

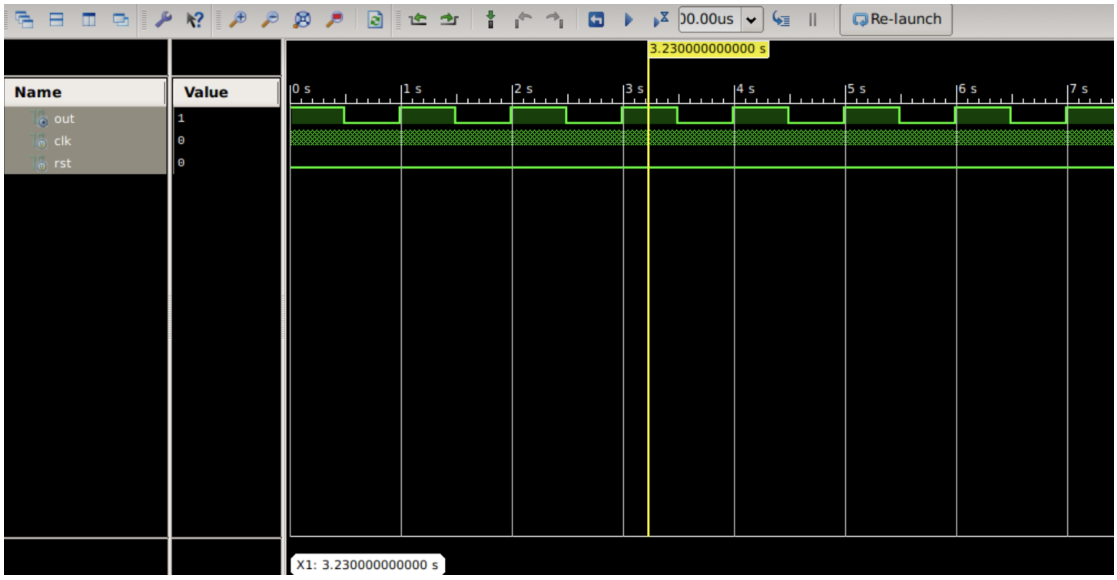
From the diagram above, we can see that before both `rst` is high and `posedge clk` the output `Q` is `xxxx`. But after `rst` is high and `posedge clk`, the value of `Q` is correctly 0. Once `rst` is low, at every `posedge clk` output `Q` increments by 1. Thus, from the wave form diagram, we know that the modern implementation of 4-bit Counter works as specified by the project guidelines.

Synthesis and Implementation Report included at end of document.

d. **Clock Divider: Counter in Action**

To test to see if my Clock Divider can actually flash a LED at a frequency of $1Hz$, I implemented a $10kHz$ clock in my test bench. The $10kHz$ clock is easily implemented by an `always` block that simply flips the `clk` with a 50000ns delay. With this $10kHz$ clock, our implementation of clock divider should output signal `flash` as high at a frequency of $1Hz$ i.e. once every second.

The wave form from my test bench is shown below:



Simulation Waveform for Clock Divider

From the diagram above, we can see that indeed every second, the output signal switches from low to high. Thus, if the output signal was an LED, it would flash at frequency of $1Hz$.

One bug I encountered as I tested my module was that my output signal did not appear to change and stayed high for the entirety of the simulation. After some debugging, I realize that my simulation was not running long enough for the output signal to change.

Synthesis and Implementation Report included at end of document.

4 Additional Questions

What is a ".ucf" file? How would you use it for Nexys3 in an actual setting on a real board to connect the inputs of the combinational circuitry to the switches on the FPGA?

Answer: A ".ucf" file in Xilinx is a constraints file format. It helps apply constraints to the Xilinx tool, such as pin mappings and timing based on your hardware. For us, we can use it to find out information about how to connect inputs of combinational circuitry to switches on the FPGA. For example, the ".ucf" file can tell us which pins we should use to connect external hardware components that our module will interact with for Nexys3. Without the ".ucf" file, it will be extremely difficult for us to know how our Verilog module will interact with Nexys3 and its hardware components.

5 Conclusion

In this project, I designed and implemented four different modules and tested each of them with its own test bench in order to gain a better understanding of Verilog and how the Xilinx ISE works. The first module is an implementation of a Combination Circuit provided by the project guidelines. It was implemented with Verilog operators and a case statement to describe a multiplexer. The second module is an implementation of a sequential 4-bit Counter based on the schematic provided. The implementation uses logic gates and 4 d flip flops, which is more complicated than the implementation in the third module. Third module implements the same 4-bit Counter but with a higher level of abstraction, directly using the plus operator provided by Verilog. The last module is a clock divider that is used to flash LED(output signal) at frequency of $1Hz$ implemented using two `always` blocks, comparators to check when signal of LED should be flipped, and concept of counter in the previous two modules.

Some challenges I faced during this project include initializing the values of signal in test bench and navigating through various parts of the Xilinx ISE to generate different reports. I was able to overcome these difficulties by looking through notes provided by the TA and debugging through looking at the wave form diagrams.

6 Reports

6.1 Synthesis Report for Combination Circuit

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Reading design: CombinationCircuit.prj

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  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
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            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "CombinationCircuit.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "CombinationCircuit"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : CombinationCircuit
```

```
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/melody/152a/Project_1/comb_circuit.v" into library work
Parsing module <CombinationCircuit>.

=========================================================================
```

```
*                            HDL Elaboration                           *
=========================================================================

Elaborating module <CombinationCircuit>.

=========================================================================
*                            HDL Synthesis                             *
=========================================================================

Synthesizing Unit <CombinationCircuit>.
    Related source file is "/home/melody/152a/Project_1/comb_circuit.v".
    Found 1-bit 8-to-1 multiplexer for signal <LED> created at line 27.
    Summary:
inferred   1 Multiplexer(s).
Unit <CombinationCircuit> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Multiplexers                                          : 1
 1-bit 8-to-1 multiplexer                               : 1
# Xors                                                  : 1
 1-bit xor2                                             : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                         *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Multiplexers                                          : 1
 1-bit 8-to-1 multiplexer                               : 1
# Xors                                                  : 1
 1-bit xor2                                             : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                          *
=========================================================================

Optimizing unit <CombinationCircuit> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block CombinationCircuit, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
```

```
================================================================================

================================================================================
*                           Partition Report                                   *
================================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

================================================================================
*                           Design Summary                                     *
================================================================================

Top Level Output File Name         : CombinationCircuit.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 1
#      LUT5                        : 1
# IO Buffers                       : 6
#      IBUF                        : 5
#      OBUF                        : 1

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                  1  out of   9112     0%
    Number used as Logic:               1  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    1
   Number with an unused Flip Flop:     1  out of      1   100%
   Number with an unused LUT:           0  out of      1     0%
   Number of fully used LUT-FF pairs:   0  out of      1     0%
   Number of unique control sets:       0

IO Utilization:
 Number of IOs:                         6
 Number of bonded IOBs:                 6  out of    232     2%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

```
=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 5.499ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 5 / 1
-------------------------------------------------------------------------
Delay:               5.499ns (Levels of Logic = 3)
  Source:            switch<1> (PAD)
  Destination:       LED (PAD)

  Data Path: switch<1> to LED
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.924  switch_1_IBUF (switch_1_IBUF)
     LUT5:I0->O            1   0.203   0.579  Mmux_LED_2_f7 (LED_OBUF)
     OBUF:I->O                 2.571          LED_OBUF (LED)
    ----------------------------------------
    Total                      5.499ns (3.996ns logic, 1.503ns route)
                                       (72.7% logic, 27.3% route)

=========================================================================

Cross Clock Domains Report:
---------------------------

=========================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.30 secs

-->
```

```
Total memory usage is 385580 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

6.2 Implementation Report for Combination Circuit

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'CombinationCircuit'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o CombinationCircuit_map.ncd CombinationCircuit.ngd
CombinationCircuit.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Apr 19 16:31:23 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    0 out of  18,224    0%
  Number of Slice LUTs:                         1 out of   9,112    1%
    Number used as logic:                       1 out of   9,112    1%
      Number using O6 output only:              1
      Number using O5 output only:              0
      Number using O5 and O6:                   0
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   2,176    0%

Slice Logic Distribution:
  Number of occupied Slices:                    1 out of   2,278    1%
  Number of MUXCYs used:                        0 out of   4,556    0%
  Number of LUT Flip Flop pairs used:           1
    Number with an unused Flip Flop:            1 out of       1  100%
    Number with an unused LUT:                  0 out of       1    0%
    Number of fully used LUT-FF pairs:          0 out of       1    0%
    Number of slice register sites lost
      to control set restrictions:              0 out of  18,224    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        6 out of     232    2%

Specific Feature Utilization:
  Number of RAMB16BWERs:                        0 out of      32    0%
  Number of RAMB8BWERs:                         0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:            0 out of      32    0%
  Number of BUFG/BUFGMUXs:                      0 out of      16    0%
  Number of DCM/DCM_CLKGENs:                    0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                  0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:        0 out of     248    0%
```

```
  Number of OLOGIC2/OSERDES2s:                  0 out of     248    0%
  Number of BSCANs:                             0 out of       4    0%
  Number of BUFHs:                              0 out of     128    0%
  Number of BUFPLLs:                            0 out of       8    0%
  Number of BUFPLL_MCBs:                        0 out of       4    0%
  Number of DSP48A1s:                           0 out of      32    0%
  Number of ICAPs:                              0 out of       1    0%
  Number of MCBs:                               0 out of       2    0%
  Number of PCILOGICSEs:                        0 out of       2    0%
  Number of PLL_ADVs:                           0 out of       2    0%
  Number of PMVs:                               0 out of       1    0%
  Number of STARTUPs:                           0 out of       1    0%
  Number of SUSPEND_SYNCs:                      0 out of       1    0%

Average Fanout of Non-Clock Nets:               1.00

Peak Memory Usage:  669 MB
Total REAL time to MAP completion:  5 secs
Total CPU time to MAP completion:   4 secs

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Section 5 - Removed Logic
Section 6 - IOB Properties
Section 7 - RPMs
Section 8 - Guide Report
Section 9 - Area Group and Partition Summary
Section 10 - Timing Report
Section 11 - Configuration String Information
Section 12 - Control Set Information
Section 13 - Utilization by Hierarchy

Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------
```

Section 5 - Removed Logic

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Sle Rat
LED	IOB	OUTPUT	LVCMOS25		12	SLO
switch<0>	IOB	INPUT	LVCMOS25			
switch<1>	IOB	INPUT	LVCMOS25			
switch<2>	IOB	INPUT	LVCMOS25			
switch<3>	IOB	INPUT	LVCMOS25			
switch<4>	IOB	INPUT	LVCMOS25			

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

```
-----------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-----------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```

6.3 Synthesis Report for 4-Bit Counter (Schematics)

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.06 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.06 secs

-->
Reading design: SeqCounter1.prj

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  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "SeqCounter1.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "SeqCounter1"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : SeqCounter1
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
```

```
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/melody/152a/Project_1/seq-counter-1.v" into library work
Parsing module <SeqCounter1>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================
```

```
Elaborating module <SeqCounter1>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <SeqCounter1>.
    Related source file is "/home/melody/152a/Project_1/seq-counter-1.v".
    Found 4-bit register for signal <Q>.
    Summary:
inferred   4 D-type flip-flop(s).
Unit <SeqCounter1> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                          : 1
 4-bit register                                      : 1
# Xors                                               : 3
 1-bit xor2                                          : 3

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                          : 4
 Flip-Flops                                          : 4
# Xors                                               : 3
 1-bit xor2                                          : 3

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <SeqCounter1> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block SeqCounter1, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 4
 Flip-Flops                                          : 4
```

```
================================================================================

================================================================================
*                           Partition Report                                   *
================================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

================================================================================
*                           Design Summary                                     *
================================================================================

Top Level Output File Name         : SeqCounter1.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 4
#      INV                         : 1
#      LUT2                        : 1
#      LUT3                        : 1
#      LUT4                        : 1
# FlipFlops/Latches                : 4
#      FDR                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 5
#      IBUF                        : 1
#      OBUF                        : 4

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              4  out of  18224     0%
 Number of Slice LUTs:                   4  out of   9112     0%
    Number used as Logic:                4  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     8
   Number with an unused Flip Flop:      4  out of      8    50%
   Number with an unused LUT:            4  out of      8    50%
   Number of fully used LUT-FF pairs:    0  out of      8     0%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                          6
 Number of bonded IOBs:                  6  out of    232     2%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
```

```
--------------------------
Partition Resource Summary:
--------------------------

  No Partitions were found in this design.

--------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.048ns (Maximum Frequency: 488.317MHz)
   Minimum input arrival time before clock: 2.335ns
   Maximum output required time after clock: 3.732ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.048ns (frequency: 488.317MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               2.048ns (Levels of Logic = 1)
  Source:            Q_0 (FF)
  Destination:       Q_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: Q_0 to Q_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.714  Q_0 (Q_0)
     INV:I->O              1   0.206   0.579  Q[0]_INV_1_o1_INV_0 (Q[0]_INV_1_o)
```

```
     FDR:D                     0.102          Q_0
    ----------------------------------------
    Total                      2.048ns (0.755ns logic, 1.293ns route)
                                       (36.9% logic, 63.1% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              2.335ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       Q_0 (FF)
  Destination Clock: clk rising

  Data Path: rst to Q_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   1.222   0.683  rst_IBUF (rst_IBUF)
     FDR:R                     0.430          Q_0
    ----------------------------------------
    Total                      2.335ns (1.652ns logic, 0.683ns route)
                                       (70.8% logic, 29.2% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              3.732ns (Levels of Logic = 1)
  Source:            Q_0 (FF)
  Destination:       Q<0> (PAD)
  Source Clock:      clk rising

  Data Path: Q_0 to Q<0>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.714  Q_0 (Q_0)
     OBUF:I->O                 2.571          Q_0_OBUF (Q<0>)
    ----------------------------------------
    Total                      3.732ns (3.018ns logic, 0.714ns route)
                                       (80.9% logic, 19.1% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.048|         |         |         |
---------------+---------+---------+---------+---------+

==========================================================================
```

```
Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.50 secs

-->


Total memory usage is 394648 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

6.4 Implementation Report for 4-Bit Counter (Schematics)

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'SeqCounter1'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o SeqCounter1_map.ncd SeqCounter1.ngd
SeqCounter1.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Apr 19 16:30:06 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    4 out of  18,224    1%
    Number used as Flip Flops:                  4
    Number used as Latches:                     0
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:               0
  Number of Slice LUTs:                         4 out of   9,112    1%
    Number used as logic:                       4 out of   9,112    1%
      Number using O6 output only:              4
      Number using O5 output only:              0
      Number using O5 and O6:                   0
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   2,176    0%

Slice Logic Distribution:
  Number of occupied Slices:                    1 out of   2,278    1%
  Number of MUXCYs used:                        0 out of   4,556    0%
  Number of LUT Flip Flop pairs used:           4
    Number with an unused Flip Flop:            0 out of       4    0%
    Number with an unused LUT:                  0 out of       4    0%
    Number of fully used LUT-FF pairs:          4 out of       4  100%
    Number of unique control sets:              1
    Number of slice register sites lost
      to control set restrictions:              4 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        6 out of     232    2%

Specific Feature Utilization:
  Number of RAMB16BWERs:                        0 out of      32    0%
  Number of RAMB8BWERs:                         0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                0 out of      32    0%
```

```
  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       1 out of      16    6%
    Number used as BUFGs:                        1
    Number used as BUFGMUX:                      0
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                   0 out of     248    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of      32    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of MCBs:                                0 out of       2    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                3.17

Peak Memory Usage:  672 MB
Total REAL time to MAP completion:  6 secs
Total CPU time to MAP completion:   6 secs

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Section 11 - Configuration String Information
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Section 13 - Utilization by Hierarchy

Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
```

```
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------

Section 5 - Removed Logic
-------------------------

Section 6 - IOB Properties
--------------------------

+----------------------------------------------------------------------------------------------------------------------
| IOB Name                          | Type             | Direction | IO Standard          | Diff  | Drive    | Sle
|                                   |                  |           |                      | Term  | Strength | Rat
+----------------------------------------------------------------------------------------------------------------------
| Q<0>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<1>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<2>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<3>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| clk                               | IOB              | INPUT     | LVCMOS25             |       |          |
| rst                               | IOB              | INPUT     | LVCMOS25             |       |          |
+----------------------------------------------------------------------------------------------------------------------

Section 7 - RPMs
----------------

Section 8 - Guide Report
------------------------
Guide not run on this design.

Section 9 - Area Group and Partition Summary
--------------------------------------------

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Area Group Information
----------------------

  No area groups were found in this design.

----------------------

Section 10 - Timing Report
--------------------------
A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
```

```
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details
-----------------------------------------
Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information
------------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```

6.5 Synthesis Report for 4-Bit Counter (Modern)

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Reading design: SeqCounterModern.prj

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            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "SeqCounterModern.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "SeqCounterModern"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : SeqCounterModern
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
```

```
Safe Implementation               : No
FSM Style                         : LUT
RAM Extraction                    : Yes
RAM Style                         : Auto
ROM Extraction                    : Yes
Shift Register Extraction         : YES
ROM Style                         : Auto
Resource Sharing                  : YES
Asynchronous To Synchronous       : NO
Shift Register Minimum Size       : 2
Use DSP Block                     : Auto
Automatic Register Balancing      : No

---- Target Options
LUT Combining                     : Auto
Reduce Control Sets               : Auto
Add IO Buffers                    : YES
Global Maximum Fanout             : 100000
Add Generic Clock Buffer(BUFG)    : 16
Register Duplication              : YES
Optimize Instantiated Primitives  : NO
Use Clock Enable                  : Auto
Use Synchronous Set               : Auto
Use Synchronous Reset             : Auto
Pack IO Registers into IOBs       : Auto
Equivalent register Removal       : YES

---- General Options
Optimization Goal                 : Speed
Optimization Effort               : 1
Power Reduction                   : NO
Keep Hierarchy                    : No
Netlist Hierarchy                 : As_Optimized
RTL Output                        : Yes
Global Optimization               : AllClockNets
Read Cores                        : YES
Write Timing Constraints          : NO
Cross Clock Analysis              : NO
Hierarchy Separator               : /
Bus Delimiter                     : <>
Case Specifier                    : Maintain
Slice Utilization Ratio           : 100
BRAM Utilization Ratio            : 100
DSP48 Utilization Ratio           : 100
Auto BRAM Packing                 : NO
Slice Utilization Ratio Delta     : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/melody/152a/Project_1/seq-counter-modern.v" into library work
Parsing module <SeqCounterModern>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================
```

```
Elaborating module <SeqCounterModern>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <SeqCounterModern>.
    Related source file is "/home/melody/152a/Project_1/seq-counter-modern.v".
    Found 4-bit register for signal <Q>.
    Found 4-bit adder for signal <Q[3]_GND_1_o_add_1_OUT> created at line 31.
    Summary:
inferred   1 Adder/Subtractor(s).
inferred   4 D-type flip-flop(s).
Unit <SeqCounterModern> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 4-bit adder                                          : 1
# Registers                                            : 1
 4-bit register                                       : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <SeqCounterModern>.
The following registers are absorbed into counter <Q>: 1 register on signal <Q>.
Unit <SeqCounterModern> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 1
 4-bit up counter                                     : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <SeqCounterModern> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block SeqCounterModern, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report
```

```
Macro Statistics
# Registers                                          : 4
 Flip-Flops                                          : 4

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : SeqCounterModern.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 4
#      INV                         : 1
#      LUT2                        : 1
#      LUT3                        : 1
#      LUT4                        : 1
# FlipFlops/Latches                : 4
#      FDR                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 5
#      IBUF                        : 1
#      OBUF                        : 4

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              4  out of  18224     0%
 Number of Slice LUTs:                   4  out of   9112     0%
    Number used as Logic:                4  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     8
   Number with an unused Flip Flop:      4  out of      8    50%
   Number with an unused LUT:            4  out of      8    50%
   Number of fully used LUT-FF pairs:    0  out of      8     0%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                          6
```

```
 Number of bonded IOBs:                   6  out of    232     2%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk<0>                             | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.048ns (Maximum Frequency: 488.317MHz)
   Minimum input arrival time before clock: 2.335ns
   Maximum output required time after clock: 3.732ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk<0>'
  Clock period: 2.048ns (frequency: 488.317MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               2.048ns (Levels of Logic = 1)
  Source:            Q_0 (FF)
  Destination:       Q_0 (FF)
  Source Clock:      clk<0> rising
  Destination Clock: clk<0> rising

  Data Path: Q_0 to Q_0
                                Gate     Net
```

```
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.714  Q_0 (Q_0)
     INV:I->O              1   0.206   0.579  Mcount_Q_xor<0>11_INV_0 (Result<0>)
     FDR:D                     0.102          Q_0
    ----------------------------------------
    Total                      2.048ns (0.755ns logic, 1.293ns route)
                               (36.9% logic, 63.1% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk<0>'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              2.335ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       Q_0 (FF)
  Destination Clock: clk<0> rising

  Data Path: rst to Q_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   1.222   0.683  rst_IBUF (rst_IBUF)
     FDR:R                     0.430          Q_0
    ----------------------------------------
    Total                      2.335ns (1.652ns logic, 0.683ns route)
                               (70.8% logic, 29.2% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk<0>'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              3.732ns (Levels of Logic = 1)
  Source:            Q_0 (FF)
  Destination:       Q<0> (PAD)
  Source Clock:      clk<0> rising

  Data Path: Q_0 to Q<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              5   0.447   0.714  Q_0 (Q_0)
     OBUF:I->O                 2.571          Q_0_OBUF (Q<0>)
    ----------------------------------------
    Total                      3.732ns (3.018ns logic, 0.714ns route)
                               (80.9% logic, 19.1% route)

==========================================================================

Cross Clock Domains Report:
---------------------------

Clock to Setup on destination clock clk<0>
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk<0>         |    2.048|         |         |         |
---------------+---------+---------+---------+---------+
```

```
================================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.40 secs

-->


Total memory usage is 393844 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

6.6 Implementation Report for 4-Bit Counter (Modern)

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'SeqCounterModern'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o SeqCounterModern_map.ncd SeqCounterModern.ngd
SeqCounterModern.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Apr 19 16:27:53 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    4 out of  18,224    1%
    Number used as Flip Flops:                  4
    Number used as Latches:                     0
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:               0
  Number of Slice LUTs:                         4 out of   9,112    1%
    Number used as logic:                       4 out of   9,112    1%
      Number using O6 output only:              4
      Number using O5 output only:              0
      Number using O5 and O6:                   0
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   2,176    0%

Slice Logic Distribution:
  Number of occupied Slices:                    1 out of   2,278    1%
  Number of MUXCYs used:                        0 out of   4,556    0%
  Number of LUT Flip Flop pairs used:           4
    Number with an unused Flip Flop:            0 out of       4    0%
    Number with an unused LUT:                  0 out of       4    0%
    Number of fully used LUT-FF pairs:          4 out of       4  100%
    Number of unique control sets:              1
    Number of slice register sites lost
      to control set restrictions:              4 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        6 out of     232    2%

Specific Feature Utilization:
  Number of RAMB16BWERs:                        0 out of      32    0%
  Number of RAMB8BWERs:                         0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                0 out of      32    0%
```

```
  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       1 out of      16    6%
    Number used as BUFGs:                        1
    Number used as BUFGMUX:                      0
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                   0 out of     248    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of      32    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of MCBs:                                0 out of       2    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                3.17

Peak Memory Usage:  671 MB
Total REAL time to MAP completion:  6 secs
Total CPU time to MAP completion:   6 secs

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-----------------
Section 1 - Errors
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Section 12 - Control Set Information
Section 13 - Utilization by Hierarchy

Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
```

```
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------

Section 5 - Removed Logic
-------------------------

Section 6 - IOB Properties
--------------------------

+----------------------------------------------------------------------------------------------------------------------
| IOB Name                          | Type             | Direction | IO Standard          | Diff  | Drive    | Sle
|                                   |                  |           |                      | Term  | Strength | Rat
+----------------------------------------------------------------------------------------------------------------------
| Q<0>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<1>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<2>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| Q<3>                              | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| clk<0>                            | IOB              | INPUT     | LVCMOS25             |       |          |
| rst                               | IOB              | INPUT     | LVCMOS25             |       |          |
+----------------------------------------------------------------------------------------------------------------------

Section 7 - RPMs
----------------

Section 8 - Guide Report
------------------------
Guide not run on this design.

Section 9 - Area Group and Partition Summary
--------------------------------------------

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Area Group Information
----------------------

  No area groups were found in this design.

----------------------

Section 10 - Timing Report
--------------------------
A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
```

```
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details
-----------------------------------------
Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information
------------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```

6.7 Synthesis Report for Clock Divider

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Reading design: clockDivider.prj

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  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
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  6) Low Level Synthesis
  7) Partition Report
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       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "clockDivider.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "clockDivider"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : clockDivider
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
```

```
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "/home/melody/152a/Project_1/clock-divider.v" into library work
Parsing module <clockDivider>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================
```

```
Elaborating module <clockDivider>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <clockDivider>.
    Related source file is "/home/melody/152a/Project_1/clock-divider.v".
    Found 1-bit register for signal <out>.
    Found 13-bit register for signal <count>.
    Found 13-bit adder for signal <count[12]_GND_1_o_add_2_OUT> created at line 36.
    Summary:
inferred   1 Adder/Subtractor(s).
inferred  14 D-type flip-flop(s).
Unit <clockDivider> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 13-bit adder                                         : 1
# Registers                                            : 2
 1-bit register                                       : 1
 13-bit register                                      : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <clockDivider>.
The following registers are absorbed into counter <count>: 1 register on signal <count>.
Unit <clockDivider> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 1
 13-bit up counter                                    : 1
# Registers                                            : 1
 Flip-Flops                                           : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <clockDivider> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block clockDivider, actual ratio is 0.
```

```
Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 14
 Flip-Flops                                          : 14

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : clockDivider.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 56
#      GND                         : 1
#      INV                         : 1
#      LUT1                        : 12
#      LUT5                        : 1
#      LUT6                        : 15
#      MUXCY                       : 12
#      VCC                         : 1
#      XORCY                       : 13
# FlipFlops/Latches                : 14
#      FD                          : 14
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 2
#      IBUF                        : 1
#      OBUF                        : 1

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              14  out of  18224     0%
 Number of Slice LUTs:                   29  out of   9112     0%
    Number used as Logic:                29  out of   9112     0%

Slice Logic Distribution:
```

```
 Number of LUT Flip Flop pairs used:     29
   Number with an unused Flip Flop:      15  out of     29    51%
   Number with an unused LUT:             0  out of     29     0%
   Number of fully used LUT-FF pairs:    14  out of     29    48%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                           3
 Number of bonded IOBs:                   3  out of    232     1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 14    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.104ns (Maximum Frequency: 322.129MHz)
   Minimum input arrival time before clock: 2.849ns
   Maximum output required time after clock: 3.634ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.104ns (frequency: 322.129MHz)
  Total number of paths / destination ports: 274 / 14
-------------------------------------------------------------------------
```

```
Delay:               3.104ns (Levels of Logic = 2)
  Source:            count_7 (FF)
  Destination:       count_2 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: count_7 to count_2
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               2   0.447   0.961  count_7 (count_7)
     LUT5:I0->O           14   0.203   1.186  GND_1_o_GND_1_o_equal_8_o<12>2 (GND_1_o_GND_1_o_equal_8_o<12>1)
     LUT6:I3->O            1   0.205   0.000  count_2_rstpot (count_2_rstpot)
     FD:D                      0.102          count_2
    ----------------------------------------
    Total                      3.104ns (0.957ns logic, 2.147ns route)
                               (30.8% logic, 69.2% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 14 / 14
--------------------------------------------------------------------------
Offset:              2.849ns (Levels of Logic = 2)
  Source:            rst (PAD)
  Destination:       count_0 (FF)
  Destination Clock: clk rising

  Data Path: rst to count_0
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   1.222   1.322  rst_IBUF (rst_IBUF)
     LUT6:I0->O            1   0.203   0.000  count_0_rstpot (count_0_rstpot)
     FD:D                      0.102          count_0
    ----------------------------------------
    Total                      2.849ns (1.527ns logic, 1.322ns route)
                               (53.6% logic, 46.4% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.634ns (Levels of Logic = 1)
  Source:            out (FF)
  Destination:       out (PAD)
  Source Clock:      clk rising

  Data Path: out to out
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               2   0.447   0.616  out (out_OBUF)
     OBUF:I->O                 2.571          out_OBUF (out)
    ----------------------------------------
    Total                      3.634ns (3.018ns logic, 0.616ns route)
                               (83.0% logic, 17.0% route)

==========================================================================
```

```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    3.104|         |         |         |
---------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.39 secs

-->


Total memory usage is 394724 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

6.8 Implementation Report for Clock Divider

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'clockDivider'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o clockDivider_map.ncd clockDivider.ngd
clockDivider.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Apr 19 16:08:17 2020

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                   14 out of  18,224    1%
    Number used as Flip Flops:                 14
    Number used as Latches:                     0
    Number used as Latch-thrus:                 0
    Number used as AND/OR logics:               0
  Number of Slice LUTs:                        29 out of   9,112    1%
    Number used as logic:                      28 out of   9,112    1%
      Number using O6 output only:             16
      Number using O5 output only:             11
      Number using O5 and O6:                   1
      Number used as ROM:                       0
    Number used as Memory:                      0 out of   2,176    0%
    Number used exclusively as route-thrus:     1
      Number with same-slice register load:     0
      Number with same-slice carry load:        1
      Number with other load:                   0

Slice Logic Distribution:
  Number of occupied Slices:                    8 out of   2,278    1%
  Number of MUXCYs used:                       16 out of   4,556    1%
  Number of LUT Flip Flop pairs used:          29
    Number with an unused Flip Flop:           15 out of      29   51%
    Number with an unused LUT:                  0 out of      29    0%
    Number of fully used LUT-FF pairs:         14 out of      29   48%
    Number of unique control sets:              1
    Number of slice register sites lost
      to control set restrictions:              2 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        3 out of     232    1%
```

```
Specific Feature Utilization:
  Number of RAMB16BWERs:                        0 out of      32    0%
  Number of RAMB8BWERs:                         0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:            0 out of      32    0%
  Number of BUFG/BUFGMUXs:                      1 out of      16    6%
    Number used as BUFGs:                       1
    Number used as BUFGMUX:                     0
  Number of DCM/DCM_CLKGENs:                    0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                  0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:        0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                  0 out of     248    0%
  Number of BSCANs:                             0 out of       4    0%
  Number of BUFHs:                              0 out of     128    0%
  Number of BUFPLLs:                            0 out of       8    0%
  Number of BUFPLL_MCBs:                        0 out of       4    0%
  Number of DSP48A1s:                           0 out of      32    0%
  Number of ICAPs:                              0 out of       1    0%
  Number of MCBs:                               0 out of       2    0%
  Number of PCILOGICSEs:                        0 out of       2    0%
  Number of PLL_ADVs:                           0 out of       2    0%
  Number of PMVs:                               0 out of       1    0%
  Number of STARTUPs:                           0 out of       1    0%
  Number of SUSPEND_SYNCs:                      0 out of       1    0%

Average Fanout of Non-Clock Nets:               3.32

Peak Memory Usage:  673 MB
Total REAL time to MAP completion:  8 secs
Total CPU time to MAP completion:   5 secs

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Section 1 - Errors
------------------

Section 2 - Warnings
--------------------

Section 3 - Informational
-------------------------
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
```

```
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------
   2 block(s) optimized away

Section 5 - Removed Logic
-------------------------

Optimized Block(s):
TYPE  BLOCK
GND  XST_GND
VCC  XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
--------------------------

+-----------------------------------------------------------------------------------------------------------------------
| IOB Name                          | Type             | Direction | IO Standard          | Diff  | Drive    | Sle
|                                   |                  |           |                      | Term  | Strength | Rat
+-----------------------------------------------------------------------------------------------------------------------
| clk                               | IOB              | INPUT     | LVCMOS25             |       |          |
| out                               | IOB              | OUTPUT    | LVCMOS25             |       | 12       | SLO
| rst                               | IOB              | INPUT     | LVCMOS25             |       |          |
+-----------------------------------------------------------------------------------------------------------------------

Section 7 - RPMs
----------------

Section 8 - Guide Report
------------------------
Guide not run on this design.

Section 9 - Area Group and Partition Summary
--------------------------------------------

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Area Group Information
----------------------

  No area groups were found in this design.

----------------------
```

```
Section 10 - Timing Report
--------------------------
A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details
-----------------------------------------
Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information
------------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```