INTERCONNECTION STRUCTURE

- A computer is a network of basic modules of mainly 3 types (Processors, Memory, I/O Modules).
- Collection of path connecting these modules is called **Interconnection Structure.**
- Design of **Interconnection Structure** depends on the Nature of Exchanges that must be made among modules.

Nature of Exchanges that are needed for each type of module:

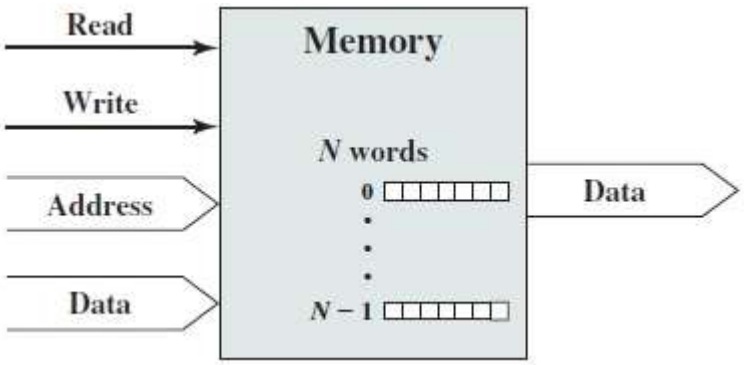
Memory:

A Memory consists of N-words of equal length.
Each word is assigned a unique numerical address (0, 1, 2, ……., N-1)

Nature of Operation (Read / Write)

Address (location of Operation)

Data (To be written or Read)



I/O Module:

From computer point of view I/O is functionally similar to memory.

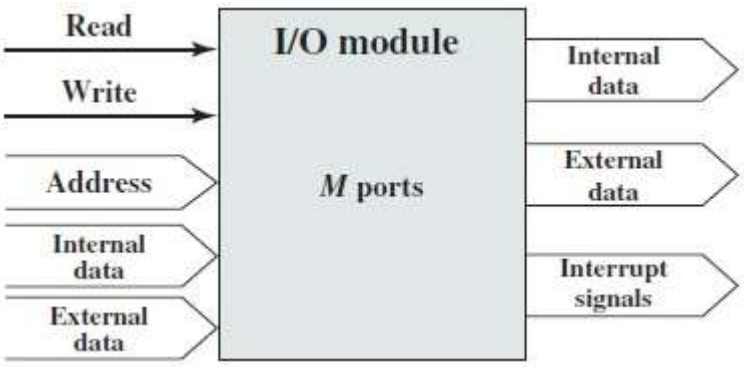
Nature of Operation (Read / Write)

Address (Port Address – Interface to each I/O device is referred as Port)

Data (To & From External Device)

Data (To & Microprocessor)

Interrupt (To Microprocessor)



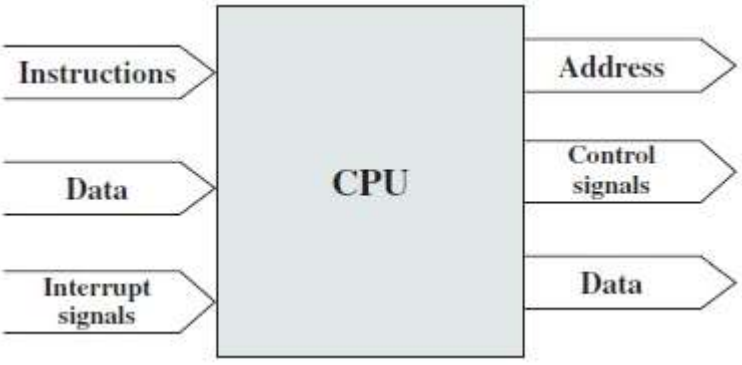
Processor

Processors read in Instructions and Data.

Writes out Data (To I/O or Memory)

Control Signals (To Subunits)

Interrupt (From attached I/O Devices)



TYPES OF INTERCONNECTION STRUCTURES

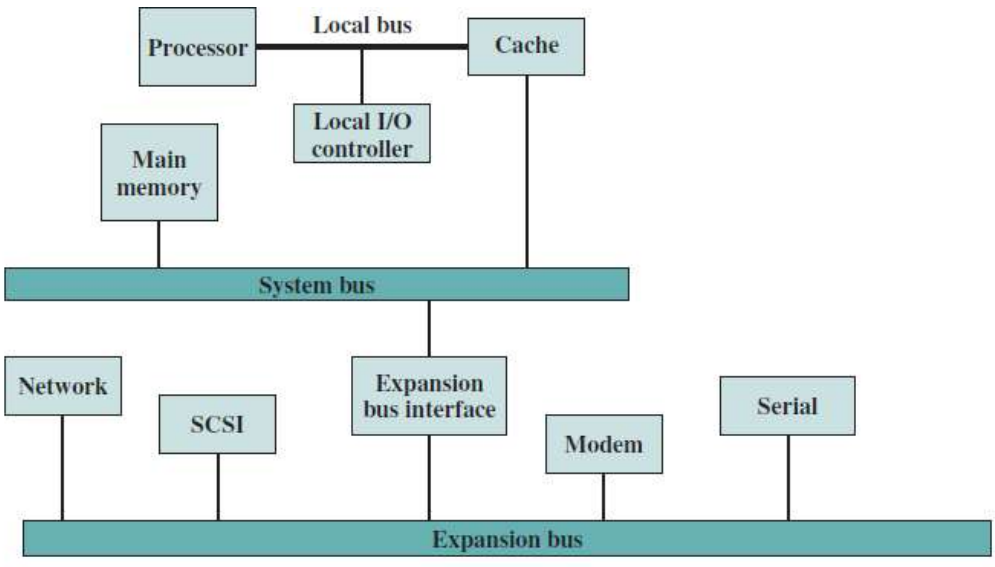
1) Bus and Multiple Bus Structure
2) Point to Point Interconnection Structure with Packetized Data Transfer

BUS INTERCONNECTION:

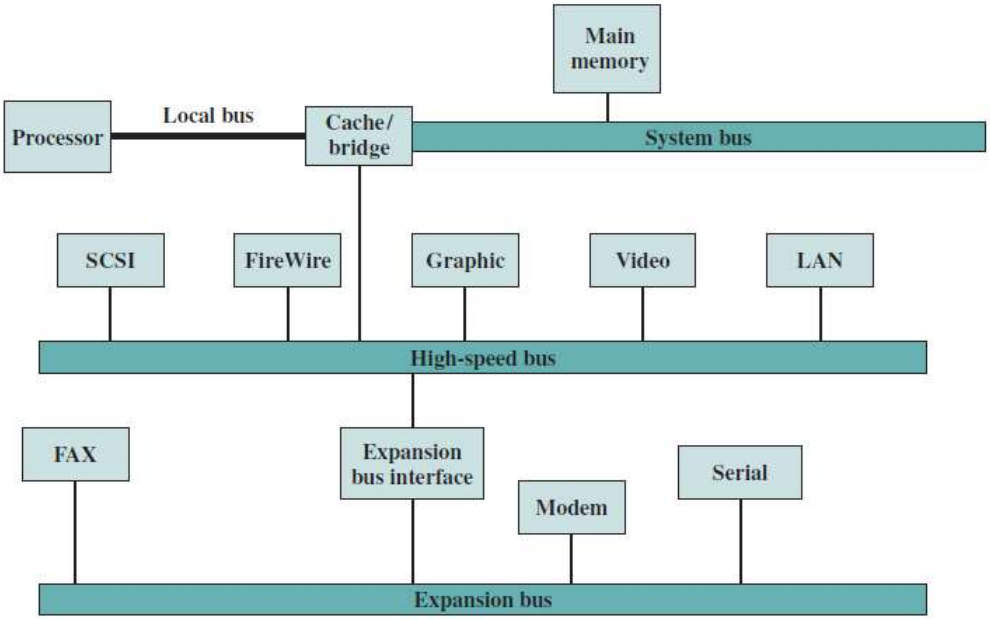
- A Bus is a communication pathway connecting two or more devices by shared transmission medium.
- In Bus Interconnection one device at a time can transmit all others can receive.
- Typically, Bus consists of multiple lines. Each line transmitting a single bit.
- Several Lines of a Bus can be used to transmit binary digits in parallel.
- Computer System contain a number of different buses to connect components at various level of computer system hierarchy.
- A Bus that connect major components (Processor, Memory and I/O) is called a System Bus.
- Common Computer Interconnection Structure are based on use of one or more System Buses.

BUS STRUCTURE:

- A system bus consists of about fifty to hundreds of separate lines.
- Each line is assigned a separate meaning or functions.
- These lines can be classified into three functional groups: * Data * Address * Control
- Number of lines for Data determine how many bits can be transferred at a time.
- Width of the Address Lines determine the maximum memory capacity of system.
- Control Lines are used to Control the access to and the use of the Data and Address Lines.
- Control Signals transmit both command and timing information among modules. Example Clock, Reset, Interrupt Request, Interrupt Ack, Bus Request, Bus Grant, Memory Read, Memory Write, I/O Read, I/O Write, Transfer Ack etc.



(a) Traditional bus architecture



(b) High-performance architecture

Elements of Bus Design:

Bus Type:

- **Dedicated:** Functional or Physical dedication.
- **Multiplexed** (Time Multiplexed): Fewer lines so less cost but complex circuitry is needed, and event that share same lines can't take place in parallel.

Method of Arbitration:

- **Centralized: Single Hardware device is Bus Controller**
- **Distributed:** Each Module contain access control logic.

Timing:

- **Synchronous:** Occurrence of events on bus is determined by a clock
- **Asynchronous:** Occurrence of event follows and depend on occurrence of previous events.

Bus Width:

- **Data Bus Width:** Number of lines for Data determine how many bits can be transferred at a time.
- **Address Bus Width:** Width of the Address Lines determine the maximum memory capacity of system.

Data Transfer Type:

- Read
- Write
- Read-Modify-Write
- Read-After-Write
- Block Transfer