Chapter 0 - Overview

Course Information

Tien-Fu Chen

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National Chiao Tung Univ.

陳添福 Contact Information

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- Fax: 03-5721490

- Course Info and Lecture Slides on E3
- Google Calendar: 2020 Computer Organization
- 討論區:
  https://hackmd.io/8LSdgoryQQy1Fnq214bC4A

陳添福 教授

- 學歷
  - 1979~1983 台灣大學 資訊工程系, BS
  - 1988~1993 美國U. of Washington, Seattle, MS and PhD
- 經歷

2010 ~迄今	國立交通大學	教授
2010 ~2018	中央研究院資訊所	合聘研究員
1993 ~2009	國立中正大學	副教授/教授
2003	美國Intel	Visiting Professor

- 擔任職務
  - 研華-交大 物聯網智慧系統研究中心 Embedded IoT PaaS Lab 主任
  - 聯發科-交大創新研究中心 副主任
  - 台灣AI on chip聯盟 AI系統軟體分項召集人
  - 國立交通大學 人工智慧系統檢測中心 主任
- 經歷與計畫
  - 國家高速網路與計算中心 副主任
  - AI計畫「實現深度學習於產業服務之邊端智慧系統架構與其設計流程」
  - 科技部深耕計畫四年計畫:
    產業用物聯網基礎技術: 大規模資料收集分析平台與產業智慧PaaS系統

TA Contact Information

- **TA： Lab @工程三館447**
- **張祐銘 yumingchang.cs03@g2.nctu.edu.tw**
- **賴柏宏 bhbruce.cs07g@nctu.edu.tw**
- **鄭俊賢 petertay1996@gmail.com**

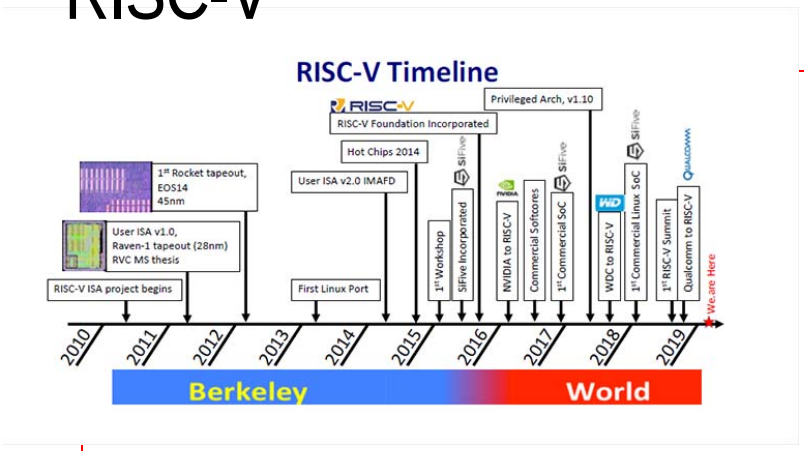
- **TA Lecture: right after Monday class**

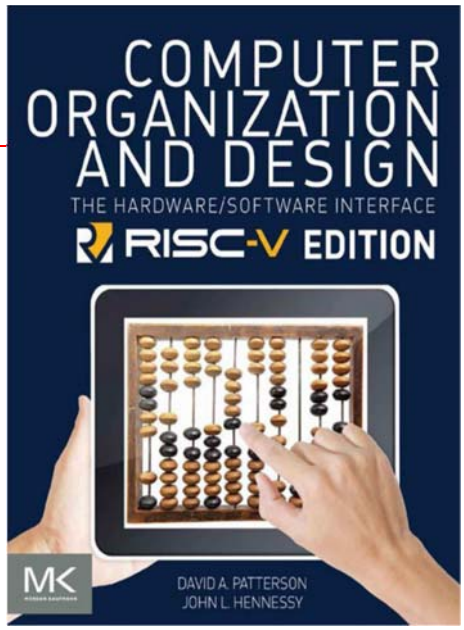
- **TA office hours:**
  - **Mon. 4:30 PM ~ 5:30 PM**
  - **Meeting room EC 500A**
  - **Always standby for any lab or lecture questions**
- 討論區:

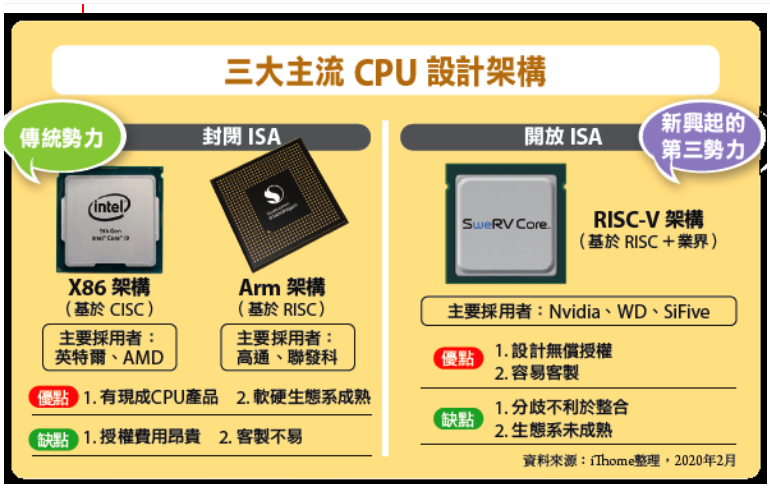
All Q&A will be on 討論區 (please share any info)

- **No repeated questions**

RISC-V







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RISC-V 專題採訪 @2020-01-20

Source:
https://www.ithome.com.tw/news/135859

【學界觀點：超級電腦臺灣杉2號建置負責人陳添福】RISC-V讓晶片新創能與世界主流競爭，但實作成熟度將是挑戰

曾任國網中心副主任的交大資工系教授陳添福認為，RISC-V的開放設計架構，讓任何企業，包括臺灣硬體公司自行設計的CPU產品，可以相容於CPU主流，與全世界站在同一個競爭基礎

文/ 余至洁 | 2020-02-20 發表

透過RISC-V開放設計架構，任何企業，包括臺灣硬體公司，自行設計的CPU產品，可以相容於CPU主流，與全世界站在同一個競爭基礎。

超級電腦臺灣杉2號建置負責人陳添福

攝影 / 洪政儒

「RISC-V就像提供了一個強大的繪圖工具，讓任何人都能夠自由發揮創意，」交大資工系教授陳添福這樣形容，而Arm和x86則像已完成的畫，顏色圖案已經定型了，要改就很難。

陳添福曾是國網中心副主任，也是打造出曾名列全球前20大超級電腦的臺灣杉2號主要建置負責人，過去在SoC設計、多核心CPU，以及嵌入式系統的研究著墨很深。

RISC-V最大價值是開放性，讓更多CPU設計創意得以實現

過去，晶片廠商設計CPU時，如果沒取得指令集授權，比如指令格式、執行方法等，即使你的RTL Code重新自己編寫，最後開發出來的CPU產品，仍會有專利侵權問題，就算取得對方授權，未來想要替CPU核心新增指令或功能，若指令集擁有者沒有提供，也沒辦法用，或對方不願開放授權，也只能等待，甚至有時遇到授權

iThome 按讚追蹤 iThome 最新報導

熱門新聞

FBI：以長密碼取代密碼，不應設定密碼變更期間或次數上限 2020-02-25

Office 365支援臺灣教育雲帳號，250萬中小學生都能快速申請免費教育版 2020-02-24

Chrome零時差漏洞已發生攻擊，Google忙修補 2020-02-26

微軟開始替Windows 10用戶升級到Chromium版Edge 2020-02-28

Safari 9月1日起將拒絕效期超過398天的新網站SSL憑證 2020-02-24

Check Point：Haken惡意程式成功進駐Google Play上的8款Android程式 2020-02-24

你申請了嗎？Let's Encrypt已發出10億個免費TLS憑證 2020-02-28

綁Google Pay的PayPal帳戶遭盜刷，美、德及俄國用戶遭殃 2020-02-25

多項合勤防火牆、NAS產品爆指令注入漏洞可執行任意程式碼

Course Contents

- Textbook:

Patterson, D. A. and Hennessy, J. L. (2017).

Computer Organization and Design: The Hardware/Software Interface: RISC-V Edition. Morgan Kaufmann

Chapter or Appendix	Sections	Software focus	Hardware focus
1. Computer Abstractions and Technology	1.1 to 1.11		
	1.12 (History)		
2. Instructions: Language of the Computer	2.1 to 2.14		
	2.15 (Compilers & Java)		
	2.16 to 2.20		
	2.21 (History)		
D. RISC Instruction-Set Architectures	D.1 to D.17		
3. Arithmetic for Computers	3.1 to 3.5		
	3.6 to 3.8 (Subword Parallelism)		
	3.9 to 3.10 (Fallacies)		
	3.11 (History)		
A. The Basics of Logic Design	A.1 to A.13		
4. The Processor	4.1 (Overview)		
	4.2 (Logic Conventions)		
	4.3 to 4.4 (Simple Implementation)		
	4.5 (Pipelining Overview)		
	4.6 (Pipelined Datapath)		
	4.7 to 4.9 (Hazards, Exceptions)		
	4.10 to 4.12 (Parallel, Real Stuff)		
	4.13 (Verilog Pipeline Control)		
	4.14 to 4.15 (Fallacies)		
	4.16 (History)		

C. Mapping Control to Hardware	C.1 to C.6		
5. Large and Fast: Exploiting Memory Hierarchy	5.1 to 5.10		
	5.11 (Redundant Arrays of Inexpensive Disks)		
	5.12 (Verilog Cache Controller)		
	5.13 to 5.17		
	5.18 (History)		
6. Parallel Process from Client to Cloud	6.1 to 6.8		
	6.9 (Networks)		
	6.10 to 6.14		
	6.15 (History)		
B. Graphics Processor Units	B.1 to B.13		

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Your Score is based on ...

- Midterm exam X 2 ➔ 20% + 20% = 40 %
- Final exam ➔ 20%
- Homework and programs ➔ 40%
  - a series of intensive Verilog (a popular hardware description language) program assignments.
  - Lab 1 ~ Lab 3: each student per team
  - Lab 4 ~ Lab 6: 2 students in a team
  - Demo and explanation are required
- Class quizzes (小考) + Extra credits ➔ 10%
  - Class participation
  - Interesting Questions/interactions
- 作業抄襲者，該次以0分計

Assignments and reports

- We will have 6 Lab assignments, plus one **bonus** lab
- Lab results are turned in via **E3 course system** due by 11:59pm .
- Assignment reports have to be submitted to 447 (lab work box) by the following day of the lab due day.

- 作業報告撰寫格式如下：(min 2 pages)
  - 作業名稱
  - 系統架構
  - 設計模組分析
  - 設計結果與功能說明
  - 遭遇困難與解決方法
  - 作業心得討論

What does industry want?

- Problem Solving Ability
- Critical Thinking
- Interpersonal Communication Skills
- Group-based Interaction Skills

- know what?
- know why?
- know how?

資料 ⟶ 資訊 ⟶ 知識 + 智能 ⟶ 智慧

Policy

- Be sure to bring
  - Lecture notes
  - Textbook
  - Your head
  - You heart
- Not to bring
  - Your breakfast/lunch
  - Your mobile
- Notebook/Laptops are discouraged…

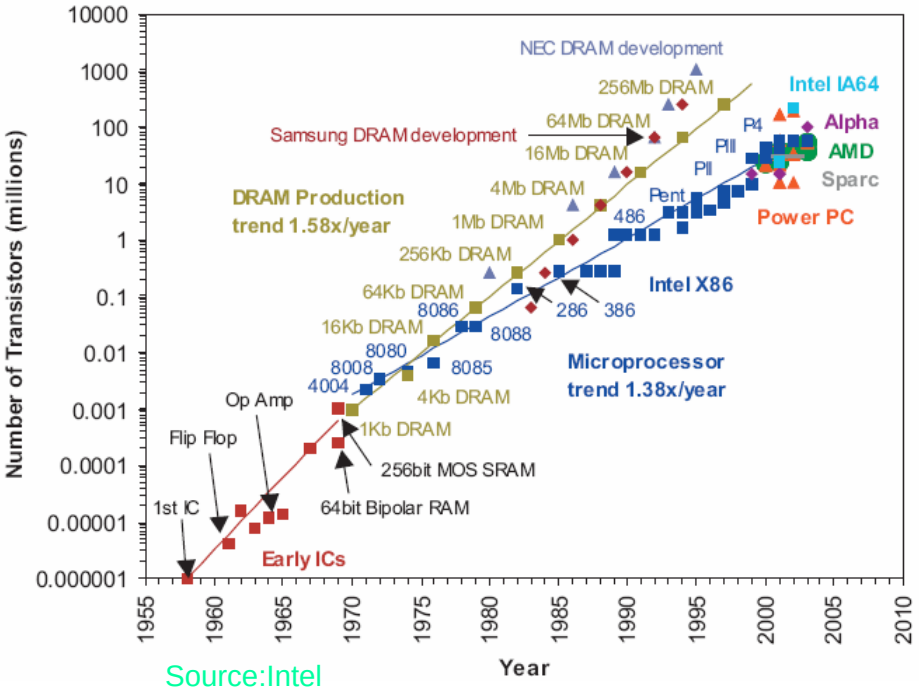
More thinking and more interaction

- Grasp info from the web
  - CPU info center: http://bwrc.eecs.berkeley.edu/CIC/
  - Microprocessor Report: http://www.mdronline.com/mpr/index.html
  - EE Times http://www.eetimes.com/
  - DigiTimes 科技網(電子時報) http://www.digitimes.com.tw/
- More thinking and More questions …

Technology Trend

Moore's Law

The number of transistors per square-inch doubles each 18 months



Source:Intel

Gordon Moore
Co-founder of Intel 1965

Technology => dramatic change

- Processor
  - logic capacity: about 30% per year
  - clock rate: about 20% per year
- Memory
  - DRAM capacity: about 60% per year (4x every 3 years)
  - Memory speed: about 10% per year
  - Cost per bit: improves about 25% per year
- Disk
  - capacity: about 60% per year
  - Total use of data: 100% per 9 months!
- Network Bandwidth
  - Bandwidth increasing more than 100% per year!

If car industry follows Moore's Law

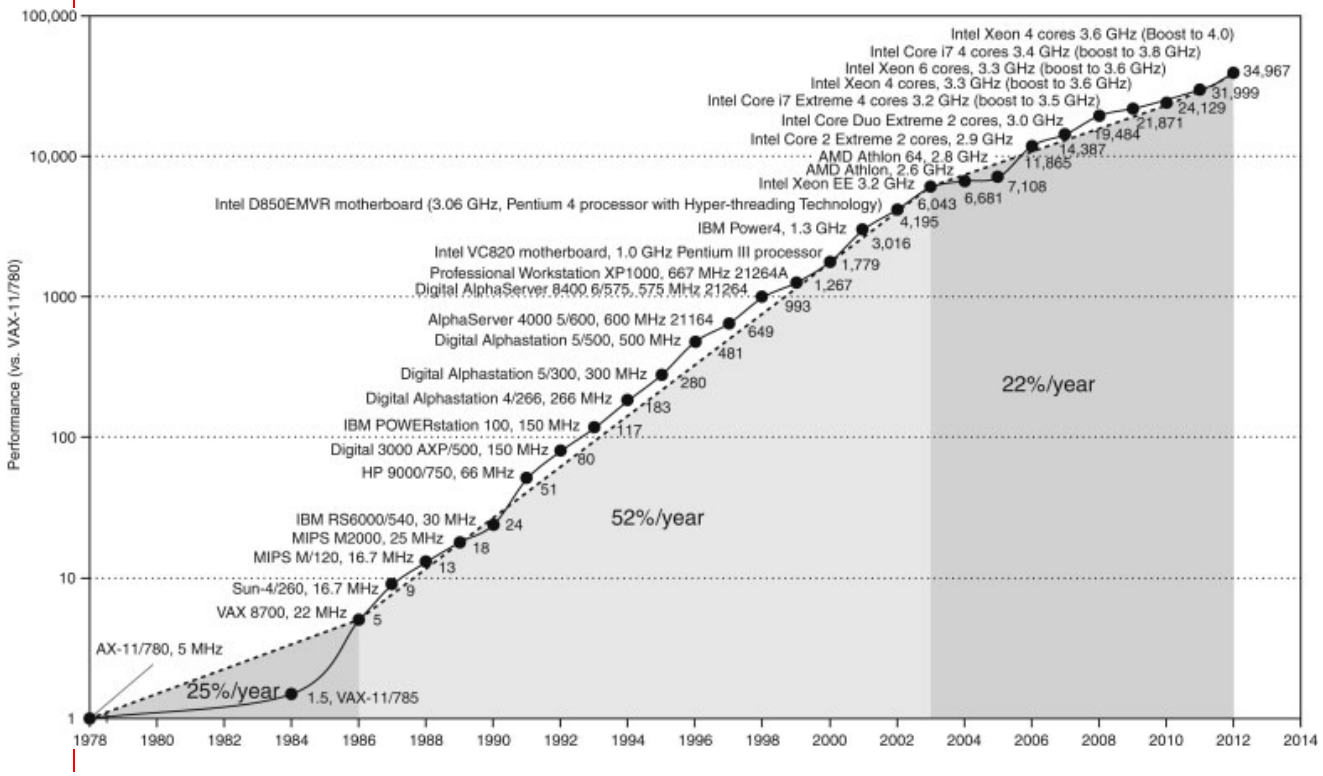
If the car industry followed the Moore's Law in the past forty years.

Nowadays the car should be

- Price → 12 cents/per car
- Speed → 40,000 km/per hour
- Gas mileage → 1200 km/per litter
- Capacity → 400,000 person/per car

Source : Prof. T. P. Ma

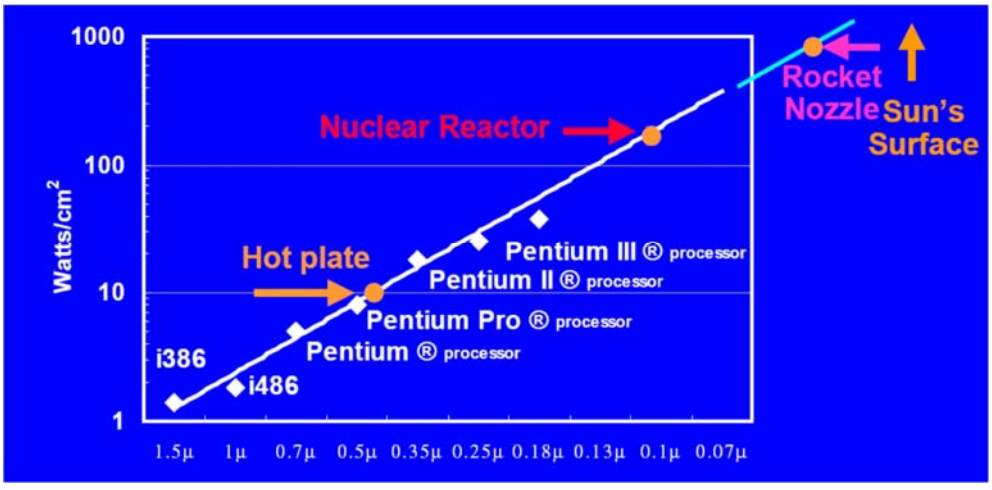
Growth in processor performance since mid-1980s



Challenges for the Hardware Designers

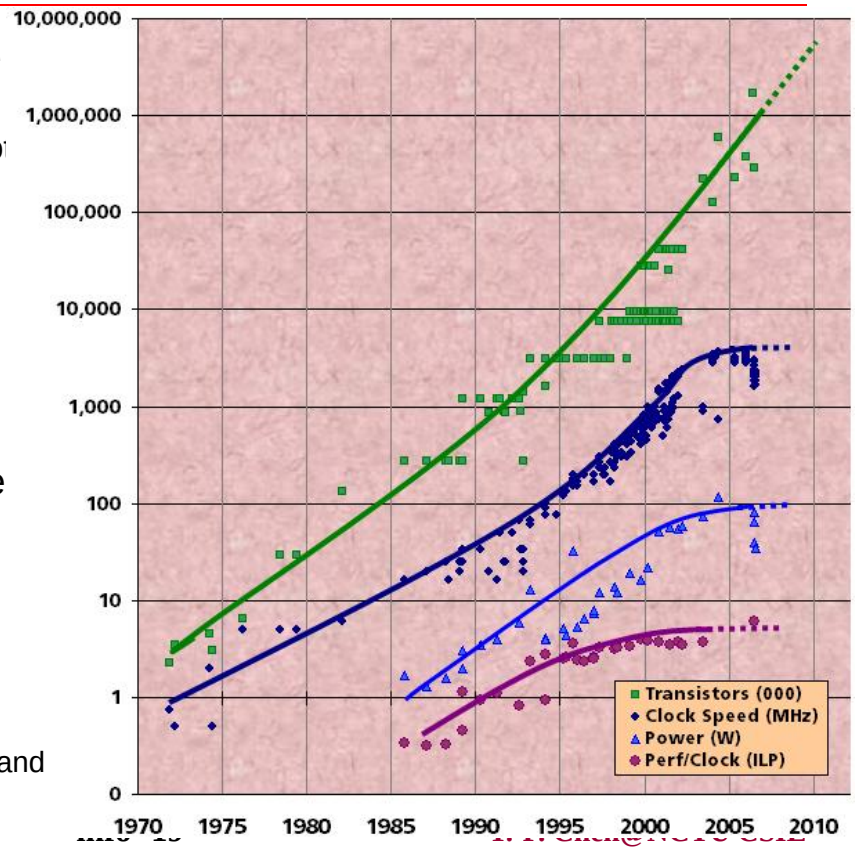
Major concerns:

- The performance problem (especially scientific workloads)
- The power dissipation problem (especially embedded processors)
- The temperature problem
- The reliability problem



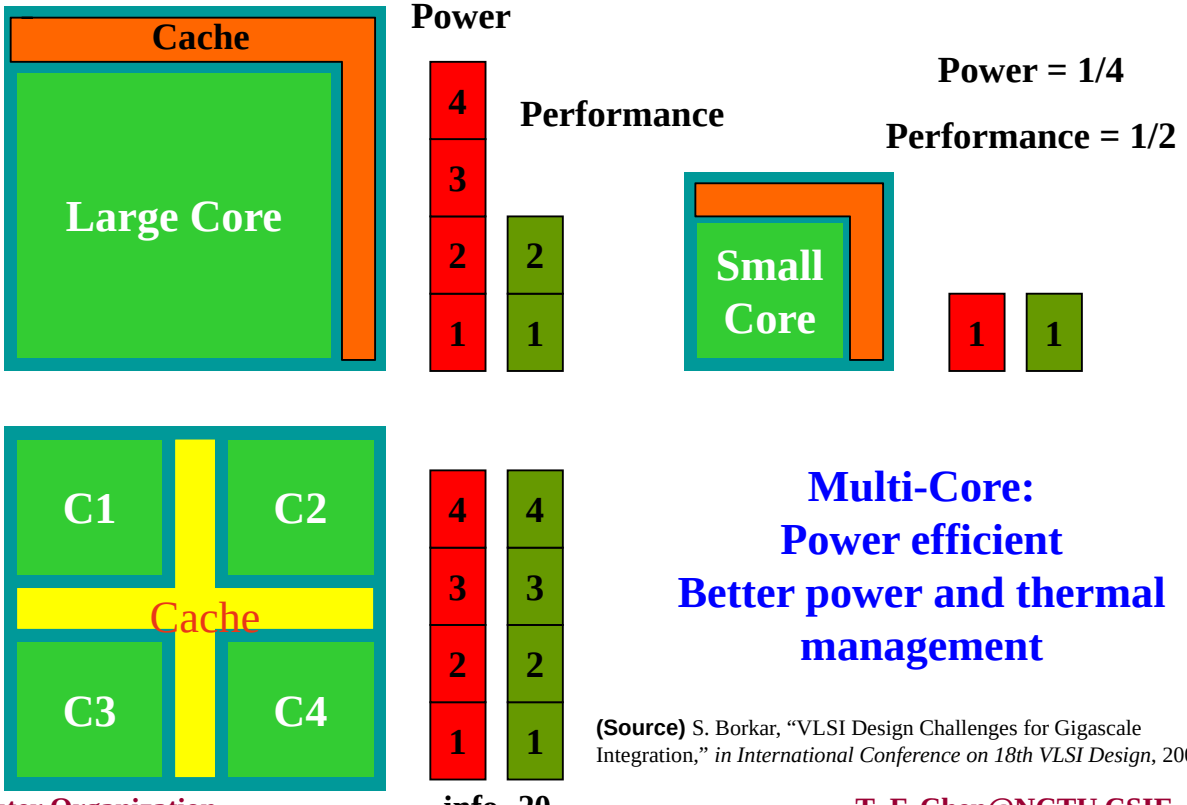
Revolution is Happening Now

- Chip density is continuing increase ~2x every 2 years
  - Clock speed is not
  - Number of processor cores may double instead
- There is little or no hidden parallelism (ILP) to be found
- Parallelism must be exposed to and managed by software



Source: Intel, Microsoft (Sutter) and Stanford (Olukotun, Hammond)

Why multicore?



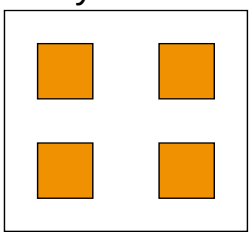
Multi-Core:
Power efficient
Better power and thermal management

(Source) S. Borkar, "VLSI Design Challenges for Gigascale Integration," *in International Conference on 18th VLSI Design*, 2005

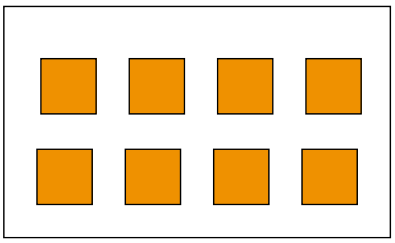
What Does This Mean to a Programmer?

- In the past, a new chip directly meant 50% higher performance for a program
- Today, one can expect only a 20% improvement, unless…the program can be broken up into multiple threads
- Expect #threads to emerge as a major metric for software quality

4-way multi-core



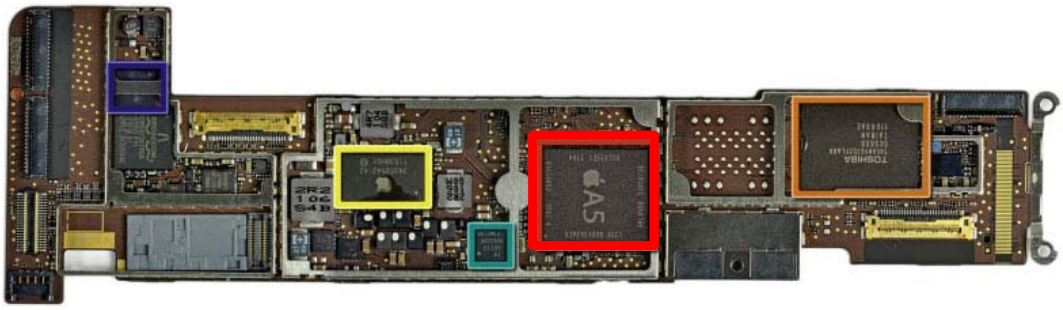
8-way multi-core



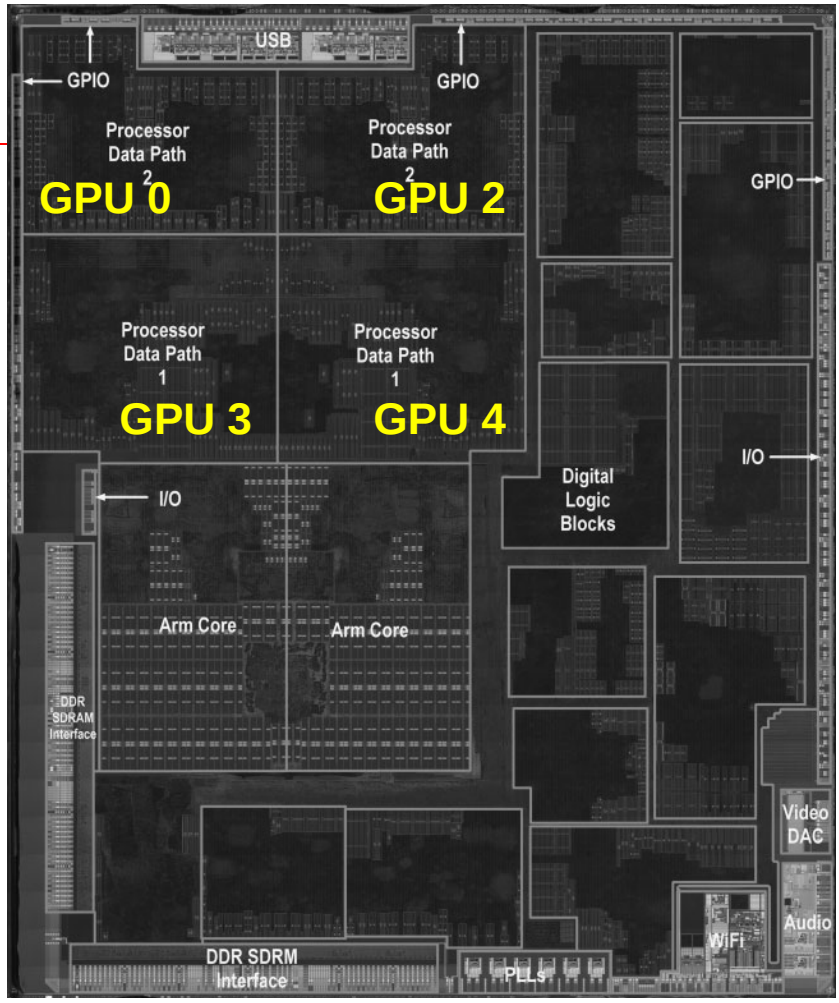
Courtesy, Intel ®

- **In Sep 2006, Intel® announced a prototype of a processor with 80 cores that can perform a trillion floating-point operations per second**

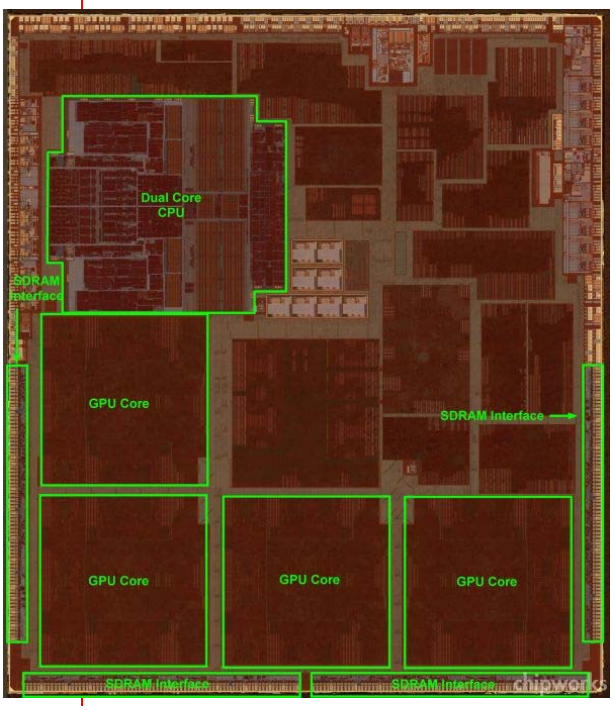
Zoom into contemporary CPU



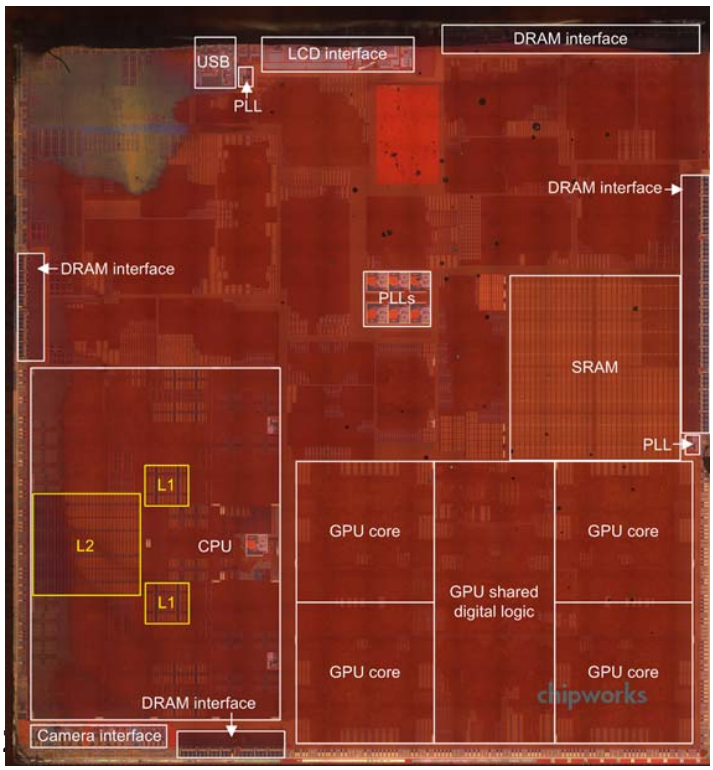
A5 inside



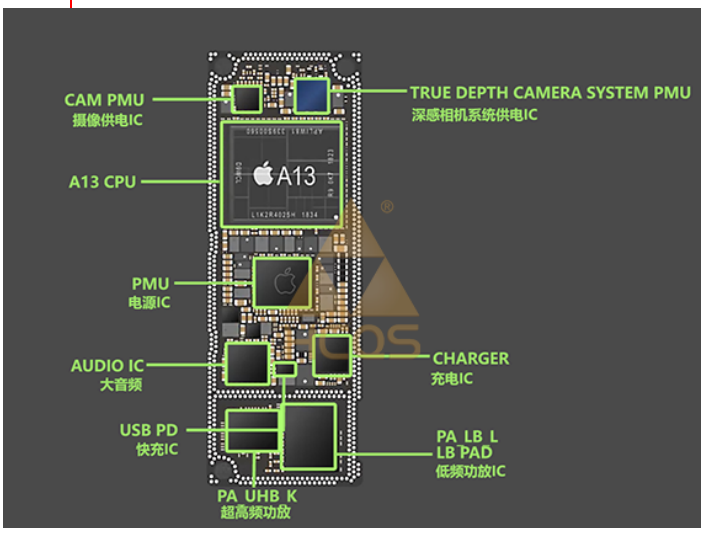
A6X



A7 (64b)



iPhone 11



iPhone 6 – A8

Recent news

- 台積電自2015年與三星分食蘋果A9晶片代工訂單之後，藉由技術及良率優勢，接連拿下蘋果A10、A11及最新的A12晶片代工訂單，業界預期台積電穩居蘋果獨家代工地位至少將延續至2020年。
- 熬十年，變Amazon金雞母！亞馬遜的雲端服務公司AWS，獲利竟超過母公司電商事業;成長速度快到看不到車尾燈，AWS 雲端服務榮登亞馬遜最新金雞母
- 物聯網三商機 五年內爆發(udn產經news)
- 物聯網開啟臺灣兆元商機(簡立峰Google 台灣董事總經理)
  - 物聯網三大商機健康照護、智能管理、智慧製造將在五年內爆發，以智慧製造成長最快，也是台廠機會所在，預估2020年產值上看1,332億美元（約新台幣4.37兆元）
- 挖角 Intel Qualcomm 專才 Google 強化硬體研發部門