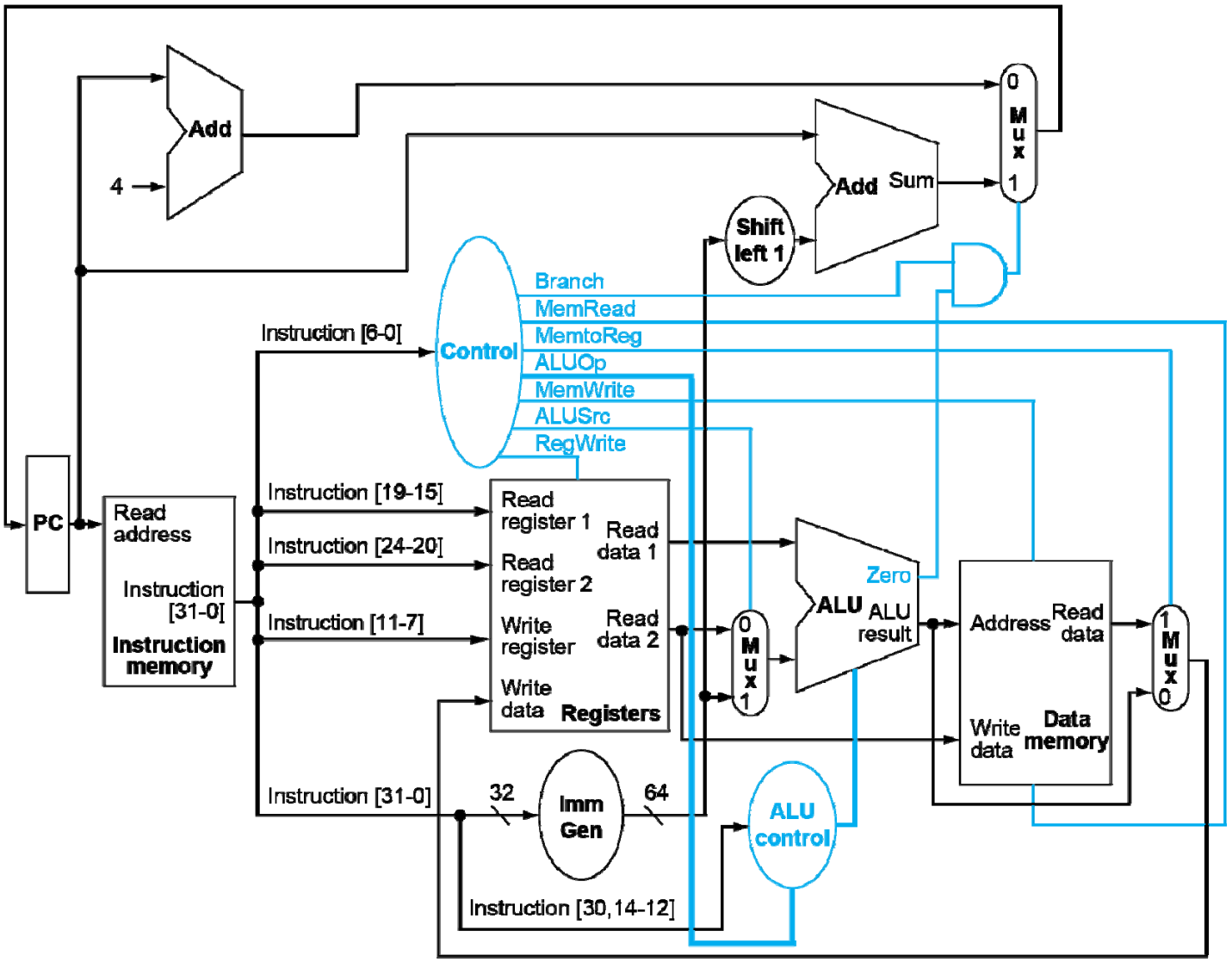
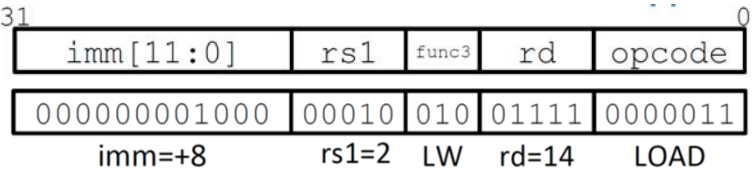
- R-type: add x9,x20,x21

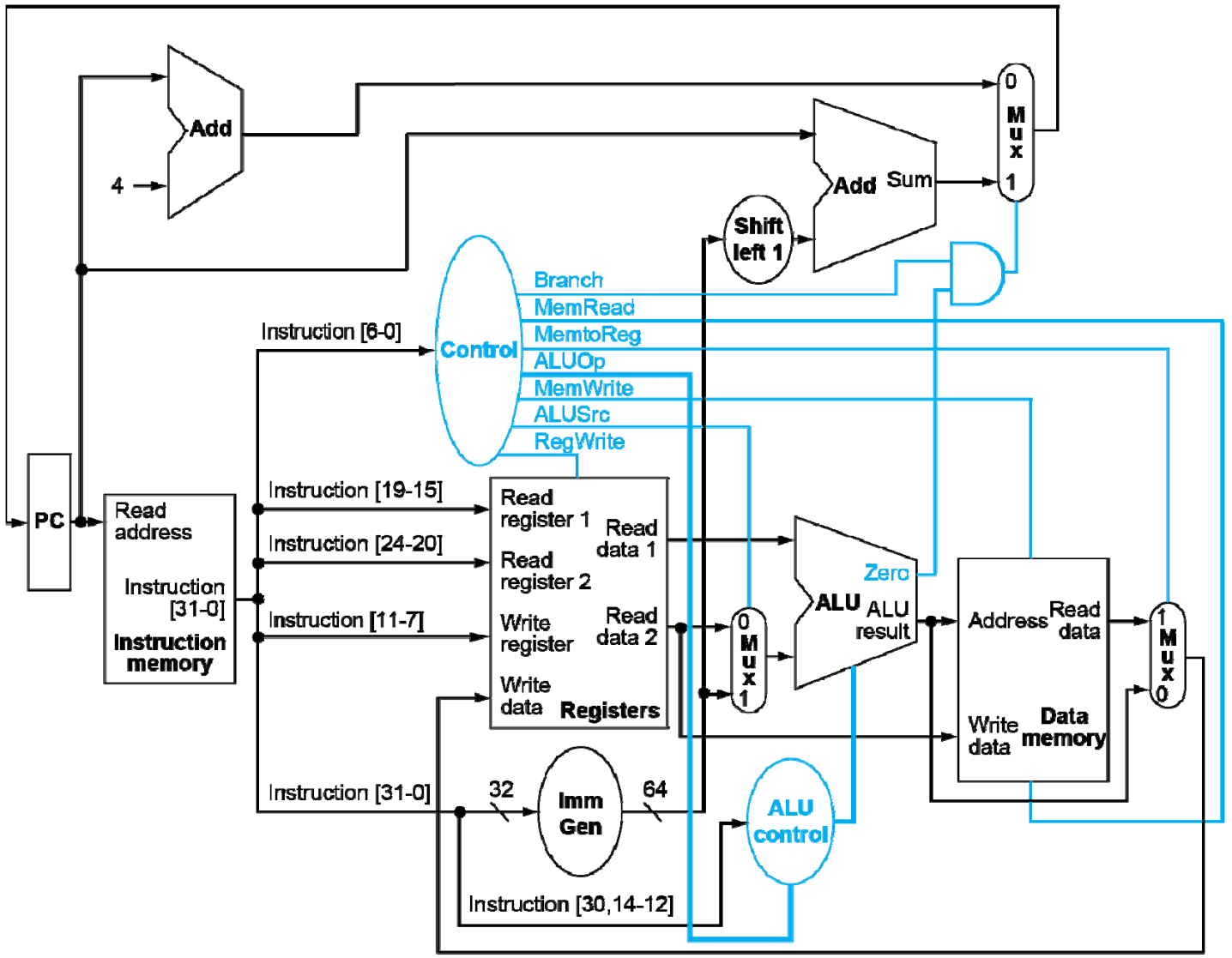
funct7	rs2	rs1	funct3	rd	opcode
7 bits	5 bits	5 bits	3 bits	5 bits	7 bits
0	21	20	0	9	51



Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
R-format								
lw								
sw								
beq								

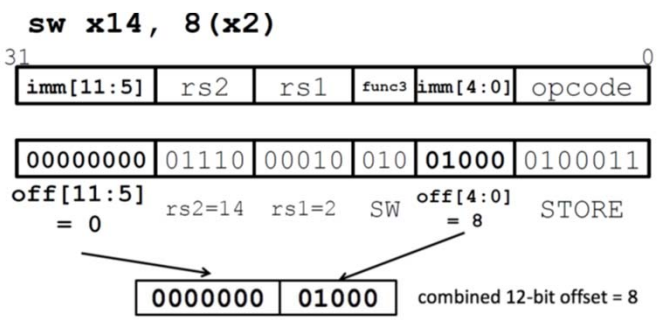
- I-Format: lw x14, 8(x2)

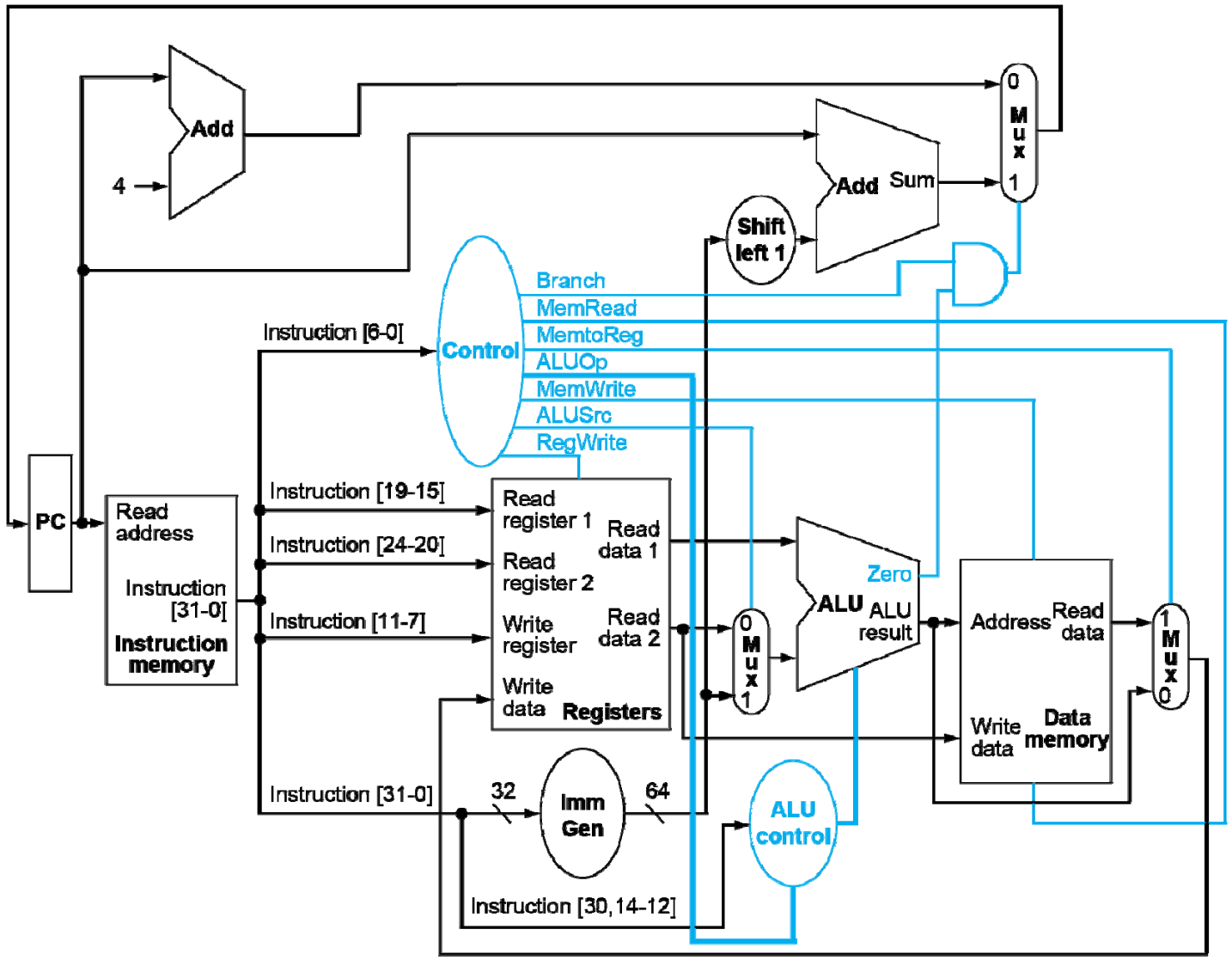




Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
R-format								
lw								
sw								
beq								

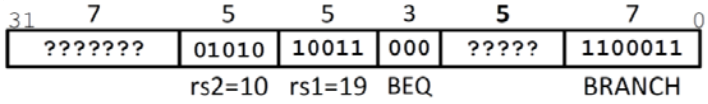
- S-Format:

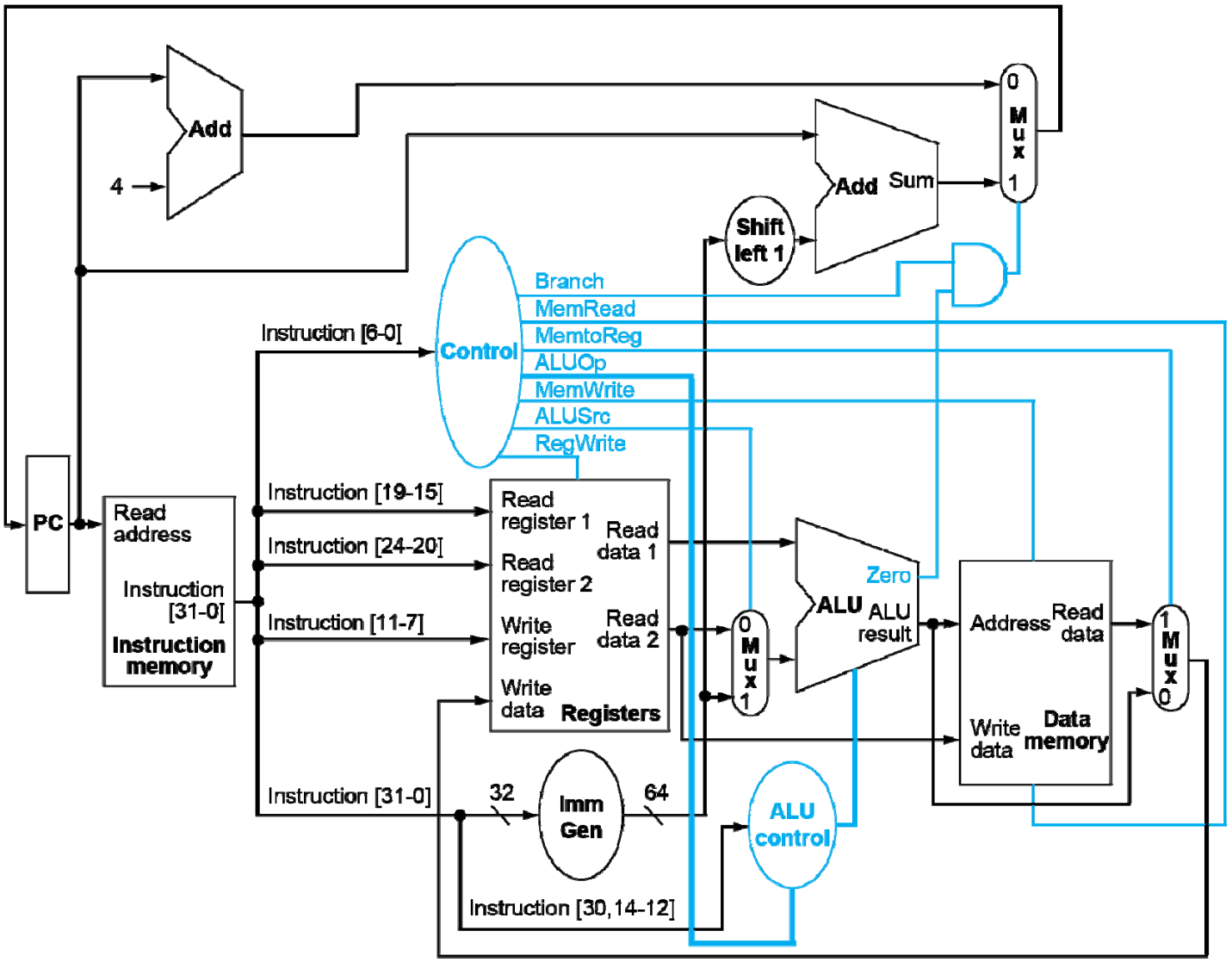




Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
R-format								
lw								
sw								
beq								

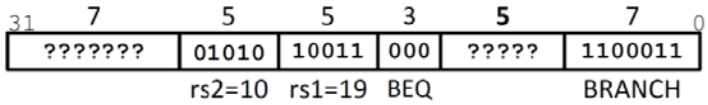
- beq x19,x10, end (true)

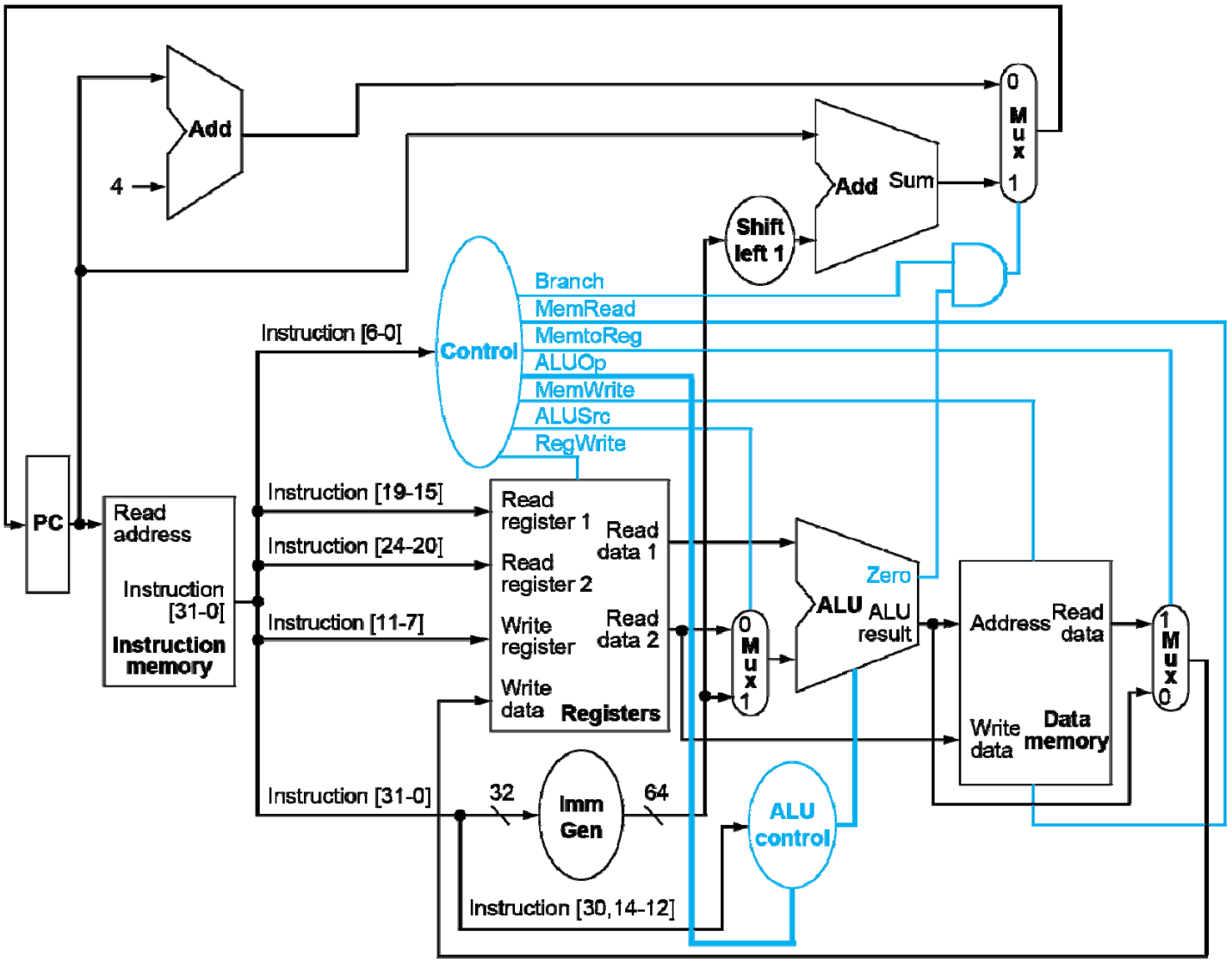




Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
R-format								
lw								
sw								
beq								

- beq x19,x10, end (false)

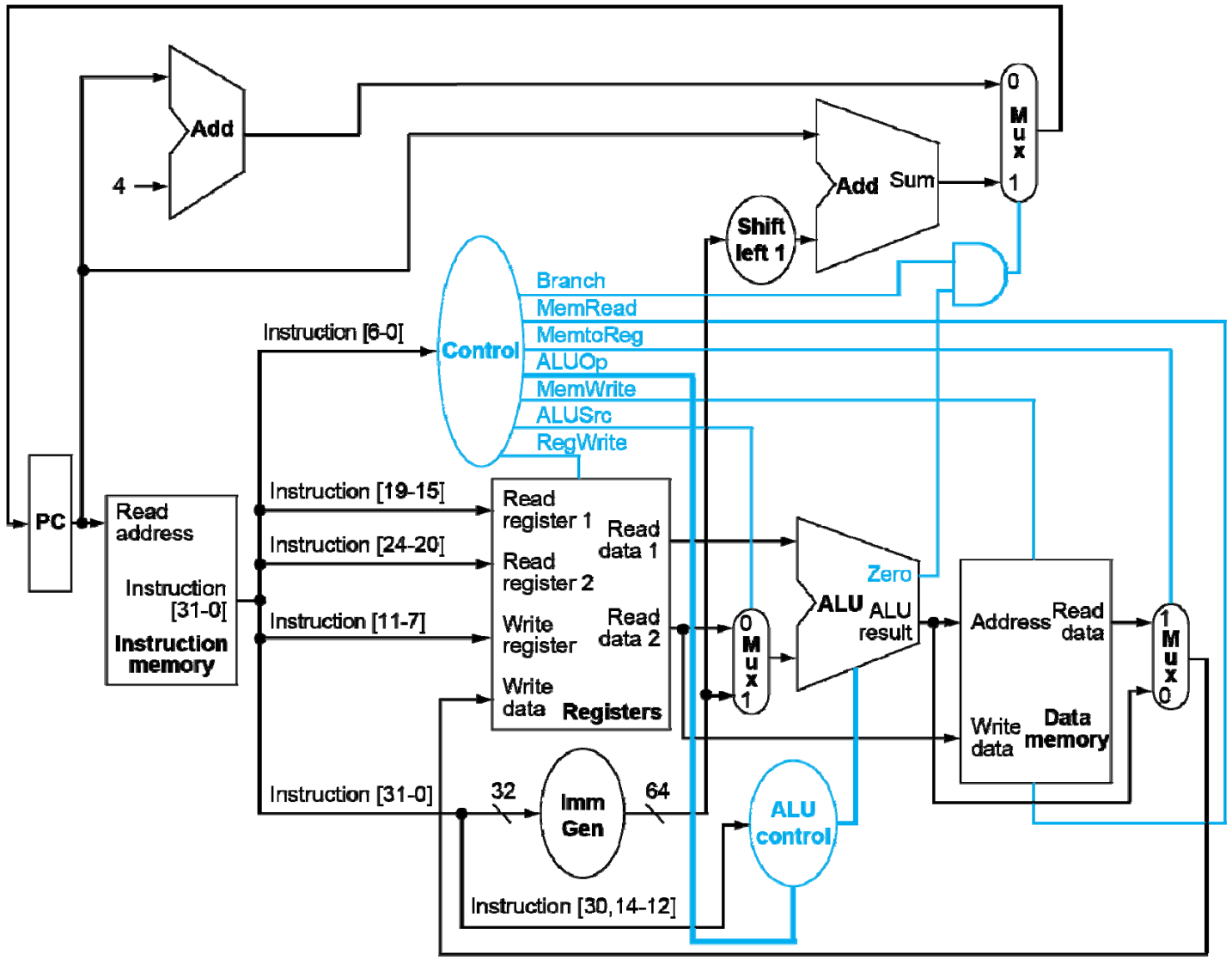




Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
R-format								
lw								
sw								
beq								

- I-Format: addi x15,x1,-50

immediate	rs1	funct3	rd	opcode
12 bits	5 bits	3 bits	5 bits	7 bits



Instruction	RegDst	ALUSrc	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALU Op0
addi								