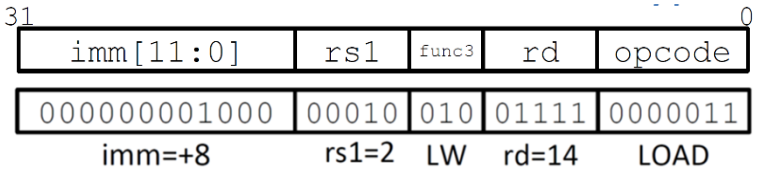
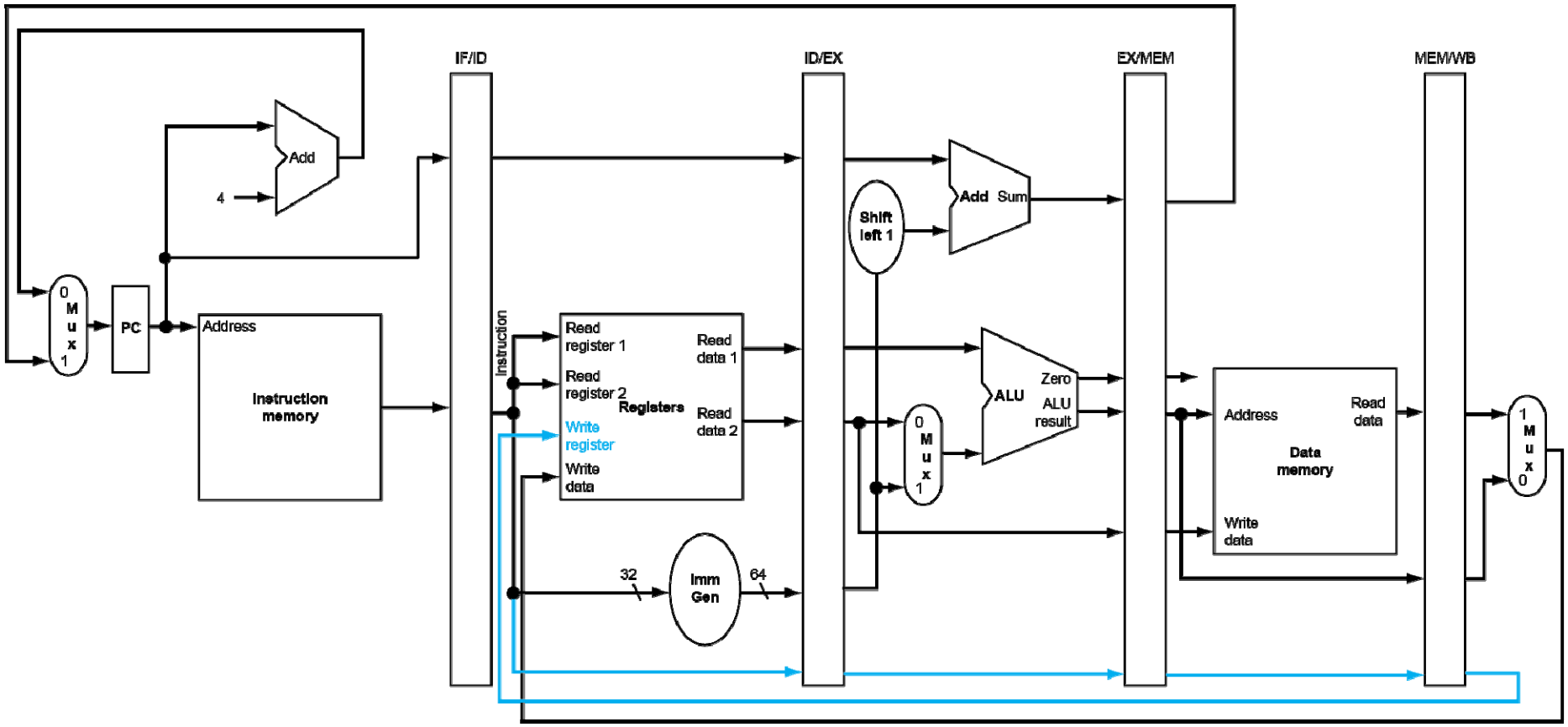
ld x14, 8(x2)

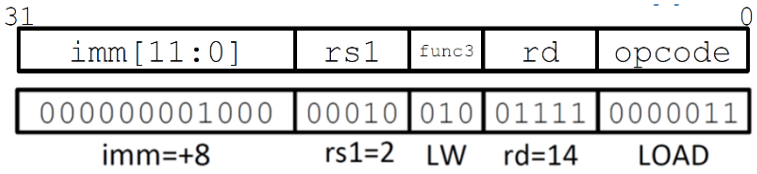
Load-1

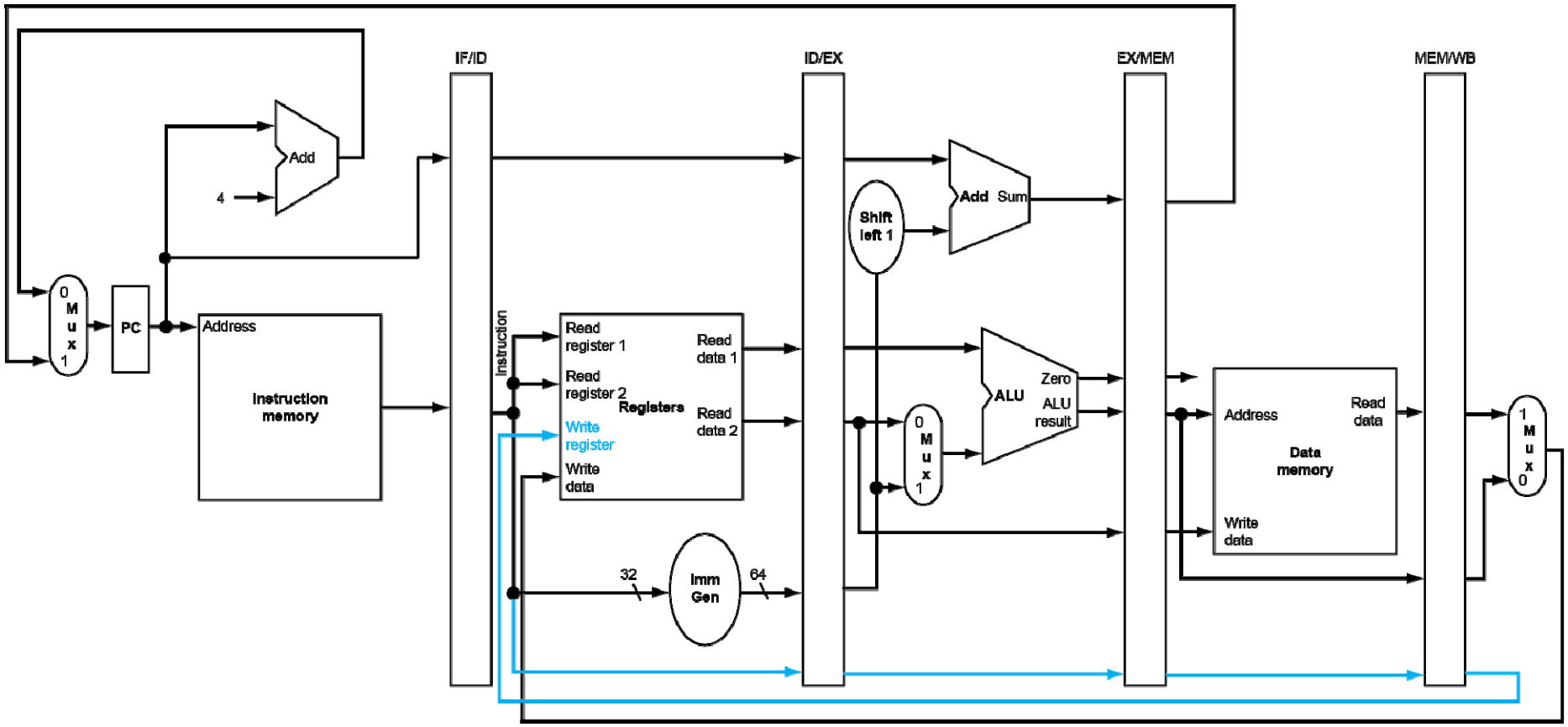




ld x14, 8(x2)

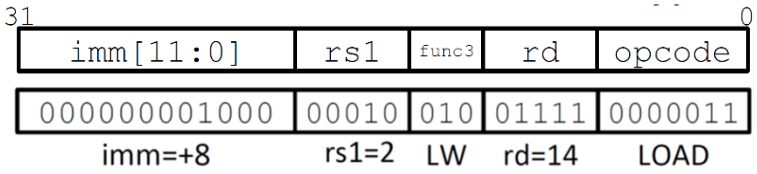
Load-2

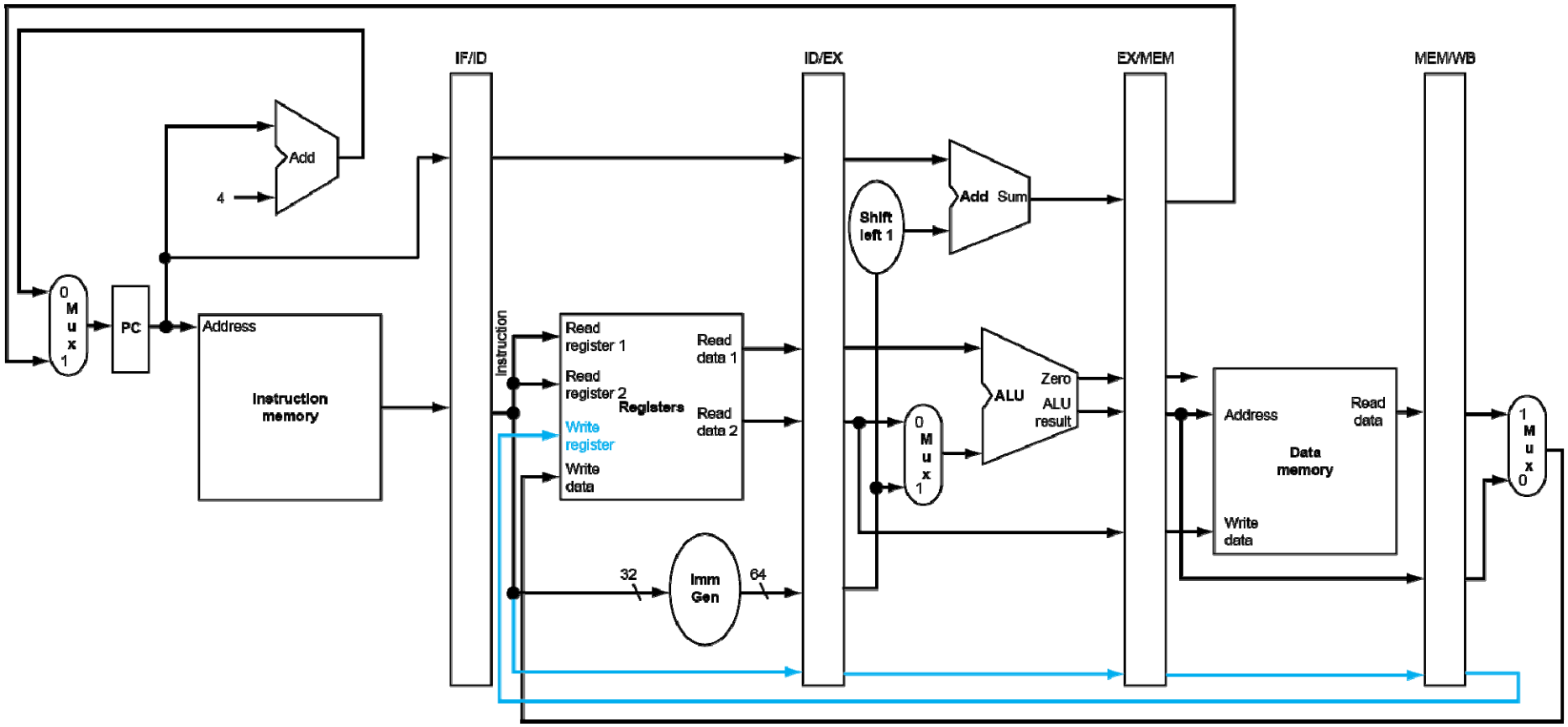




ld x14, 8(x2)

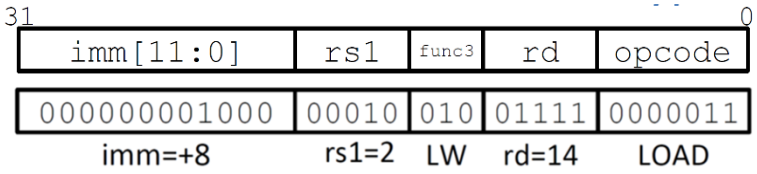
Load-3

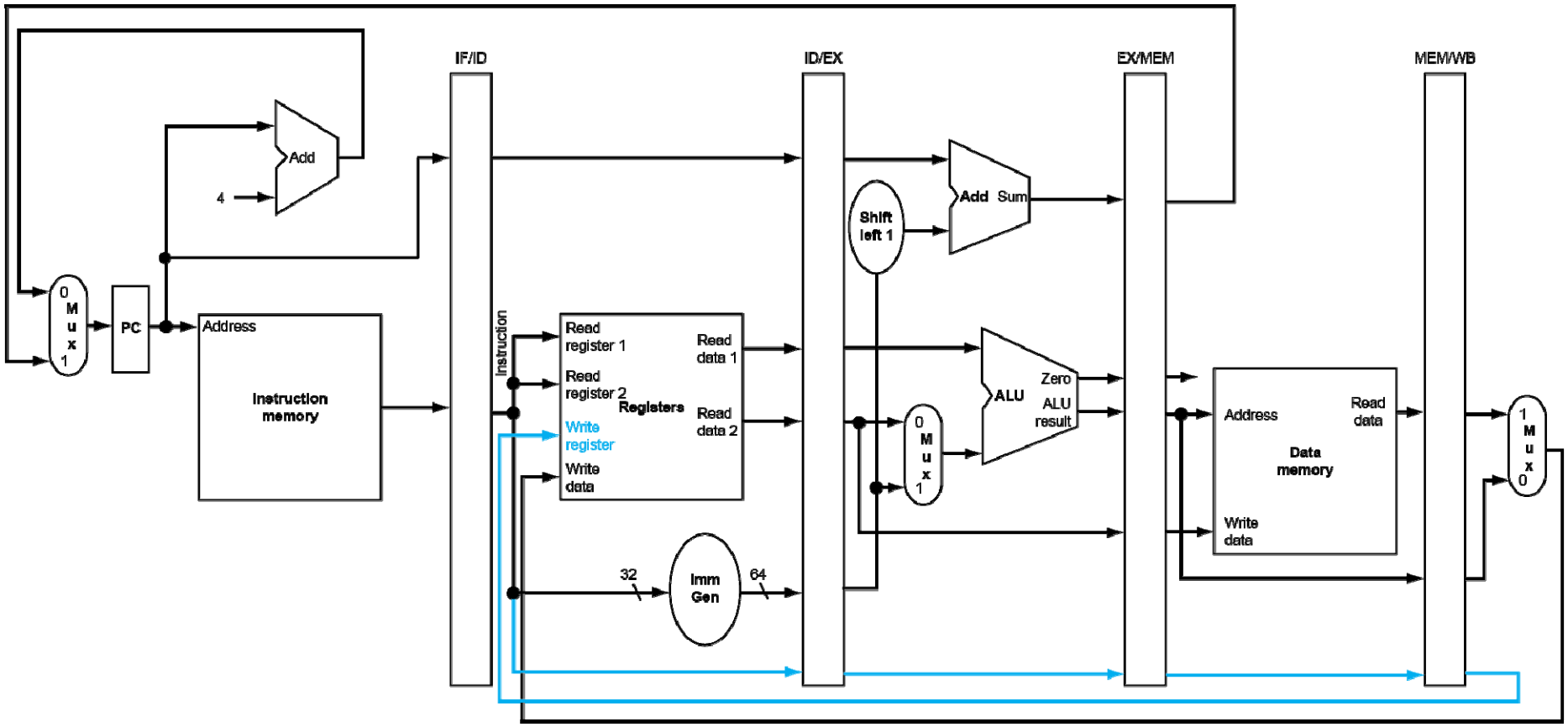




ld x14, 8(x2)

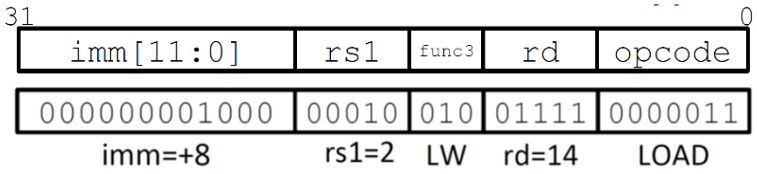
Load-4

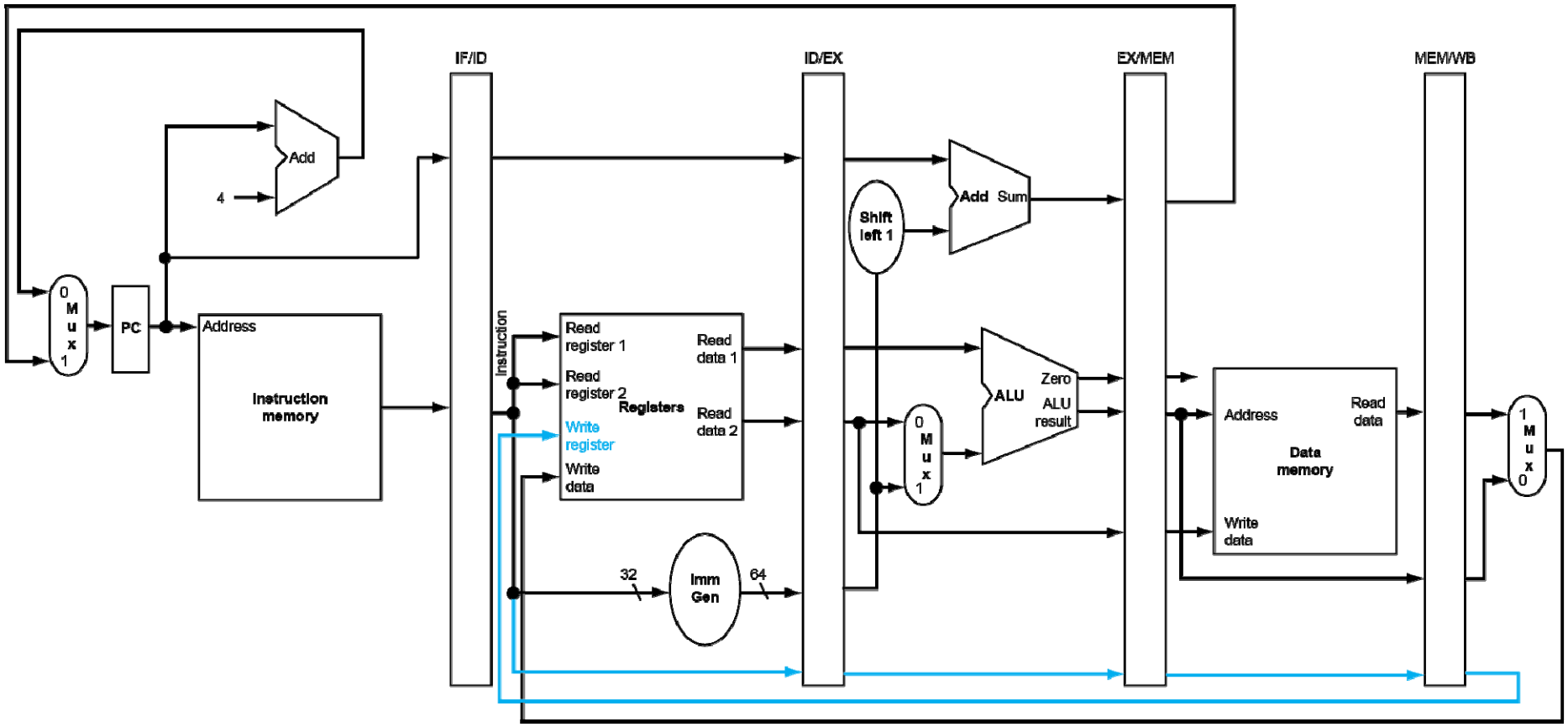


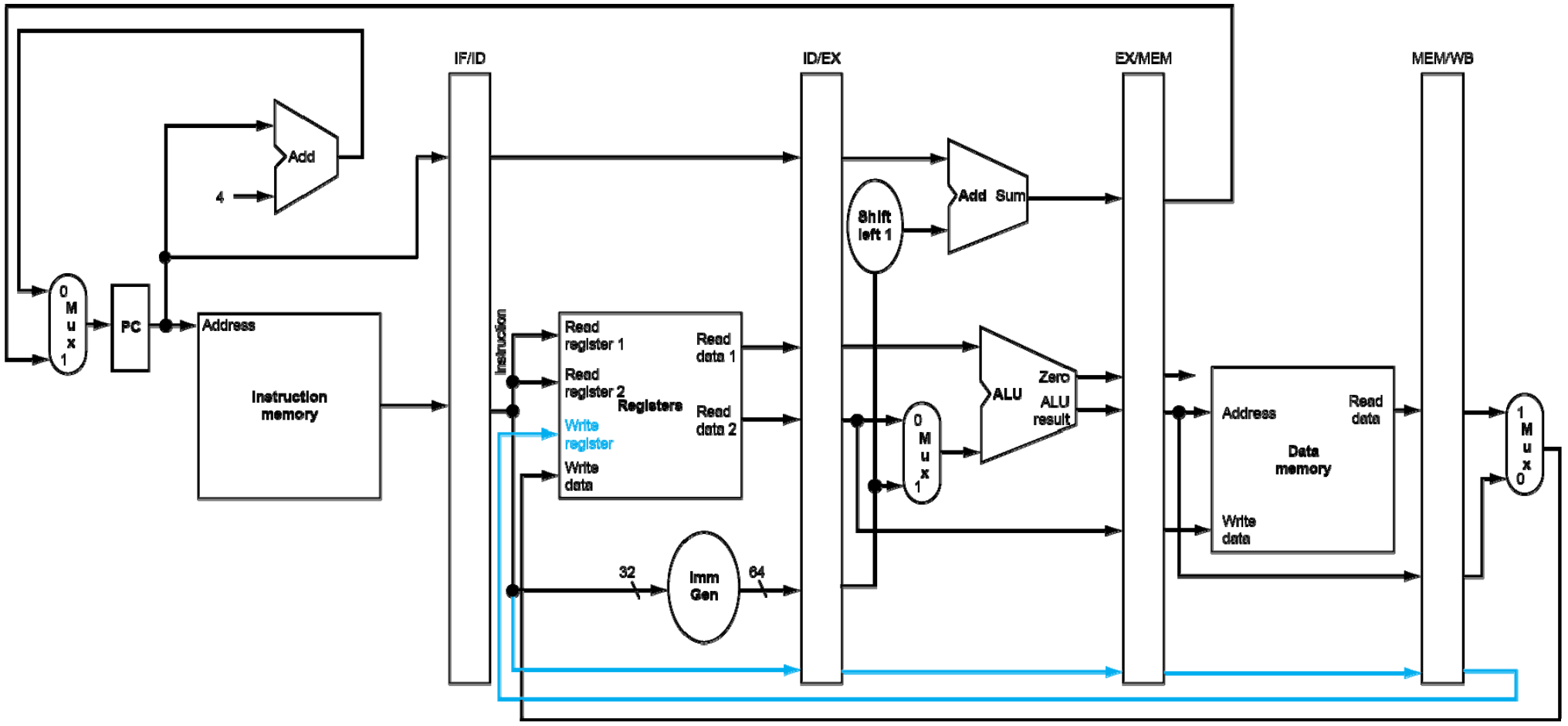


ld x14, 8(x2)

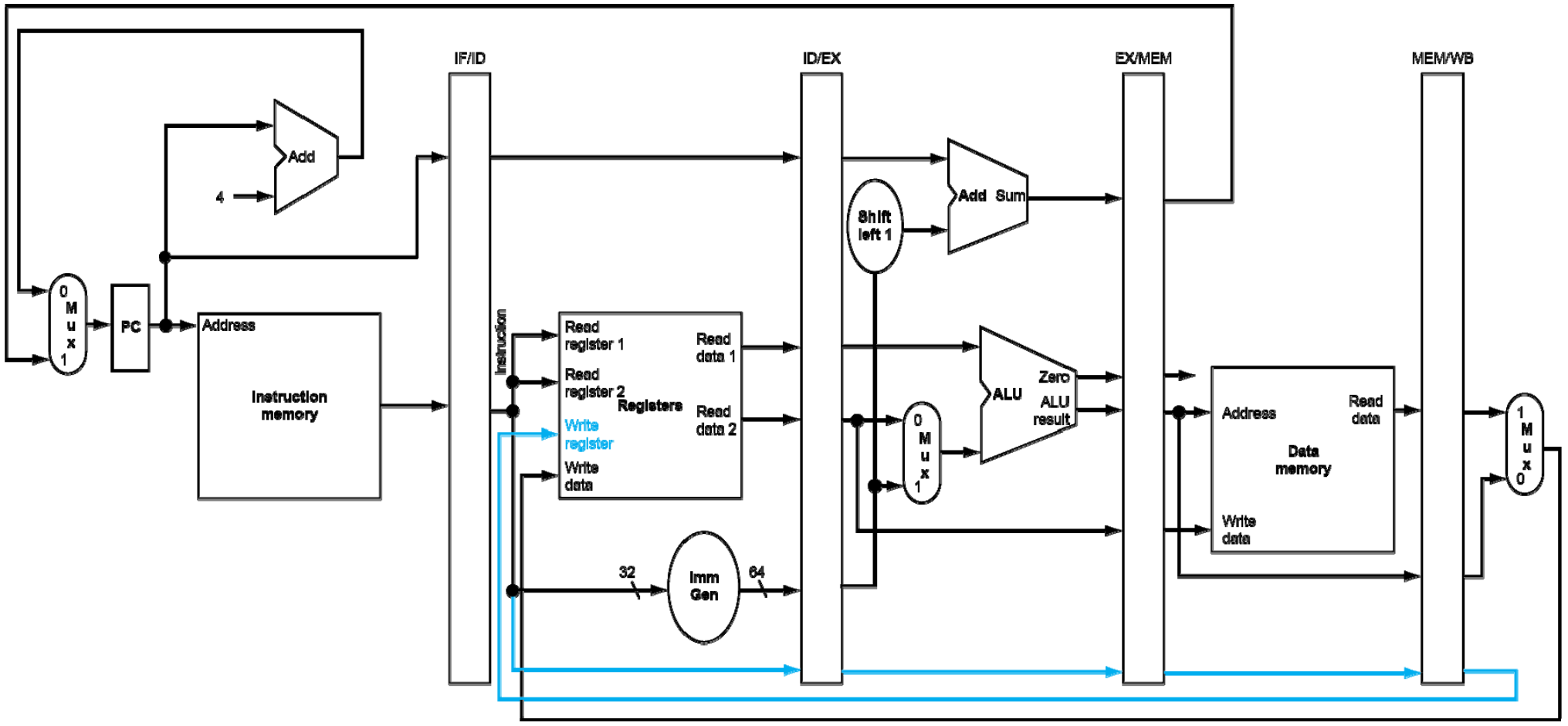
Load-5



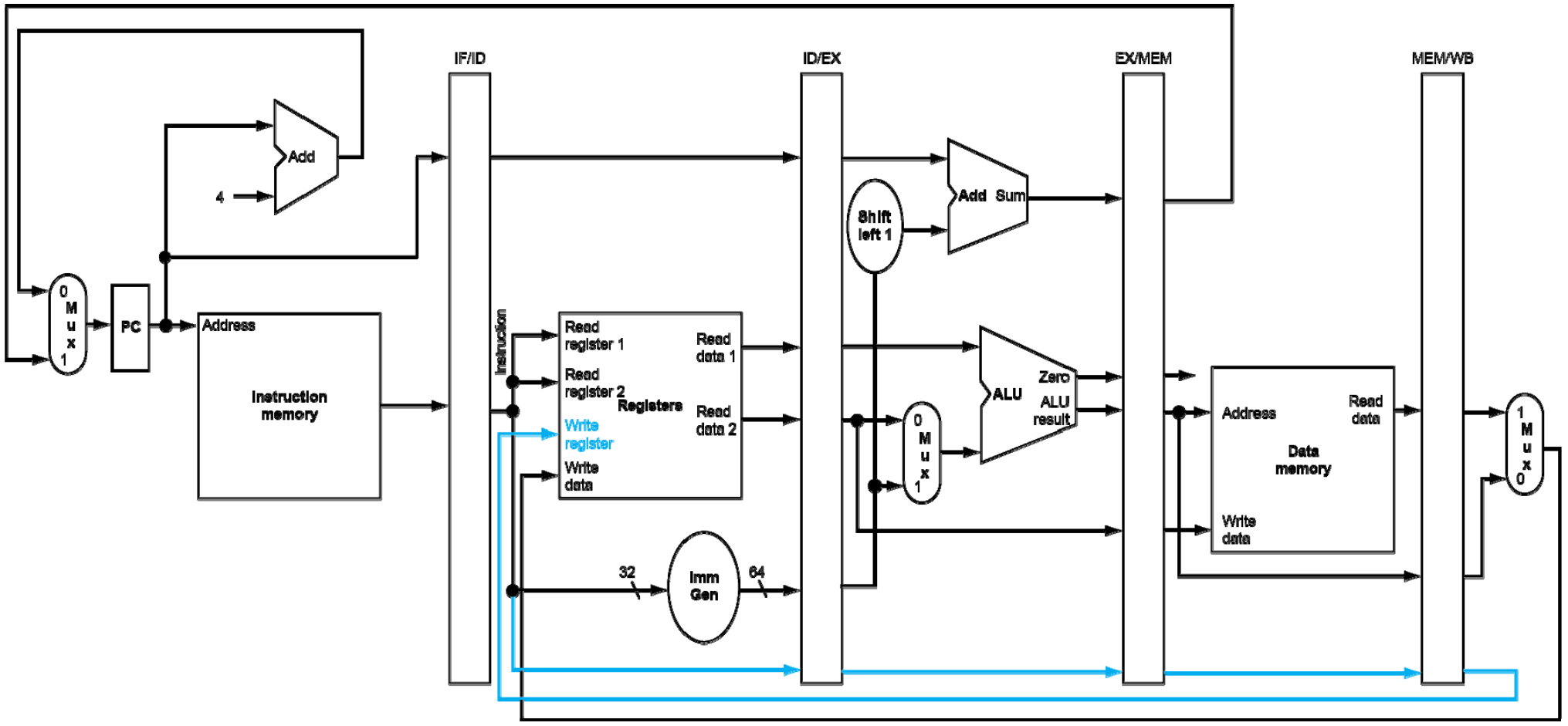




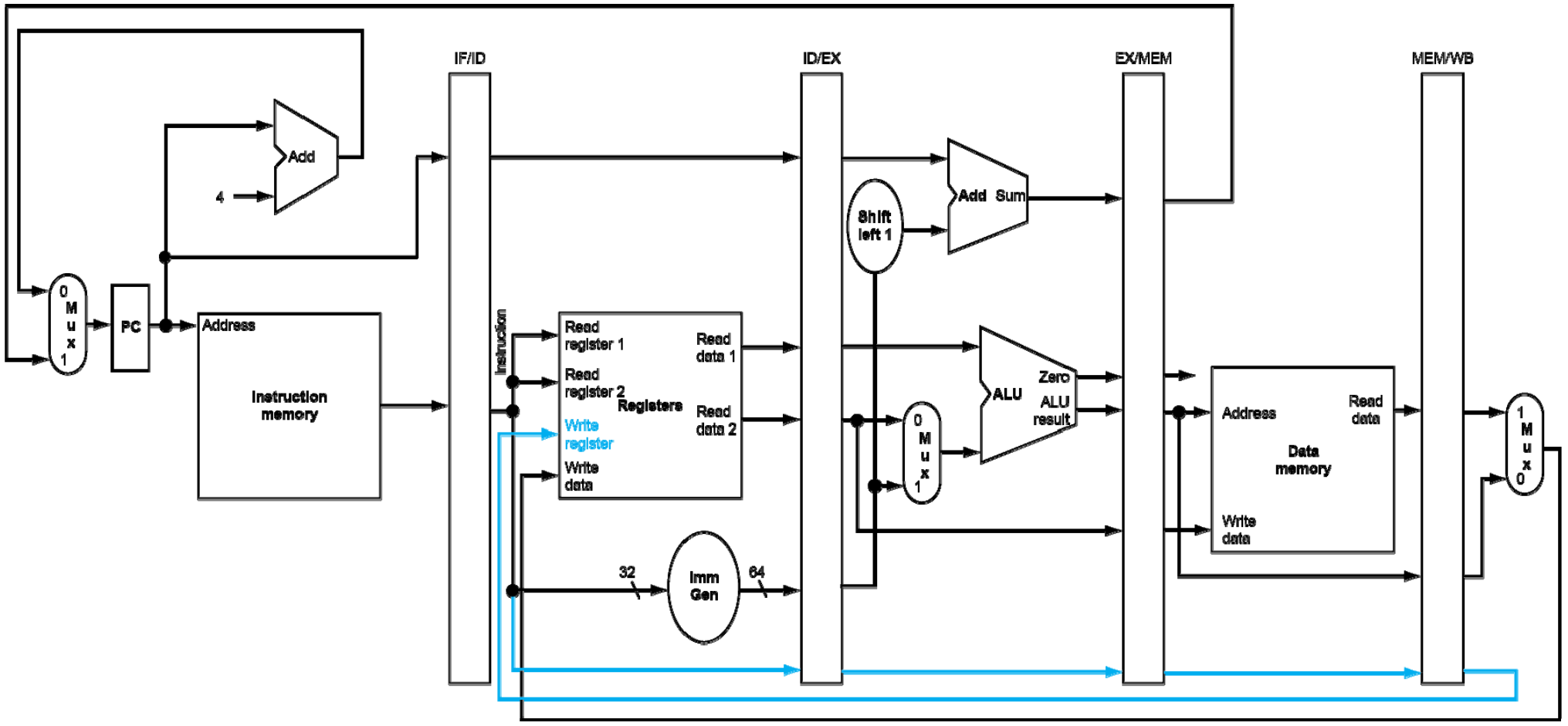
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



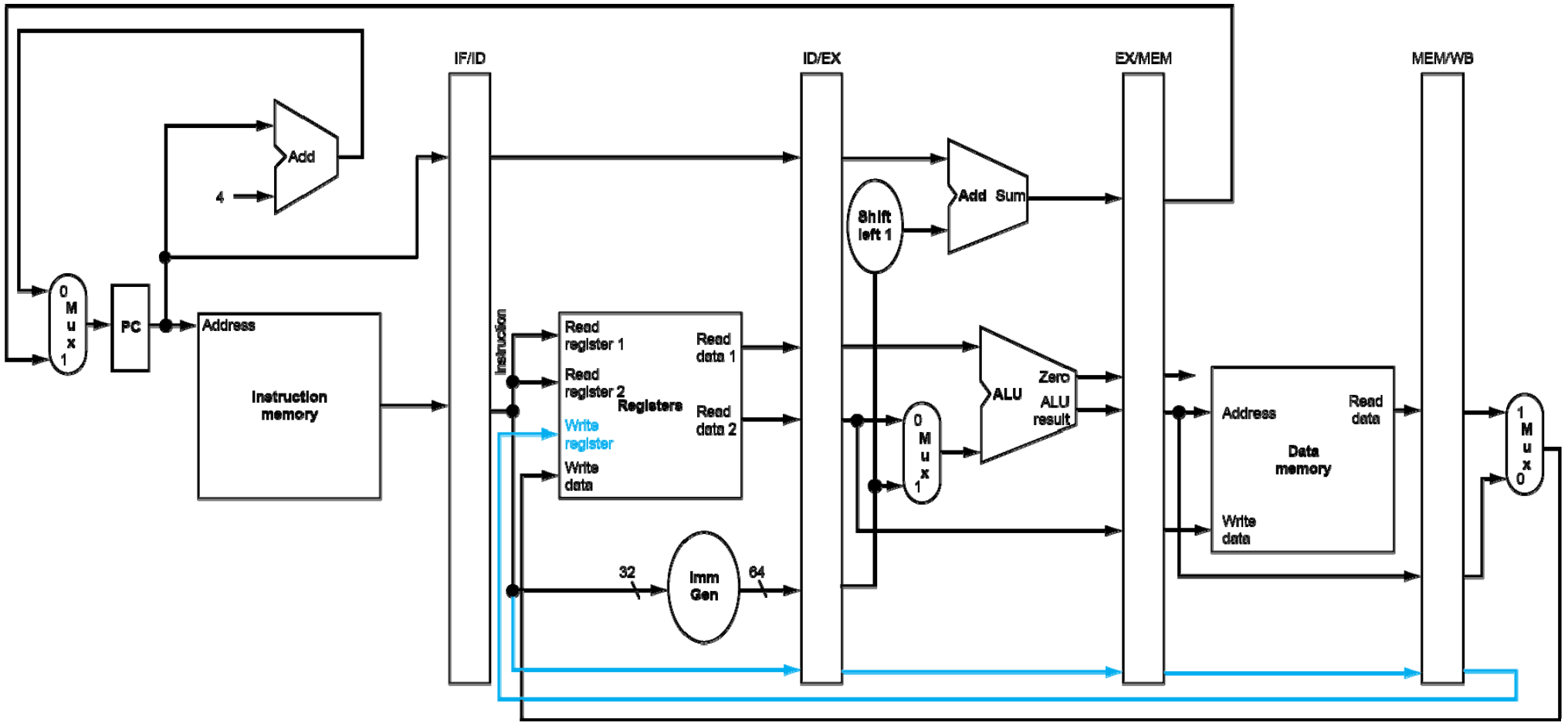
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



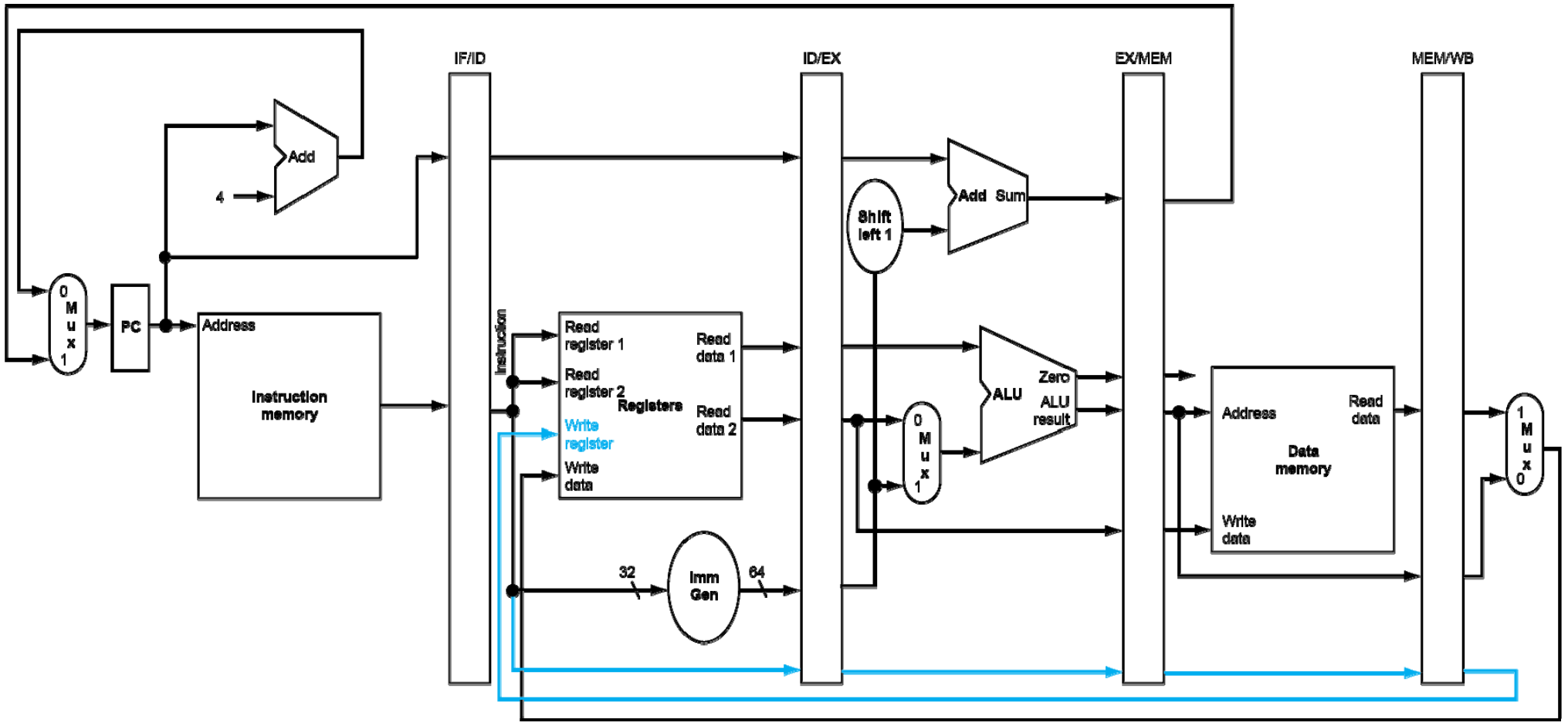
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



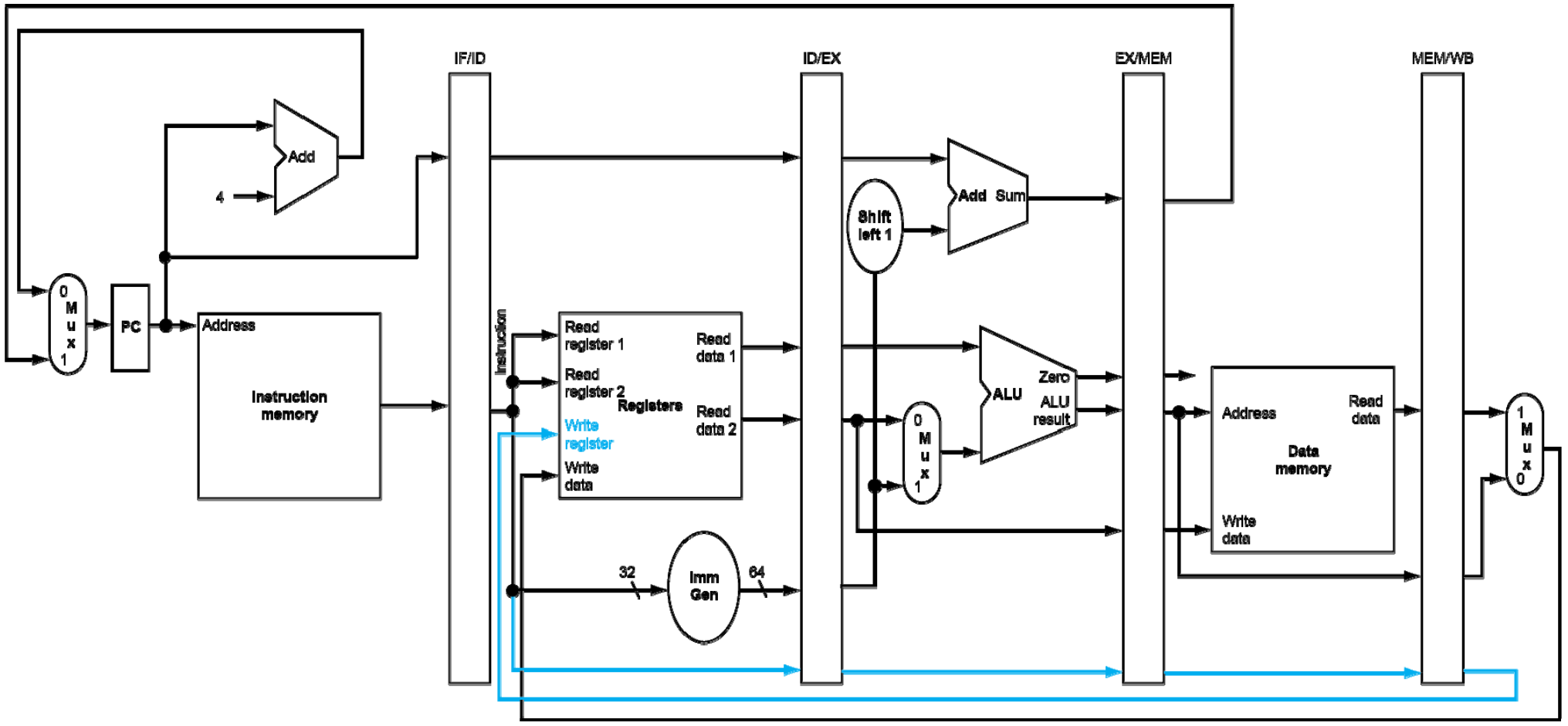
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



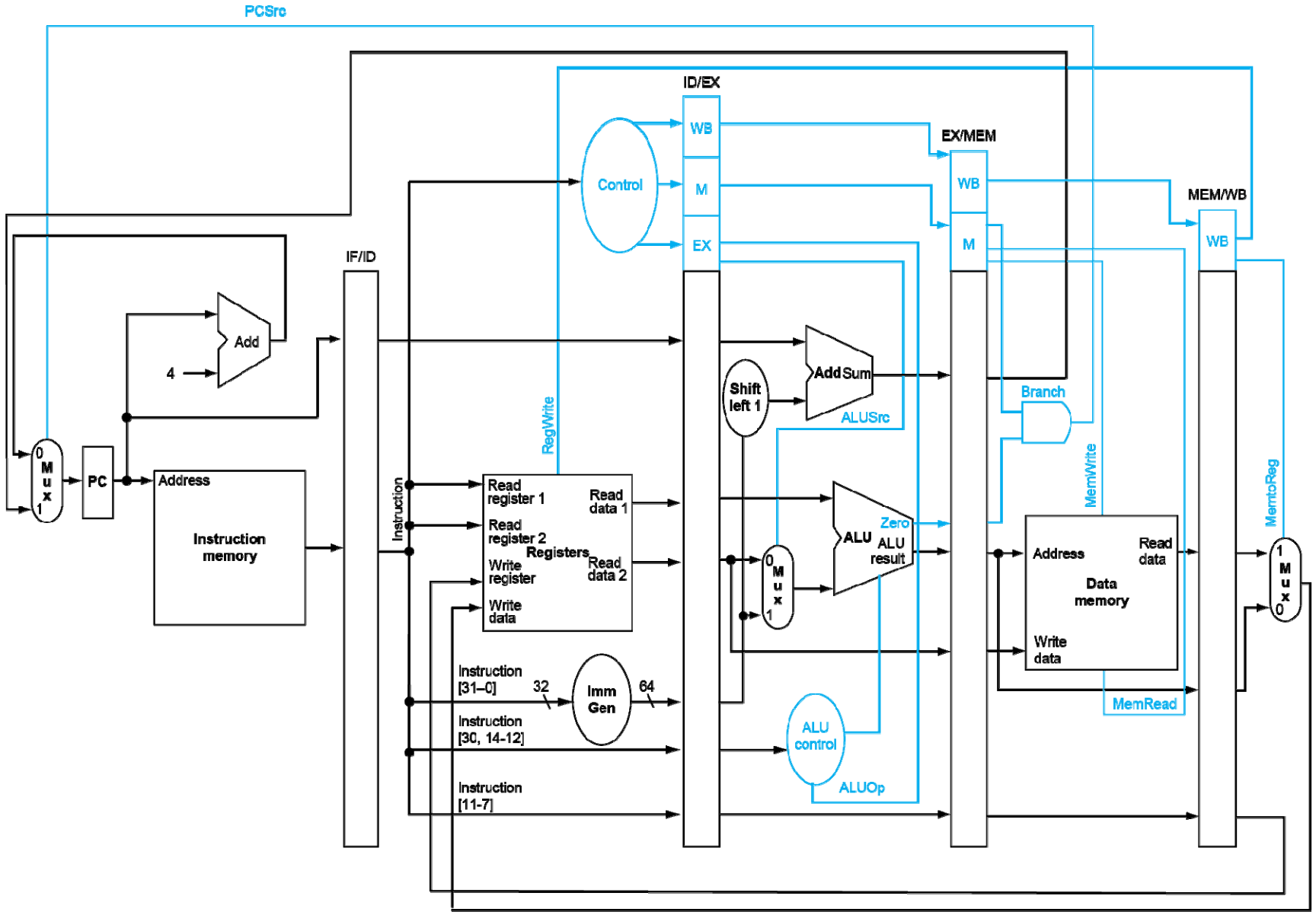
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100

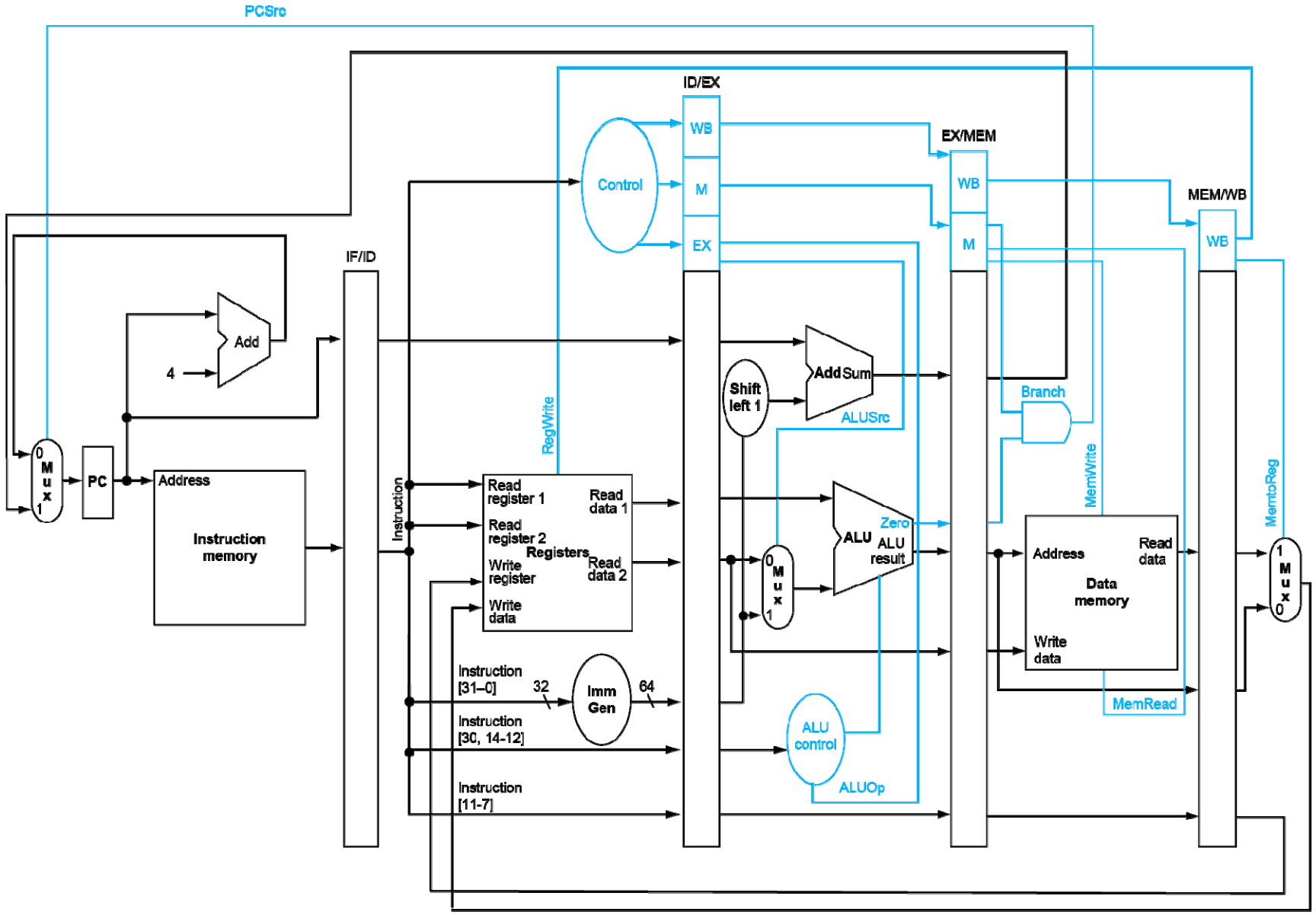
B-2

Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	Reg Dst	ALU Op1	ALU Op0		Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format									
lw									
sw									
beq									



add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100

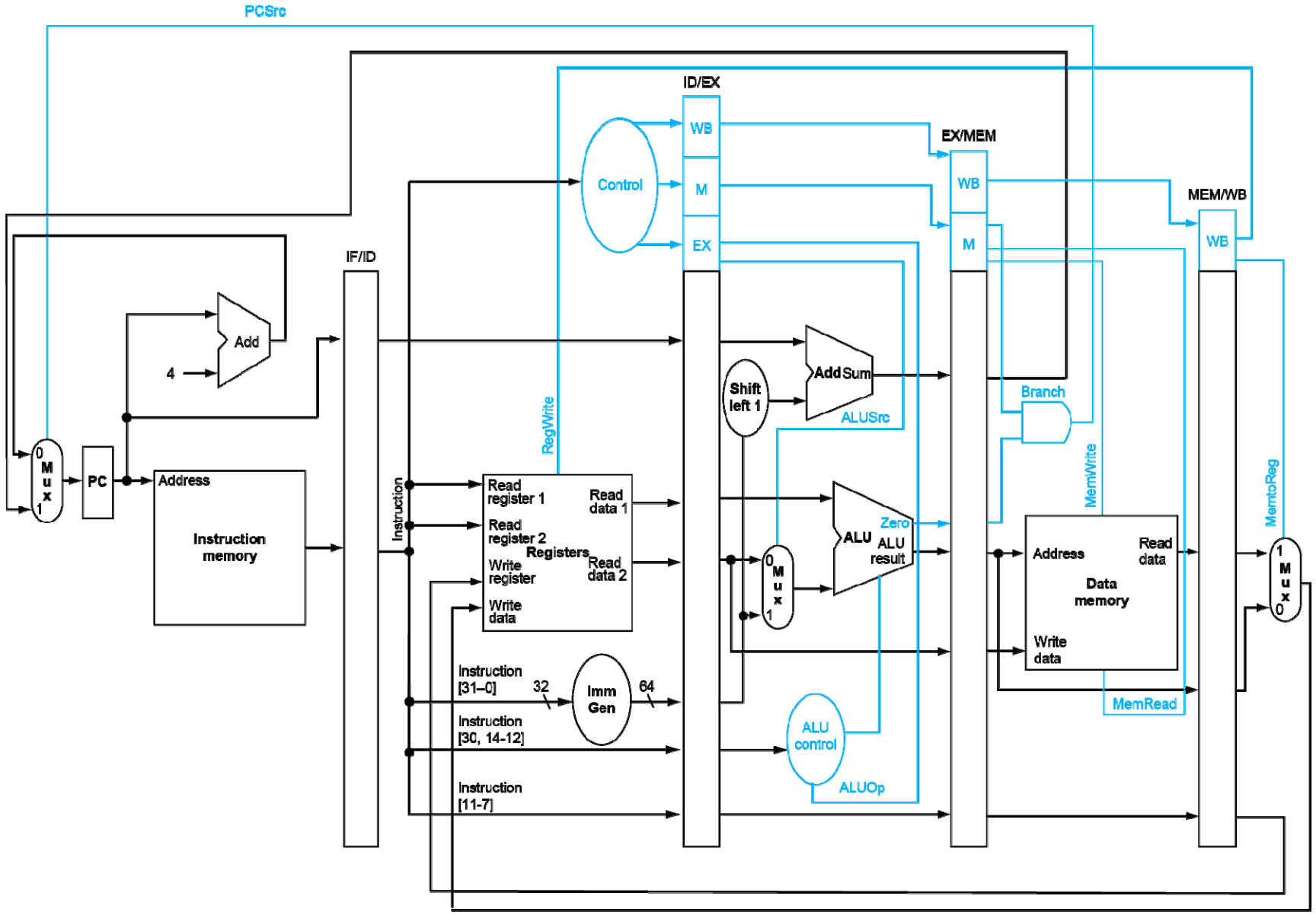
Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	Reg Dst	ALU Op1	ALU Op0		Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format									
lw									
sw									
beq									



add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100

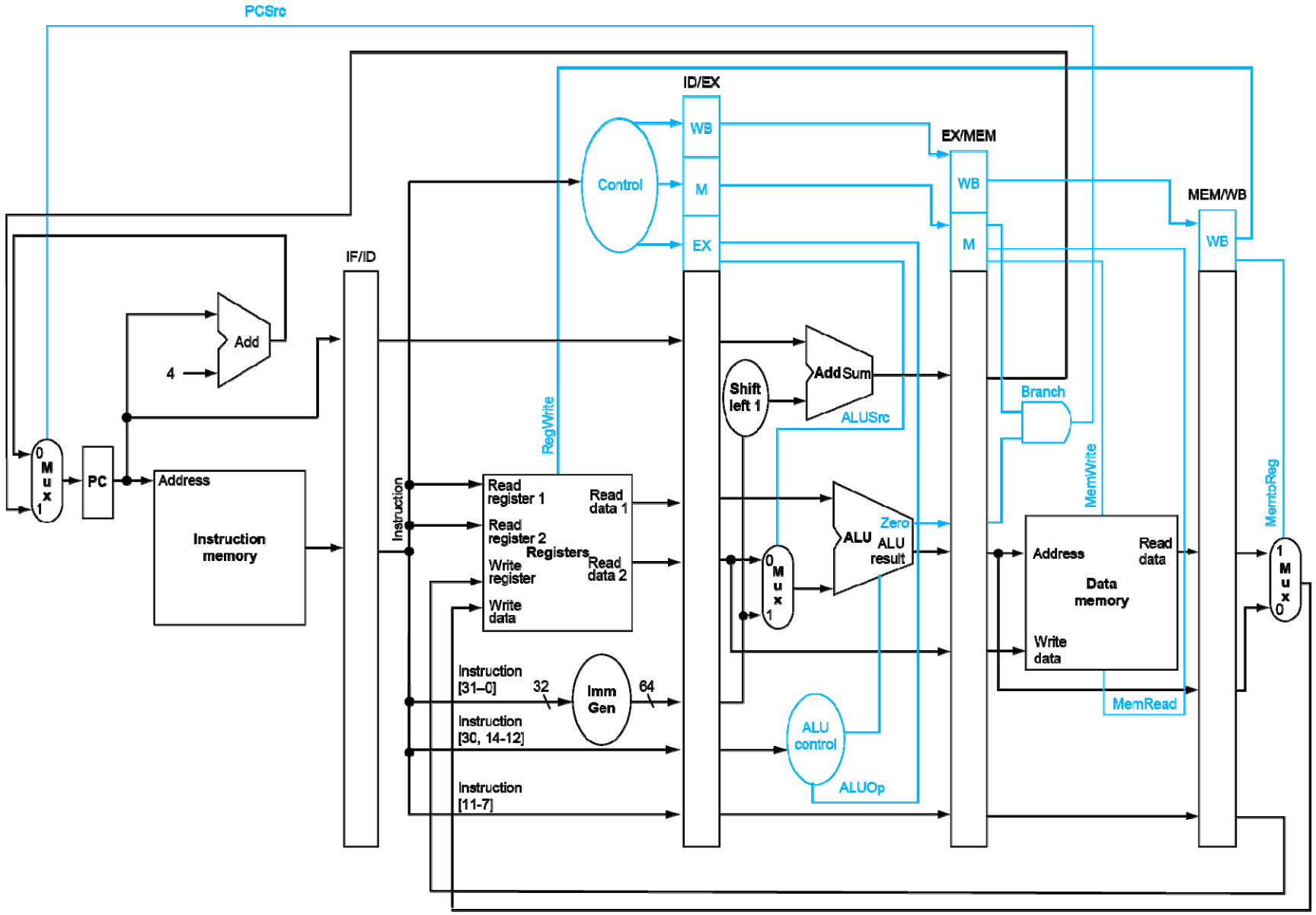
B-4

Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	Reg Dst	ALU Op1	ALU Op0		Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format									
lw									
sw									
beq									



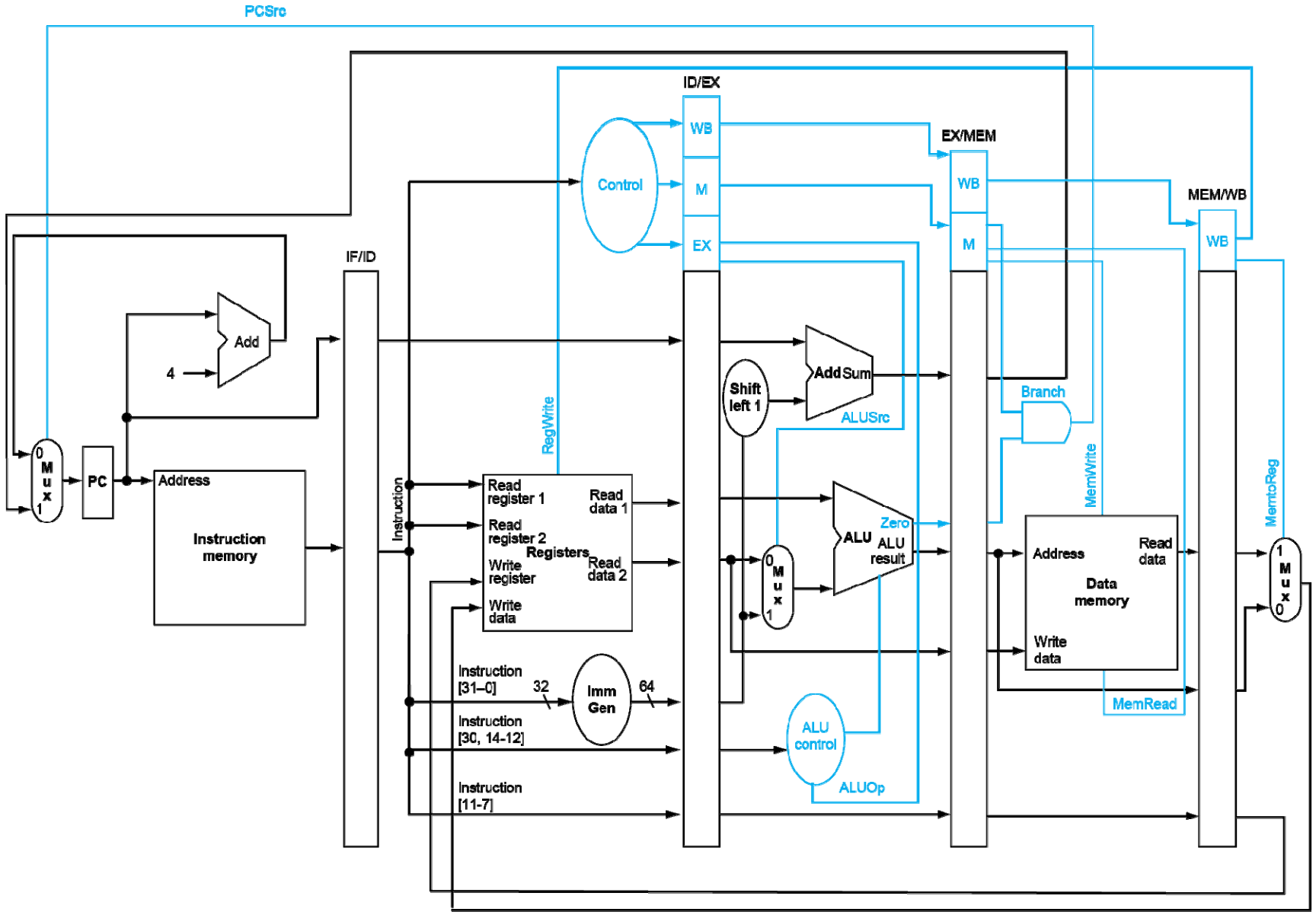
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100

Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	Reg Dst	ALU Op1	ALU Op0		Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format									
lw									
sw									
beq									

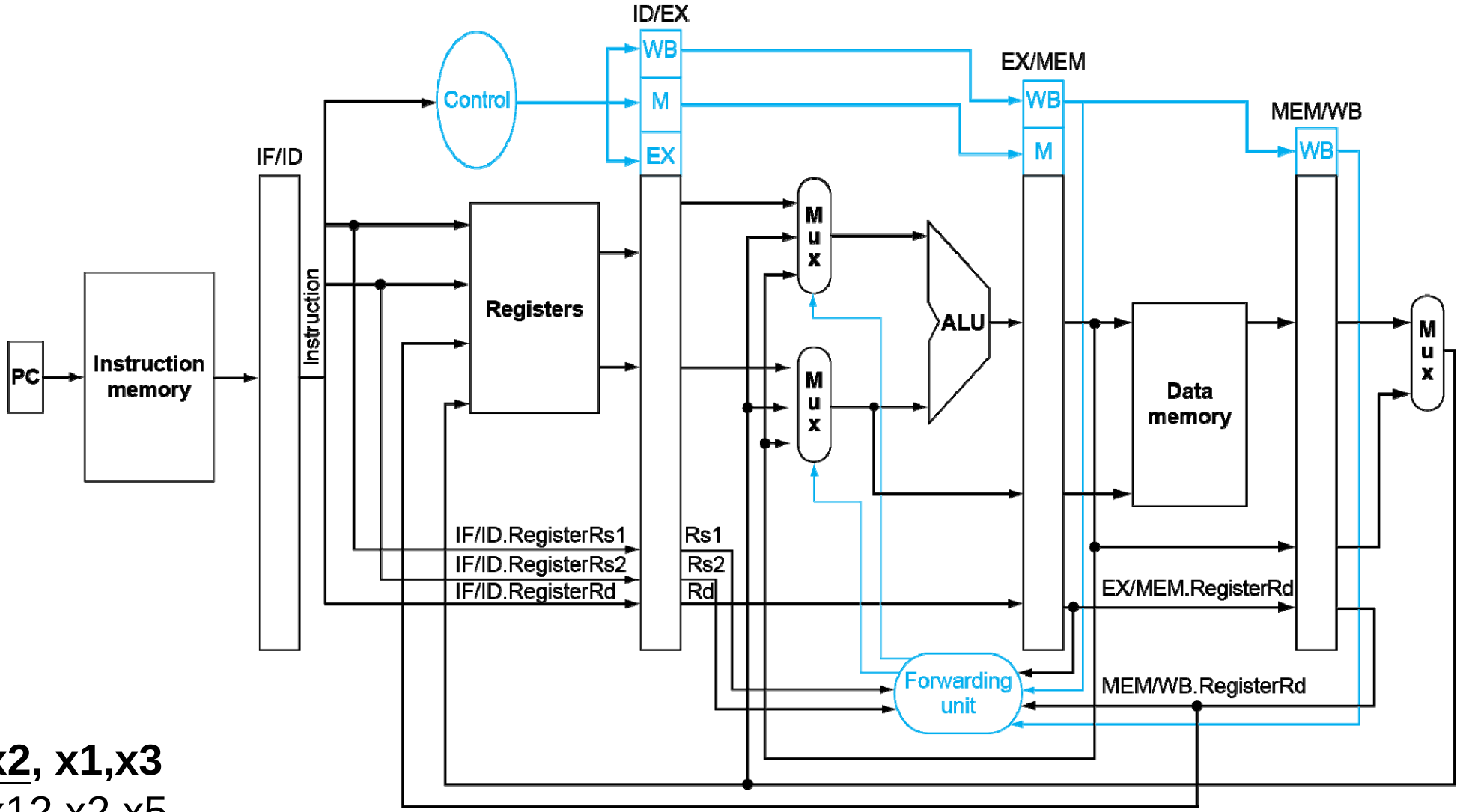


add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100

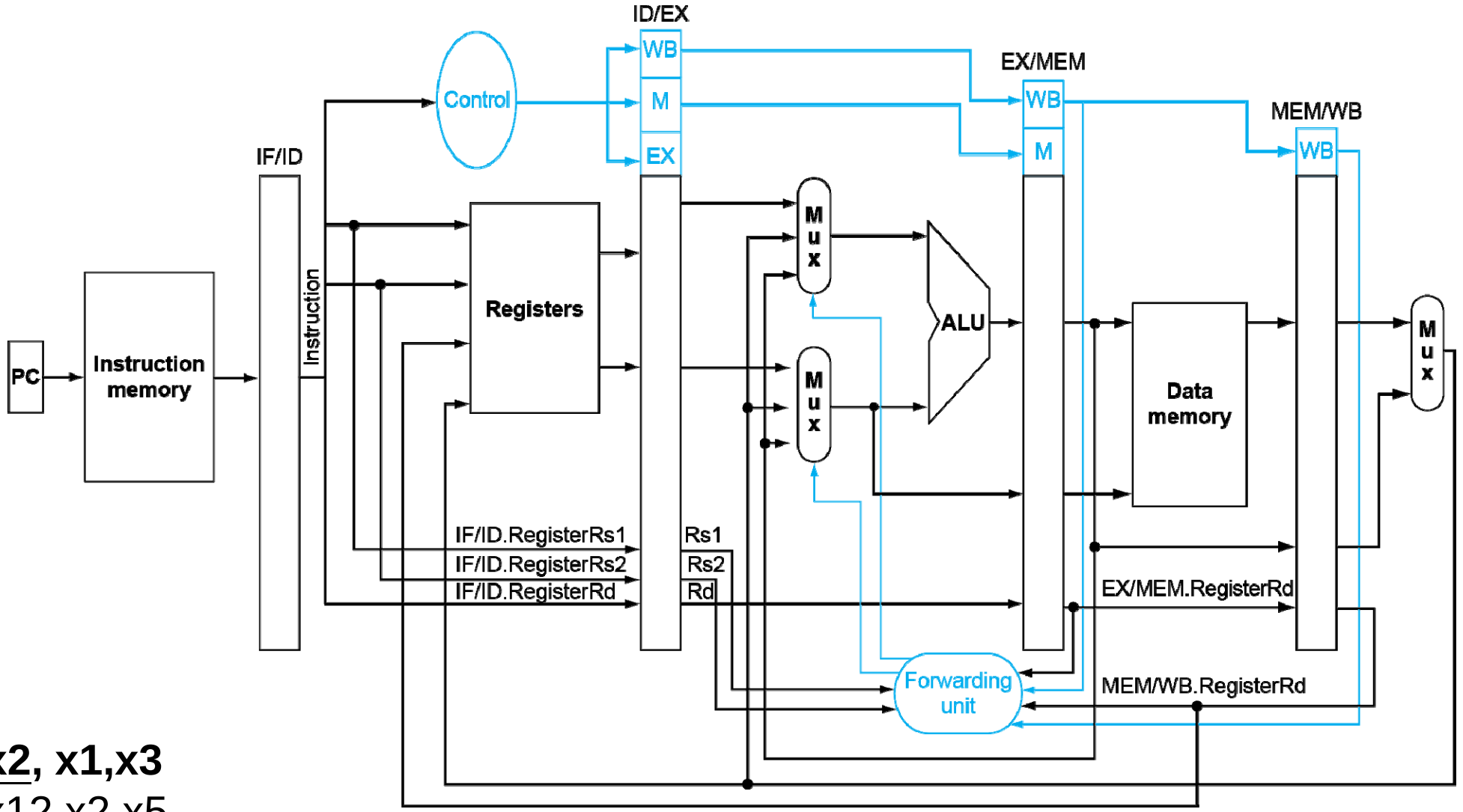
Instruction	Execution/Address Calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	Reg Dst	ALU Op1	ALU Op0		Branch	Mem Read	Mem Write	Reg write	Mem to Reg
R-format									
lw									
sw									
beq									



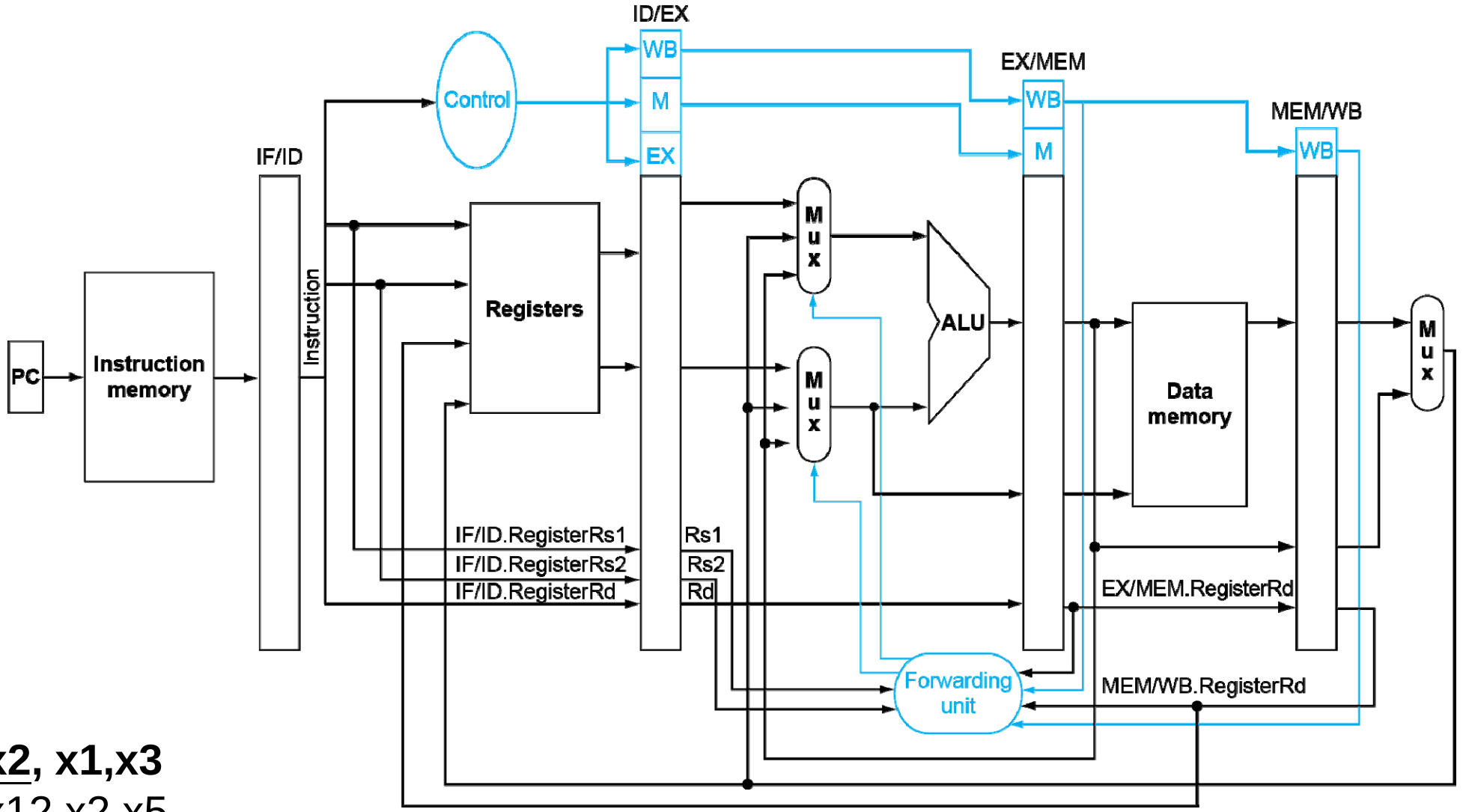
add x4, x1,x3
lw x12,30(x2)
sw x13,50(x6)
beq x14,x2,100



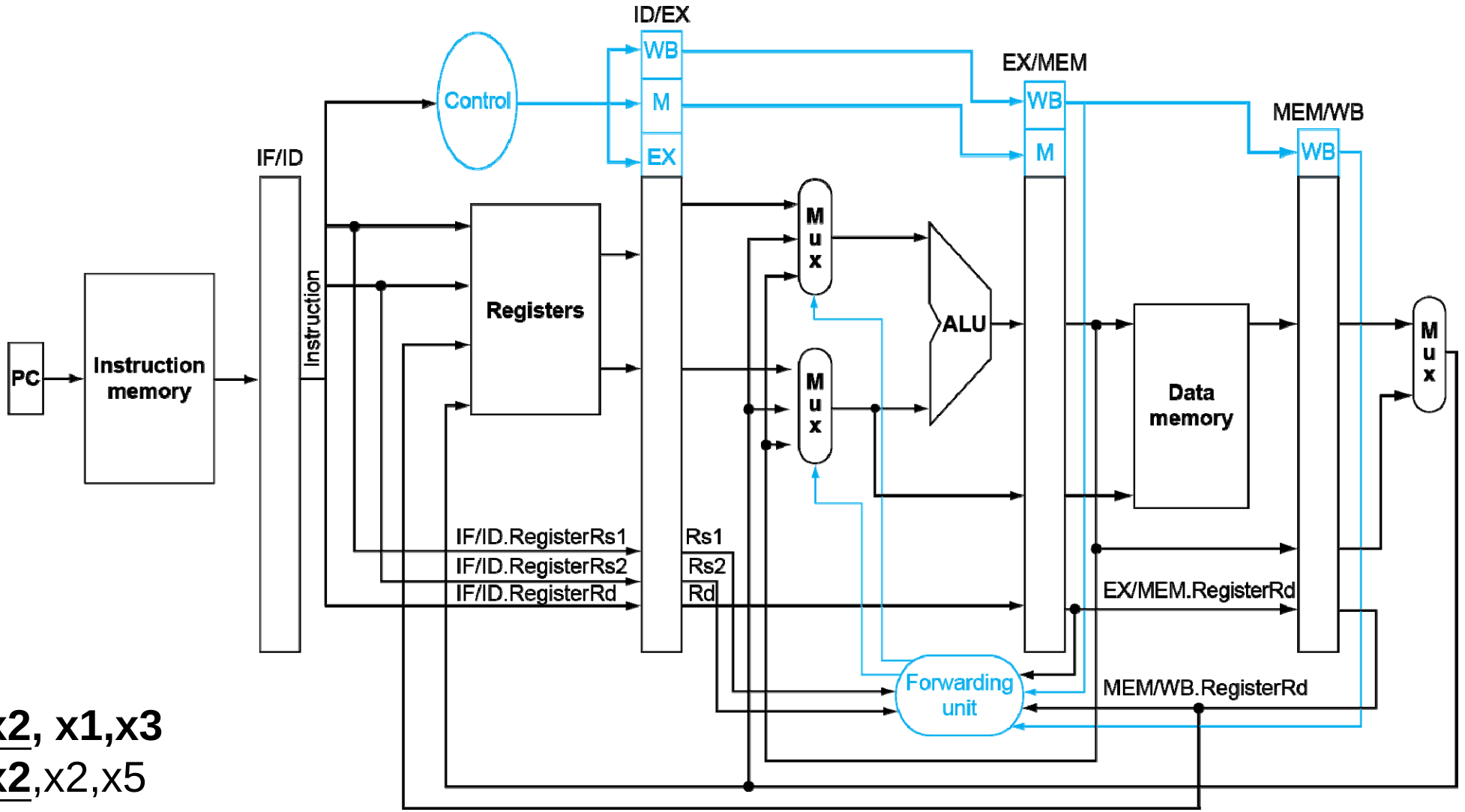
sub x2, x1,x3
and x12,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



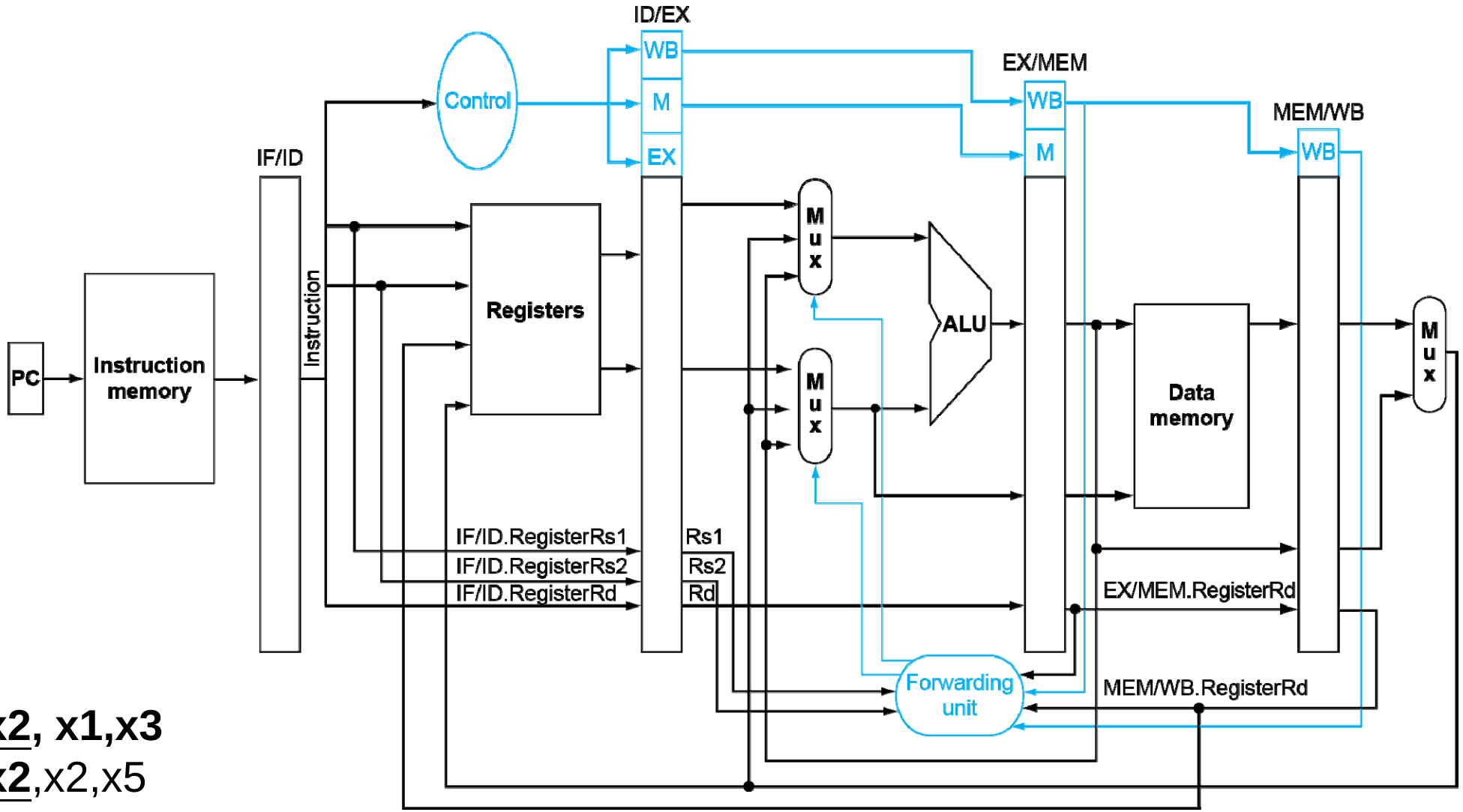
sub x2, x1,x3
and x12,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



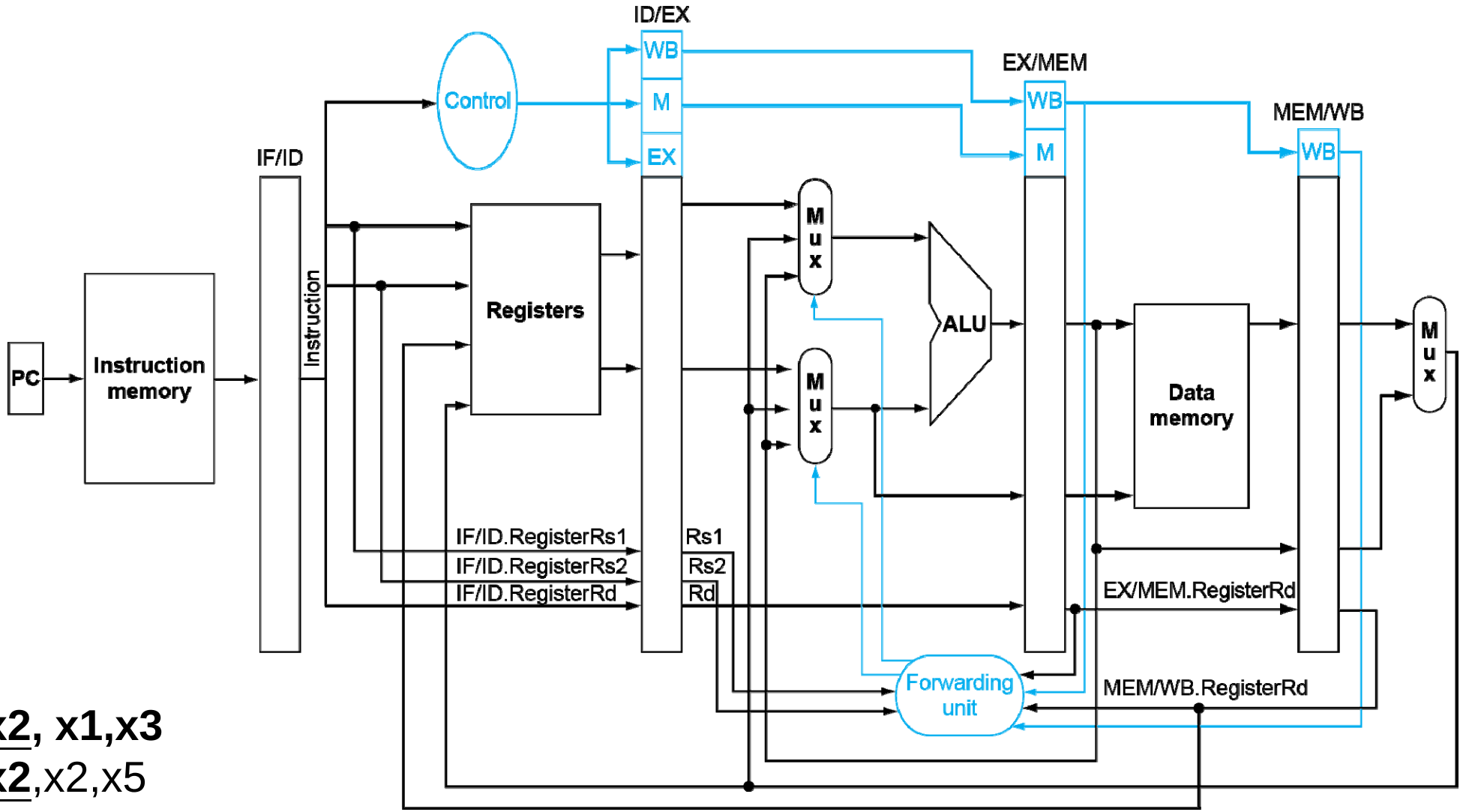
sub x2, x1,x3
and x12,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



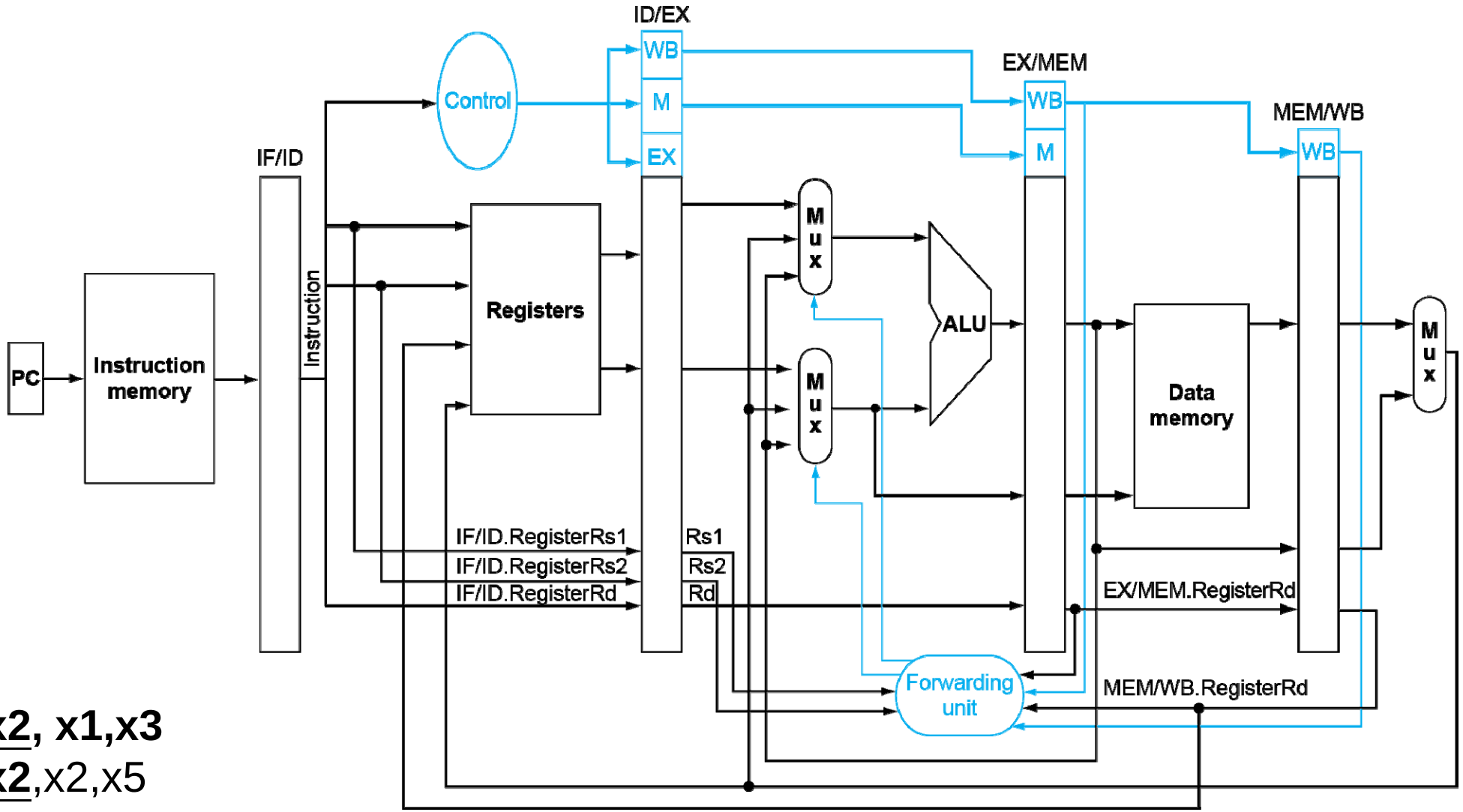
sub **<u>x2</u>, x1,x3**
and **<u>x2</u>**,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



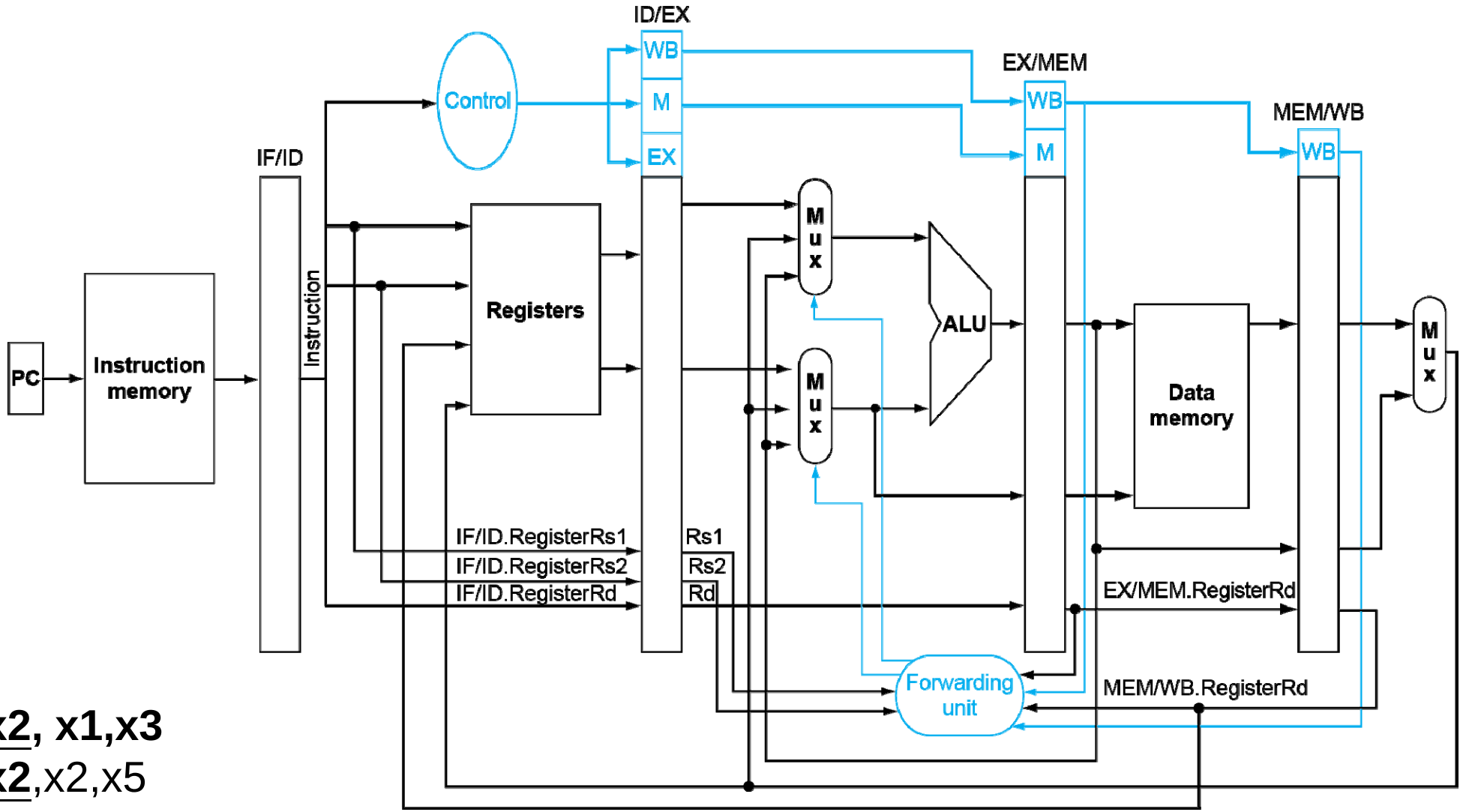
sub **<u>x2</u>, x1,x3**
and **<u>x2</u>**,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



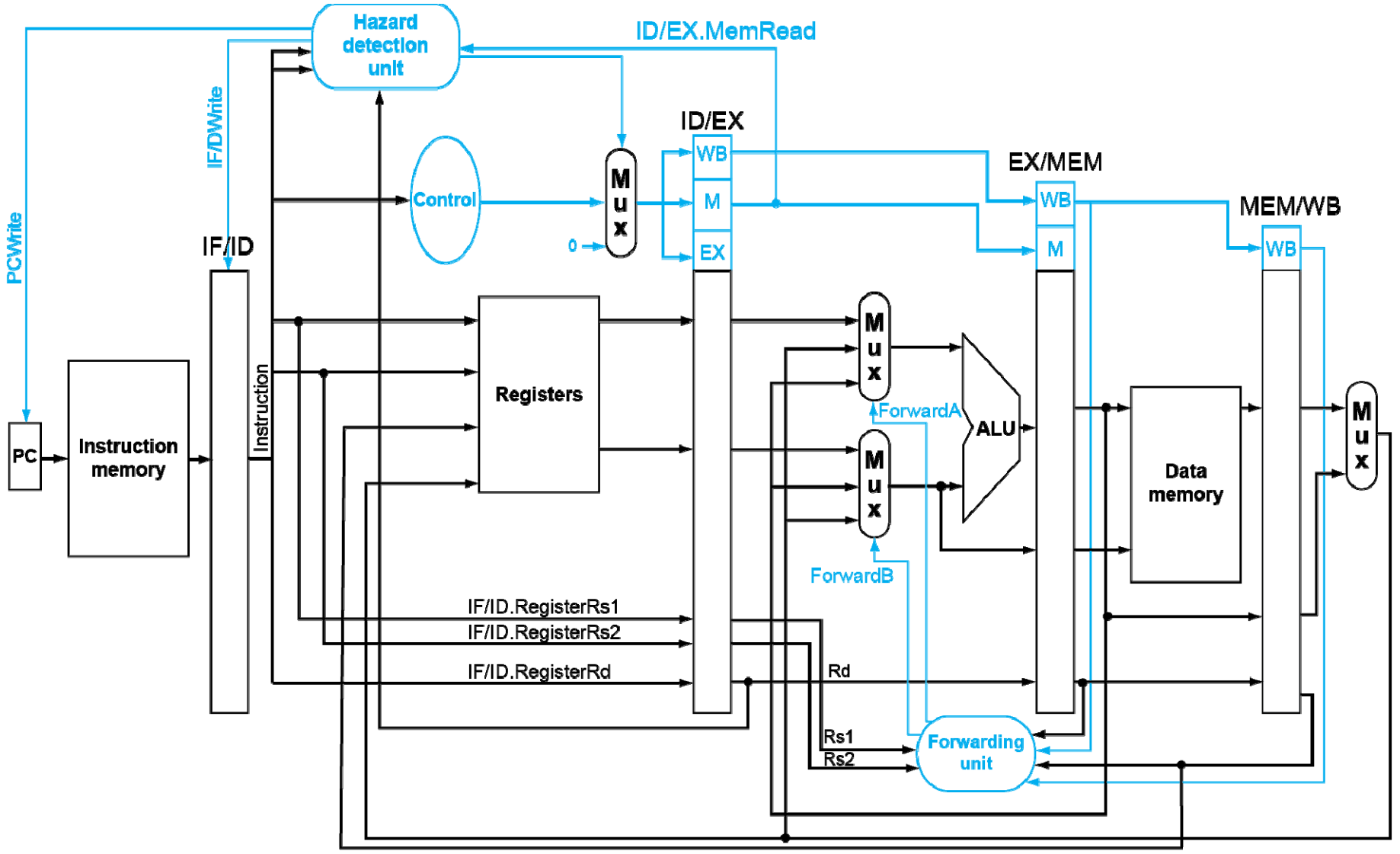
sub **<u>x2</u>, x1,x3**
and **<u>x2</u>**,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



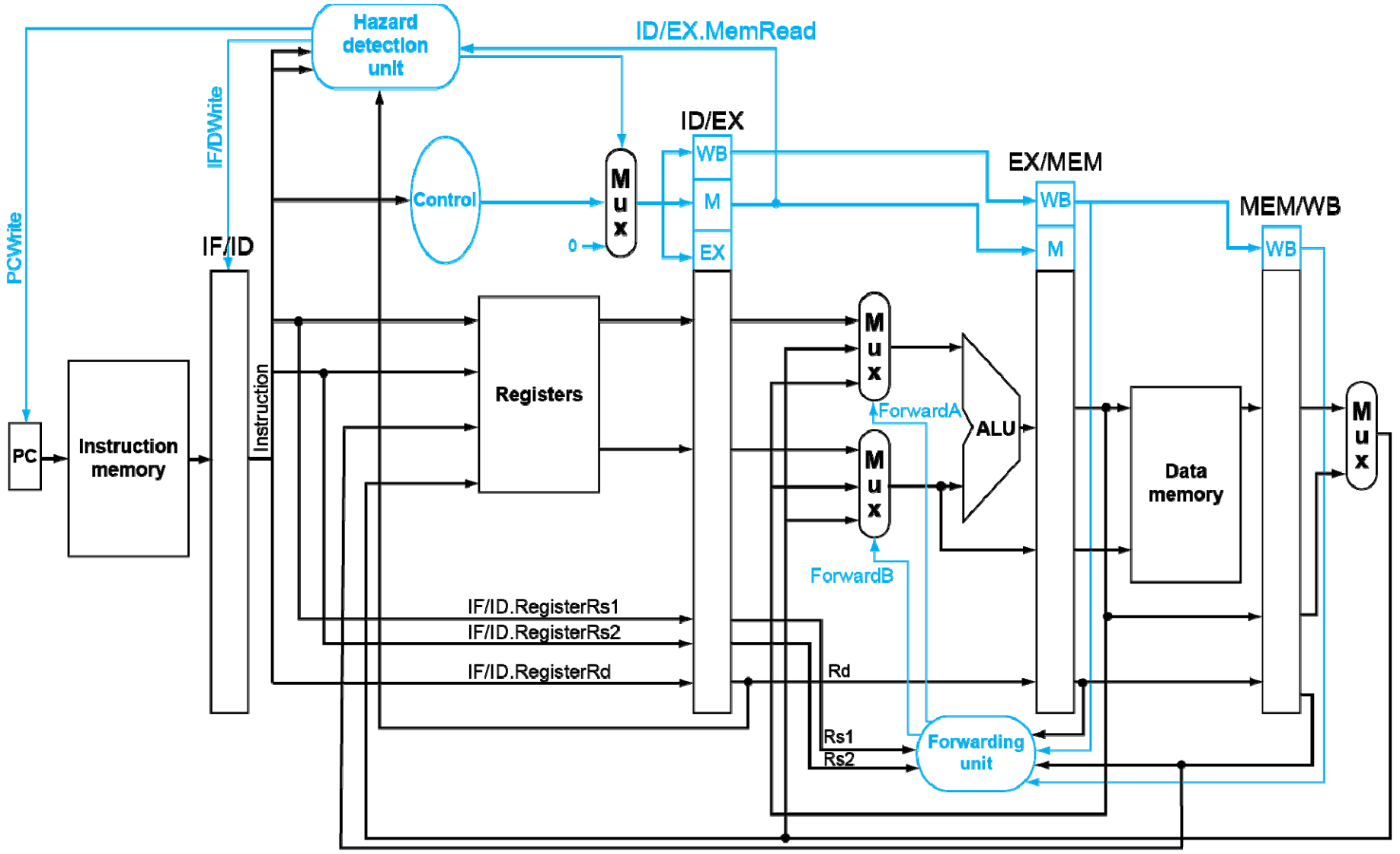
sub **<u>x2</u>, x1,x3**
and **<u>x2</u>**,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



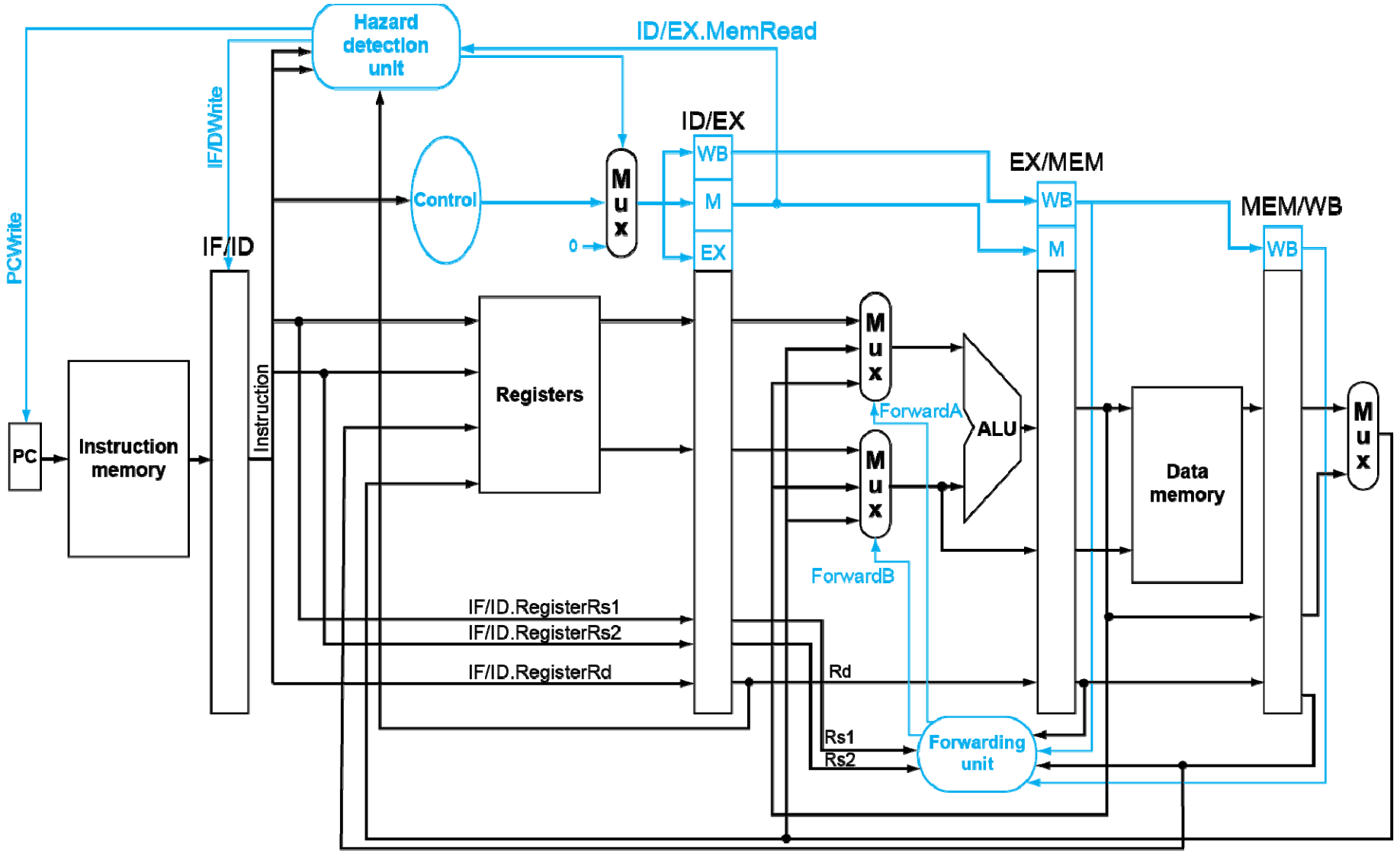
sub **<u>x2</u>, x1,x3**
and **<u>x2</u>**,x2,x5
or x13,x6,x2
add x14,x2,x2
sw x15,100(x2)



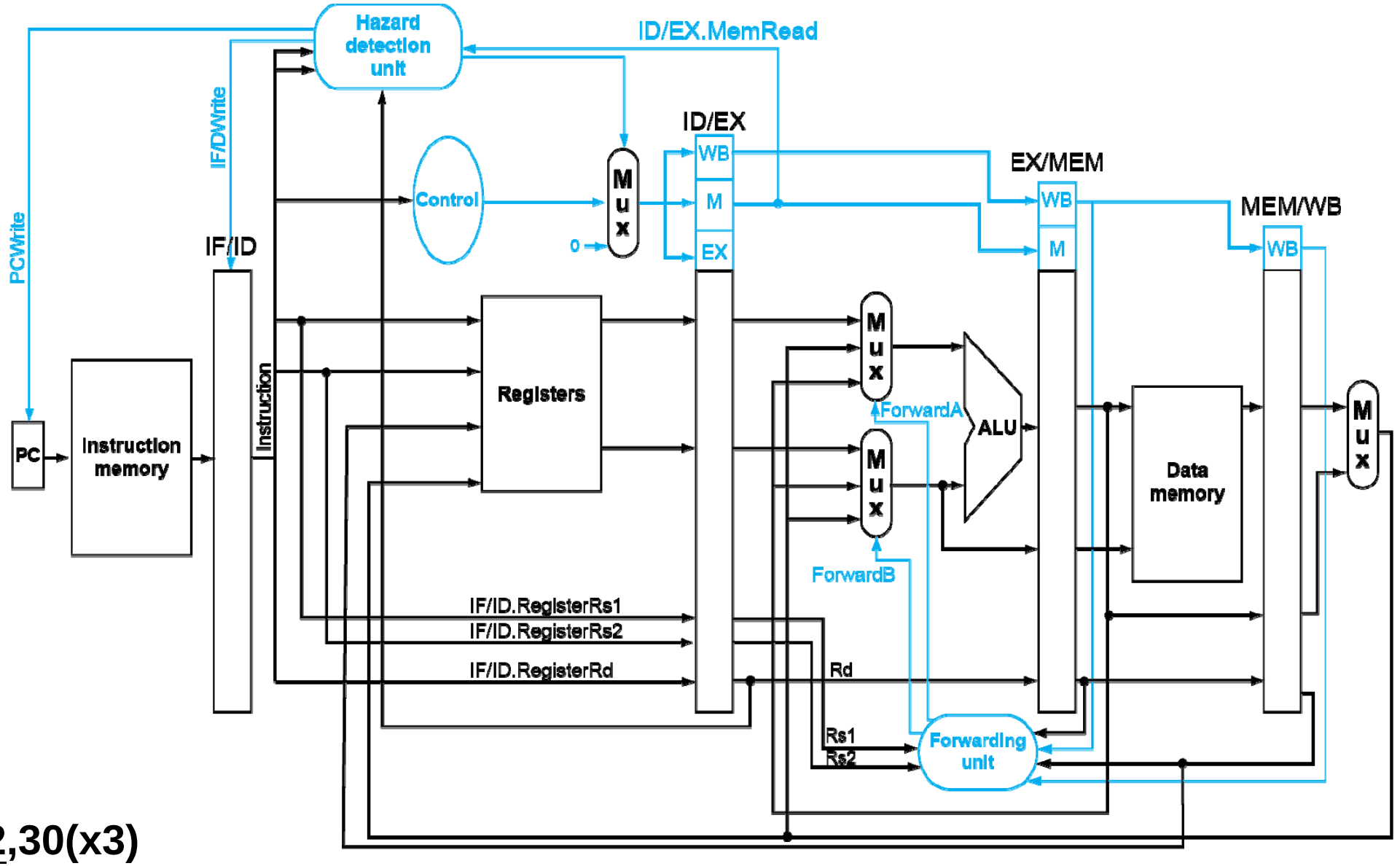
lw **x2,30(x3)**
and x4,x2,x5
or x13,x6,x4
add x14,x8,x9



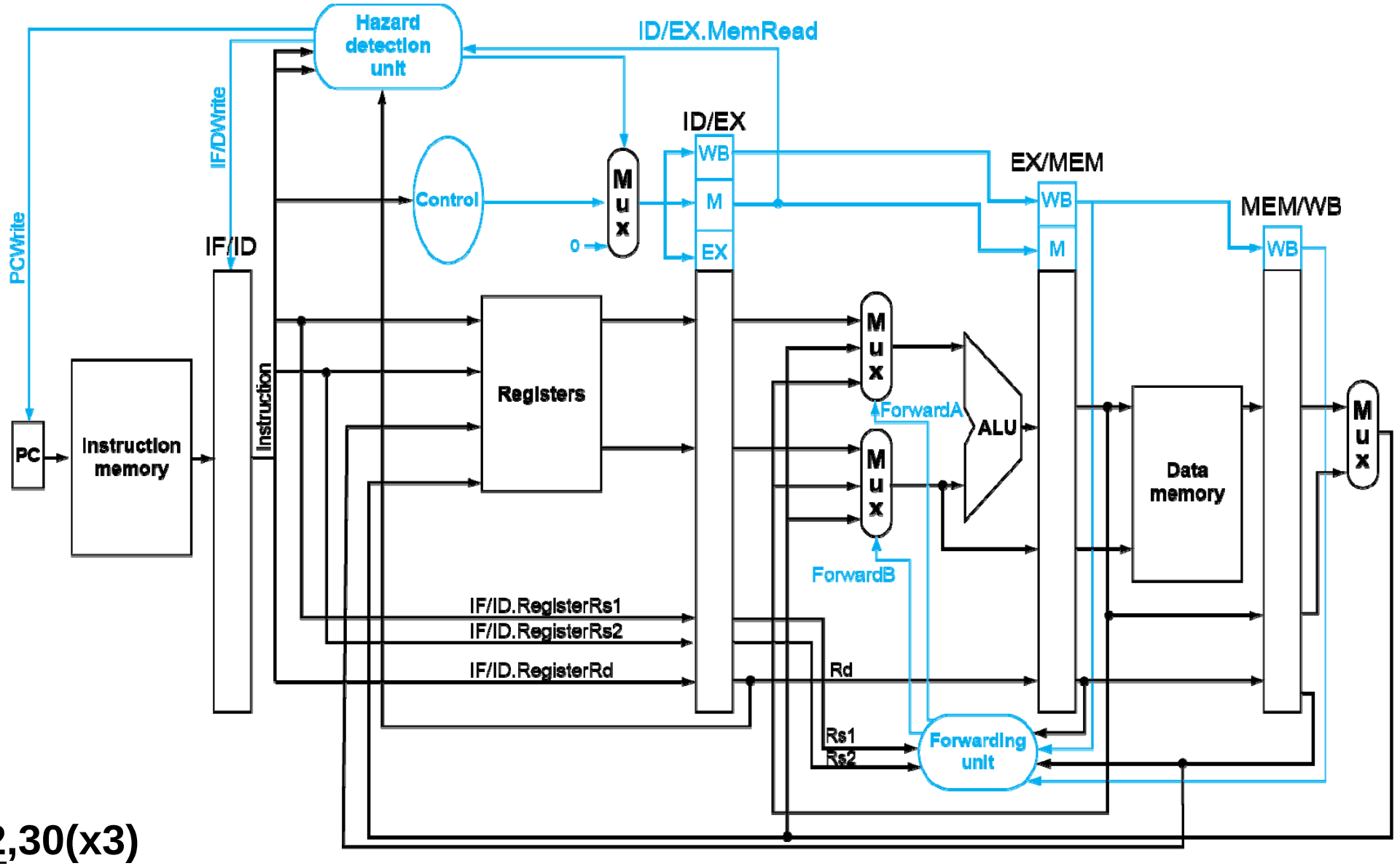
lw **x2,30(x3)**
and x4,x2,x5
or x13,x6,x4
add x14,x8,x9



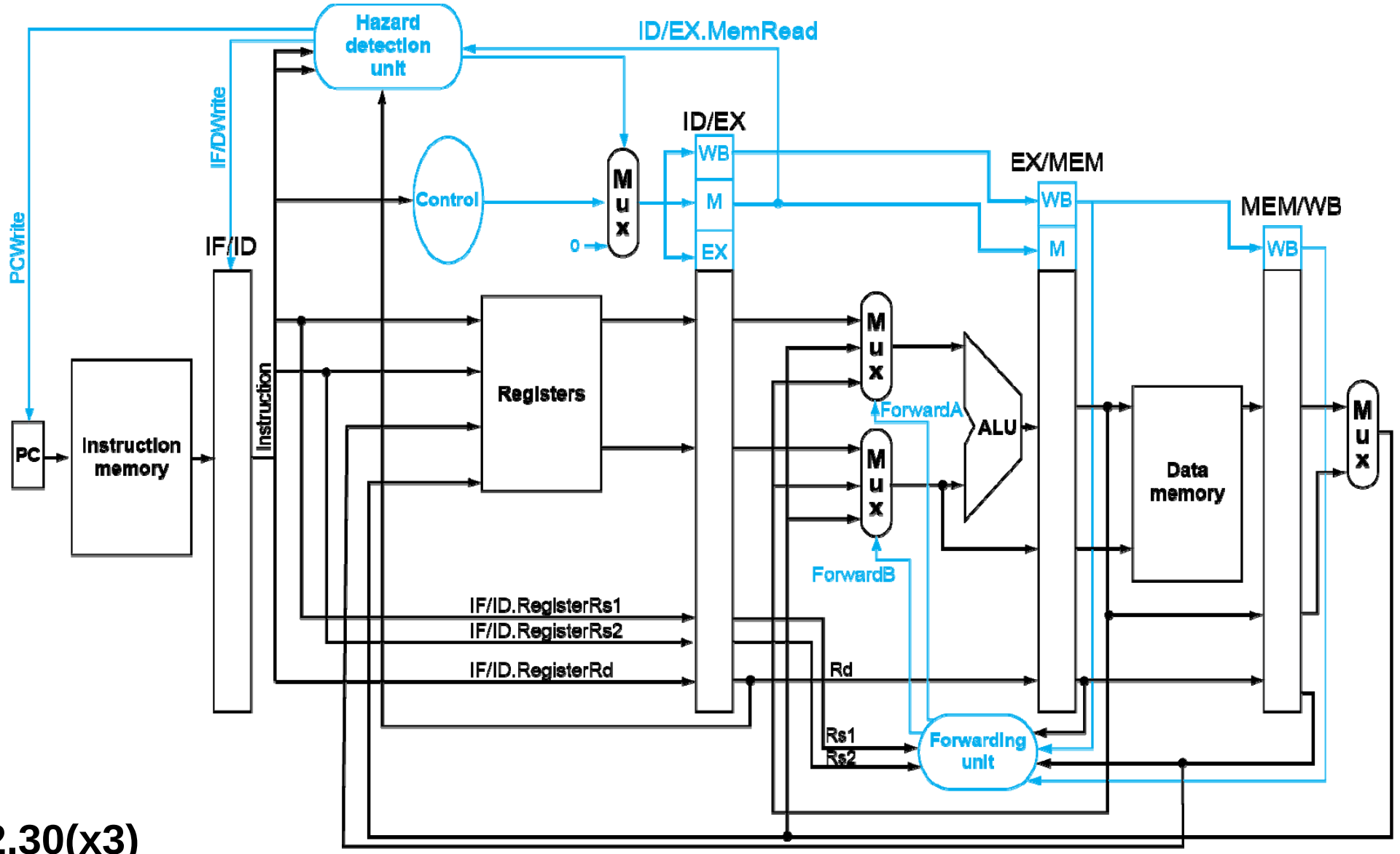
lw **x2,30(x3)**
and x4,x2,x5
or x13,x6,x4
add x14,x8,x9



lw **x2,30(x3)**
and **x2**,x2,x5
or x13,x6,x2
add x14,x8,x9



lw **x2,30(x3)**
and **x2**,x2,x5
or x13,x6,x2
add x14,x8,x9



lw **x2,30(x3)**
and **x2**,x2,x5
or x13,x6,x2
add x14,x8,x9