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|  | 1.  我們會優先使用Ex Forwarding，因為他的值一般來說會比Mem還要新，但是如果已經確定Ex不會發生，那就要取用Mem的值  2.  sub.rd = 2(Mem/WB.rd), sub.rs2 = 3 (Mem/WB.rs2), and.rd = 3(Ex/Mem.rd), or.rs1(ID/Ex.rs1) = 6, or.rs2(ID/Ex.rs2) = 2  故Ex/Mem.rd != ID/Ex.rs1，於是forwarding Mem/Wb回去 |
|  | When the hazard detection is true, it will set PC.write, IF/ID.Write, and MUX after the instruction control.  It means PC will not be updated, and so does IF/ID, and other stage will continue jumping to next stage.  All in all, there will be a stall between ID and Mem, and therefore it will be detected a data hazard between WB and EX. |
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|  | 1.  優點：Reduce compulsory misses due to spatial locality.  缺點：Larger block takes longer to move, so higher penalty for miss.  More conflicts now though, because there are fewer blocks in the cache, so more memory blocks map to the same cache blocks.  2.  64K 因為byte數比較多,所以改block size 相對4K來說比例較小所以4K會比較sensitive |
|  | 1.spatial locality  2. Least recently use  3. LRU才會有這個狀況  4. 加法器一起要比較的項目變多了 |
|  | 1. L1 is nearest by cpu, so it could make influence on cpu. Therfore, we always make L1 small to decrease access time.  2. The size of L1 and L2 are 2\*32, 2 represents that it has 2 core work simultaneosly. And L3 is shared with all cores.  3. L1 is a split cache and L2 is a unified cache. |
|  | 1. send to multiple banks and read data at the same time. Increase bandwidth  2.把memory部分，可以同時，也節省空間  3. 1+15+1=17cycles；1+15+4\*1=20cycles |