Name: Muhammad Waleed Akram **EE-272L Digital Systems Design**

Reg. No.: 2023-EE-165(B) Marks Obtained: _____

Lab Manual

Experiment No. 2

Combinational Circuits: Structural Modelling using Vivado

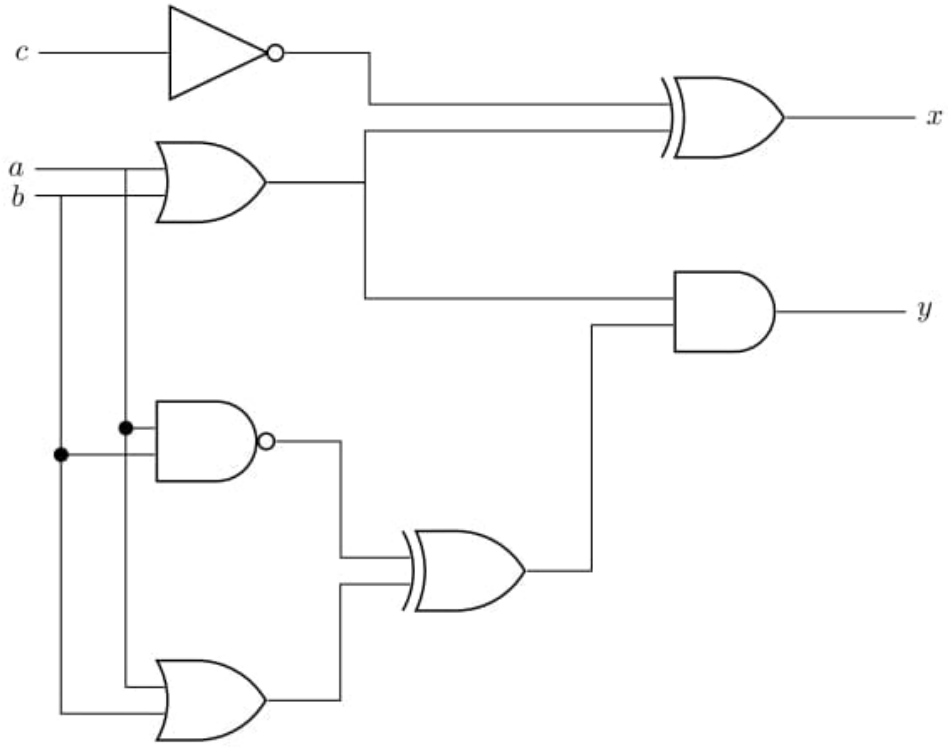
DSD Lab Manual Evaluation Rubrics

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization (CLO1)	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation (CLO2)	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms

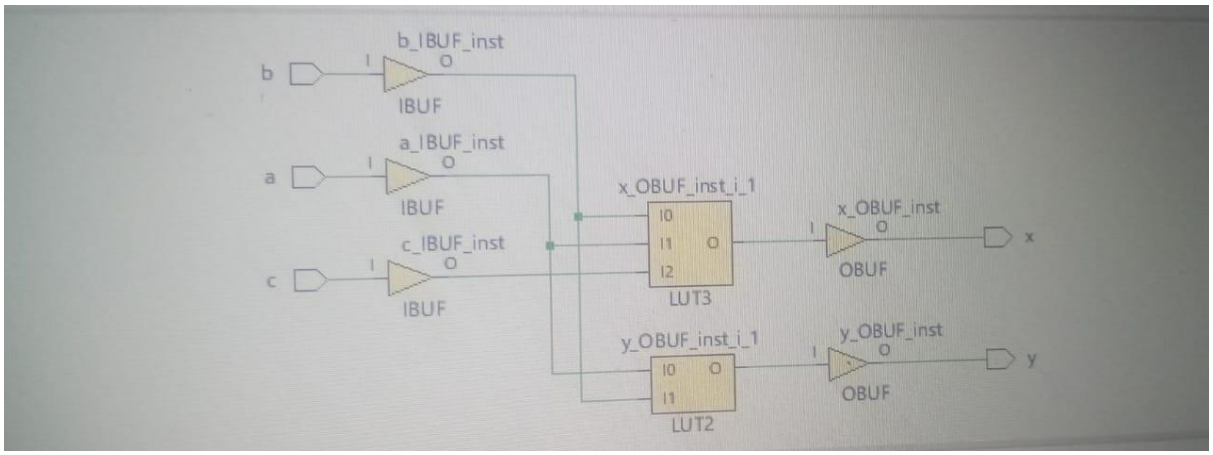
FPGA (CLO2)	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

Experiment # 02

Schematic Diagram:



Implemented Circuit:



TASK 1(A)

Truth Table of the above circuit is shown as follows:

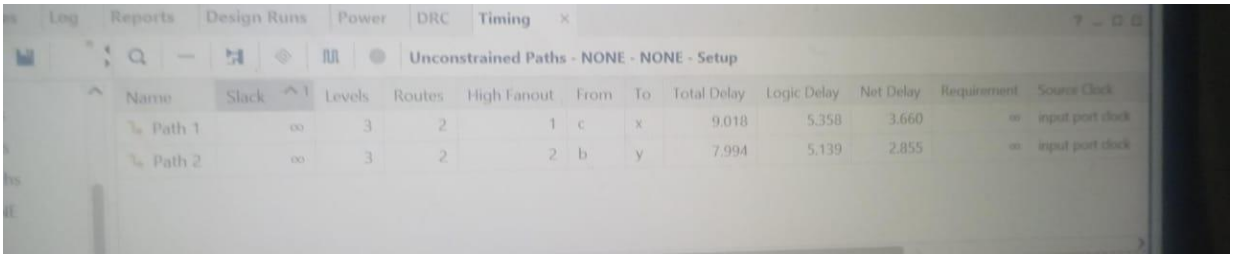
a	b	c	c`	a + b	(a.b)`	z = (a.b)` ⊕ (a + b)	x = c` ⊕ (a + b)	y = z .(a + b)
0	0	0	1	0	1	1	1	0
0	0	1	0	0	1	1	0	0
0	1	0	1	1	1	0	0	0
0	1	1	0	1	1	0	1	0
1	0	0	1	1	1	0	0	0
1	0	1	0	1	1	0	1	0
1	1	0	1	1	0	1	0	1
1	1	1	0	1	0	1	1	1

(A) Truth table for output x and y

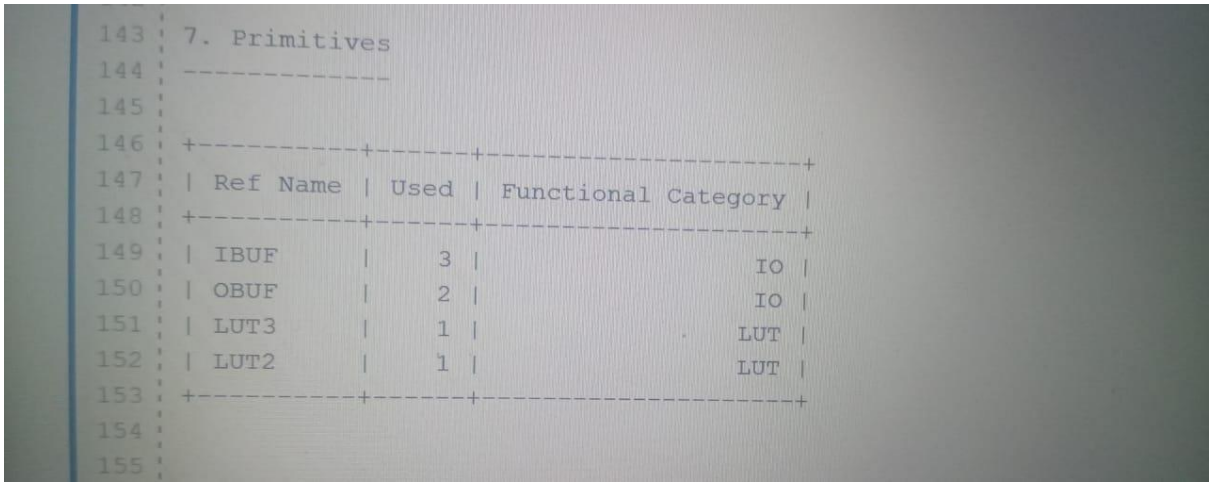
TASK 1(B)

Max combinational delay = 3.66

Min combinational delay = 2.855



TASK 1(C)



SYSTEM VERILOG CODE

```
1
2     module design_file(
3         input a,
4         input b,
5         input c,
6         output x,
7         output y
8         );
9         assign or_out = a | b;
10        assign x = (~c) ^ or_out;
11        assign xor_out = (~(a & b)) ^ (or_out);
12        assign y = or_out & xor_out;
13    endmodule
```