

CMP201

Microprocessors Systems

Lab 1 – Circuit Design using
Intel Quartus Prime

1- Setup & Run Quartus

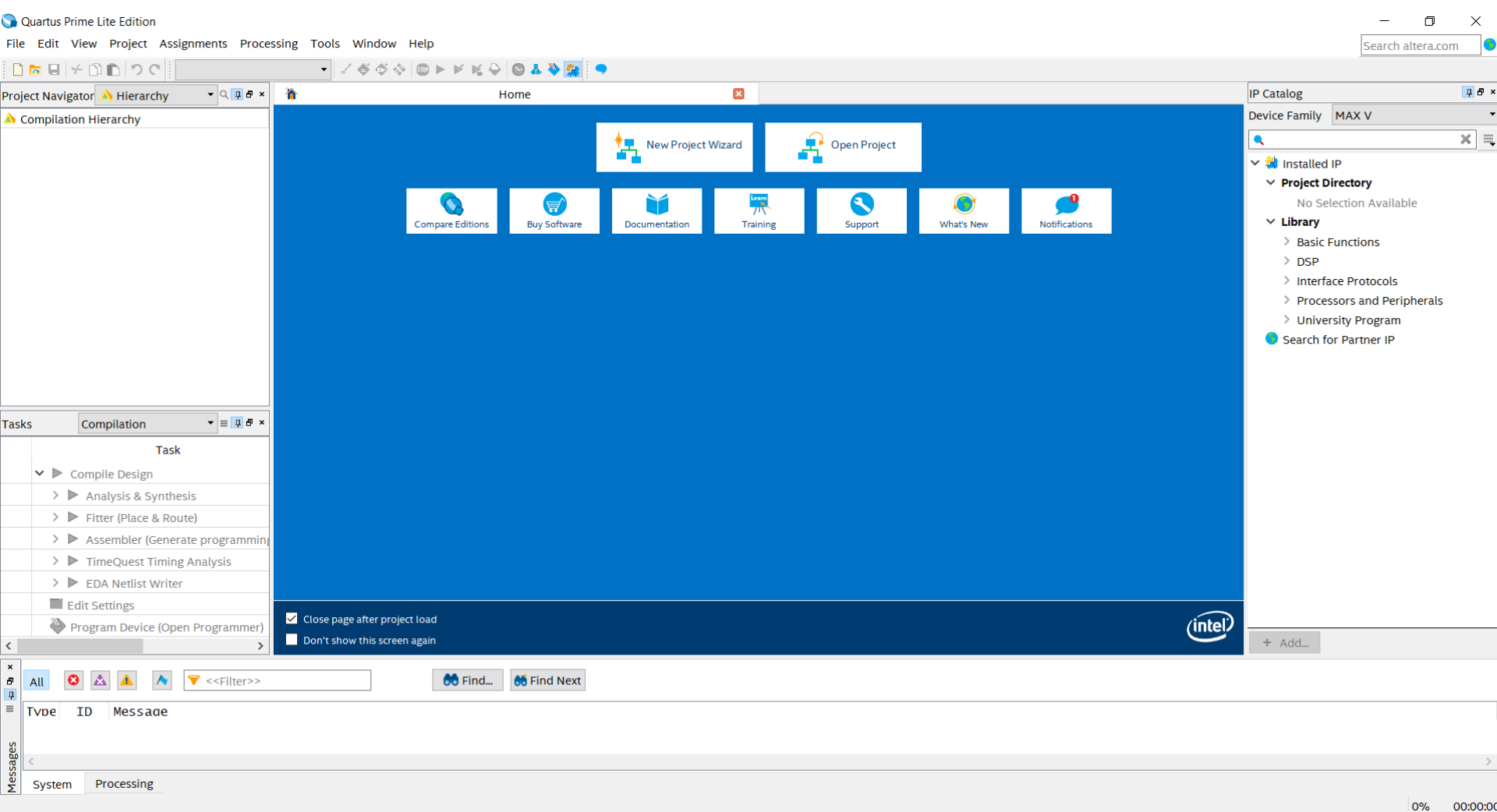
- When You download (or copy) the setup file, Get 3 files:
 - Quartus Prime Lite
 - Modelsim Altera Starter edition
 - Max V
- Put all 3 setup files in one folder and run Quartus setup file

1- Setup & Run Quartus

- Quartus Prim (Lite / Web edition)
 - No need for Lic
 - Next, Next, Next, ...
- Run Quatrus Prim icon on the desktop or from the start window

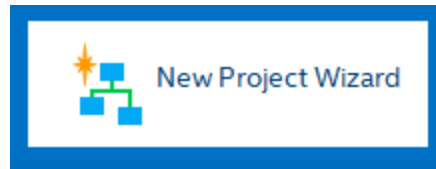


1- Setup & Run Quartus

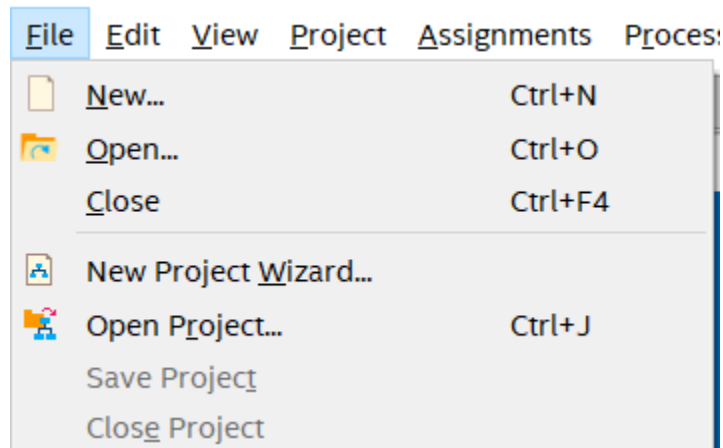


2- New Project

- Click on

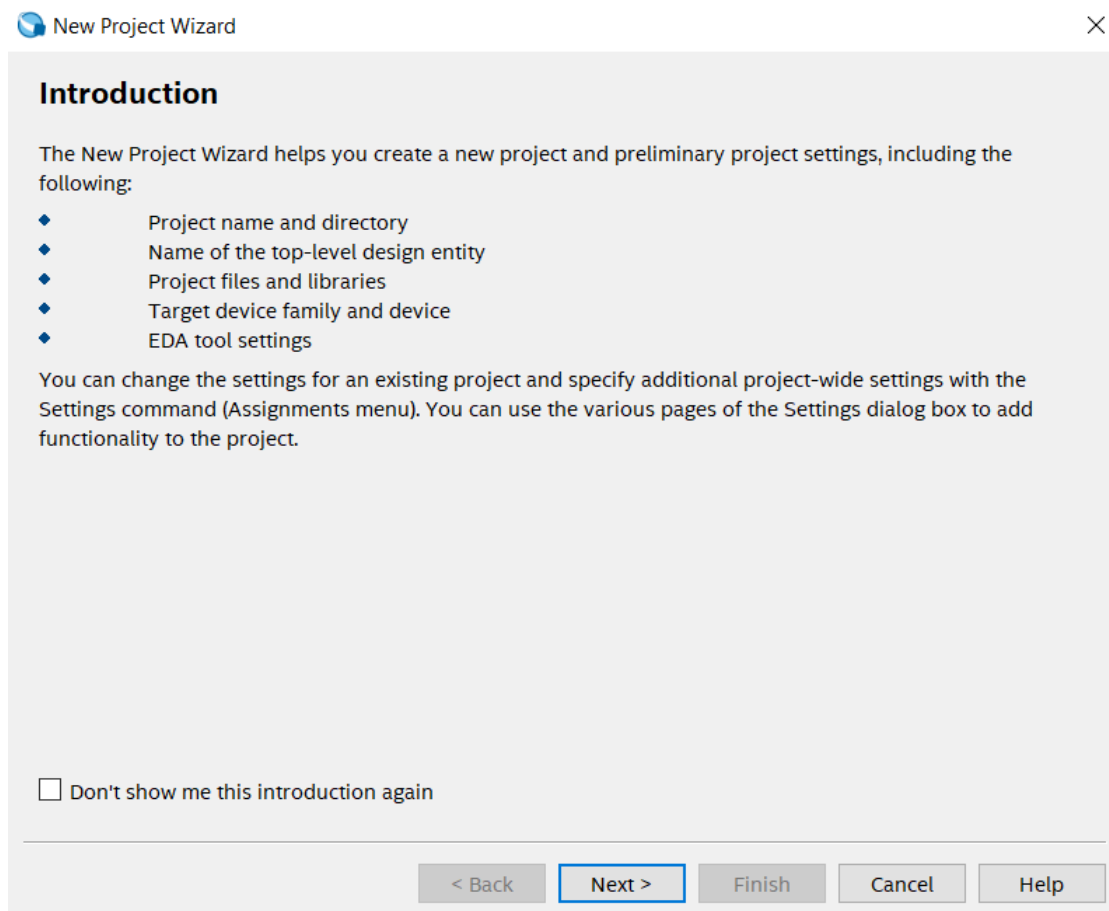


- Or “File” then “New Project Wizard”



2- New Project

- Click Next



2- New Project

- Enter Your Project Directory & Name

New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

C:\intelFPGA_lite\16.1

What is the name of this project?

Test

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

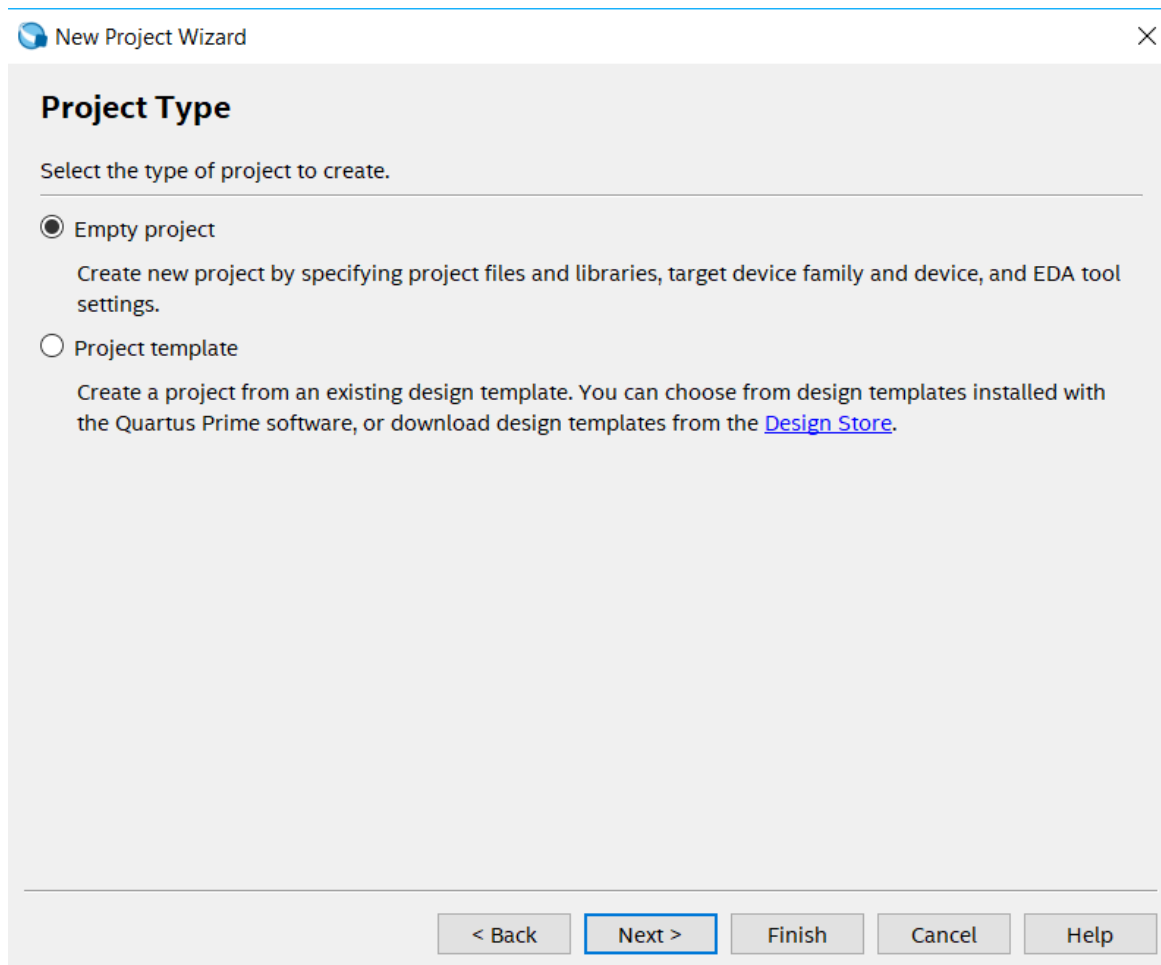
Test

Use Existing Project Settings...

< Back Next > Finish Cancel Help

2- New Project

- Select Empty Project & Click Finish



The screenshot shows the 'New Project Wizard' dialog box. The title bar reads 'New Project Wizard' with a close button. The main area is titled 'Project Type' and contains the instruction 'Select the type of project to create.' There are two radio button options: 'Empty project' (selected) and 'Project template'. The 'Empty project' option has a description: 'Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.' The 'Project template' option has a description: 'Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).' At the bottom, there are five buttons: '< Back', 'Next >' (highlighted with a blue border), 'Finish', 'Cancel', and 'Help'.

New Project Wizard

Project Type

Select the type of project to create.

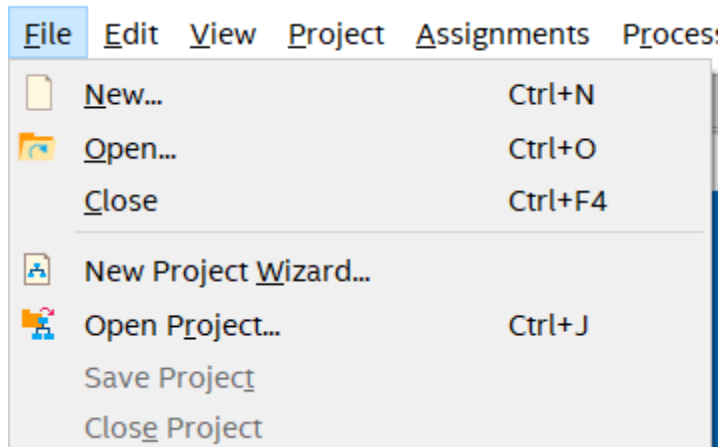
☒ Empty project
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

☐ Project template
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).

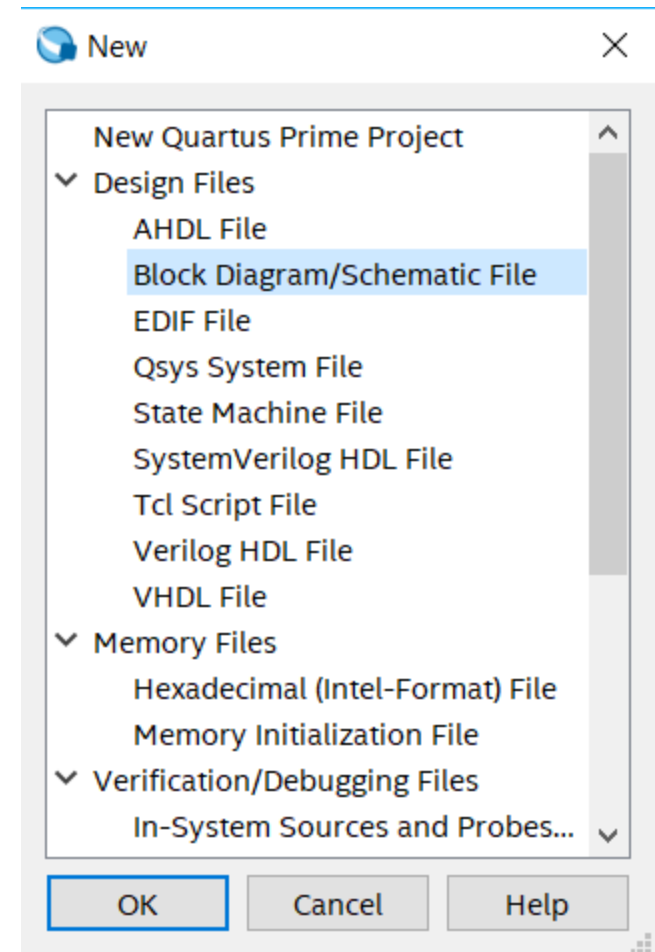
< Back Next > Finish Cancel Help

3- New Schematic File

- Click on “File” then “New”

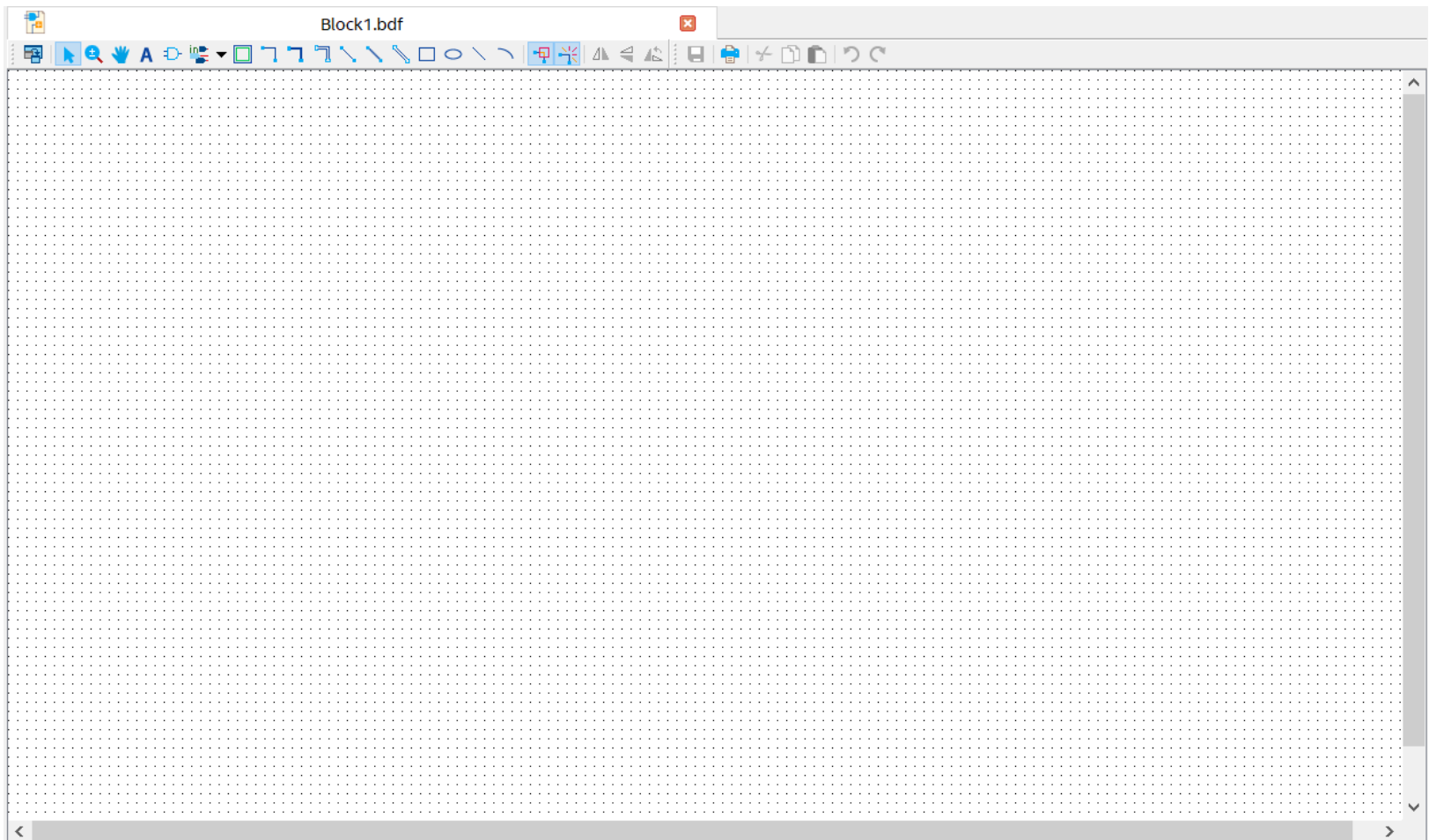


- Create a new
“Block Diagram/Schematic File”



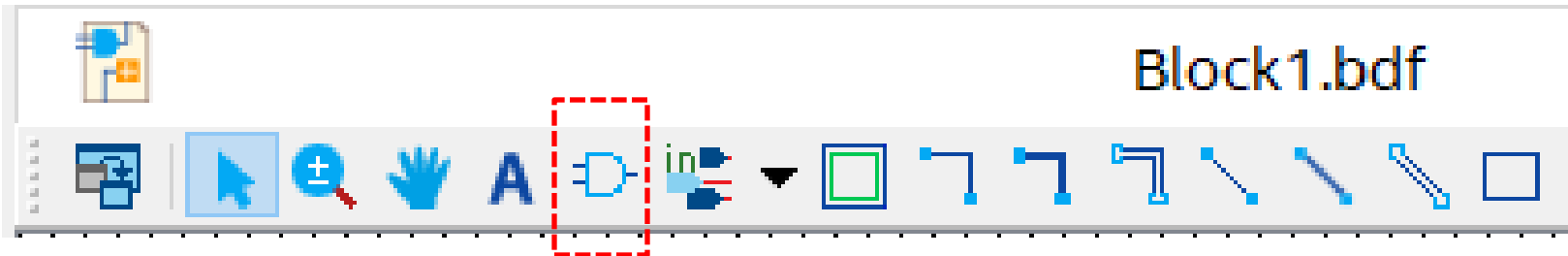
3- New Schematic File

- The new window is our schematic workspace



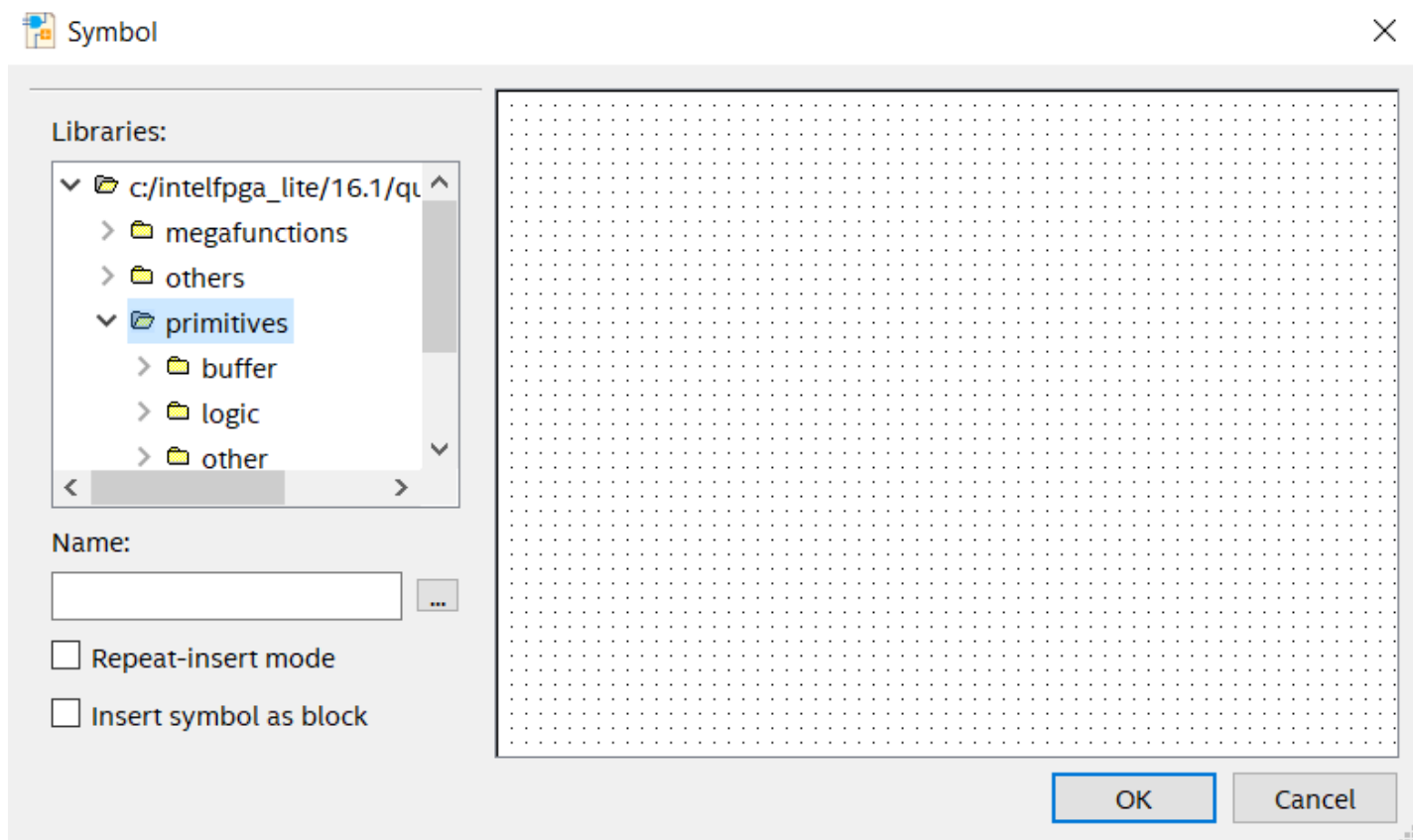
4- Add Gates

- Add a gate by double click in any place in the workspace
- Or by clicking on “Symbol Tool” icon



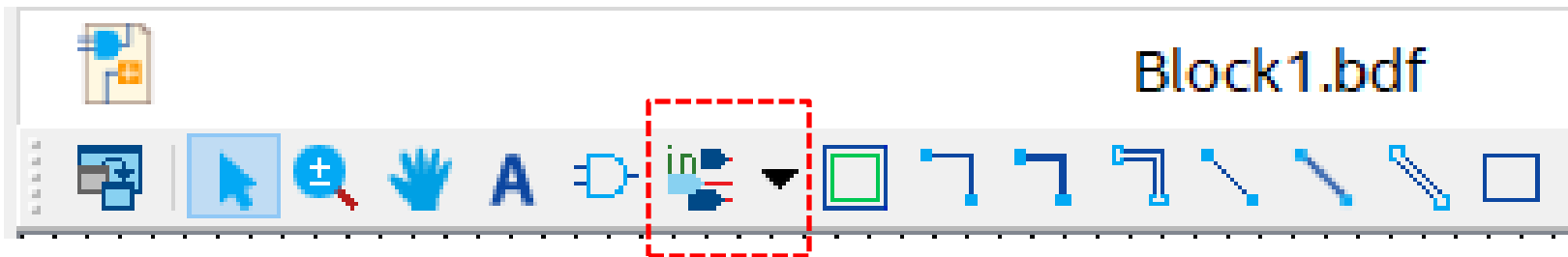
4- Add Gates

- Write the Gate Name (ex: and2)
- Or select it from “primitives” library



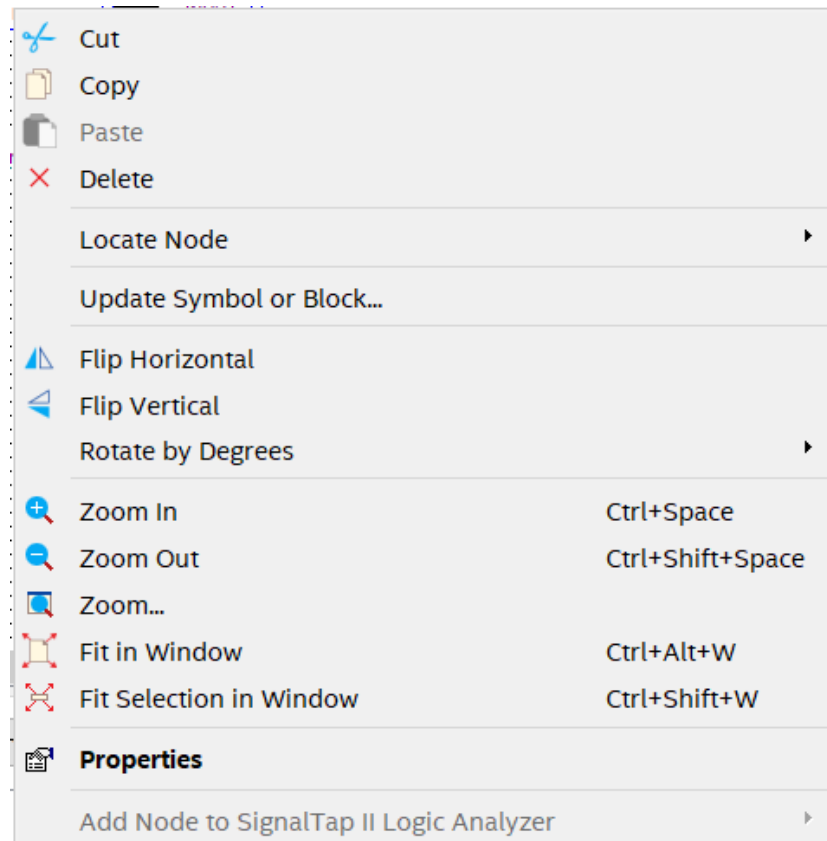
4- Add Gates

- Add a IO pin by selecting it from Toolbox



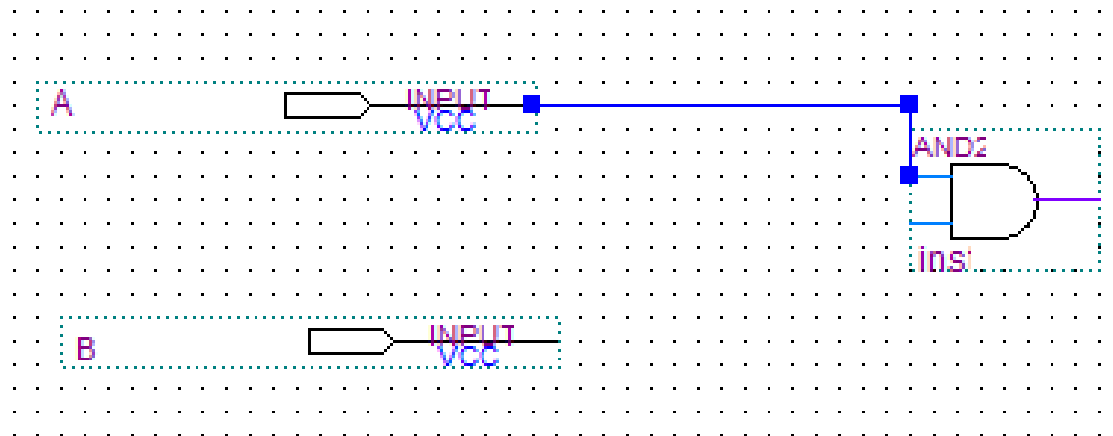
4- Add Gates

- Change an input/output pin name by double click on its label or right click then “Properties”



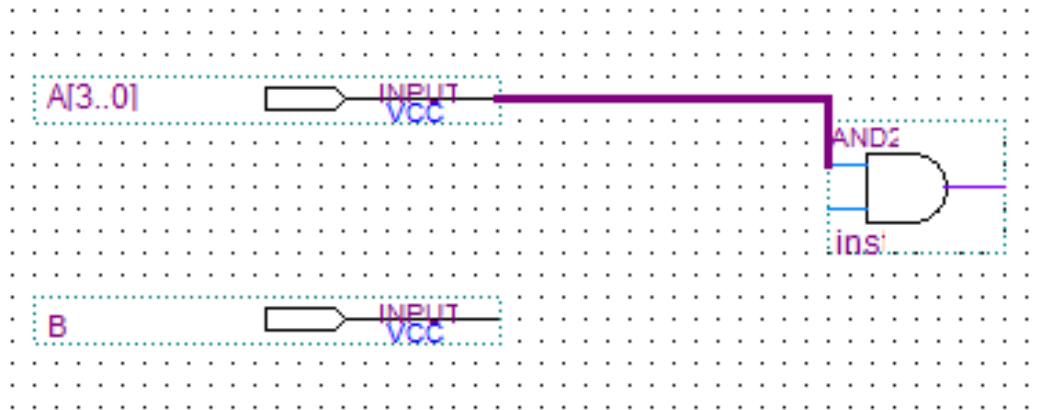
5- Add Connections/Wires

- Connect 2 pins by putting the mouse on the edge of the gate then drag to the other pin
- Or write the wire name on the 2 pins

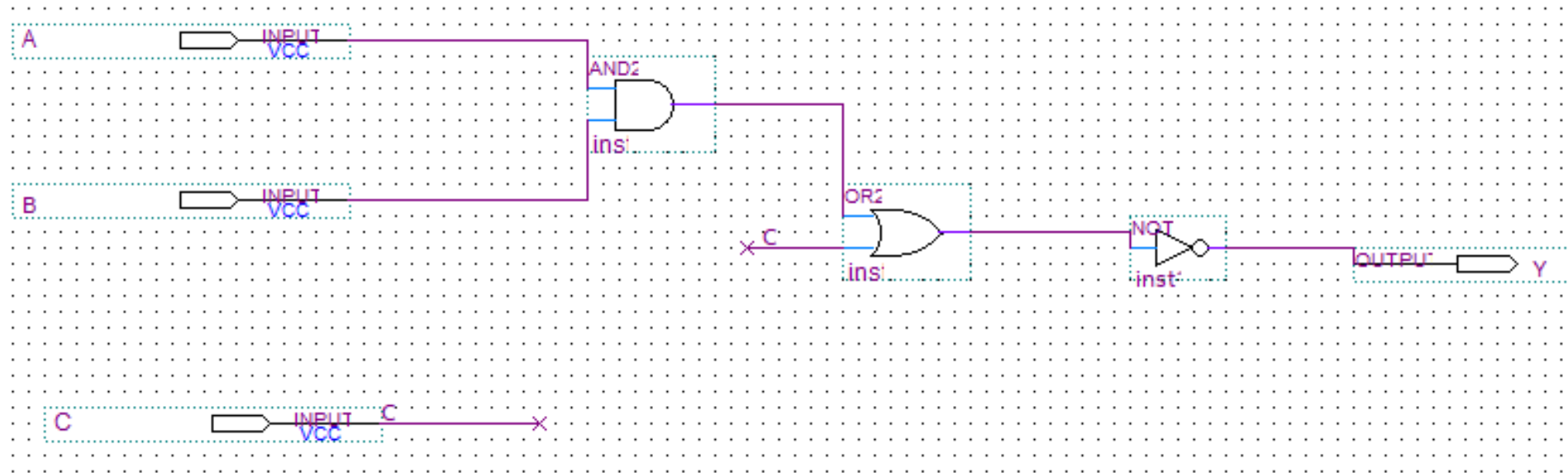


5- Add Connections/Wires

- You can define a connection as a bus instead of a 1-bit wire
- Name the input as “Bus_name[Start_bit..End_bit]”
 - For Example “A[0..3]” will create a 4-bit bus named “A”

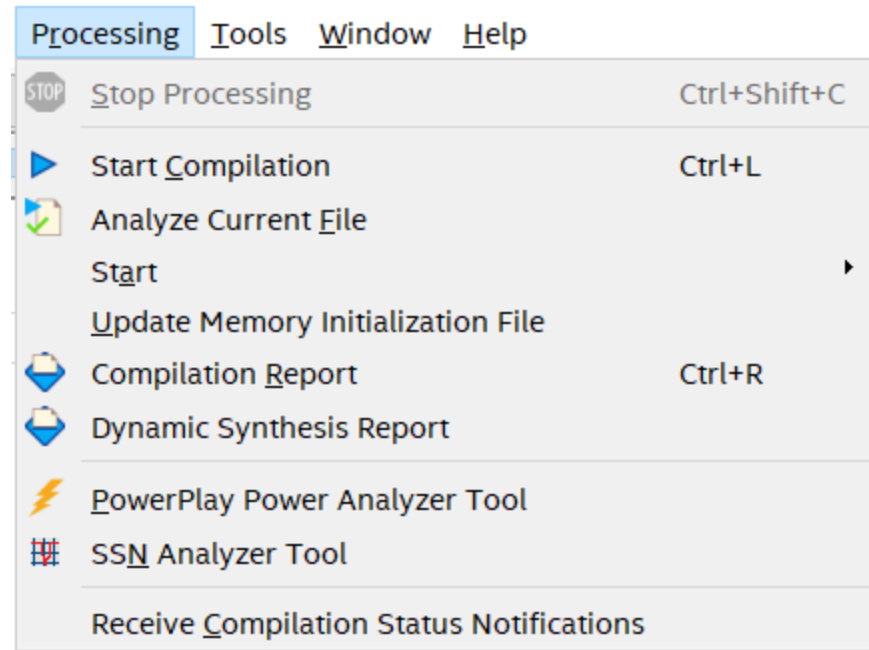


6- Draw the Circuit



7- Compile the Circuit

- Save the schematic file
- Compile the circuit by clicking on “Processing” then “Start Compilation”



7- Compile the Circuit

Quartus Prime Lite Edition - C:/intelFPGA_lite/16.1/Test - Test

File Edit View Project Assignments Processing Tools Window Help

Test

Project Navigator Hierarchy Test.Bdf Compilation Report - Test IP Catalog

EntityInstance

MAX V: AUTO

Test

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Sat Sep 22 18:36:17 2018
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	Test
Top-level Entity Name	Test
Family	MAX V
Total logic elements	1 / 40 (3 %)
Total pins	4 / 30 (13 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)
Device	5M40ZM64C4
Timing Models	Final

Tasks

Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate programming)
 - TimeQuest Timing Analysis
 - EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Messages

All

<<Filter>>

Find... Find Next

Type	ID	Message
Warning	332102	Design is not fully constrained for hold requirements
Information		Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 3 warnings
Information	293000	Quartus Prime Full Compilation was successful. 0 errors, 12 warnings

System Processing (87)

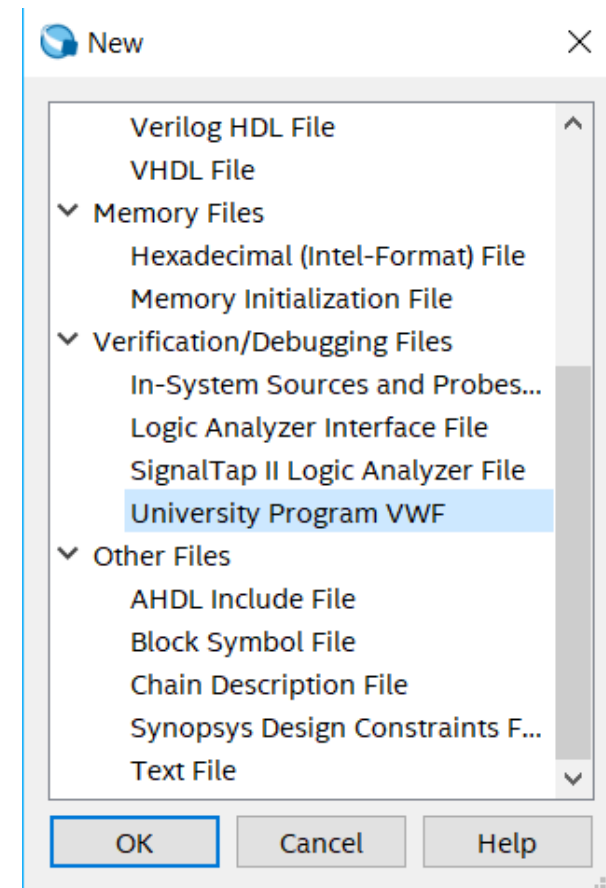
135, 2 100% 00:00:48

7- Compile the Circuit

- It will check the circuit for any:
 - Unconnected Pins
 - Short Circuits
 - Loops
 - Multiple pins/gates with same name

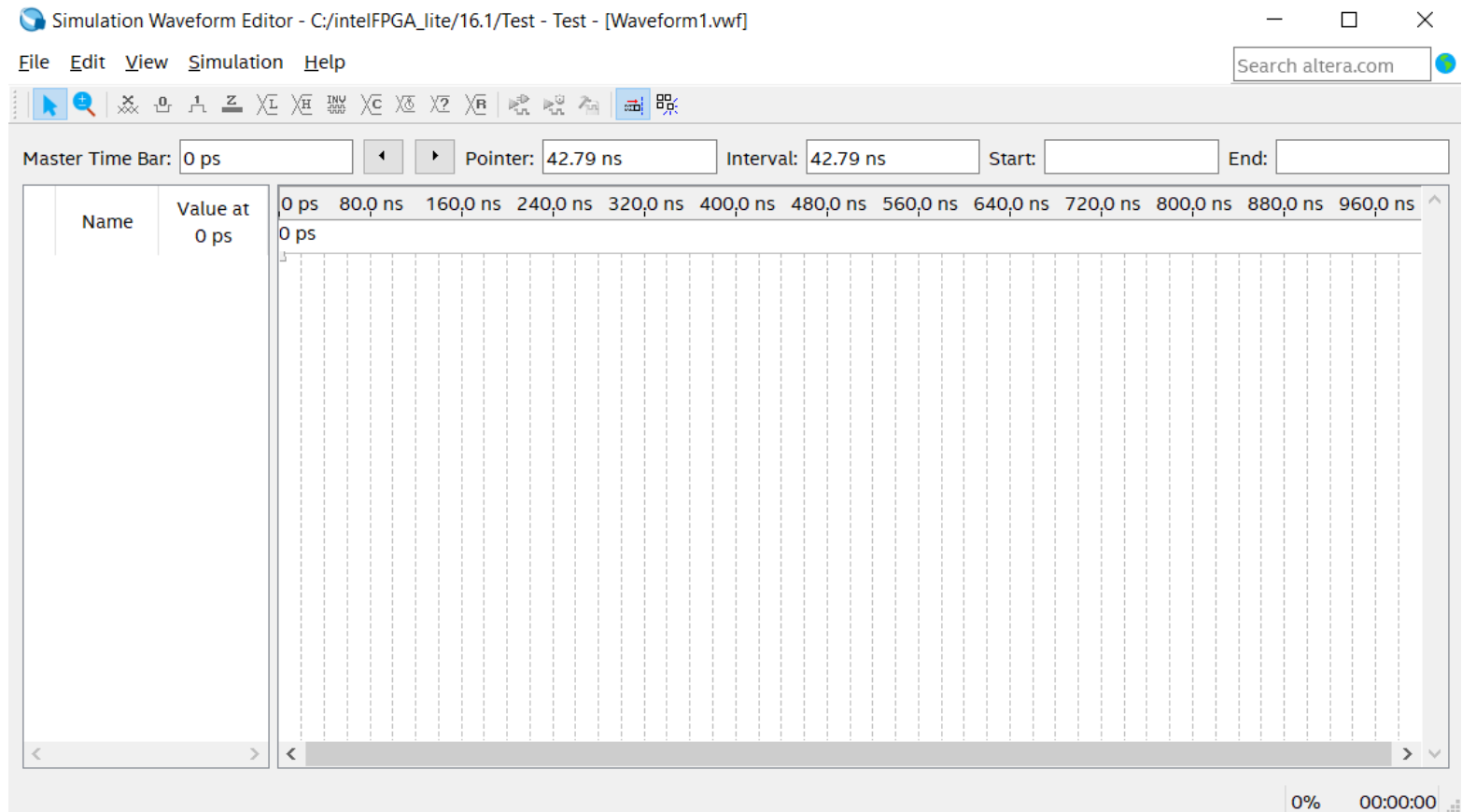
8- Simulate the Circuit

- Create a waveform to test your design
- Select “New” from “File” menu
- Then select
“University Program VWF”



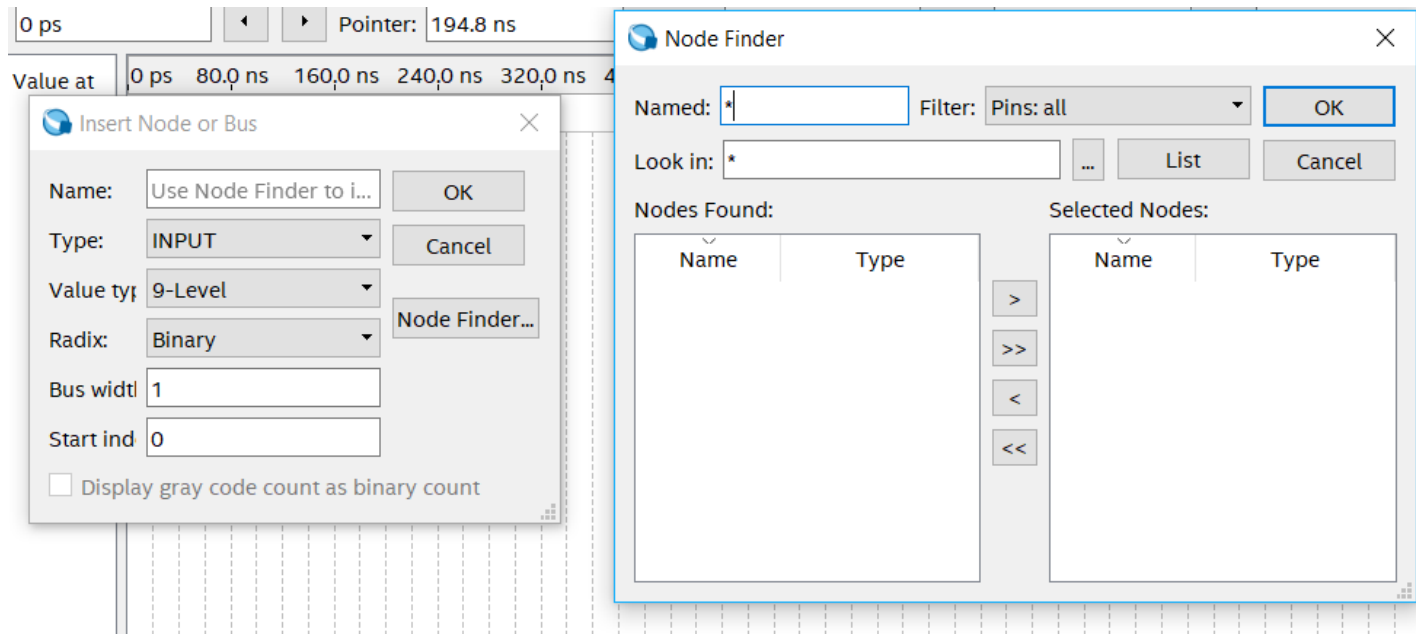
8- Simulate the Circuit

- The new window will be used to create the waveform



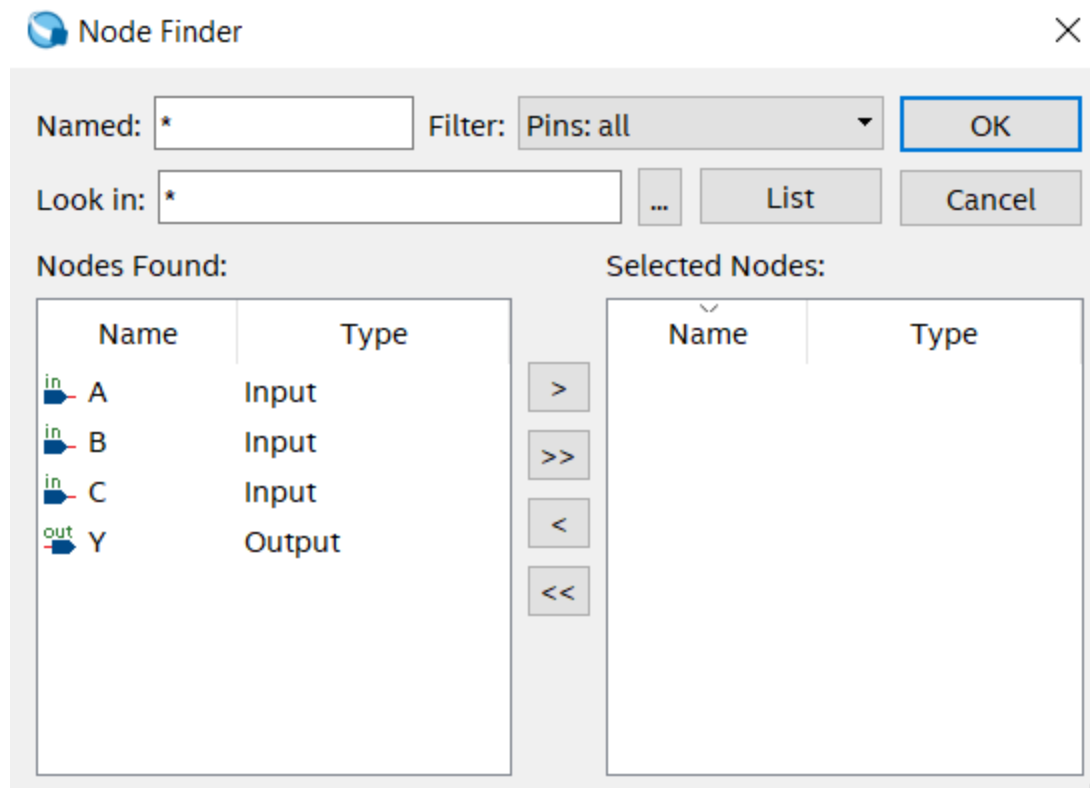
8- Simulate the Circuit

- To add an input/output/wire
 - Double click on a cell in the name column
 - Or right click and select “Insert Node or Bus”



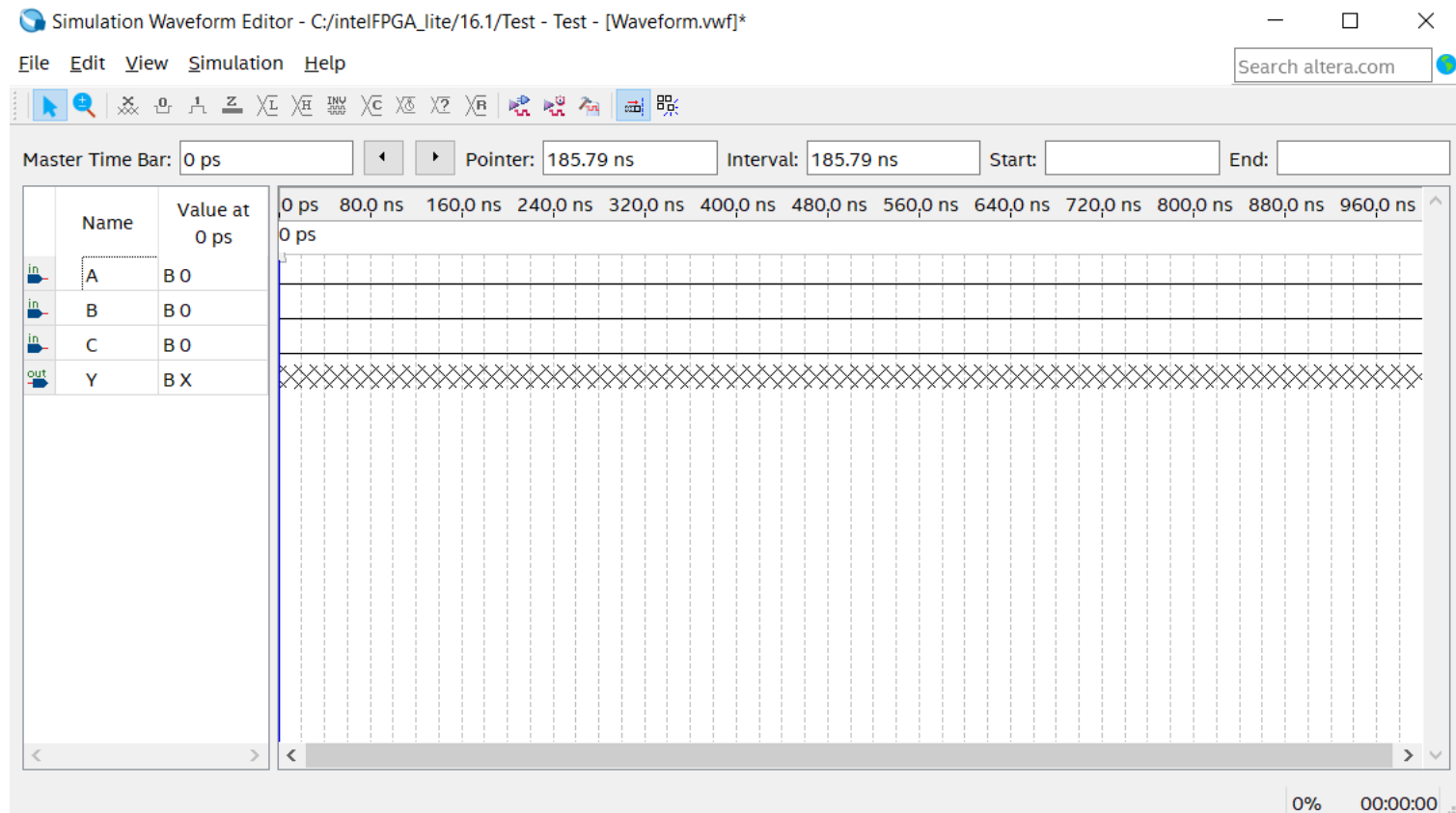
8- Simulate the Circuit

- Write the node name & select its parameters
- Or click “List” to see all the nodes in your design



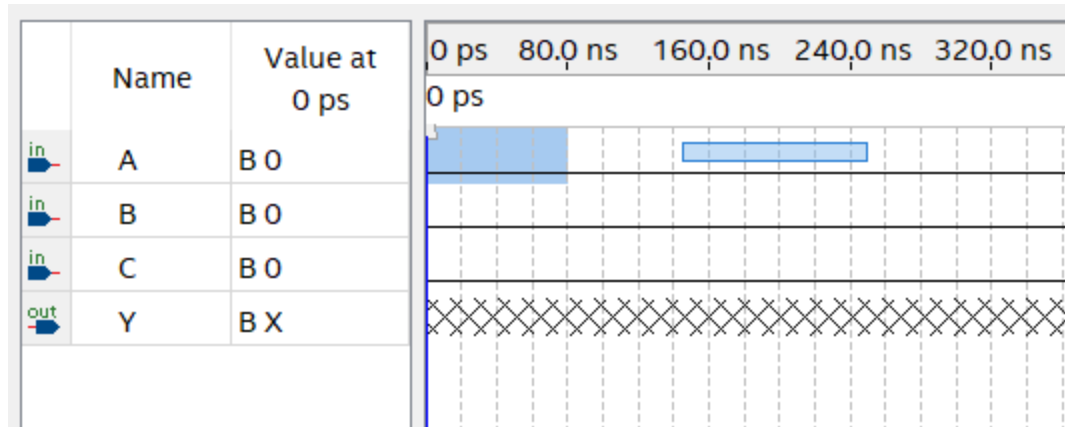
8- Simulate the Circuit

- Add all inputs/outputs you want to observe



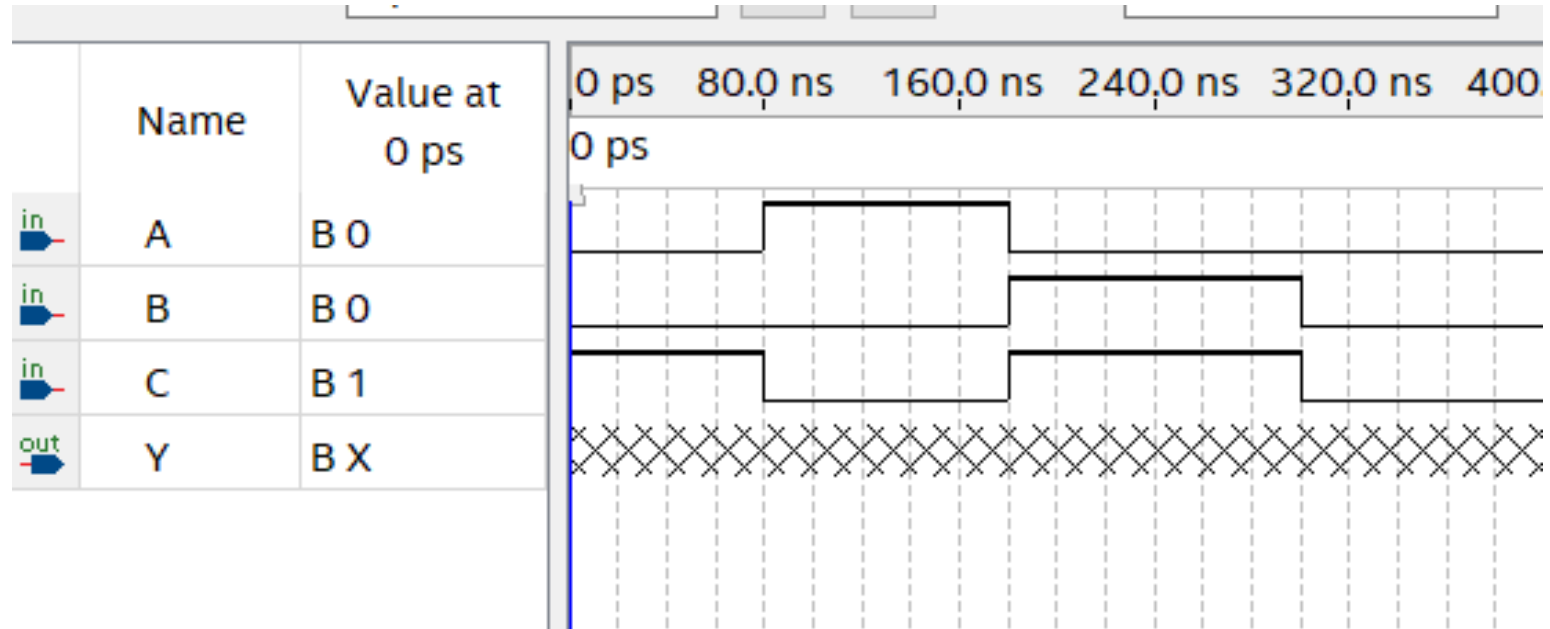
8- Simulate the Circuit

- The waveform is divided into sets of 10ns
- To change the value of a specific part
 - Click on the part you want to change then drag
 - Change the value from the tool bar or by right click



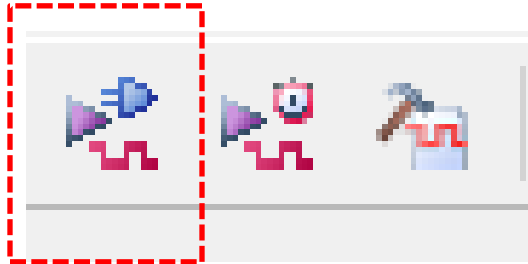
8- Simulate the Circuit

- Set your test scenario



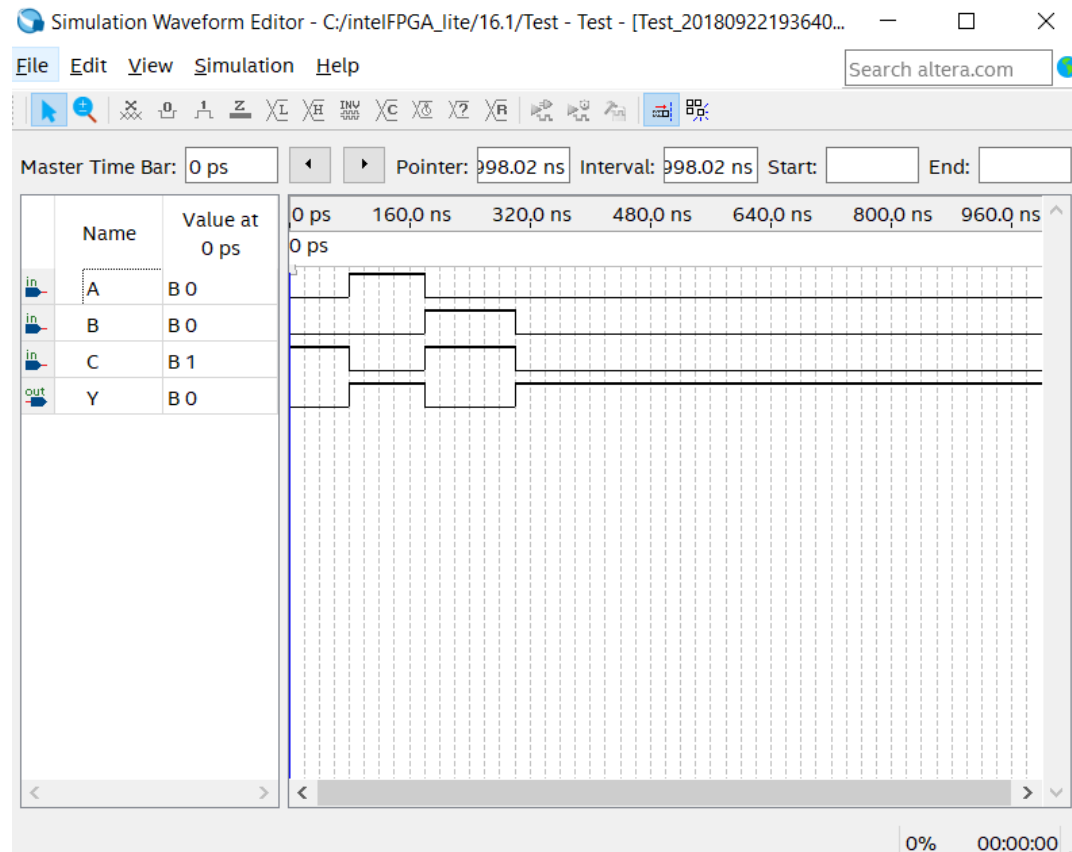
8- Simulate the Circuit

- Run the waveform simulation by clicking on this button from the tool bar



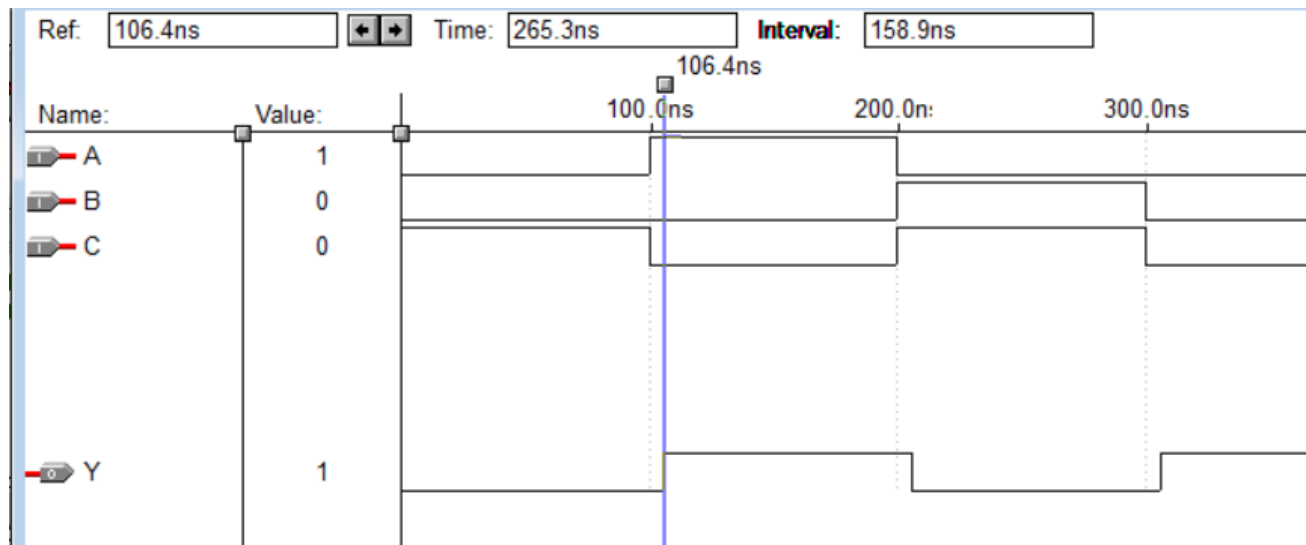
8- Simulate the Circuit

- The output pins values will be changed in the waveform window



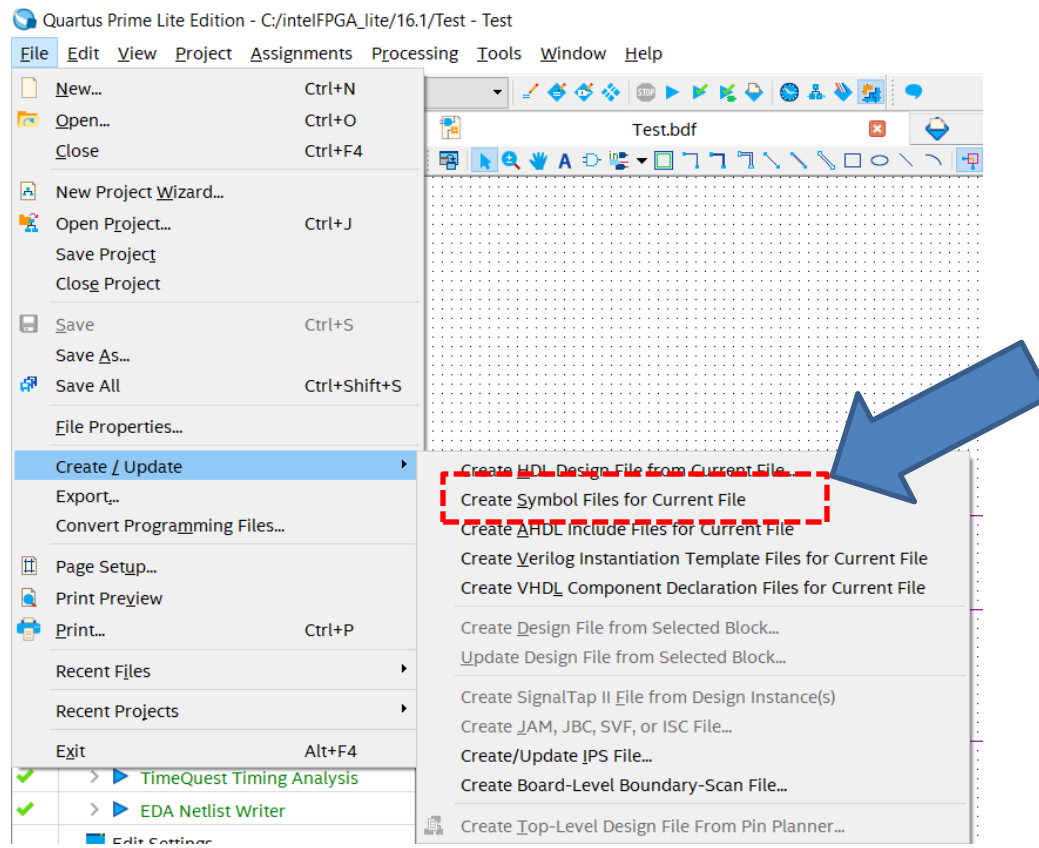
8- Simulate the Circuit

- In Advanced Settings (More Realistic)
- The output do not change instantly, it takes a little delay to see the output

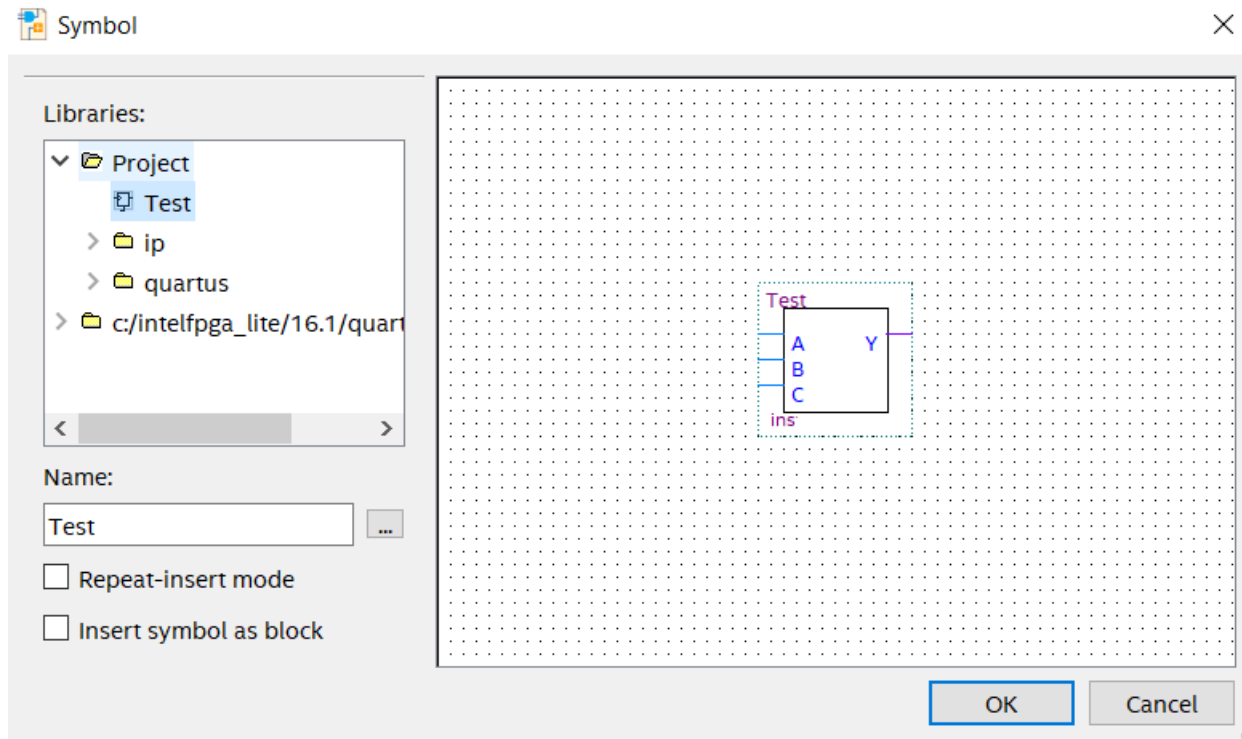


9- Reuse Your Circuit

- To reuse your circuit as a component
- Select “Create Symbol Files from Current File”



9- Reuse Your Circuit



10- Tips

- Do not name a project/file/label as “2” or “7aga” there is no variables that starts with “number”
- Do not add spaces or special characters in your file name or component name
- Save all your files in the same project directory

10- Tips

- Run Quartus as administrator
- Read the Error messages if any appears
- If Simulation is stuck
 - Add “onbreak {resume}” to simulation options