LAB1-MP

8086 and I/O Address Mapping

CMP(N)211

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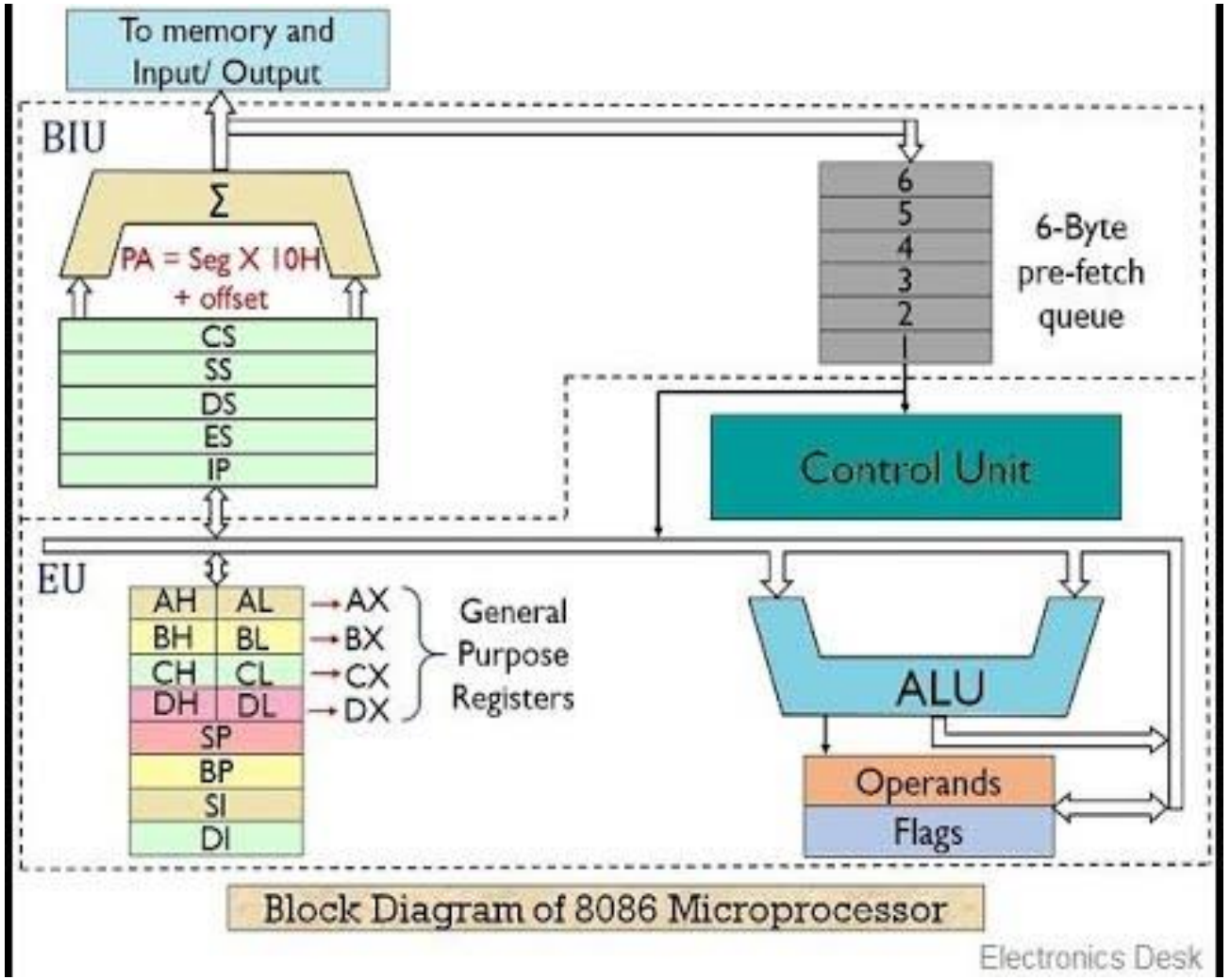
Lab outline

- ✓8086 architecture review
- ✓8086 connectivity
- ✓I/O addressing
  - ✓I/O instruction
  - ✓Address decoding
  - ✓74LS373
  - ✓74LS244
- ✓SimulIDE overview
- ✓Lab requirement

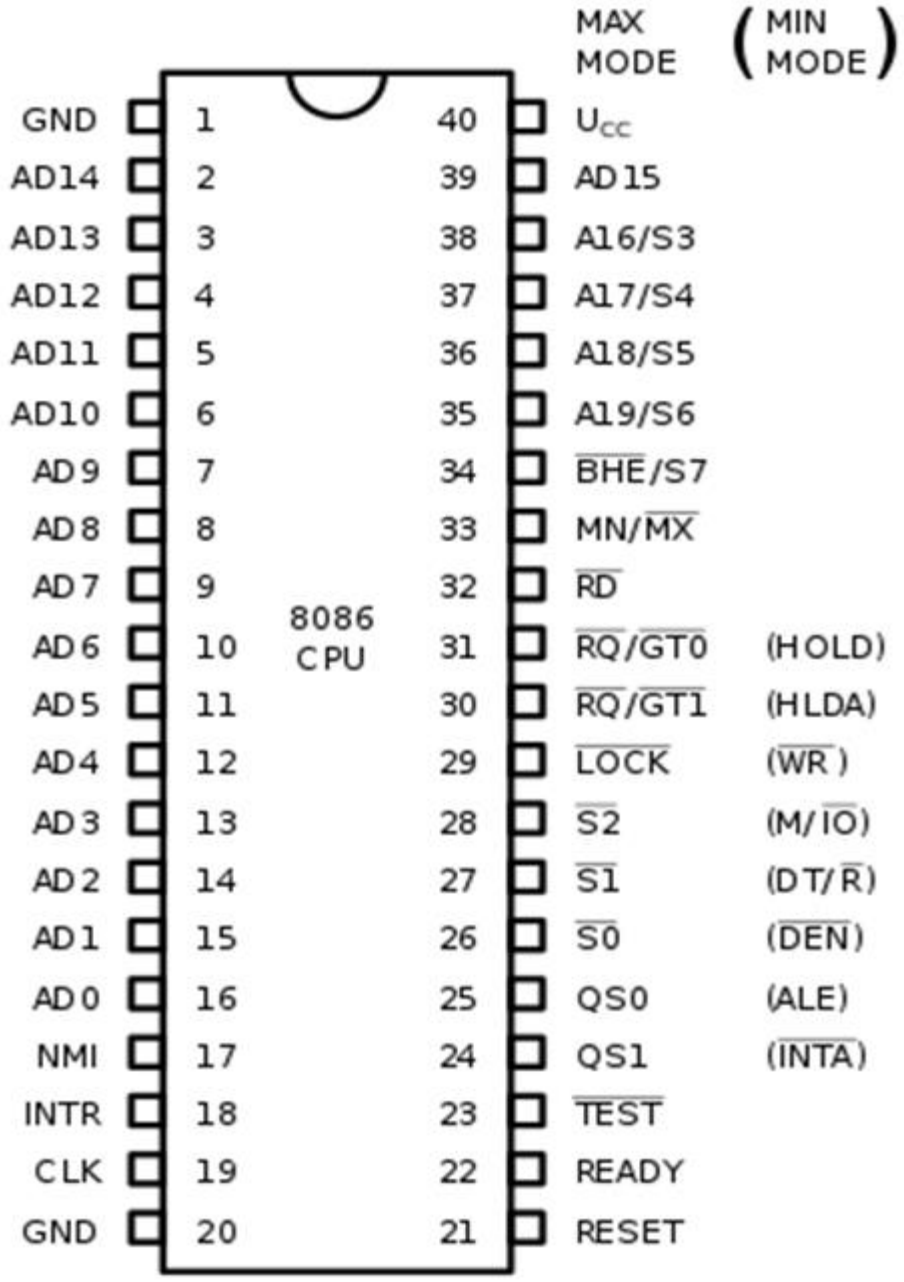
8086 architecture

- It is a 16-bit architecture (reg and ALU).
- Fourteen 16-bit registers.
- A 16-bit data bus.
- A 20-bit address bus.
- Memory is byte addressable.
- 16-bit I/O addresses.



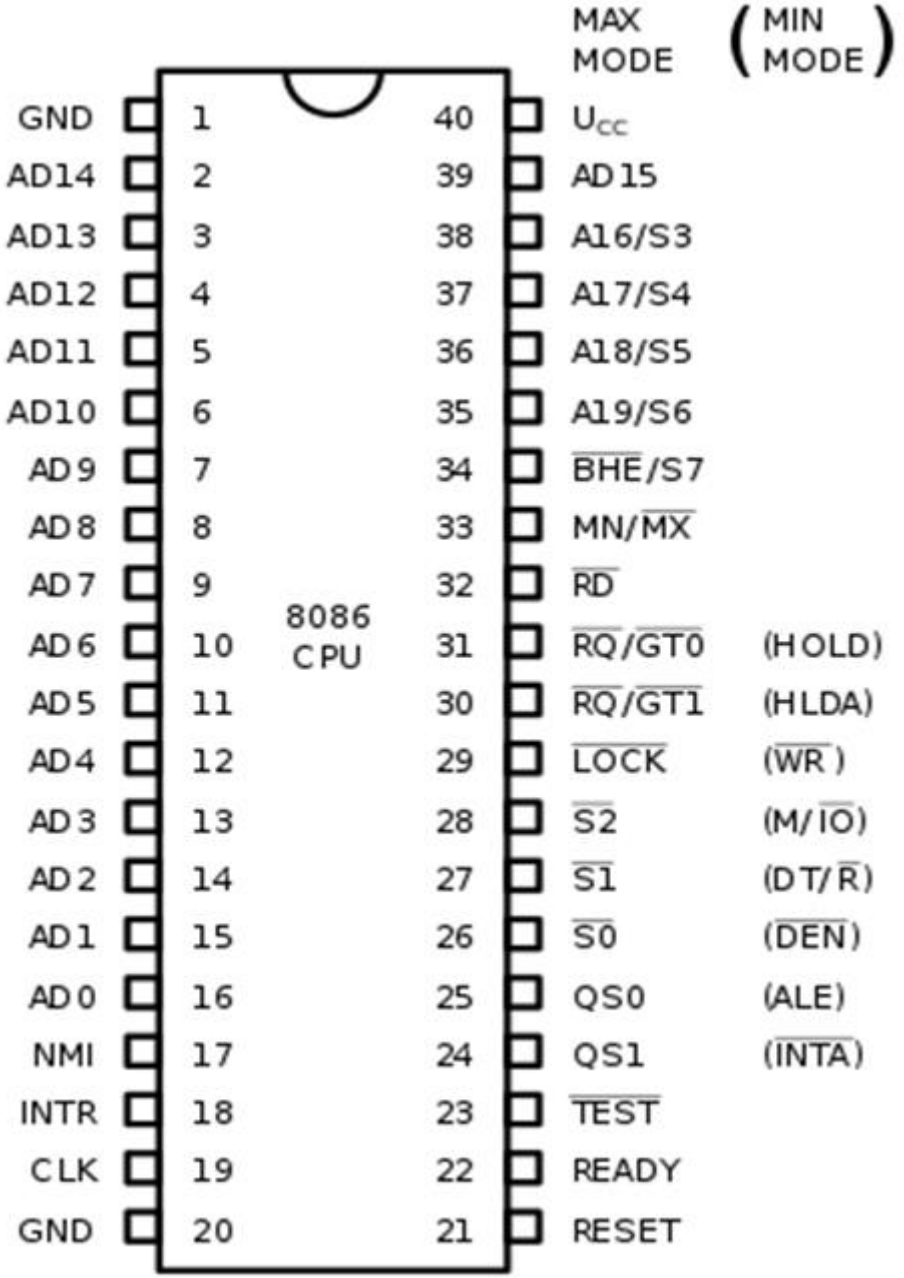
8086 Pin diagram

- The 20-bit address bus and the 16-bit data bus are multiplexed to save pins.
- AD [0:15] are multiplexed with the data.
- A [16:19] are multiplexed with the status signals.
- During the first half of the clock cycle A[0:19] pins work as address bus.
- In the second clock cycle AD[0:15] pins works as data bus.



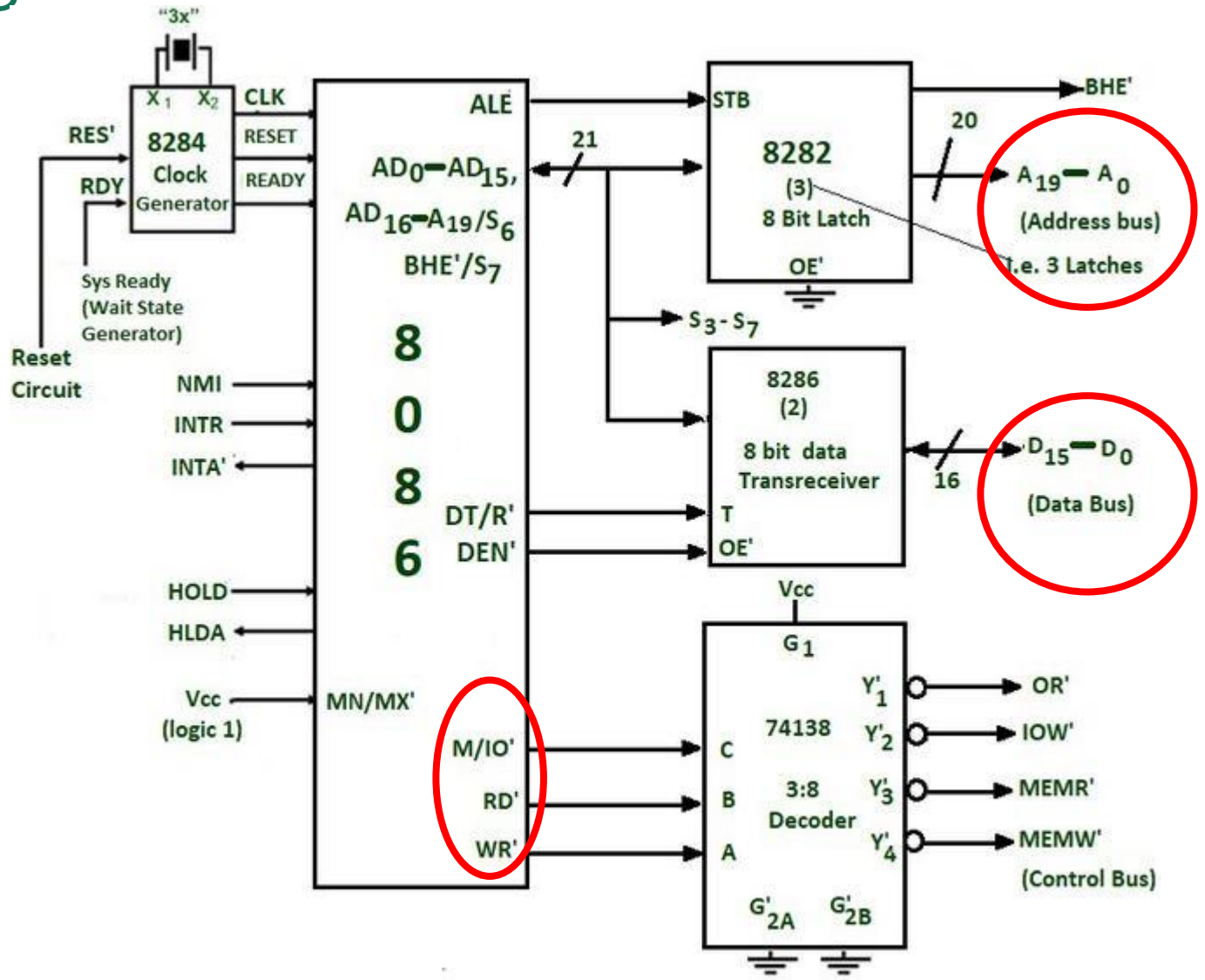
8086 Pin diagram

- Status bits help determine the status of the 8086 in terms of :
  - interrupts
  - HLT
  - memory read
  - memory write
  - I/o port read
  - I/o port write
  - code access
  - ….etc.



8086 I/O addressing

- The M/IO pin selects between the memory addressing and the I/O devices addressing.
- I/O devices lessen to the address bus.
- When the device address is called and the I/O pin is enabled, then it knows that the following data cycle is for its use (whether read or write).



I/O addressing

- The addressing mode used in the 8086 is called port I/O addressing mode.
- Where the I/0 address are separated from the memory.
- There is another mode in other microprocessors called memory mapped I/O addressing mode.
- In that mode, a certain space inside the main memory is reserved for the I/O devices.

I/O addressing instructions

- How the processor itself knows when to enable the memory and when to enable the I/o addressing in the port address mode?
- I/O addressing use only specific instructions [IN and OUT].
- The OUT instruction copies a byte from AL or a word from AX to the specified port.
- For simplicity: think of the port as a temporary register on the data bus connected to the device, and the port address is the device address.
- DX register is used for 16 bit addresses.
- AX or AL register is used for the 16 or 8 bits data.

```
Mov DX,3B2FH
Mov AL,05h
OUT DX,AL
```

I/O addressing instructions

- How the processor knows when to enable the memory and when to enable the I/o addressing in the port address mode?
- I/O addressing use only specific instructions [IN and OUT].
- The IN instruction copies data from a port to the AL or AX register.
- DX register is used for 16 bit addresses.
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```
Mov DX,3B2FH
IN AX,DX
```

I/O addressing instructions

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- I/O addressing use only specific instructions [IN and OUT].
- The IN instruction copies data from a port to the AL or AX register.
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```
Mov DX,3B2FH
IN AX,DX
```

I/O addressing scenario with input device connected to address 3B2FH

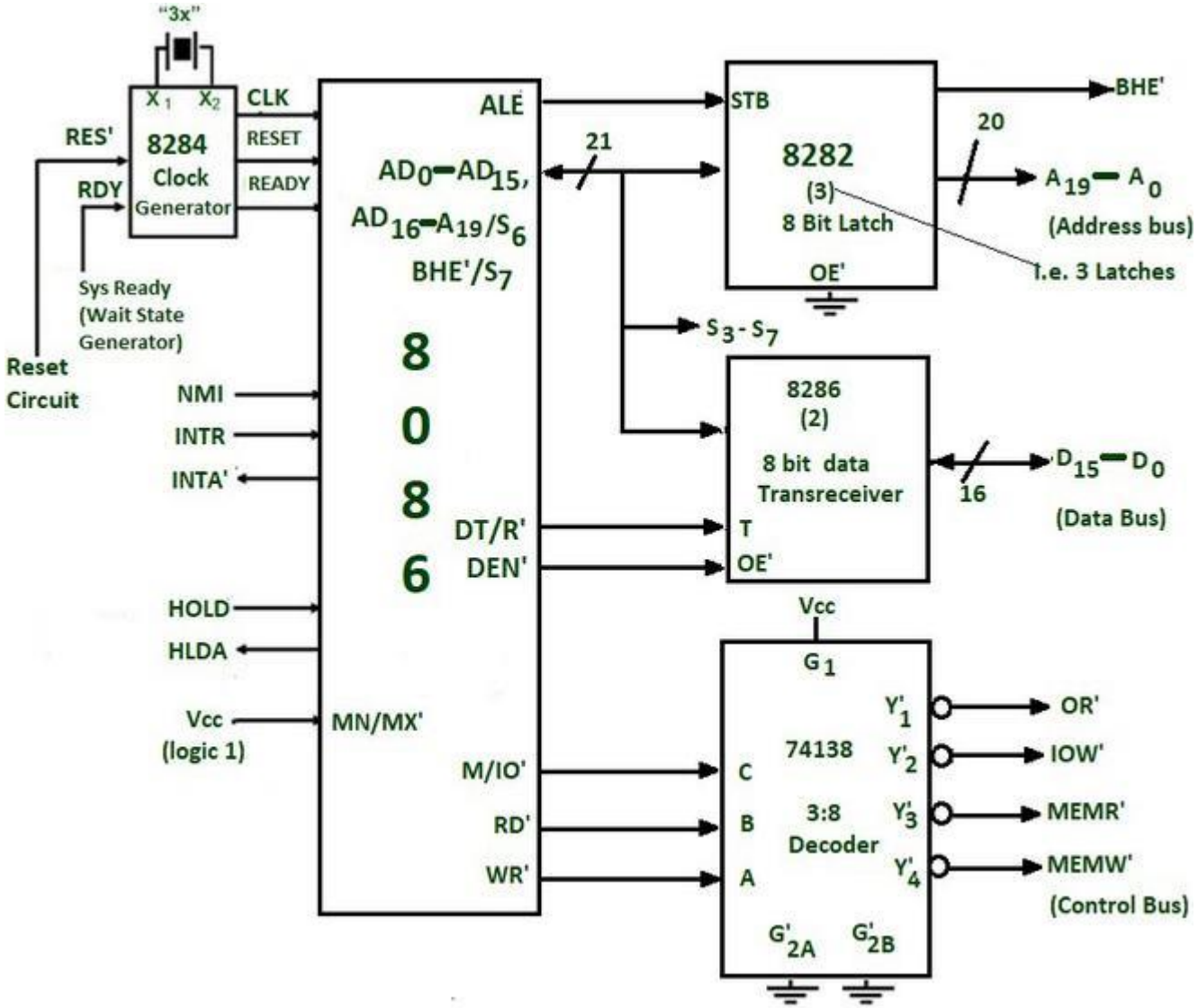
- 1) The user writes :

```
Mov DX,3B2FH
IN AX,DX
```

- 2) The 8086 fetches and decodes the instructions

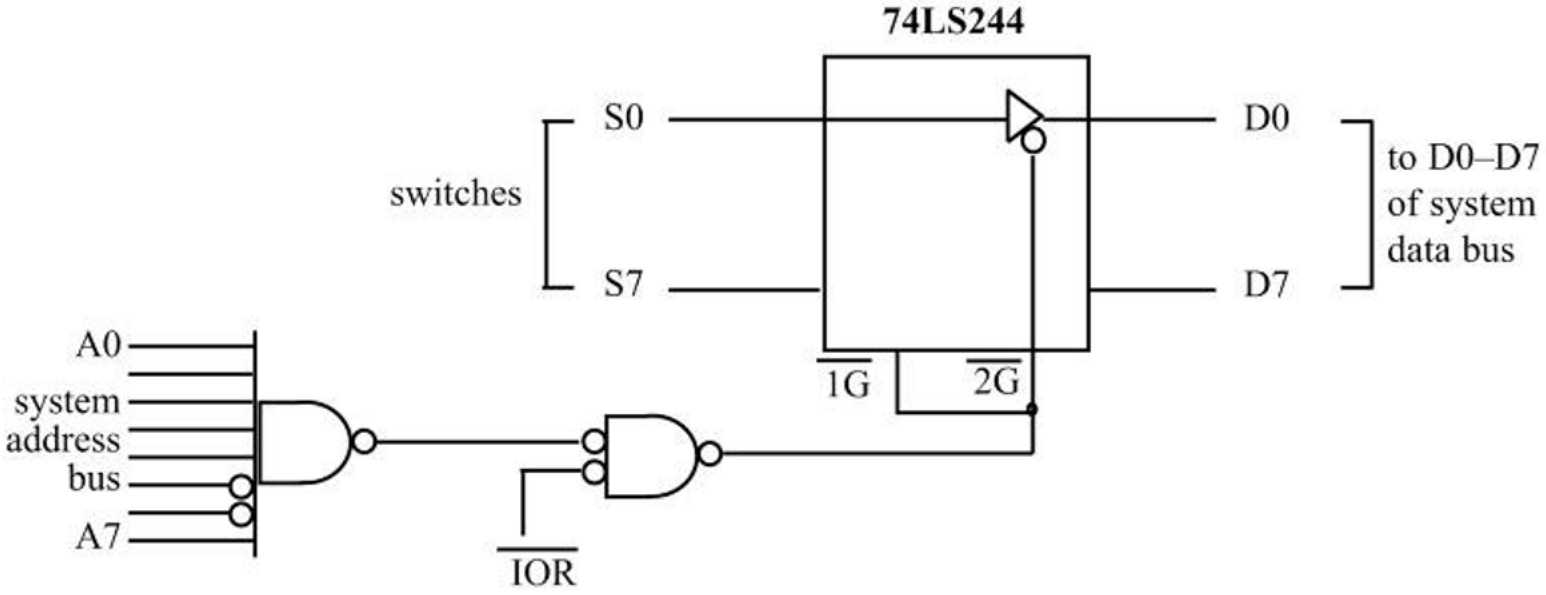
I/O addressing scenario with sensor device connected to address 3B2FH

- 3) the 8086 and the 74138 decoder signals the IOR pin.
- 4)The device listen to the address bus and is enabled. (in the first half cycle).
- 5)The device puts its data on the data bus. (in the second half cycle).



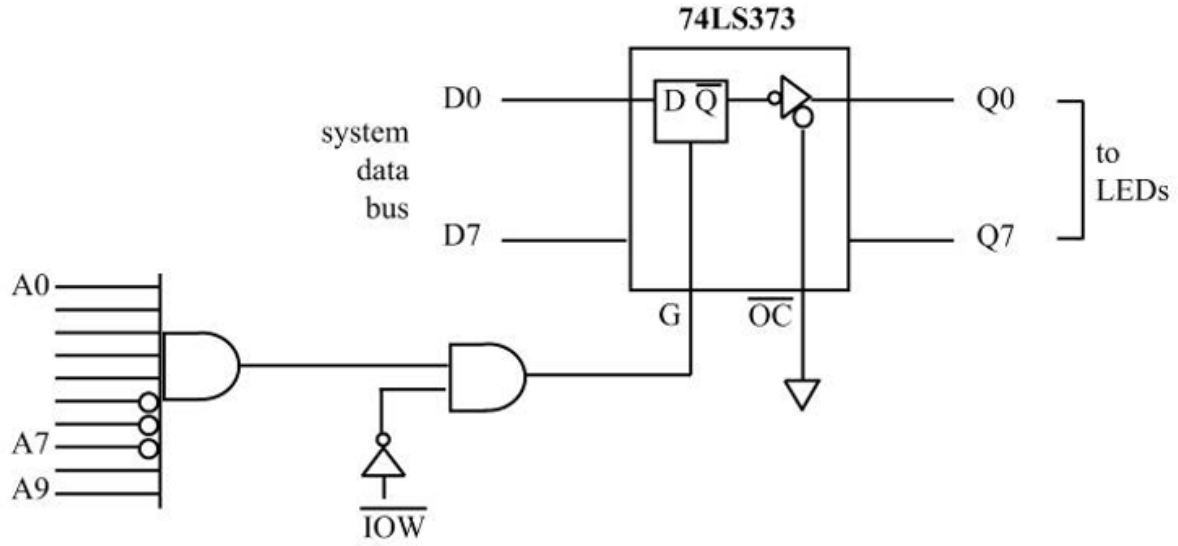
74LS244

- Input devices by nature, provide data all the time
- There is a need for access management to the data bus
- The 74LS244 chip consisted of tristate buffers that controls the data flow.

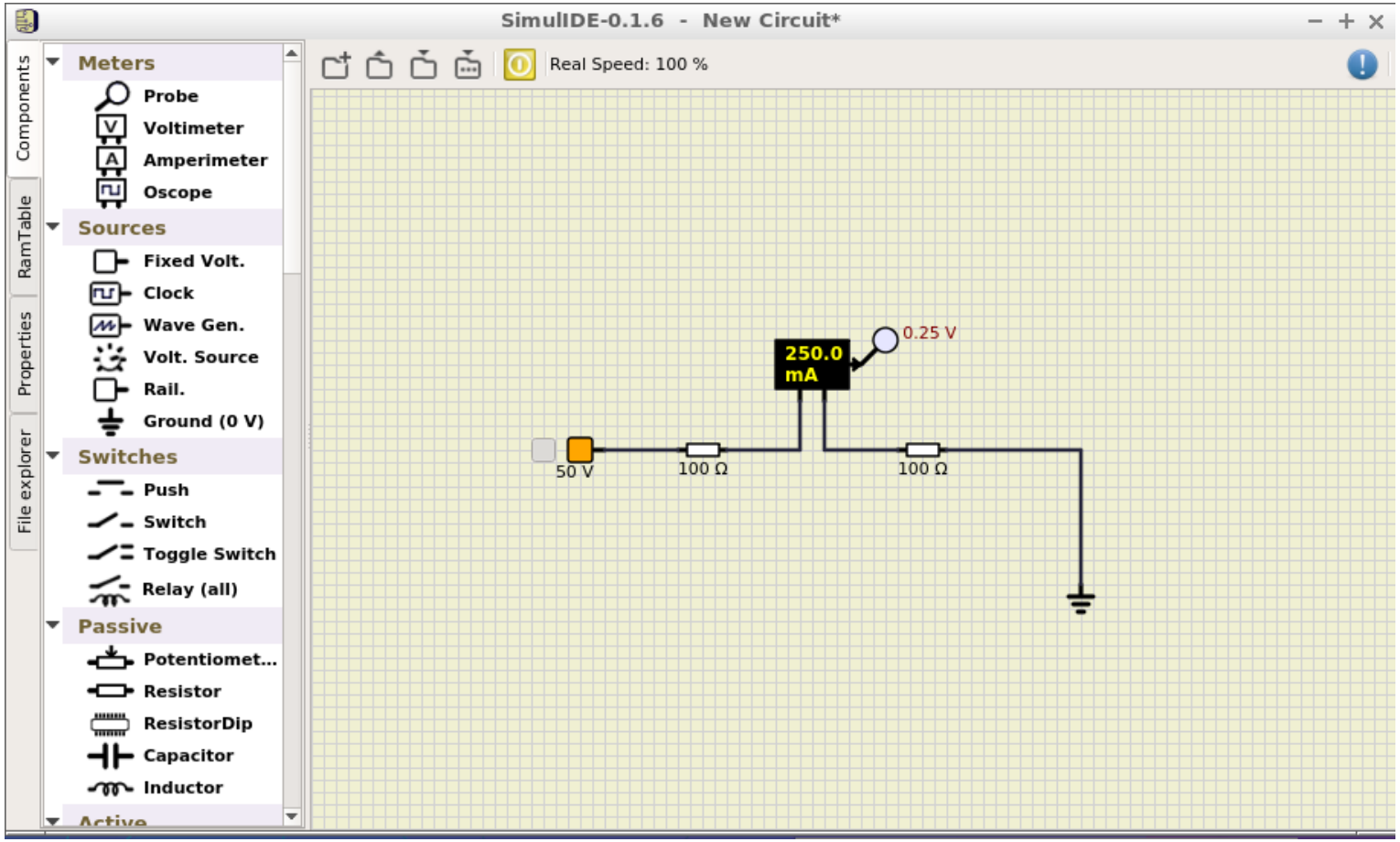


74LS373

- We cannot output to the output devices all the time.
- There is a need for access management to the device.
- The 74LS373 chip consisted of tristate buffers that controls the data flow.



SimullDE overview



Lab requirement

- You have two devices: an output device (8-led-bar) at address 33CC h and an input device (8-switch-dip) at address 11EE h.
- Using SimulIDE, Draw a circuit diagram for the devices connection using the following components:
  - One 74LS373
  - One 74LS244
  - One 8-bits Data Bus takes the input from a switch dip
  - One 16-bits address bus takes the input from a switch dip
  - One IOW input switch and one IOR input switch
  - two 8-ledsBar act like the output of the both devices (one is actual and the other is the bus).
  - two 8-switchsDip act like the input of the both devices (one is actual and the other is the bus).
  - Any number of any inputs (AND, OR, NOT, NOR, NAND, XOR, XNOR)
  - Any number of intermediate connection only busses.
  - Leds/rails/ground

Lab requirement

- The simulation must run without errors.
- Work in pairs.
- Make your address decoding extendable (i.e. consider the possibility of adding more I/O devices in the future).
- The design neatness is graded.
- Add labels as much as you can.