Computer Systems 414 1 May 2021

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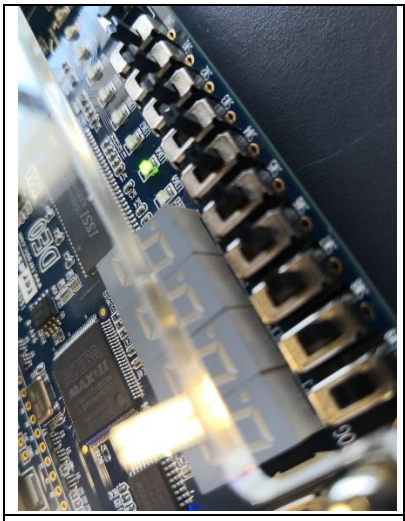
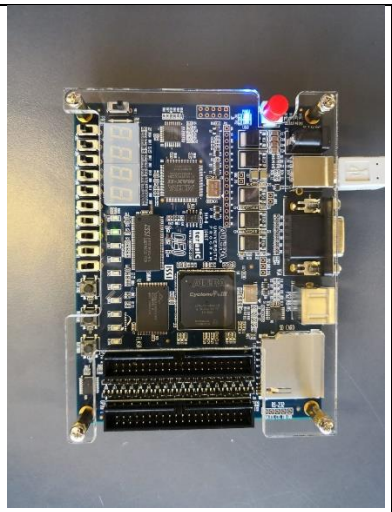
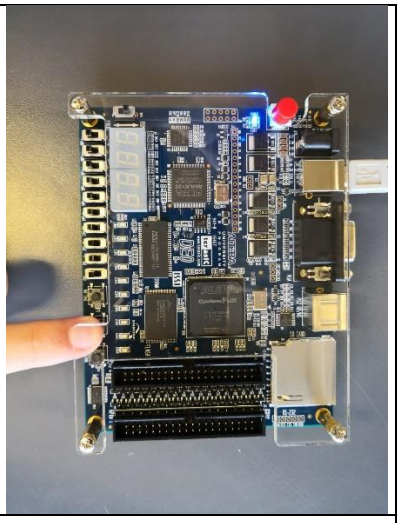
Connecting peripherals to an FPGA.

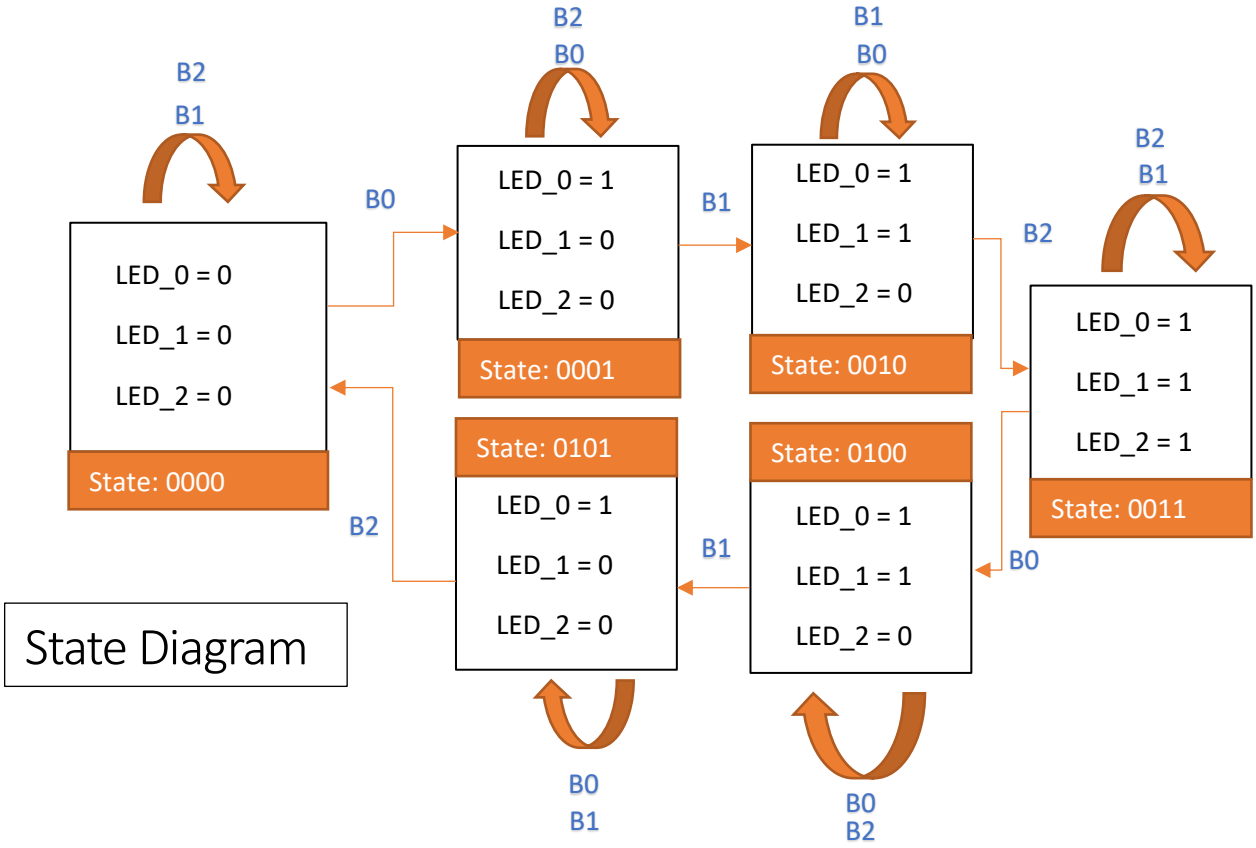






Q6) The compilation process differs in the fact the code is executed on an actual FPGA instead of being simulate via software on a computer. The output is an actual LED turning on instead via a connected made in hardware instead of a simulated timing diagram.

State Diagram



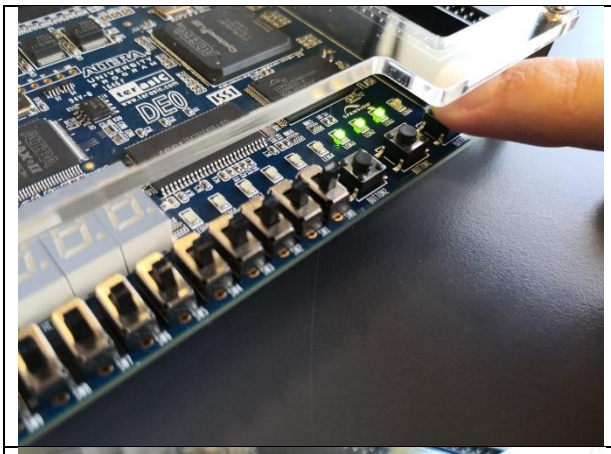
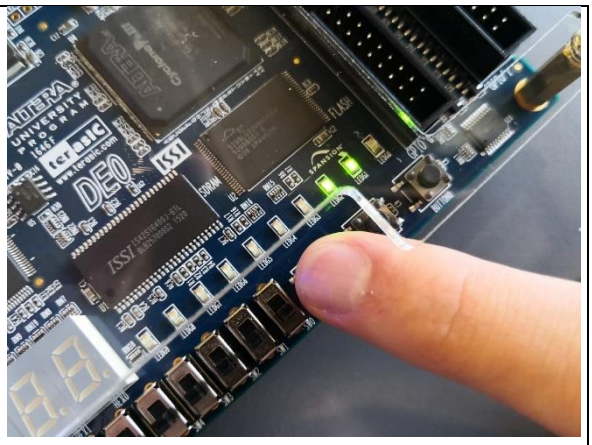
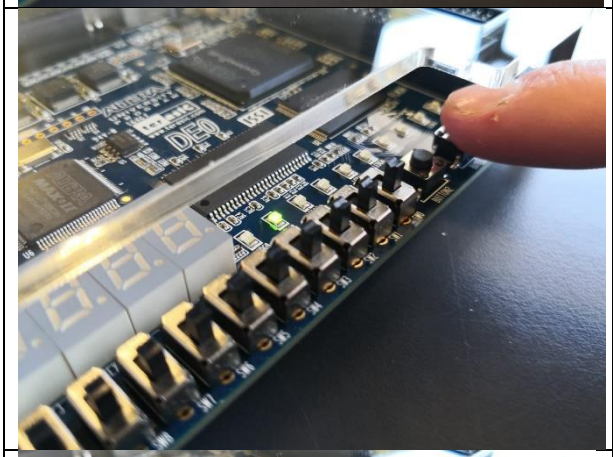
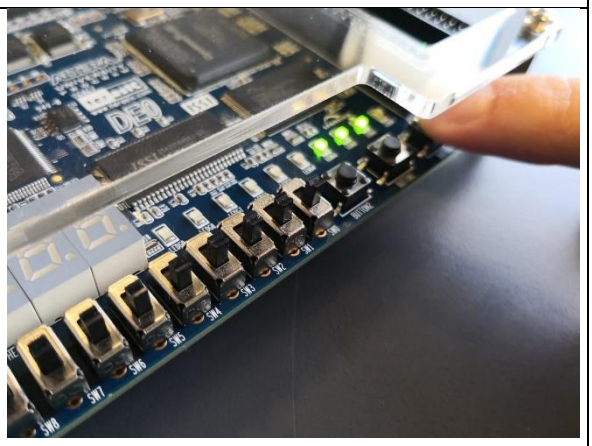
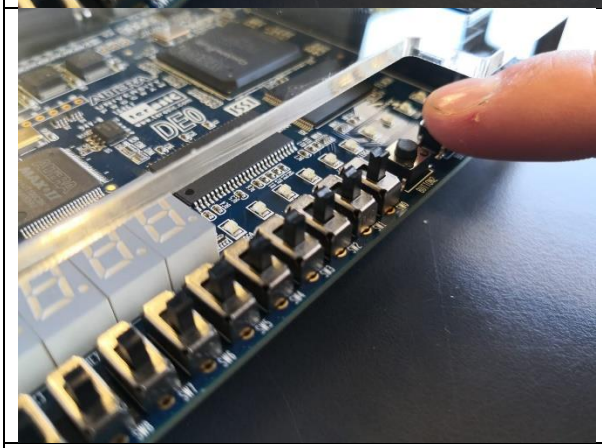
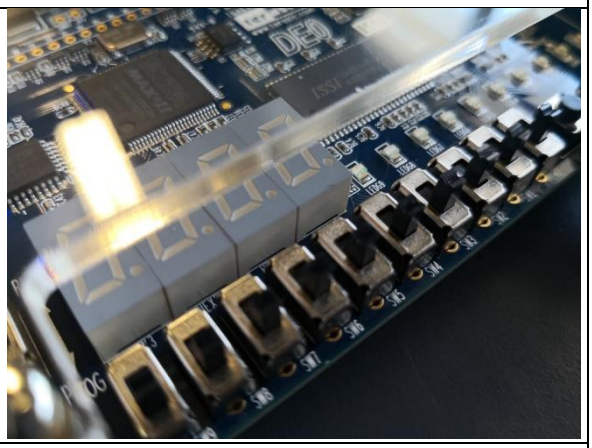







Photo results of implemented code on A FPGA board. (We did lose some of our photos due to corrupted files.)

```
77
78  ARCHITECTURE structure OF DE0 IS
79  signal state : unsigned (3 downto 0) := "0000";
80  BEGIN
81
82  PROCESS(CLOCK_50)
83  BEGIN
84  --state <= "0000"; -- Starting State is zero
85      -- NEXT BUTTON 0
86  if BUTTON(0) = '0' then
87      if state = "0000" then
88          state <= "0001";
89          LEDG(0) = 1;
90          LEDG(1) = 0;
91          LEDG(2) = 0;
92      elsif state = "0011" then
93          state <= "0100";
94          LEDG(0) = 1;
95          LEDG(1) = 1;
96          LEDG(2) = 0;
97      end if;
98      -- NEXT BUTTON 1
99  elsif BUTTON(1) = '0' then
100     if state = "0001" then
101         state <= "0010";
102         LEDG(0) = 1;
103         LEDG(1) = 1;
104         LEDG(2) = 0;
105     elsif state = "0100" then
106         state <= "0101";
107         LEDG(0) = 1;
108         LEDG(1) = 0;
109         LEDG(2) = 0;
110     end if;
111     -- NEXT BUTTON 2
112 elsif BUTTON(2) = '0' then
113     if state = "0010" then
114         state <= "0011";
115         LEDG(0) = 1;
116         LEDG(1) = 1;
117         LEDG(2) = 1;
118     elsif state = "0101" then
119         state <= "0000";
120         LEDG(0) = 0;
121         LEDG(1) = 0;
122         LEDG(2) = 0;
123     end if;
124 end if;
125
126 END PROCESS;
127 END structure;
128
```

Code version of the state diagram drawn above.