U N I V E R S I T E I T S T E L L E N B O S C H U N I V E R S I T Y
j o u k e n n i s v e n n o o t k n o w l e d g e p a r t n e r

Computer Systems 414

Practical 5

2021

Aim of Practical 5:

1. To get practical experience in writing, compiling and simulating VHDL code

Rules of Engagement

1. Attendance is not required for this practical – students can complete the practical on their own time.

2.This practical is individual work.

3. Supporting documentation is available on learn.sun.ac.za, but students also have to do their own research.

4.The report is to be submitted on learn.sun.ac.za. The deadline for the reports is (14:00) Wednesday, 21 April 2021. **No late submissions will be accepted.**

5. Do not forget to cite and give credit for any information reported which is not your property.

8. Google is your friend. Any information not given is left out on purpose. Search for your solution and on the internet or relevant manuals and documentation.

Task (Use the uploaded files from SunLearn as required)

Assignment 5A

For this practical we will use GHDL, an Opensource VHDL compiler.

Please refer to the attached document for the GHDL installation instructions.

Task (Use the uploaded files from SunLearn as required)

1. Follow the instruction form the attached file to install GHDL and GTLWave.

2. The setup and use of GHDL is also explained in this video:

   https://www.youtube.com/watch?v=H2GyAIYwZbw

2. Then go to the GHDL user manual and work through the ‘heartbeat’ and ‘full adder’ examples (create source files and follow the instructions to compile and simulate the code.

   https://ghdl.readthedocs.io/en/latest/quick_start/

3. Identify the entity and architecture portions of the code and draw a block diagram of the entities showing the input and output signals.

3. Search for the truth table of a full adder and compare the equations used in the full adder example to the truth table. Do you agree with their equations?

4. Consider the full adder testbench code. This is a special VHDL program that is used to apply signals to the full adder entity and to check if the outputs are as expected. Work through the file and note the instantiation of the adder entity. Identify the places where the adder is declared as a component, associated with the entity and instantiated as a component. Compare the pattern array to the truth table and work through the last portion of the code where the signals are applied.

5. Use the instructions of the ‘heartbeat’ example to use GTKWave to display the output of the simulation

6. Submit your ‘heartbeat’ and ‘full adder’ code to Sunlearn

Please note:

We have not yet covered VHDL in great detail. The major aim of the practical is therefore to create an awareness of how VHDL code is compiled and simulated. As we progress through the term the detail of the code and the set-up and use of testbenches will become more apparent.