UNIVERSITEIT STELLENBOSCH UNIVERSITY
jou kennis vennoot • your knowledge partner

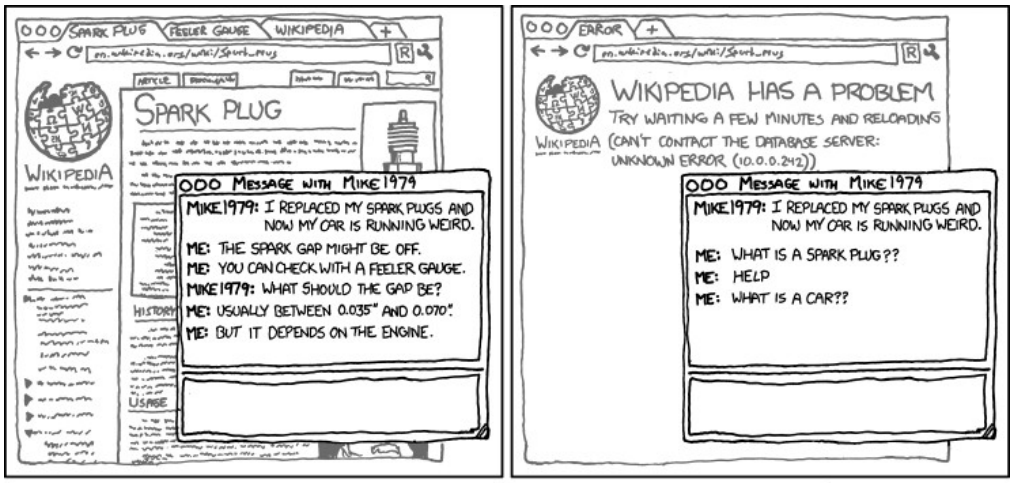
Computer Systems 414

Tutorial 2

2021

Aim of Tutorial 2:

a) To gain experience with the content of the course thus far -especially with VHDL



WHEN WIKIPEDIA HAS A SERVER OUTAGE, MY APPARENT IQ DROPS BY ABOUT 30 POINTS.

Rules of Engagement

1. Complete the tutorial on your own time. You may work in groups of two or three. A memo will be made available the week after the tutorial.

2. Google is your friend. Any information not given is left out on purpose. Search your solution and on the internet or relevant manuals and documentation.

Preparation

- Open your textbook!!!
- Go through chapter 7 of Wolfe, Chapter 4 of Harris and the relevant chapters of Freerange VHDL.

Assignment

1. Who are the people that must be present at a design review and what documentation do they need?

2. What is a PDR and list four aspects that a PDR document should address? Hint: Google for the ‘Cansat’ project and look at the PDR documents you can find there.

VHDL:

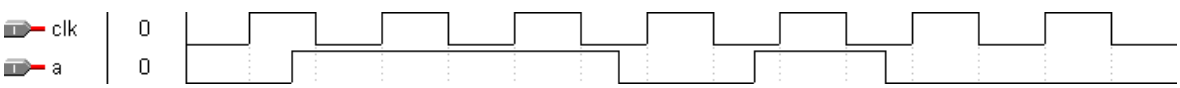
3. The most common port types in VHDL are ‘in’, ‘out’ and ‘inout’. Describe briefly what each means.

4. When are latches or flip-flops generated by VHDL code?

5. Why do VHDL state machines need the clock signal in the sensitivity list?

6. Sketch the signals and variable (b, c, d, e, f and g) for the design below and given input signals. Assume all latches and flip-flops are zero at time zero. Assume that delay times are much shorter than the clock period.

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY vraag2 IS
  PORT( clk, a     : IN STD_LOGIC;
        b, c, d, e  : OUT STD_LOGIC);
END vraag2;

ARCHITECTURE logic OF vraag2 IS
  SIGNAL f : STD_LOGIC;

BEGIN
  PROCESS(clk, a, f)
    VARIABLE g : STD_LOGIC;
  BEGIN
    IF rising_edge(clk) THEN
      b <= a;
      f <= a;
      e <= f;
      c <= g;
      g := a;
    END IF;

    d <= f;

  END PROCESS;
END ARCHITECTURE logic;
```



7. The VHDL code below is supposed to generate a slow clock, but contains functional and syntax errors. Correct the errors.

```
LIBRARY ieee;
USE ieee.std_logic_arith.ALL;

ENTITY vraag3 IS
  PORT( clk         : IN STD_LOGIC;
        slow_clock   : OUT STD_LOGIC );
END vraag3;

ARCHITECTURE logic OF vrg3 IS
  constant divider : integer range 0 to 255 := 55;
  VARIABLE counter : integer range 0 to 255;

BEGIN

  PROCESS( clk )
  BEGIN

    IF rising_edge(clk) then

      IF counter = divider THEN

        slow_clock <= not slow_clock;
      ELSE
        counter := counter + 1;
    END IF;

  END PROCESS;
END ARCHITECTURE logic;
```

8. A part of a reaction-time game design must determine which one of 4 players pressed his button first. The system uses a 10kHz clock to test whether a button has been pressed 10 000 times a second. The 'button' inputs are active low. The person or persons who pressed their buttons first are indicated with the 'winner' output. For each game the system waits for a high on 'start' before it starts testing the buttons. After a winner has been determined the 'winner' outputs stay valid until a high 'reset' pulse is received, which restarts everything. See the diagram of the component below.

8a. Draw the state machine diagram of the design for the reaction-time game. Indicate all states and the conditions which determine the states.

8b. Show the full VHDL code for the design.