

ELECTRONICS 365 PRACTICAL 3 – NON-IDEAL OP AMPS

5 October – 9 October 2020

INTRODUCTION:

Practical 3 is due at midnight (24:00) on Friday 9th October. This practical includes both a spice submission and a practical report. These two submissions must be called 12345678.cir and 12345678.pdf respectively (replacing 12345678 with your student number). The spice submission counts for two marks and the practical report counts for eight marks. The theoretical calculations may be handwritten; however, they must be neat and logically laid out. All other parts of the report must be typed.

For this practical you will need to use Ngspice version 3.2 which can be downloaded from SUNLearn. The necessary spice files provided for this practical are:

- Compensation_ex.cir (template for spice submission)
- Prac3Test1.cir
- Prac3Test2.cir
- Prac3Test3.cir
- Prac3Test4.cir
- Prac3Test5.cir
- LM741.cir (op amp model for Section A only)

AIMS:

This practical is divided into three sections. The first section involves analysis and simulation of frequency and gain related non-idealities in an op amp circuit. The second section involves the design and simulation of compensation circuitry to minimize the effects of input bias current and offset voltage. The third section includes analysis of the noise in an op amp circuit.

As in practical 1 and 2, there are slightly different variations of this practical depending on your student number. Ensure that you carefully read the practical brief and use the correct values, models and testbench. Table 1 below shows which sets of circuit values you should use according to student number for Sections A, B and C.

Table 1: Student Number Set Assignment

STUDENT NO. ENDING IN	CIRCUIT VALUES
0 OR 6 OR 8	SET 1
1 OR 7	SET 2
2 OR 3	SET 3
4 OR 9	SET 4
5	SET 5

SECTION A – FREQUENCY, GAIN AND RESISTANCE:

For section A, use the amplifier circuit given in Figure 1. The op amp used in this circuit is the LM741 (the datasheet and spice file for this opamp are both available on SUNLearn). There is no spice submission for this section, but all relevant spice code must be included in an appendix of the report. V_+ is taken as 15 V and V_- as -15V.

Figure 1: Circuit Diagram for Section A

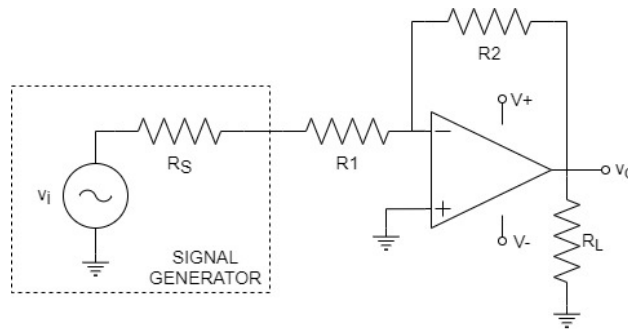


Table 2: Circuit Values for Section A

CIRCUIT VALUES	SET 1	SET 2	SET 3	SET 4	SET 5
R₁ (kΩ)	1	1	2	3	1
R₂ (kΩ)	20	5	8	9	7.5
R_L (kΩ)	200	100	150	175	100

Table 2 contains the circuit values that should be used for this section. Use Table 1 to determine which Set is assigned to you.

SECTION A TASKS:

- The signal generator has a source resistance of $R_S = 50\Omega$. Determine the accurate closed loop voltage gain of the given circuit using relevant values from the LM741 datasheet. You may assume the output resistance of the op amp $R_o = 0\Omega$.
- Simulate the circuit with spice and determine the closed-loop voltage gain. Include a spice plot of gain against frequency in the report. Compare this with the value obtained in a).
- Determine the small-signal bandwidth of the circuit by calculation and through spice simulation. Compare the values obtained and discuss potential reasons for differences in the values.
- Determine the theoretical FBPW of the op amp circuit. Then use a 1V step function ("PULSE") to determine the slew rate of the op amp and from that calculate the FBPW for the simulated circuit. Compare the values obtained and discuss potential reasons for difference in the values.

There are three marks available for Section A. One mark for a) and b) combined, one mark for c) and one for d). Remember to include spice plots to support your answer and the relevant spice code in an appendix to the report.

SECTION B – OFFSET VOLTAGE AND BIAS CURRENT COMPENSATION:

There are five variations of this section depending on your student number. Each variation requires the use of different resistor values, bias currents and offset voltages and has a different testbench. Use Tables 3 and 4 below to determine which values and testbench you should use and what requirements you should meet according to Table 1 and your student number. Figure 2 is the multi-stage op amp circuit used for the whole of Section B.

Figure 2: Circuit Diagram for Section B

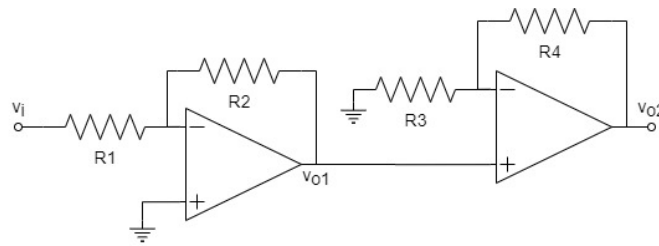


Table 3: Circuit Values for Section B

CIRCUIT VALUES	SET 1	SET 2	SET 3	SET 4	SET 5
R1 (kΩ)	10	15	20	20	10
R2 (kΩ)	50	30	80	60	100
R3 (kΩ)	20	10	15	10	15
R4 (kΩ)	40	40	45	100	30
V_{os} (mV)	5	10	2	20	15
I_B (μA) (AVERAGE)	2	1	3	5	4
I_{os} (μA)	0.4	0.2	0.4	0.6	0.2

EXAMPLE: If your student number ends in 1, you should use Set 2, Prac3Test2.cir and design for $|V_{o1}(\text{max})| = 6.1 \text{ mV}$ and $|V_{o2}(\text{max})| = 49 \text{ mV}$.

SECTION B ANALYSIS:

You may assume $v_i = 0 \text{ V}$.

- Determine the value of the maximum output voltages at v_{o1} and v_{o2} .
- Simulate your circuit in spice and compare the values obtained by simulation with those from your theoretical calculations. Include your spice code in an appendix of the report – no spice submission is required.

SECTION B DESIGN:

Design bias current and offset voltage compensation to minimise the effects of the input bias current and offset voltage on the output voltage of the circuit. Include all theoretical calculations required to design the compensation circuitry in your report. Calculate the new value of the maximum output voltages v_{o1} and v_{o2} when the compensation circuitry is included. These values should be smaller than the requirements given in Table 4. You will be required to submit a spice file containing the circuit with your chosen compensation circuitry included. This spice file will be run through the specified testbench in Table 4.

Table 4: Section B Requirements

STUDENT NO. ENDING IN	TESTBENCH	$ V_{o1}(\text{max}) $	$ V_{o2}(\text{max}) $
0 OR 6 OR 8	Prac3Test1.cir	21 mV	82 mV
1 OR 7	Prac3Test2.cir	6.1 mV	49 mV
2 OR 3	Prac3Test3.cir	33 mV	149 mV
4 OR 9	Prac3Test4.cir	37 mV	483 mV
5	Prac3Test5.cir	21 mV	84 mV

A template for the spice file submission is given on SUNLearn (Compensation_ex.cir). Please use this template and replace only the highlighted sections with your own code:

```
*-----
* SPICE model for amplifier with compensation

* -----
* Surname: Your surname
* First name: Your first name
* Student number: Your student number
* -----

* op amp model
.subckt opamp non inv out
Ri non inv 1e14
Eout out 0 non inv 1e7
.ends

* Define amplifier circuit with compensation as a subcircuit
.subckt comps pa na pb nb vcc vee vo1 vo2 vx1 vx2

* ----- Start of student code -----

*Op amps for amplifier
XOPAMPA pa na vo1 opamp
XOPAMPB pb nb vo2 opamp

* Original circuit with random values
R1 0 na 10k
R2 na vo1 20k
R3 vx3 nb 10k
R4 nb vo2 50k

* Dummy components in the place of compensation
Rd1 vx1 0 1m
Rd2 pb vx2 1m
Rd3 vx3 0 1m

* ----- End of student code -----

.ends

*-----
```

The testbench requires certain nodes in your circuit to have specific names. If the nodes are not named correctly, the testbench will fail to run. These nodes are shown in red in Figure 3. The green boxes in Figure 3 are where your compensation circuitry should be included. The voltage sources labelled V_{OS} in blue are provided by the testbench. **DO NOT INCLUDE THEM IN YOUR CIRCUIT!** The testbench provides two voltage sources (V_{cc} vcc 0 10 and V_{ee} vee 0 -10). You can apply these where desired in your compensation circuitry by using the node names vcc and vee. Do not include any of your own voltage sources of any kind in your submission – all required sources are provided by the testbench.

The testbench includes the line “.include yourstudentnumber.cir”. In order to test your circuit, replace “yourstudentnumber” with your student number (the name of your spice file) and run the testbench in Ngspice.

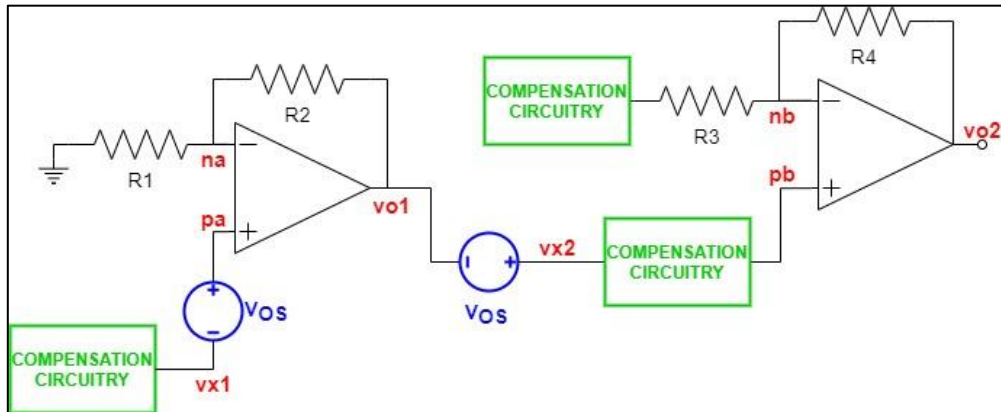


Figure 3: Layout for spice simulation including node names

There are 5 marks available for section B. One mark for the theoretical calculations and spice of the circuit with no compensation. One mark for the theoretical calculations related to designing the required compensation circuitry. Two marks for the testbench results. One mark for the calculation of the output voltages after compensation and comparison with spice results. If no logical theoretical calculations for the compensation design are included in the report, you will receive 0 for the testbench results.

SECTION C – NOISE ANALYSIS:

Figure 4 shows two non-inverting op amp circuits. Calculate the output noise and equivalent input noise for each of them. What useful information can be determined from the results? Use the circuit values from table 4 according to your student number as laid out in table 1. You can take $T = 293 \text{ K}$. $I_n = 1 \text{ pA}/\sqrt{\text{Hz}}$ and $E_n = 2.828 \text{ nV}/\sqrt{\text{Hz}}$.

Figure 4: Circuits for Section C (Cir. 1 left and Cir. 2 right)

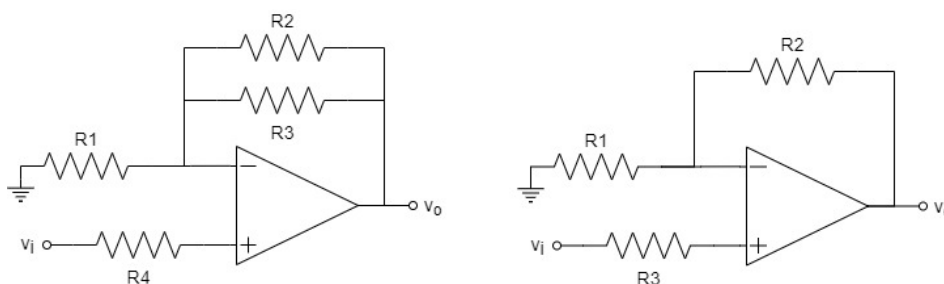


Table 5: Circuit Values for Section C

CIRCUIT VALUES	SET 1	SET 2	SET 3	SET 4	SET 5
CIR. 1 R1 (k Ω)	10	10	15	2	5
CIR. 1 R2 (k Ω)	100	40	90	12	50
CIR. 1 R3 (k Ω)	100	40	90	12	50
CIR. 1 R4 (k Ω)	8.333	8	11.25	1.5	4.167
CIR. 2 R1 (k Ω)	10	10	15	2	5
CIR. 2 R2 (k Ω)	50	20	45	6	25
CIR. 2 R3 (k Ω)	8.333	8	11.25	1.5	4.167

This section counts for 2 marks. One for the calculations and the other for discussion of the results.

IMPORTANT NOTES:

- If your spice submission does not run through the testbench you will receive 0 for it.
- **DO NOT INCLUDE ANY VOLTAGE SOURCES IN YOUR SUBMISSION.** The required voltages will be supplied by the testbench. You will receive 0/5 for the spice submission if you include your own voltage sources.
- If the spice submission does not correspond with the report – specifically if differences between theoretical values and spice values aren't addressed – then the report mark will be penalized.
- **PLEASE ENSURE YOU USE THE CORRECT CIRCUIT VALUES AND TESTBENCH OR YOU WILL BE PENALISED.**
- **THIS PRACTICAL IS NOT OPTIONAL.** If you do not submit a valid spice files you will receive 0 for the report as well.
- **START EARLY.**