Self-Test 1: Flags Condition

Assume the following register conditions:

AX = AB00H, BX = 200CH, CX = 3003H, DX = DEFFH

Find the status of the CF, PF, AF, ZF and SF for the following operations: BX (location)

1. MOV BX, 3FH
   ADD BL, 45H
2. ADD BX, DX
3. CMP AX, DX compare
4. NOT DX

SF → 最大bit有沒有1
AF → Bit 3去4有/沒carry
ZF → All 0的话就on
CF → 最大bit有/沒carry
PF → even number of 1

① BX = 3F

BL = BX

45 H	8 4 2 1
+ 3F H	1 0 0 0 0 1 0 0 [AF=1, ZF=0, CF=0, PF=1]
84 H	45 H [SF = 1]

② BX + DX

200CH
+ DEFF H
FF0B H

1111 1111 0000 1011

[AF = 1, ZF = 0, CF = 0, PF = 0, SF = 1]

③ compare = ⊖

[SF=1] 1 1010 1011 0000 0000
− 1101 1110 1111 1111
1100 1100 0000 0001

2nd method → two complement 倒转all 0/1 然后 ⊕1 ⊕ ↓ 原本加的no.

[AF = 1, ZF = 0, CF = 1, PF = 0, SF = 1]

④ NOT DX

DEFF H

DX : 1101 1110 1111 1111

NOT. 0010 0001 0000 0000

[AF = 0 , ZF = 0 , CF = 0 , PF = 0 , SF = 0]

Self test 2

① AL = CDH

AX = full container

AL = half of AX

AH = half of AX

AX = AH AB | AL CDH

BX = BH EF | BL 01H

DX = DH 23 | DL 45H

} Value of register

AL = CDH

XOR = 兩个一样的 1/0 = 0

1100 1101

0111 1001

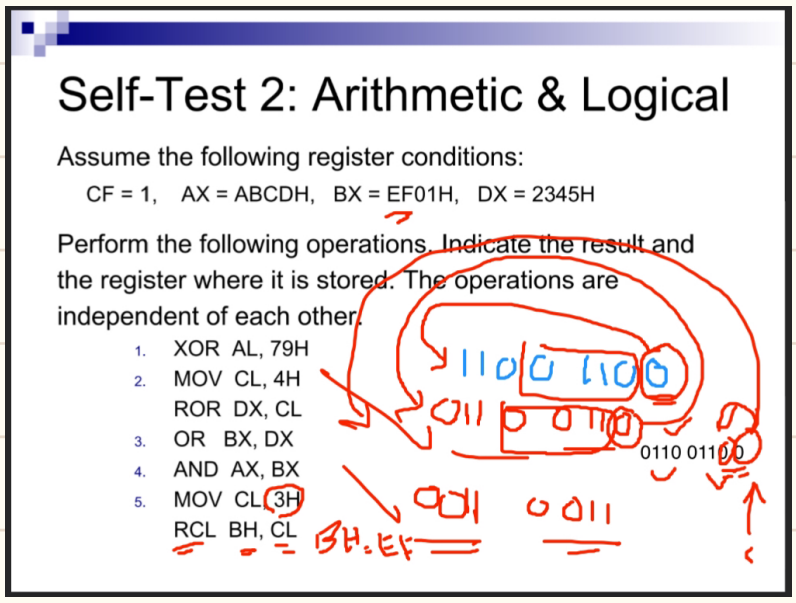
1011 0100

② DX = 2345

Rotate 4 = ROR 4 → CL = 4H

1次1个 number，對的 copy

RCL = Rotate carry left



DX = 2345 H → binary DX = 0010 0011 0100 0101

0101 0010 0011 0100 #

③ BX = EF01H , DX = 2345H

BX = 1110 1111 0000 0001

DX = 0010 0011 0100 0101

1110 1111 0100 0101 #

④ AX = 1010 1011 1100 1101

BX = 1110 1111 0000 0001

1010 1011 0000 0001 #

⑤ BH = EF = 1110 1111 不確定

110 1111 1 #

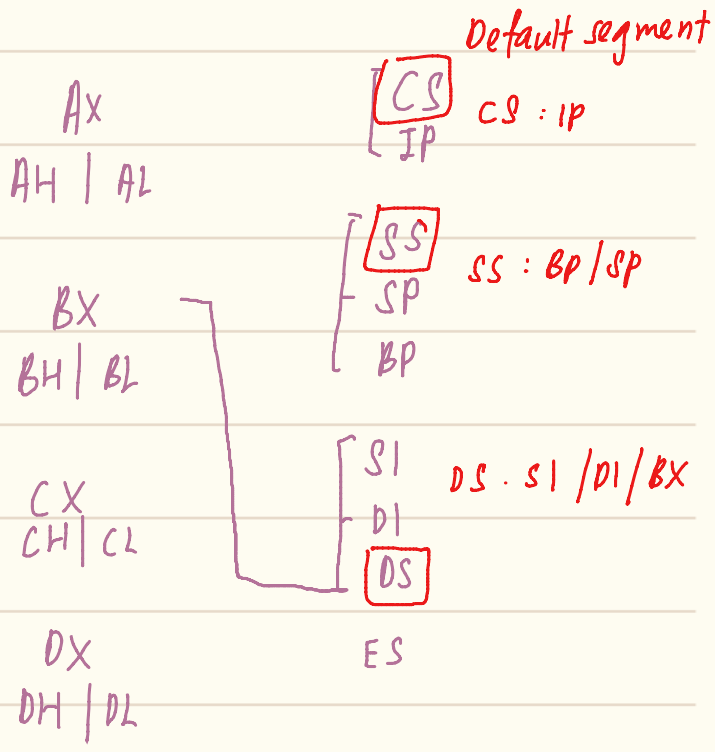
Self-Test 3: Physical Address

The register content for an Intel 8086 microprocessor is as follows:

CS = 1000H, DS = 2000H, SS = 3000H, SI = 4000H, DI = 5000H
BX = 6080H, BP = 7000H, AX = 25FFH, CX = 8791H, DX = 1299H

Calculate the physical address of the memory where the operand is stored and the contents of the memory locations in each of the addresses shown below:

1. MOV [SI], AL
2. MOV [DI+6H], BX
3. MOV [SI+BX–8H], AX
4. MOV [DI][BX]+28H, CX
5. MOV [BP][SI]+10H, DX



(data)

① move AL into [SI]

AL = FF

SI = 4000 (SI default segment DS, ⊕ 0 ⇒ DS 2000+0 = 20000)

[ ] = location

physical address

DS → 20000

SI → 4000

24000 → FFH #

② DI = 5000 , default segment = DS → 2000H ⊕ 0 = 20000H

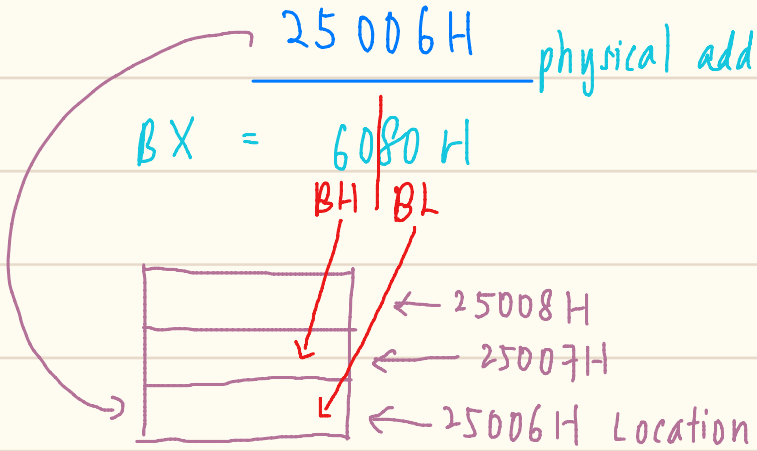
DS → 20000H

DI → 5000H

6H

25006H physical address

BX = 6080H



25006H = BL = 80H #

25007H = BH = 60H #

③ 20000 DS default segment

6080 BX = 6080H

+ 4000 SI = 4000H

2A080 (16)

- 8 8H

data locate → 2A078 = AL ⇒ FF

2A079 = AH ⇒ 25

④ MOV [DI][BX] + 28H , CX

DS default segment

20000H (DS)
+ 5000H (DI)
25000H
+ 6080H (BX)
H
+ 28H

87 CH
91 CL

⑤ MOV [BP][SI] + 10H , DX

SS default segment

30000H (SS)
+ 7000H (BP)
37000H
+ (DS)
(SI)

Microprocessor Exercise

A. ① BX = 3F H

BL = 3F H

3F = 0011 1111

45 = 0100 0101

1000 0100 = 84 H

[CF = 0, PF = 1, AF = 1, ZF = 0, SF = 1]

② BX = B00EH

DX = D23CH

BX → 1011 0000 0000 1110

DX → 1101 0010 0011 1100

1 1000 0010 0100 1010

[CF = 1, PF = 0, AF = 1, ZF = 0, SF = 1]

③ AX = A112H, DX = 023CH

AX → 1010 0001 0001 0010

DX → 0000 0010 0011 1100

1001 1110 1101 0110

[CF = 0, PF = 1, AF = 0, ZF = 0, SF = 1]

④ DX = D23CH

DX : 1101 0010 0011 1100

NOT : 0010 1101 1100 0011

B. ① AL = 1D H

XOR 79H

AL : 0001 1101

XOR 0111 1001

0110 0100

AL → 0110 0100 = 68 H

② CL = 4H

DX = EEFF H

DX : 1110 1110 1111 1111

1111 1110 1110 1111 = FEEF H #

③ BX = CD67H

DX = EEFFH

BX : 1100 1101 0110 0111

DX : 1110 1110 1111 1111

1110 1111 1111 1111 = EFFF H #

④ AX = A11D H, BX = CD67H

AX : 1010 0001 0001 1101

BX : 1100 1101 0110 0111

1000 0001 0000 0101 = 8105 H #

⑤ BH = CD

CD : 1100 1101

100 11011 #

c. ① SI default segment = DS , AH = 25 H

DS = 2000 H , locate 20000 H

```
  20000
+ 4000
-------
  24000 H → Location
```

24000 H = AH = 25 H

② DI = 5000H , default segment = DS = 2000H

BX = 6080H

```
  20000 H
+  5000 H
---------
  25000 H
+     6 H
---------
  25006 H
```

25006 H = BL = 80H

25007 H = BH = 60H

③

```
  20000 H
   4000 H
+  6080 H
---------
  2A080 H
      7
-     8 H
---------
  2A078 H
```

2A078 H = AL = FFH

2A079 H = AH = 25H

④ DI = 5000H , BX = 6080H , 28H , CX

```
  20000 H
   5000 H
   6080 H
+    28 H
---------
  2B0A8 H
```

2B0A8 H = CL = 91H

2B0A9 H = CH = 87H

⑤ BP = 7000 H , SI = 4000 H ,

SS = 3000 H , DS = 2000 H

$$\begin{array}{r} 30000\ H \\ 7000\ H \\ \hline 20000\ H \\ 4000\ H \\ +\quad 10\ H \\ \hline 5B010\ H \end{array}$$

5B010 H = DL = 99H

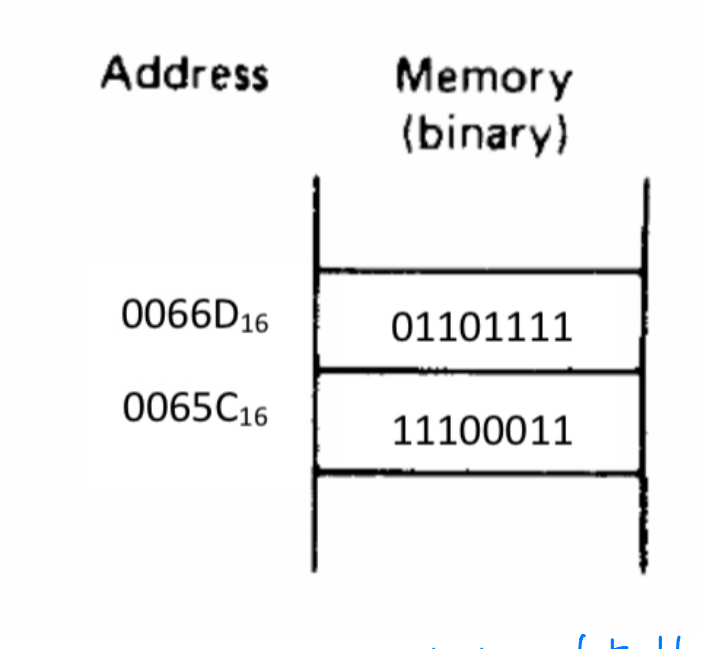
5B011 H = DH = 12H

1 byte = 8 bits

2 byte = 1 word = 16 bits

D. Fill in the blank with the correct answer;

1. There are 16 bits in word.
2. Double word consist of 32 byte.
3. 16-bit is equal to 2 byte.
4. Bytes and words at even-addressed boundaries can be accessed by one bus cycle.
5. Bytes and words at odd-addressed boundaries require two bus cycles to access.
6. A word of data stored at an even address boundary is called Even Bank.
7. A word of data stored at an odd address boundary is called Odd Bank.
8. 8086 processor has a 20-line address bus, thus can address up to 20 bit or 220 memory locations.
9. A pointer is a double word used to access data or code in memory. The higher address word represents the segment base address while the lower address word represents the offset.



E.

$0110\ 1111_2 = 6FH$, $1110\ 0011_2 = E3H$

1. What is the data shown in the Figure above? Express the result in hexadecimal form.

2. Is it stored at an even or odd addressed word boundary? Is it aligned or misaligned word of data?

$0065C_{16}$ is odd addressed word boundary. It is misaligned word of data.

F.

Address	Memory (hexadecimal)	
$0000B_{16}$	0110 0011	63H
$0000A_{16}$	1110 1000	E8H
00009_{16}	1010 1010	AAH
00008_{16}	0100 0001	41H

From figure above, determine;

1. What is the higher address word 63E8H = $0110\ 0011_2$
2. What us the lower address word. AA41H = $1010\ 1010\ 0100\ 0001_2$
3. What is the complete double word in hexadecimal 63E8H , AA41H
4. Is it stored at an even or odd addressed word boundary? Is it aligned or misaligned word of data?
   Even addressed word boundary. Aligned.
5. What is the segment base address and offset address?
   Segment base address = higher address word = 63E8H.
   offset address = lower address word = AA41H

G. Define the following; AX, BX, CX, DX,SP,BP,SI,DI,CS,DS,SS,ES

H. Calculate the physical address corresponding to logical address A1B0H in the stack segment. Repeat for logical address 7C4DH in the code segment. Given register SS = 1234H and CS = 457BH

(G) AX, BX, CX and DX are general purpose register.
AX is accumulator register.
BX is base register. CX is counter register. DX is data register.
SP, BP are pointer register. BP is base pointer. SP is stack pointer.
SI and DI are index register. SI is source index, DI is destination index.
CS, DS, SS and ES are segment register. CS is code segment register. DS is data segment register. SS is stack segment register.

(H)

$$\begin{array}{r} A1B00\,H \\ +\ 1234\,H \\ \hline A2D34\,H \end{array}$$

$$\begin{array}{r} {}^{1}7{}^{1}C4D\,H \\ +\ 457B\,H \\ \hline B1B8\,H \end{array}$$