2022 Digital IC Design Homework 3

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Simulation Result

Functional simulation	Pass/ Fail (encoder)	Pass/ Fail (decoder)	Gate-level simulation	Pass/ Fail (encoder)	Pass/ Fail (decoder)

(your pre-sim result) encoder/decoder img0

```
# cycle 0105c, expect(7,7,8) , get(7,7,8) >> Pass
# cycle 0105e, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Encoder.sv(250)
#    Time: 125760 ns  Iteration: 1  Instance: /testfixture_encoder
# 1

# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
```

(your post-sim result) encoder/decoder img0

```
cycle 00803, expect 0, get 0 >> Pass
cycle 00804, expect 8, get 8 >> Pass
--------- Decoding finished, ALL PASS ---------
** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
   Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
1
```

(your pre-sim result) encoder/decoder img1

```
# cycle 01002, expect(3,2,f) , get(3,2,f) >> Pass
# cycle 01004, expect(0,0,6) , get(0,0,6) >> Pass
# cycle 01006, expect(0,0,$) , get(0,0,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Encoder.sv(250)
#    Time: 123120 ns  Iteration: 1  Instance: /testfixture_encoder
# 1
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
```

(your post-sim result) encoder/decoder img1

```
# cycle 00803, expect f, get f >> Pass
#   == Decoding string "6"
# cycle 00804, expect 6, get 6 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
```

(your pre-sim result) encoder/decoder img2

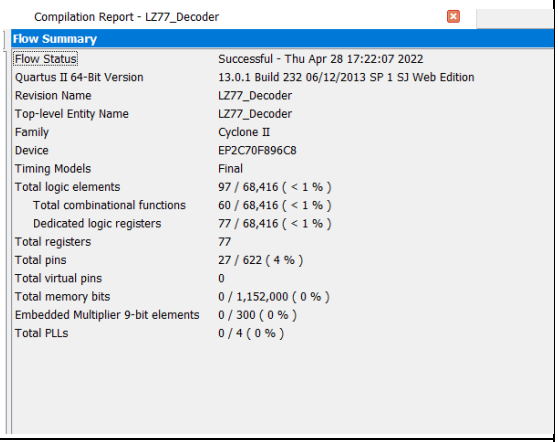
```
# cycle 00b46, expect(5,5,7) , get(5,5,7) >> Pass
# cycle 00b48, expect(5,7,6) , get(5,7,6) >> Pass
# cycle 00b4a, expect(7,7,7) , get(7,7,7) >> Pass
# cycle 00b4c, expect(7,6,$) , get(7,6,$) >> Pass
# ------------------------------------------------
# --------- Encoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Encoder.sv(250)
#    Time: 86820 ns  Iteration: 1  Instance: /testfixture_encoder
# 1

# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
```

(your post-sim result) encoder/decoder img2

```
# cycle 00802, expect 7, get 7 >> Pass
# cycle 00803, expect d, get d >> Pass
# cycle 00804, expect 7, get 7 >> Pass
# ------------------------------------------------
# --------- Decoding finished, ALL PASS ---------
# ------------------------------------------------
# ** Note: $finish    : C:/dic2022/HW3/tb_Decoder.sv(228)
#    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
# 1
# Break in Module testfixture_decoder at C:/dic2022/HW3/tb_Decoder.sv line 228
```

Synthesis Result	**encoder**	**decoder**
Total logic elements		97
Total memory bit		0
Embedded multiplier 9-bit element		0
Simulation time img0	125760 (ns)	61620(ns)
Simulation time img1	123120 (ns)	61620 (ns)

Simulation time img2	86820 (ns)	61620 (ns)
(your flow summary) encoder	(your flow summary) decoder 	

Compilation Report - LZ77_Decoder

Flow Summary

Flow Status	Successful - Thu Apr 28 17:22:07 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	LZ77_Decoder
Top-level Entity Name	LZ77_Decoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	97 / 68,416 (< 1 %)
Total combinational functions	60 / 68,416 (< 1 %)
Dedicated logic registers	77 / 68,416 (< 1 %)
Total registers	77
Total pins	27 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

Decode: 兩個 state READ(讀資料)資料存到 search，同時讀資料、shift、output 資料，END(把 finish 拉起來)

Encode: 分成 READ、FIRSET、RESULT、COMPARE，合成的時候 total login elements(102%)，這個問題還無法解決。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*