2022 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Clock width	19.0 (ns)	Gate-level simulation time	37191.595 (ns)

```
# ----------------------------------------------------------------
#
#     START!!! Simulation Start .....
#
# ----------------------------------------------------------------
#
#
#
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ----------------------------------------------------------------
#
# ** Note: $finish    : C:/dic2022/HW4/file/testfixture.v(176)
#    Time: 37183 ns  Iteration: 0  Instance: /TB_ELA
# 1
# Break in Module TB_ELA at C:/dic2022/HW4/file/testfixture.v line 176
```

```
# ----------------------------------------------------------------
#
#     START!!! Simulation Start .....
#
# ----------------------------------------------------------------
#
#
#
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ----------------------------------------------------------------
#
# ** Note: $finish    : C:/dic2022/HW4/file/testfixture.v(176)
#    Time: 37191595 ps  Iteration: 0  Instance: /TB_ELA
# 1
# Break in Module TB_ELA at C:/dic2022/HW4/file/testfixture.v line 176
```

Synthesis Result

Total logic elements	1016
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Summary

Flow Status	Successful - Fri May 27 11:15:19 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	1,016 / 68,416 (1 %)
Total combinational functions	801 / 68,416 (1 %)
Dedicated logic registers	574 / 68,416 (< 1 %)
Total registers	574
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

第一次讀兩個 row 存到 image_buffer_row_one 跟 image_buffer_row_two (REQUEST)，計算 D1 D2 D3(Interpolation)，找出最小(MIN)，相加除 2 寫進 memory(WRITE)，跳到(REQUEST)從這次開始只讀一個 row，新的值寫進 image_buffer_row_two，原本 image_buffer_row_two 寫進 image_buffer_row_one，計算 D1 D2 D3(Interpolation)，找出最小(MIN)，相加除 2 寫進 memory(WRITE)。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*