# ECEN 325 Lab 8: BJT Amplifier Configurations

## Objectives

The purpose of the lab is to examine the properties of the BJT amplifier configurations and investigate their small-signal performance, with the emphasis on the design of BJT amplifiers.

## Introduction

### Superposition Theorem - Linear and Nonlinear Circuit Solution

The superposition theorem states that in a linear circuit with multiple sources, any branch current or node voltage is the sum of the currents or voltages produced by each source applied individually. Linear components include resistors, capacitors, inductors, and controlled sources, therefore any combination of these elements yield a linear circuit. Figure 1 shows the application of superposition theorem to solve linear circuits, where the DC and AC solutions are obtained by applying only DC and AC sources, respectively, providing the total solution as $V_o = V_{o,dc} + V_{o,ac}$.

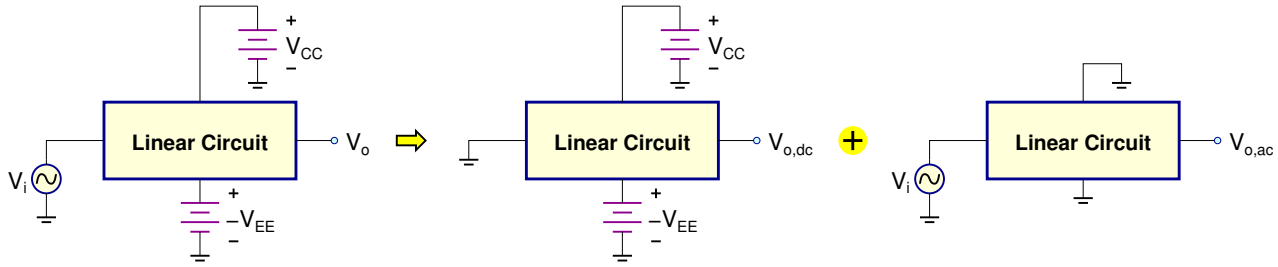



Figure 1: Application of the superposition theorem to linear circuits

The superposition theorem can be extended to solve nonlinear circuits under certain restrictions, which are known as small-signal conditions. The DC solution usually requires using simplified DC models for the nonlinear devices (such as using the constant-voltage-drop model for a diode or a base-emitter junction, instead of the exponential model), and can be obtained by applying only DC sources. AC small-signal model parameters are dependent on the DC solution, as well as other device parameters. Once the linearized circuit using AC small-signal models is constructed, AC solution can be obtained by applying only AC sources. Figure 2 illustrates extension of the superposition theorem to nonlinear circuits, where the approximate solution is $V_o \approx V_{o,dc} + V_{o,ac}$.

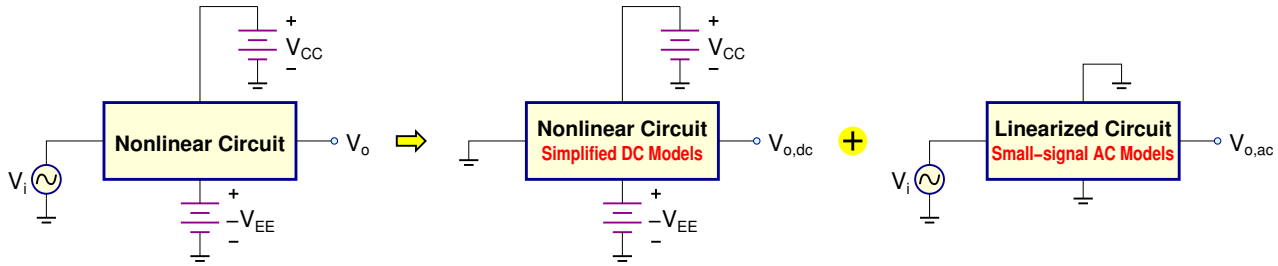



Figure 2: Extension of the superposition theorem to nonlinear circuits

### BJT Small-Signal AC models

BJTs are nonlinear devices, where the collector current is an exponential function of the base-emitter voltage. Typical BJT amplifiers include DC sources providing the DC bias, as well as AC sources as the signals to be amplified. Extension of superposition to BJT amplifiers requires finding the DC solution first, where the BJTs must be biased in the **active** region. Figure 3 shows the AC small-signal models for NPN and PNP BJTs in the active region.

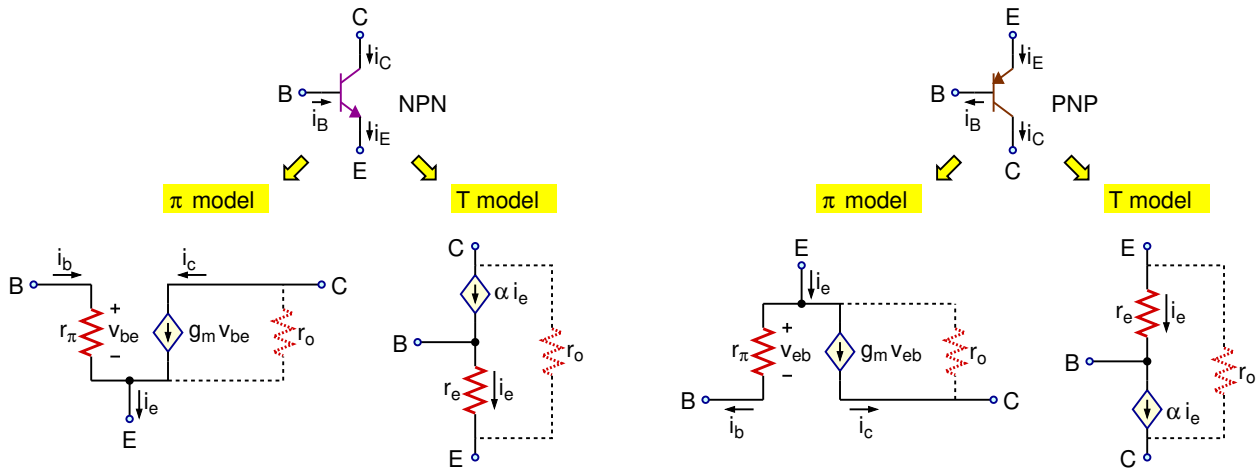


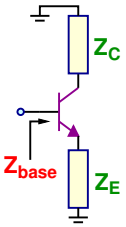
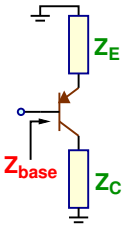
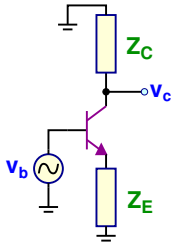
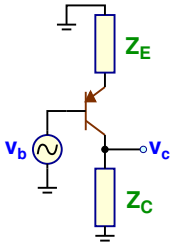
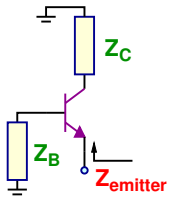
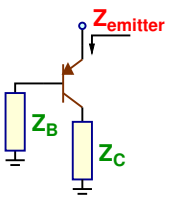
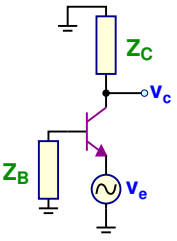
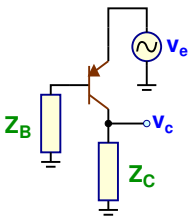
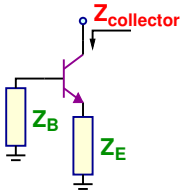
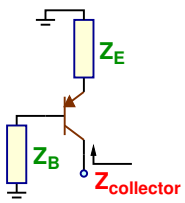
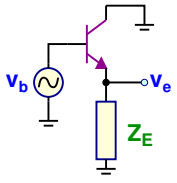
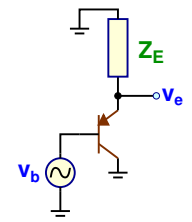

Figure 3: Small-signal AC models for NPN and PNP BJTs

Small-signal parameters in Fig. 3 can be calculated as

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_e = \frac{V_T}{I_E} \qquad \alpha = \frac{\beta}{\beta+1} \qquad r_o = \frac{V_A}{I_C} \tag{1}$$

where $I_C$ and $I_E$ are DC collector and emitter currents, respectively, $V_T$ is the thermal voltage (approximately 25mV at room temperature), $\beta$ is the current gain of the transistor (around 100 or larger), and $V_A$ is the Early Voltage (around 100V). For typical discrete BJT circuit implementations, $r_o$ will not have a significant impact, therefore will be ignored. For small-signal AC analysis, $\pi$-model and T-model provide identical results, however the T-model allows more intuitive analysis with simpler calculations. Table 1 shows node impedances and node-to-node gains for generic BJT configurations, which are derived by substituting the transistor with its T-model, where $r_o = \infty$.

Table 1: BJT Node Impedances and Node-to-Node Gains when $r_o = \infty$

| NPN | PNP | Impedance | NPN | PNP | Gain |
|---|---|---|---|---|---|
|  |  | $Z_{base} = (\beta+1)(r_e+Z_E)$ |  |  | $\frac{v_c}{v_b} = \frac{-\alpha Z_C}{r_e + Z_E}$ |
|  |  | $Z_{emitter} = r_e + \frac{Z_B}{\beta+1}$ |  |  | $\frac{v_c}{v_e} = \frac{\alpha Z_C}{Z_{emitter}}$ |
|  |  | $Z_{collector} = \infty$ |  |  | $\frac{v_e}{v_b} = \frac{Z_E}{r_e + Z_E}$ |

## BJT Amplifier Configurations

### Common-Emitter Configuration

Figures 4 and 5 show the common-emitter configurations for NPN and PNP BJTs, respectively. Analysis of this configuration yields

$$\textbf{DC:} \qquad V_{RB2} \approx \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} \qquad V_{RE} = V_{RB2} - 0.7 \qquad I_E = \frac{V_{RE}}{R_E} \approx I_C \tag{2}$$

$$\textbf{AC:} \qquad A_v = \frac{V_{o,ac}}{V_i} \approx -\frac{R_C}{r_e + (R_E \parallel R_G)} \qquad R_i = R_{B1} \parallel R_{B2} \parallel (\beta+1)(r_e + (R_E \parallel R_G)) \qquad R_o = R_C \tag{3}$$

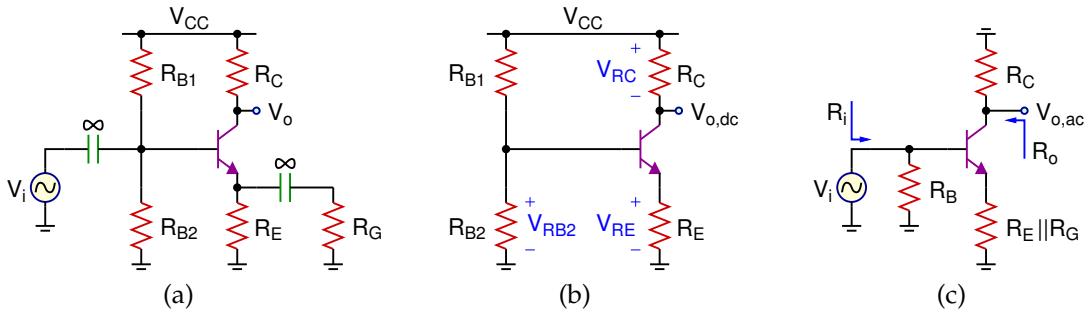



Figure 4: (a) NPN Common-Emitter Configuration (b) DC equivalent (c) AC equivalent

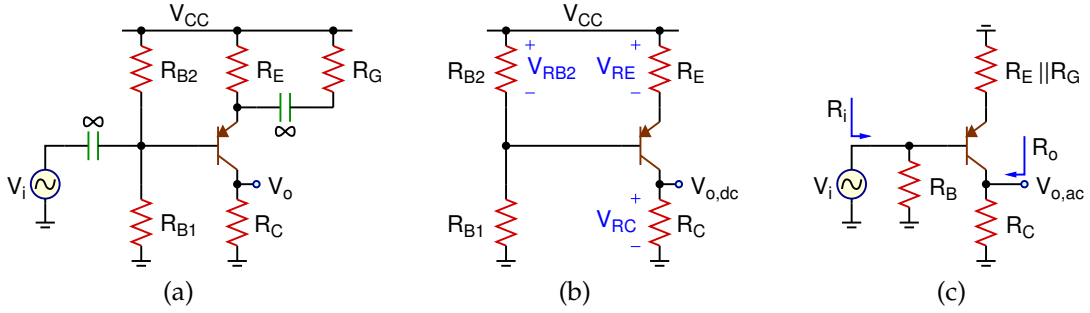



Figure 5: (a) PNP Common-Emitter Configuration (b) DC equivalent (c) AC equivalent

Typical design specifications for the common-emitter configuration includes:

- 0-to-peak unclipped output voltage swing: $\hat{V}_o$
- Voltage gain: $A_v = \dfrac{V_{o,ac}}{V_i}$
- Input and output resistances: $R_i$ and $R_o$
- THD at the maximum output level
- Sensitivity to $\beta$ and $|V_{BE}|$ variations

Based on the typical specifications, design procedure for the common-emitter amplifier in Figs. 4 and 5 can be given as follows:

- Choose $V_{RE} \geq 1V$ to have less than 10% variation of $I_C$ when $V_{BE} = 0.7 \pm 0.1$.
- To have an unclipped output swing of $\hat{V}_o$, $V_{RC}$ should be chosen such that $(V_{CC} - \hat{V}_o - V_{RE} - 0.2) \geq V_{RC} \geq \hat{V}_o$. Choice of $V_{RC}$ does not only affect the available signal swing at the output, but also determines the available gain as well as the linearity of the amplifier as follows:

☆ $R_G = 0 \Rightarrow |A_v| = \dfrac{R_C}{r_e} = \dfrac{V_{RC}/I_C}{V_T/I_C} = \dfrac{V_{RC}}{V_T} \Rightarrow |A_v|_{max} = \dfrac{V_{RC,max}}{V_T} = \dfrac{V_{CC} - \hat{V}_o - V_{RE} - 0.2}{V_T}$

☆ Small-signal condition: $\hat{v}_{be} = \dfrac{\hat{V}_o}{V_{RC}} V_T \ll V_T \Rightarrow \hat{V}_o \ll V_{RC}$

To maximize the available gain and linearity, choose $V_{RC} = V_{RC,max} = V_{CC} - \hat{V}_o - V_{RE} - 0.2$
Note that $V_{CE,sat} \approx 0.2V$ is an approximation, you may increase it up to $0.5V$ to avoid clipping in case operating point shifts due to resistor tolerances.

➪ Choose $I_C$ such that

$$I_C \leq \frac{\beta}{R_i} \frac{1}{\dfrac{N}{V_{RE}+0.7} + \dfrac{N}{V_{CC}-V_{RE}-0.7} + \dfrac{|A_v|}{V_{RC}}}$$

where $R_i$ is the minimum input resistance specified, and $N \approx \dfrac{I_{RB1}}{I_B} \geq 10$ for $\beta$-insensitive design.
Note that as long as $V_{RC}$ and $V_{RE}$ are kept the same, choice of $I_C$ does not change the output swing or the available gain, but affects the input and output resistances, as well as the resistor values in the amplifier.

➪ Find the resistor values

$$R_C = \frac{V_{RC}}{I_C} \quad R_E = \frac{V_{RE}}{I_C} \quad R_G \approx \frac{R_C}{|A_v|} - r_e \quad R_{B1} = \frac{\beta(V_{CC} - V_{RE} - 0.7)}{NI_C} \quad R_{B2} = \frac{\beta(V_{RE} + 0.7)}{NI_C}$$

➪ Simulate the circuit for the final adjustment of $R_G$.

**Common-Collector Configuration**

Figures 6 and 7 show the common-collector configurations for NPN and PNP BJTs, respectively. Also known as the emitter-follower, analysis of this configuration yields

$$\textbf{DC:} \quad V_{RB2} \approx \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} \qquad V_{RE} = V_{RB2} - 0.7 \qquad I_E = \frac{V_{RE}}{R_E} \approx I_C \tag{4}$$

$$\textbf{AC:} \quad A_v = \frac{V_{o,ac}}{V_i} = \frac{R_E}{r_e + R_E} \qquad R_i = R_{B1} \parallel R_{B2} \parallel (\beta+1)(r_e + R_E) \qquad R_o = R_E \parallel r_e \tag{5}$$

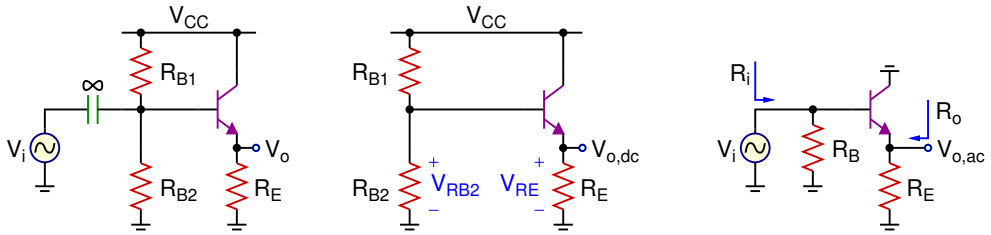



Figure 6: (a) NPN Common-Collector (Emitter-Follower) Configuration (b) DC equivalent (c) AC equivalent

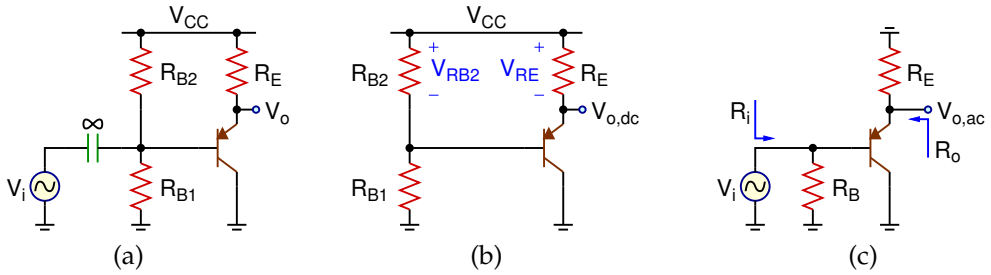



Figure 7: (a) PNP Common-Collector (Emitter-Follower) Configuration (b) DC equivalent (c) AC equivalent

In typical multi-stage amplifiers, emitter follower is directly connected to a gain stage, such as a common-emitter amplifier, without the extra biasing resistors $R_{B1}$ and $R_{B2}$. Therefore, DC voltage levels in an emitter follower is typically dependent on the previous amplifier stage.

**Common-Base Configuration**

Figures 8 and 9 show the common-base configurations for NPN and PNP BJTs, respectively. Analysis of this configuration yields

$$\textbf{DC:} \qquad V_{RB2} \approx \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} \qquad V_{RE} = V_{RB2} - 0.7 \qquad I_E = \frac{V_{RE}}{R_E} \approx I_C \tag{6}$$

$$\textbf{AC:} \qquad A_v = \frac{V_{o,ac}}{V_i} = \frac{R_C}{r_e} \qquad R_i = R_E \parallel r_e \qquad R_o = R_C \tag{7}$$

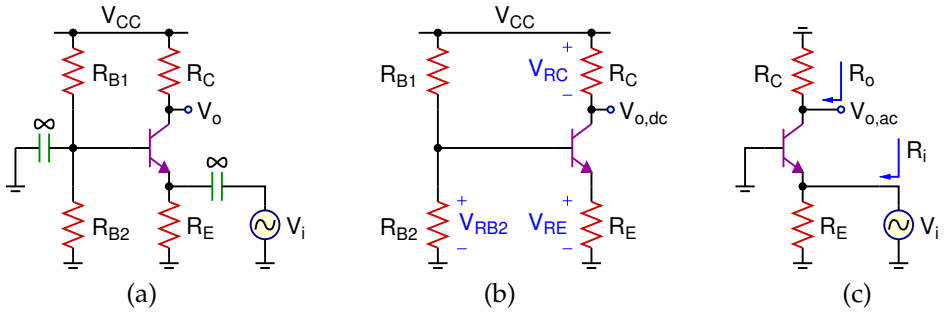



Figure 8: (a) NPN Common-Base Configuration (b) DC equivalent (c) AC equivalent

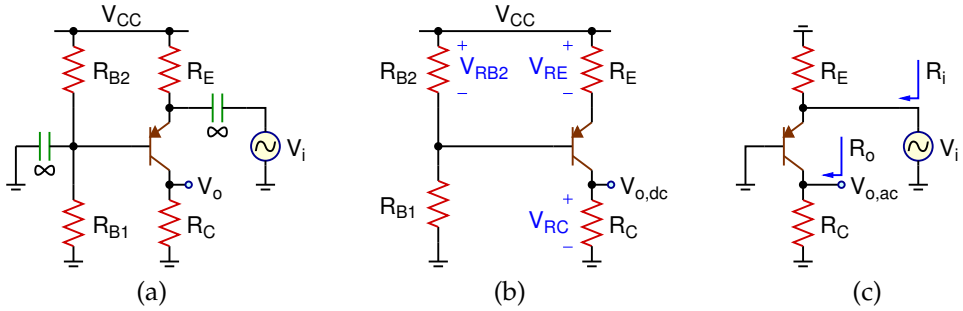



Figure 9: (a) PNP Common-Base Configuration (b) DC equivalent (c) AC equivalent

Common-base stages are typically used in cascode or folded-cascode amplifiers, where a common-base stage is directly following a common-emitter amplifier.

# Calculations

1. Design the common-emitter amplifier in Fig. 4(a) with the following specifications:

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 5V |
| 0-to-Peak Output Swing, $\hat{V}_o$ | $\geq 1V$ |
| Voltage Gain, $\lvert A_v \rvert$ | 25 |
| Input Resistance, $R_i$ | $\geq 2k\Omega$ |
| Output Resistance, $R_o$ | $\leq 1.8k\Omega$ |
| THD for 5kHz 1V (0-to-peak) Sine Wave Output Voltage, $V_o$ | $\leq 4\%$ |
| Relative Variation of $I_C$ for $V_{BE} = 0.7 \pm 0.1V$ | $\leq 10\%$ |
| Transistor's Current Gain, $\beta$ | $\geq 100$ |

   Show your design procedure and all your calculations. Your design should be insensitive to $\beta$ variations.

2. Using the same $R_{B1}$, $R_{B2}$ and $R_E$ values from your common-emitter amplifier, calculate $A_v$, $R_i$ and $R_o$ for the emitter follower in Fig. 6.

3. Using the same $R_{B1}$, $R_{B2}$, $R_C$ and $R_E$ values from your common-emitter amplifier, calculate $A_v$, $R_i$ and $R_o$ for the common-base amplifier in Fig. 8.

## Simulations

**For all simulations, provide screenshots showing the schematics and the plots with the simulated values properly labeled.**

1. Draw the common-emitter amplifier schematics in Figs. 4(a) and 5(a) using the calculated component values and 2N3904 and 2N3906 transistors. For both circuits,
   - **(a)** Perform **DC operating point** or **interactive simulation** to obtain the **DC solution** for $V_{RB2}$, $V_{RE}$, $V_{RC}$, $V_{o,dc}$ and $I_C$.
   - **(b)** Perform **AC simulation** to obtain $A_v$, $R_i$ and $R_o$.
   - **(c)** Apply a 5kHz 40mV sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using **transient simulation**. Perform **Fourier simulation** to measure the **total harmonic distortion (THD)** on the output waveform.
   - **(d)** Increase the input amplitude to measure the clipping levels at the output voltage $V_o$.
2. Draw the emitter-follower schematics in Figs. 6(a) and 7(a) using the calculated component values and 2N3904 and 2N3906 transistors. For both circuits,
   - **(a)** Perform **DC operating point** or **interactive simulation** to obtain the **DC solution** for $V_{RB2}$, $V_{RE}$ and $I_C$.
   - **(b)** Perform **AC simulation** to obtain $A_v$, $R_i$ and $R_o$.
   - **(c)** Apply a 5kHz 0.8V sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using **transient simulation**. Perform **Fourier simulation** to measure the **total harmonic distortion (THD)** on the output waveform.
3. Draw the common-base amplifier schematics in Figs. 8(a) and 9(a) using the calculated component values and 2N3904 and 2N3906 transistors. For both circuits,
   - **(a)** Perform **DC operating point** or **interactive simulation** to obtain the **DC solution** for $V_{RB2}$, $V_{RE}$, $V_{RC}$, $V_{o,dc}$ and $I_C$.
   - **(b)** Perform **AC simulation** to obtain $A_v$, $R_i$ and $R_o$.
   - **(c)** Apply a 5kHz 8mV sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using **transient simulation**. Perform **Fourier simulation** to measure the **total harmonic distortion (THD)** on the output waveform.

## Measurements

**For all measurements, provide screenshots showing the plots with the measured values properly labeled.**

1. Build the common-emitter amplifiers in Figs. 4(a) and 5(a) using the simulated component values and 2N3904 and 2N3906 transistors. For both circuits,
   - **(a)** Measure the **DC** values for $V_{RB2}$, $V_{RE}$, $V_{RC}$, $V_{o,dc}$ and $I_C$ using the **voltmeter** or **scope**.
   - **(b)** Measure $A_v$, $R_i$ and $R_o$ using the **network analyzer**.
   - **(c)** Apply a 5kHz 40mV sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using the **scope**. Measure the **total harmonic distortion (THD)** on the output waveform using the **spectrum analyzer**.
   - **(d)** Increase the input amplitude to measure the clipping levels at the output voltage $V_o$ using the **scope**.
2. Build the emitter-follower circuits in Figs. 6(a) and 7(a) using the simulated component values and 2N3904 and 2N3906 transistors. For both circuits,
   - **(a)** Measure the **DC** values for $V_{RB2}$, $V_{RE}$ and $I_C$ using the **voltmeter** or **scope**.
   - **(b)** Measure $A_v$, $R_i$ and $R_o$ using the **network analyzer**.
   - **(c)** Apply a 5kHz 0.8V sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using the **scope**. Measure the **total harmonic distortion (THD)** on the output waveform using the **spectrum analyzer**.

3. Build the common-base amplifiers in Figs. 8(a) and 9(a) using the simulated component values and 2N3904 and 2N3906 transistors. For both circuits,

   **(a)** Measure the **DC** values for $V_{RB2}$, $V_{RE}$, $V_{RC}$, $V_{o,dc}$ and $I_C$ using the **voltmeter** or **scope**.

   **(b)** Measure $A_v$, $R_i$ and $R_o$ using the **network analyzer**.

   **(c)** Apply a 5kHz 8mV sine wave signal to the input $V_i$ and obtain the **time-domain waveforms** for the input and output voltages using the **scope**. Measure the **total harmonic distortion (THD)** on the output waveform using the **spectrum analyzer**.

## Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

## Demonstration

1. Build the common-emitter amplifier circuits in Figs. 4(a) and 5(a) on your breadboard and bring it to your lab session. Be prepared to convert these two circuits into emitter followers in Figs. 6(a) and 7(a), and common-base amplifiers in Figs. 8(a) and 9(a).
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. For the common-emitter amplifiers in Figs. 4(a) and 5(a):
   - Measure $A_v$, $R_i$, and $R_o$ using the network analyzer.
   - Apply a 5kHz 40mV sine wave input and show the time-domain output voltage using the scope.
   - With the 5kHz 40mV sine wave input, measure the THD at the output using the spectrum analyzer.
5. Convert Figs. 4(a) and 5(a) to Figs. 6(a) and 7(a) by short-circuiting $R_C$ with a wire and removing the bypass capacitor at the emitter, then
   - Apply a 5kHz 0.8V sine wave input and show the time-domain waveforms at the input and the output using the scope.
6. Remove the wire short-circuiting $R_C$, add the bypass capacitor back to the emitter, remove $R_G$, and AC-ground the base through the capacitor to obtain the common-base amplifiers in Figs. 8(a) and 9(a), then
   - Apply a 5kHz 8mV sine wave input and show the time-domain waveforms at the input and the output using the scope.