ECEN 325 Lab 7: Characterization and DC Biasing of the BJT

Objectives

The purpose of this lab is to characterize NPN and PNP bipolar junction transistors (BJT), and to analyze and design DC biasing circuits to set the DC operating point of BJTs.

Introduction

Figure 1 shows typical symbols for the NPN and PNP BJTs. Depending on the applied DC bias, BJT has three regions of operation:

- **Cutoff Region:** If both base-emitter and base-collector junctions are reverse biased, the BJT enters the cutoff region. All terminal currents are extremely small, and the transistor is off.
- **Active Region:** The base-emitter junction is forward biased, and the base-collector junction is reverse biased to make a BJT operate in the active region. The active region is used to design a linear amplifier.
- **Saturation Region:** When both the base-emitter and base-collector junctions are forward biased, the BJT enters the saturation region.

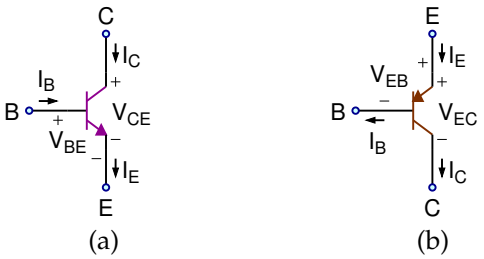


Figure 1: Bipolar junction transistor (BJT) (a) NPN (b) PNP

In the active region, the collector current (I_C) of NPN and PNP devices are exponential functions of base-emitter voltage (V_{BE}) and emitter-base voltage (V_{EB}), respectively, given by

$$I_{C,npn} = I_S e^{V_{BE}/V_T} \qquad I_{C,pnp} = I_S e^{V_{EB}/V_T} \tag{1}$$

where I_S is the saturation current and V_T is the thermal voltage, which is approximately 25mV at room temperature. For both NPN and PNP, the base current I_B is a small fraction of I_C, given by

$$I_B = \frac{I_C}{\beta} \tag{2}$$

and the emitter current I_E is the sum of the base and collector currents, given by

$$I_E = I_C + I_B = (\beta + 1) I_B = \frac{I_C}{\alpha} \tag{3}$$

where

$$\alpha = \frac{\beta}{\beta + 1} \tag{4}$$

β is known as the current gain of the transistor, which varies significantly with temperature, and it can be different between two transistors of the same type. Typical value of β is around 100, resulting in $\alpha = 0.99$.

BJT Characterization

Figure 2 shows a characterization circuit for an NPN BJT. To obtain I_C as a function of V_{BE}, V_1 is swept while V_2 is kept constant, resulting in the exponential function in Fig. 3(a). If V_1 is kept constant and V_2 is swept, I_C can be obtained as a function of V_{CE} as shown in Fig. 3(b).

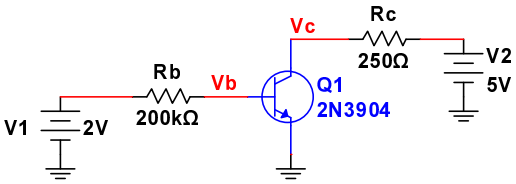
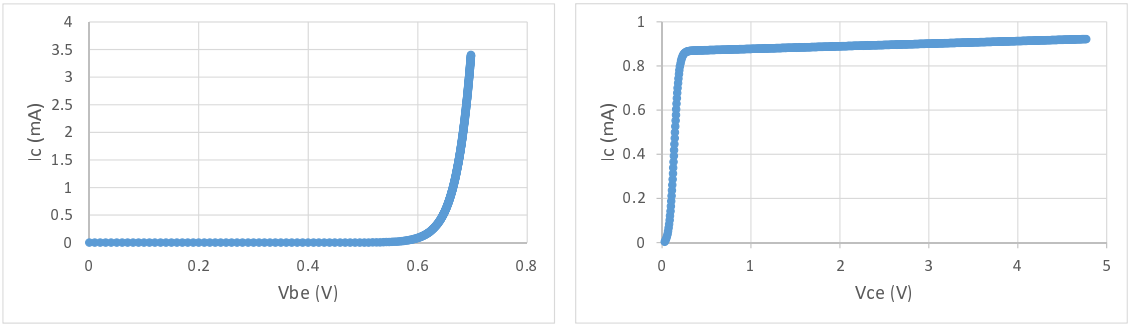


Figure 2: NPN BJT characterization circuit



(a) (b)

Figure 3: Collector current (I_C) of an NPN BJT as a function of (a) V_{BE} (b) V_{CE}

Characterization circuit for a PNP BJT is shown in Fig. 4. Keeping V_2 constant and sweeping V_1 provides I_C as an exponential function of V_{EB} as shown in Fig. 5(a). Sweeping V_2 while V_1 is kept constant provides the I_C vs. V_{EC} characteristics as shown in 5(b).

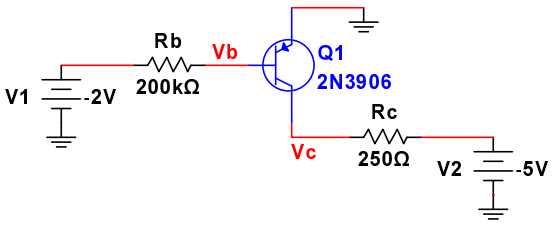
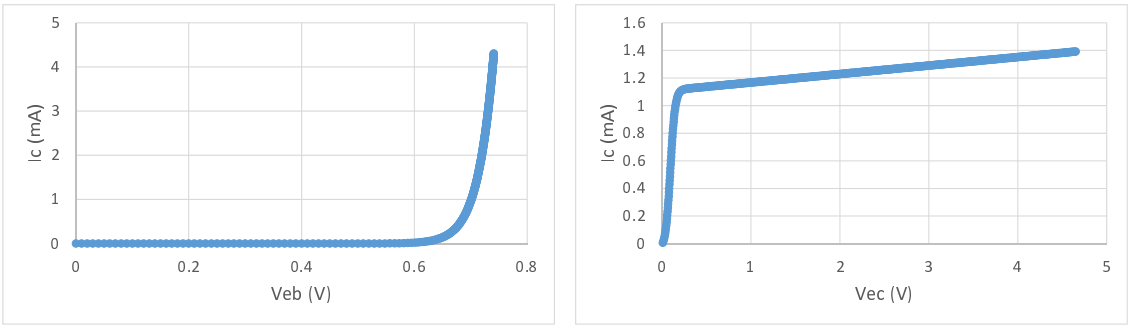


Figure 4: PNP BJT characterization circuit



(a) (b)

Figure 5: Collector current (I_C) of a PNP BJT as a function of (a) V_{EB} (b) V_{EC}

BJT DC Biasing - Resistive

Figures 6(a) and (b) show typical resistive biasing circuits for NPN and PNP transistors, respectively.

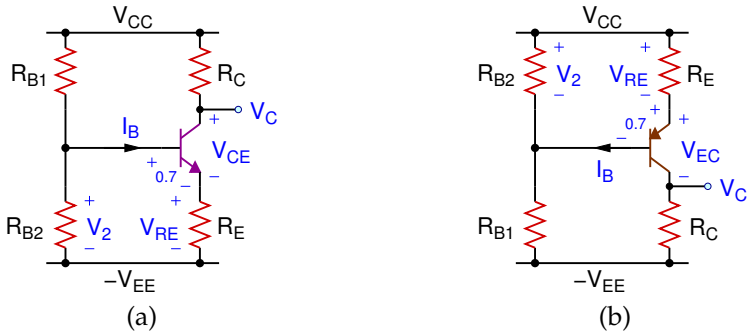


Figure 6: Resistive DC biasing circuit for (a) NPN (b) PNP

For each circuit in Figs. 6(a) and (b), assume that the transistor is active, and I_B is negligible, which means R_{B1} and R_{B2} form a voltage divider to set the V_2 voltage. Therefore, I_E and I_C can be found as

$$V_2 \approx \frac{R_{B2}}{R_{B1}+R_{B2}}(V_{CC}+V_{EE}) \;\Rightarrow\; I_E = \frac{V_2-0.7}{R_E} \approx I_C \tag{5}$$

All assumptions must be verified to complete the DC analysis. For the circuits in Figs. 6(a) and (b), I_B is negligible only if $I_B \ll I_{RB1}$, which requires

$$I_B = \frac{I_C}{\beta} \ll I_{RB1} \approx \frac{V_{CC}+V_{EE}}{R_{B1}+R_{B2}} \tag{6}$$

To verify that the NPN transistor is active, $V_{CE} \geq V_{CE,sat}$ should be satisfied as follows

$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C+R_E) \geq V_{CE,sat} \tag{7}$$

For the PNP transistor, active operation requires $V_{EC} \geq V_{EC,sat}$ as follows

$$V_{EC} = V_{CC} + V_{EE} - I_C R_C + R_E \geq V_{EC,sat} \tag{8}$$

where $V_{CE,sat} \approx V_{EC,sat} \approx 0.2V$

BJT DC Biasing - Current Source

An alternative method for BJT DC biasing is to use a current source connected to the emitter terminal, which directly sets the I_E current, and hence the I_C current. Figure 7(a) shows the DC biasing of an NPN BJT using a current source, which can be realized using the circuits in Fig. 7(b) or (c). Figure 8 shows the DC biasing circuit of a PNP BJT using a current source, as well as current source and current mirror realizations.

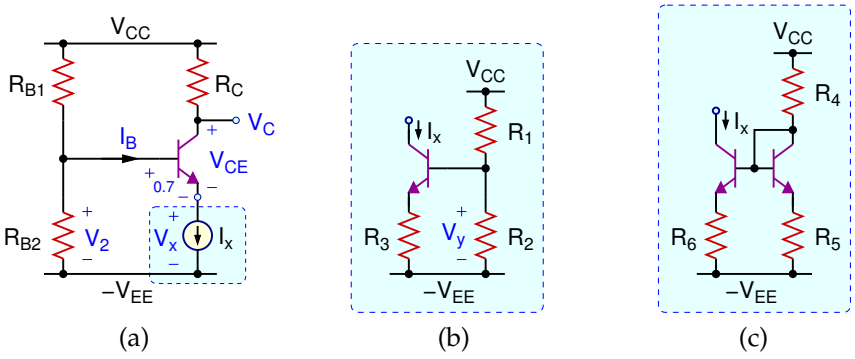


Figure 7: (a) DC biasing circuit for an NPN BJT using a current source (b) Current source (c) Current mirror

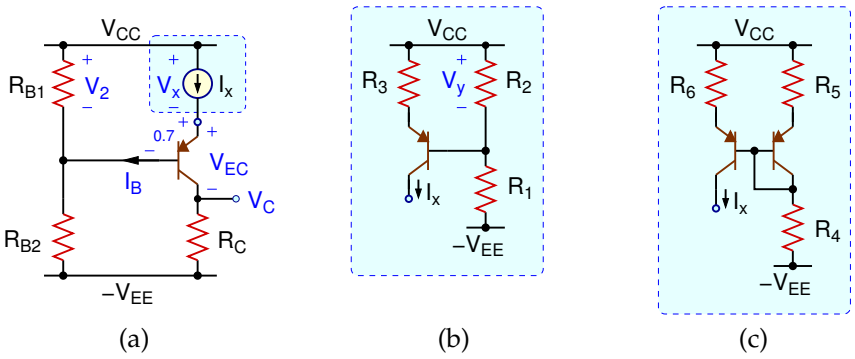


Figure 8: (a) DC biasing circuit for a PNP BJT using a current source (b) Current source (c) Current mirror

For the current sources in Figs. 7(b) and 8(b), I_x can be calculated as

$$V_y \approx \frac{R_2}{R_1 + R_2}(V_{CC} + V_{EE}) \;\Rightarrow\; I_x \approx \frac{V_y - 0.7}{R_3} \tag{9}$$

For the current mirrors in Figs. 7(c) and 8(c), assuming matching transistors and $R_5 = R_6$, I_x can be calculated as

$$I_x \approx \frac{V_{CC} + V_{EE} - 0.7}{R_4 + R_5} \tag{10}$$

All transistors in Figs. 7 and 8 are assumed to be active, and all I_B currents are assumed to be negligible. These assumptions need to be verified after finding the DC solution.

Calculations

1. Design the circuits in Figs. 6(a) and 6(b) with the following specifications:

NPN	
I_C	$1mA$
V_C	$3.5V$
V_{CE}	$\geq 1V$
V_{RE}	$\geq 1V$
V_{CC}	$5V$
V_{EE}	0
β	100
V_T	$25mV$
I_{supply}	$\leq 2mA$

PNP	
I_C	$1mA$
V_C	$1.5V$
V_{EC}	$\geq 1V$
V_{RE}	$\geq 1V$
V_{CC}	$5V$
V_{EE}	0
β	100
V_T	$25mV$
I_{supply}	$\leq 2mA$

For both circuits, DC biasing should be insensitive to variations in β and $|V_{BE}|$, and I_B currents should be designed to be negligible.

2. Design the circuits in Figs. 7(a) and 8(a) using the current sources in Figs. 7(b) and 8(b), respectively, with the following specifications:

NPN	
I_C	$2mA$
V_C	$3.5V$
V_{CE}	$\geq 1V$
V_x	$\geq 1.5V$
V_{CC}	$5V$
V_{EE}	0
β	100
V_T	$25mV$
I_{supply}	$\leq 5mA$

PNP	
I_C	$2mA$
V_C	$1.5V$
V_{EC}	$\geq 1V$
V_x	$\geq 1.5V$
V_{CC}	$5V$
V_{EE}	0
β	100
V_T	$25mV$
I_{supply}	$\leq 5mA$

For both circuits, DC biasing should be insensitive to variations in β and $|V_{BE}|$, and I_B currents should be designed to be negligible.

Simulations

For all simulations, provide screenshots showing the schematics and the plots with the simulated values properly labeled.

1. Draw the schematics for the NPN characterization circuit in Fig. 2 using the 2N3904 transistor
   - Perform a **DC sweep** of V_1 from 0 to 5V, while $V_2 = 5V$. Export the simulation data to Excel, and plot I_C as a function of V_{BE}.
   - Perform a **DC sweep** of V_2 from 0 to 5V, while $V_1 = 2V$. Export the simulation data to Excel, and plot I_C as a function of V_{CE}.
2. Draw the schematics for the PNP characterization circuit in Fig. 4 using the 2N3906 transistor
   - Perform a **DC sweep** of V_1 from -5V to 0, while $V_2 = -5V$. Export the simulation data to Excel, and plot I_C as a function of V_{EB}.
   - Perform a **DC sweep** of V_2 from -5V to 0, while $V_1 = -2V$. Export the simulation data to Excel, and plot I_C as a function of V_{EC}.
3. Draw the schematics in Figs. 6(a) and 6(b) using the calculated component values and 2N3904 and 2N3906 transistors. For both circuits, perform **DC operating point** or **interactive simulation** to obtain the **DC solution** for I_C, V_C, V_{RE} and V_2.
4. Draw the schematics in Figs. 7(a) and 8(a) using the current sources in Figs. 7(b) and 8(b), respectively, with the calculated component values and 2N3904 and 2N3906 transistors. For both circuits, perform **DC operating point** or **interactive simulation** to obtain the **DC solution** for I_C, V_C, V_2, V_x and V_y.

Measurements

For all measurements, provide screenshots showing the plots with the measured values properly labeled.

1. Build the NPN characterization circuit in Fig. 2 using the 2N3904 transistor
   - Apply a ramp signal from 0 to 5V at 1Hz for V_1 while $V_2 = 5V$. Export the voltage measurements from the **scope** to Excel, and plot I_C as a function of V_{BE}.
   - Apply a ramp signal from 0 to 5V at 1Hz for V_2 while $V_1 = 2V$. Export the voltage measurements from the **scope** to Excel, and plot I_C as a function of V_{CE}.
2. Build the PNP characterization circuit in Fig. 4 using the 2N3906 transistor
   - Apply a ramp signal from -5V to 0 at 1Hz for V_1 while $V_2 = -5V$. Export the voltage measurements from the **scope** to Excel, and plot I_C as a function of V_{EB}.
   - Apply a ramp signal from -5V to 0 at 1Hz for V_2 while $V_1 = -2V$. Export the voltage measurements from the **scope** to Excel, and plot I_C as a function of V_{EC}.
3. Build the circuits in Figs. 6(a) and 6(b) using the calculated component values and 2N3904 and 2N3906 transistors. For both circuits, measure the **DC** values for I_C, V_C, V_{RE} and V_2 using the **voltmeter** or **scope**.
4. Build the circuits in Figs. 7(a) and 8(a) using the current sources in Figs. 7(b) and 8(b), respectively, with the calculated component values and 2N3904 and 2N3906 transistors. For both circuits, measure the **DC** values for I_C, V_C, V_2, V_x and V_y using the **voltmeter** or **scope**.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Build the circuits in Figs. 2, 4, 6(a), 6(b), 7(a)&(b) and 8(a)&(b) on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. For the NPN characterization circuit in Fig. 2:
   - Apply a ramp 0 to 5V at 1Hz for V_1 while $V_2 = 5V$, and export the measurements from scope to Excel.
   - Plot I_C as a function of V_{BE} in Excel.
5. For the PNP characterization circuit in Fig. 4:
   - Apply a ramp -5V to 0 at 1Hz for V_2 while $V_1 = -2V$, and export the measurements from scope to Excel.
   - Plot I_C as a function of V_{EC} in Excel.
6. For the resistive NPN and PNP biasing circuits in Figs. 6(a) and 6(b):
   - Measure the DC voltages V_C, V_B, V_E.
   - Calculate I_C from the voltage measurements.
7. For the current-source NPN and PNP biasing circuits in Figs. 7(a)&(b) and 8(a)&(b):
   - Measure the DC voltages V_C, V_B, V_E for both transistors.
   - Calculate I_C from the voltage measurements.