ECEN 325 Lab 9: BJT Amplifier Design

Objectives

The purpose of this experiment is to design a multi-stage BJT amplifier based on a list of specifications.

Introduction

Design of an amplifier typically requires multiples of stages to satisfy all specifications, so a system-level evaluation of the requirements is necessary to determine how many and what type of stages will be needed. Based on the gain and output swing requirements, the number of gain stages can be estimated. Depending on the load resistor, adding a buffer may become necessary to preserve the gain. If performed accurately, the initial assessment may be sufficient to determine the overall topology, but it usually takes a few iterations to complete the design.

Figure 1 shows two versions of two-stage amplifiers composed of a gain stage and a buffer. Assuming $R_{i2} \ll R_C$, the maximum available gain for these circuits can be determined as V_{RC}/V_T when R_G is zero. The gain can always be reduced by increasing R_G, but cannot be increased beyond $A_{v,max} = V_{RC,max}/V_T$, where $V_{RC,max} = V_{CC} - V_{RE} - \hat{V}_o - |V_{CE,sat}|$. Therefore, if the gain specification is higher than $A_{v,max}$, an extra gain stage is needed. The buffer stage is usually necessary when the load resistor is small, i.e., a few hundreds of ohms or smaller. Driving such a low resistance directly from the amplifier stage significantly reduces the gain or requires a gain stage with a very high power dissipation.

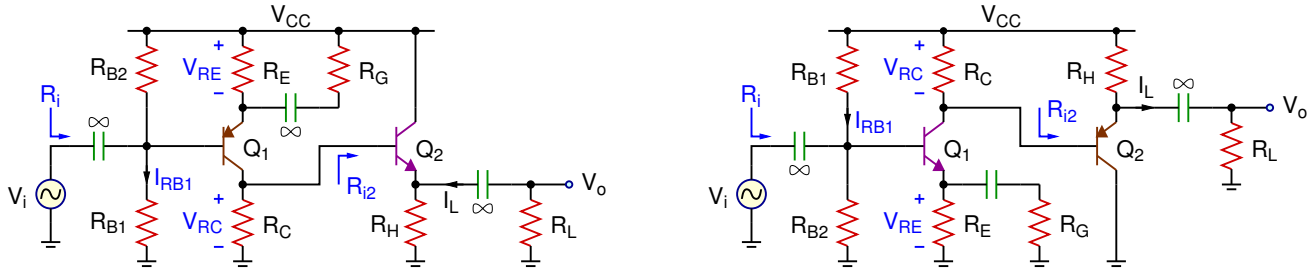

Figure 1: Two-stage BJT amplifier

Assuming that one gain stage followed by a buffer is sufficient for the design requirements, the circuits in Fig. 1 can be used as a starting point. Typical specifications include, but not limited to:

- **0-to-peak output swing:** $\hat{V}_o$
- **Gain:** $A_v = A_{v1}A_{v2}$ (where A_{v1} is the amplifier gain and A_{v2} is the buffer gain)
- **Input resistance:** R_i
- **Load resistance:** R_L
- **Linearity:** $\hat{v}_{be1} \ll V_T$
- **β-insensitivity:** $I_{RB1} \gg I_{B1}$, $I_{C1} \gg I_{B2}$
- **V_{BE}-insensitivity:** $V_{RE} \gg 0.1V$

Using one of the circuits in Fig. 1, the design procedure can be given as follows:

- Assume $A_{v2} \approx 1$ and $R_{i2} \gg R_C$, which is necessary to make the overall gain insensitive to β, as R_{i2} is directly dependent on β.
- Choose $V_{RE} \gg 0.1V$, which requires $V_{RE} \geq 1V$. Smaller values of V_{RE} cause the DC biasing to be sensitive to variations of V_{BE}, whereas larger values decrease the available output swing.

- Since the buffer gain A_{v2} is assumed to be close to unity, the AC signal magnitudes at the output, at the emitter of Q_2, and at the collector of Q_1 will be similar, where the main difference among these voltages will be their DC levels. To avoid voltage clipping, V_{RC} should be chosen such that

$$V_{CC} - \hat{V}_o - V_{RE} - |V_{CE,sat}| \geq V_{RC} \geq \hat{V}_o$$

  To maximize the available gain and linearity, V_{RC} should be maximized, however the value of $|V_{CE,sat}|$ can be chosen slightly larger (0.3 to 0.5V) than the typical value of 0.2V to account for variations in the circuit, as well as the small AC signal content at V_{RE}.

- The output voltage is a sine wave with the amplitude $\hat{V}_o$, therefore the maximum value of I_L in Fig. 1 is $\hat{V}_o/R_L$. When I_L reaches its maximum level, the voltage drop on R_H reaches its minimum. Since I_{E2} is always a positive current (leaving the emitter for NPN, or entering the emitter for PNP), the current on R_H must always be larger than I_L to avoid current clipping. Therefore, R_H should be chosen such that

$$\frac{V_{RC} - 0.7 - \hat{V}_o}{R_H} \geq \frac{\hat{V}_o}{R_L}$$

  Once R_H is chosen, I_{C2} can be determined from

$$I_{C2} = \frac{V_{RC} - 0.7}{R_H}$$

- The maximum value of I_{C1} is determined by the input resistance requirement, whereas the minimum value of I_{C1} depends on I_{B2}, since for β-insensitive design $I_{C1} \gg I_{B2}$ is required. Therefore, I_{C1} should be chosen such that

$$N\frac{I_{C2}}{\beta} \leq I_{C1} \leq \frac{\beta}{R_i} \frac{1}{\frac{N}{V_{RE}+0.7} + \frac{N}{V_{CC}-V_{RE}-0.7} + \frac{|A_v|}{V_{RC}}}$$

  where $N \geq 10$.

- Calculate the resistor values:

$$R_C = \frac{V_{RC}}{I_{C1}},\ R_E = \frac{V_{RE}}{I_{C1}},\ R_G \approx \frac{R_C}{|A_v|} - r_{e1},\ R_{B1} = \frac{\beta(V_{CC} - V_{RE} - 0.7)}{NI_{C1}},\ R_{B2} = \frac{\beta(V_{RE} + 0.7)}{NI_{C1}}$$

- Calculate $A_{v2} = \dfrac{R_H \parallel R_L}{r_{e2} + (R_H \parallel R_L)}$ and $R_{i2} = (\beta + 1)(r_{e2} + (R_H \parallel R_L))$ to verify the initial assumptions.

- Further adjustments can be done after simulation. R_{B1} and R_{B2} can be re-adjusted for DC biasing, whereas R_G can be used to fine-tune A_v and R_i. R_H may also be modified (typically decreased) in case of current clipping at the buffer.

Calculations

Design a BJT amplifier based on the specifications provided in the table below. Your design should be insensitive to β variations, and both the input and the output should be AC coupled as in Fig. 1.

Supply Voltage, V_{CC}	5V
Load Resistance, R_L	100Ω
Transistor's Current Gain, β	≥ 100
Relative Variation of I_C for $V_{BE} = 0.7 \pm 0.1V$	$\leq 10\%$
0-to-Peak Output Swing, $\hat{V}_o$	$\geq 1V$
Voltage Gain, $\lvert A_v \rvert$	20
Input Resistance, R_i	$\geq 1k\Omega$
THD for 5kHz 1V (0-to-peak) Sine Wave Output Voltage, V_o	$\leq 5\%$

Simulations

For all simulations, provide screenshots showing the schematics and the plots with the simulated values properly labeled.

1. Draw the schematics of the amplifier you designed, and obtain the **DC solution** for all node voltages and branch currents using **DC operating point** or **interactive simulation**. Adjust your component values if the results are significantly different from your calculations.
2. Obtain A_v and R_i using **AC simulation**. If necessary, adjust the resistor values to satisfy the specifications.
3. Apply a 5kHz 50mV sine-wave input and obtain the **time-domain waveforms** at the input and the output using **transient simulation**. If your output voltage is clipped or significantly distorted, adjust your design values until you have unclipped 1V (0-to-peak) output signal, while keeping A_v and R_i requirements satisfied.
4. With the 5kHz 50mV sine-wave input, obtain the **total harmonic distortion (THD)** on the output waveform using **Fourier simulation**.

Measurements

For all measurements, provide screenshots showing the plots with the measured values properly labeled.

1. Build your amplifier using the simulated component values, and measure **DC voltages** at all nodes using the **voltmeter** or **scope**.
2. Measure A_v and R_i using the **network analyzer**. If necessary, adjust the resistor values to satisfy the specifications.
3. Apply a 5kHz 50mV sine-wave input and obtain the **time-domain waveforms** at the input and the output using the **scope**. If your output voltage is clipped or significantly distorted, adjust your design values until you have unclipped 1V (0-to-peak) output signal, while keeping A_v and R_i requirements satisfied.
4. Apply a 5kHz 50mV sine-wave input and obtain the **total harmonic distortion (THD)** on the output waveform using the **spectrum analyzer**.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Build the two-stage amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Measure A_v and R_i of the amplifier using the network analyzer.
5. Apply a 5kHz 50mV sine wave input and show the time-domain output voltage using the scope.
6. With the 5kHz 50mV sine wave input, measure the THD at the output using the spectrum analyzer.