ECEN 325 Lab 12: MOSFET Amplifier Design

Objectives

The purpose of this experiment is to design a multi-stage MOSFET amplifier based on a list of specifications.

Introduction

Figure 1 shows a two-stage amplifier composed of a common-source gain stage and a source follower, where the small-signal gain can be calculated as

$$A_v = A_{v1}A_{v2} \qquad A_{v1} = -g_{m1}R_D = -\frac{2V_{RD}}{V_{ov1}} \qquad A_{v2} = \frac{R_L}{\frac{1}{g_{m2}} + R_L} \tag{1}$$

Linearity of this amplifier depends on the condition $\hat{V}_d \ll 4V_{RD}$, where $\hat{V}_d = \hat{V}_o/A_{v2}$ is the peak AC signal at the output of the common-source amplifier (or at the input of the source follower). To avoid voltage clipping at the output of the common-source stage, V_{RD} should be chosen such that

$$V_{DD} + V_{SS} - \hat{V}_d - V_{RS} - V_{ov1} \geq V_{RD} \geq \hat{V}_d \tag{2}$$

To avoid voltage clipping at the output of the source follower, V_{RD} has an additional requirement

$$V_{RD} \geq V_{RX} + V_{ov3} + \hat{V}_o + V_{tn} + V_{ov2} \tag{3}$$

Furthermore, the value of I_X must be chosen larger than the maximum value of I_L as

$$I_X \geq \frac{\hat{V}_o}{R_L} \tag{4}$$

To maximize the available gain and linearity for a given output swing requirement of $\hat{V}_o$, V_{RD} should be chosen as large as possible. V_{RS} and V_{RX} can be chosen around the value of V_t to reduce DC biasing sensitivity to V_t variations, however if the voltage swing is limited, any value over 0.5V may be sufficient.

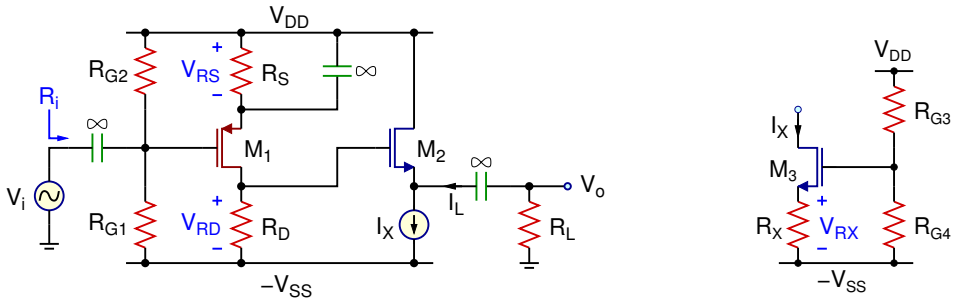

Figure 1: Two-stage MOSFET amplifier and current source implementation

Assuming that one gain stage followed by a buffer is sufficient for the design requirements, the circuit in Fig. 1 can be used as a starting point. Typical specifications include, but not limited to:

- **0-to-peak output swing:** $\hat{V}_o$
- **Gain:** $A_v = A_{v1}A_{v2}$
- **Input resistance:** R_i
- **Load resistance:** R_L
- **Linearity:** $\hat{v}_{sg1} \ll 2V_{ov1}$

Using the circuit in Fig. 1, the design procedure can be given as follows:

- Use 2N7000G for the NMOS, and CD4007P for the PMOS device.
- Choose $I_X \geq \dfrac{\hat{V}_o}{R_L}$.
- Since $I_{D2} = I_{D3} = I_X$, calculate V_{ov2}, V_{ov3}, g_{m2}, A_{v2}, and $\hat{V}_d$.
- Choose $V_{RX} \geq 0.5V$ and $V_{RS} \geq 0.5V$, then choose the maximum possible value of V_{RD} based on (2) and (3). Note that you can substitute $V_{ov1} = \dfrac{2V_{RD}}{|A_{v1}|} = \dfrac{2V_{RD}}{|A_v|}A_{v2}$ in (2).
- Calculate $V_{ov1} = \dfrac{2V_{RD}}{|A_{v1}|}$, then I_{D1}.
- Calculate $R_D = \dfrac{V_{RD}}{I_{D1}}$, $R_S = \dfrac{V_{RS}}{I_{D1}}$, and $R_X = \dfrac{V_{RX}}{I_{D3}}$.
- Find R_{G1} and R_{G2} such that $V_{RG2} = V_{RS} + |V_{tp}| + V_{ov1}$ and $R_{id} = R_{G1} \| R_{G2}$, where R_{id} is the desired input resistance.
- Find R_{G3} and R_{G4} such that $V_{RG4} = V_{RX} + V_{tn} + V_{ov3}$.

Calculations

Design a MOSFET amplifier based on the specifications provided in the table below. Both the input and the output should be AC coupled as in Fig. 1.

Dual Supply Voltage	$\pm 5V$
Load Resistance, R_L	100Ω
0-to-Peak Output Swing, $\hat{V}_o$	$\geq 2V$
Voltage Gain, $\lvert A_v \rvert$	50
Input Resistance, R_i	$\geq 10k\Omega$
THD for 5kHz 2V (0-to-peak) Sine Wave Output Voltage, V_o	$\leq 8\%$

Simulations

For all simulations, provide screenshots showing the schematics and the plots with the simulated values properly labeled.

1. Draw the schematics of the amplifier you designed, and obtain the **DC solution** for all node voltages and branch currents using **DC operating point** or **interactive simulation**. Adjust your component values if the results are significantly different from your calculations.
2. Obtain A_v and R_i using **AC simulation**. If necessary, adjust the resistor values to satisfy the specifications.
3. Apply a 5kHz 40mV sine-wave input and obtain the **time-domain waveforms** at the input and the output using **transient simulation**. If your output voltage is clipped or significantly distorted, adjust your design values until you have unclipped 2V (0-to-peak) output signal, while keeping A_v and R_i requirements satisfied.
4. With the 5kHz 40mV sine-wave input, obtain the **total harmonic distortion (THD)** on the output waveform using **Fourier simulation**.

Measurements

For all measurements, provide screenshots showing the plots with the measured values properly labeled.

1. Build your amplifier using the simulated component values, and measure **DC voltages** at all nodes using the **voltmeter** or **scope**.
2. Measure A_v and R_i using the **network analyzer**. If necessary, adjust the resistor values to satisfy the specifications.
3. Apply a 5kHz 40mV sine-wave input and obtain the **time-domain waveforms** at the input and the output using the **scope**. If your output voltage is clipped or significantly distorted, adjust your design values until you have unclipped 2V (0-to-peak) output signal, while keeping A_v and R_i requirements satisfied.
4. Apply a 5kHz 40mV sine-wave input and obtain the **total harmonic distortion (THD)** on the output waveform using the **spectrum analyzer**.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Build the two-stage amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Measure A_v and R_i of the amplifier using the network analyzer.
5. Apply a 5kHz 40mV sine wave input and show the time-domain output voltage using the scope.
6. With the 5kHz 40mV sine wave input, measure the THD at the output using the spectrum analyzer.