

ECEN 325 Lab 10: Characterization of the MOSFET

Objectives

The purpose of this lab is to characterize N and P type metal-oxide-semiconductor field-effect transistors (MOSFETs), also known as NMOS and PMOS transistors.

Introduction

Figure 1 shows typical symbols for the NMOS and PMOS transistors. Depending on the applied DC bias, MOSFETs have three regions of operation:

- **Cutoff Region:**

$$\text{NMOS: } V_{GS} < V_{tn} \Rightarrow I_D = 0$$

$$\text{PMOS: } V_{SG} < V_{tp} \Rightarrow I_D = 0$$

- **Triode (Linear) Region:**

$$\text{NMOS: } V_{DS} < V_{ov} \Rightarrow I_D = k'_n \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right), \quad V_{ov} = V_{GS} - V_{tn}$$

$$\text{PMOS: } V_{SD} < V_{ov} \Rightarrow I_D = k'_p \frac{W}{L} \left(V_{ov} V_{SD} - \frac{V_{SD}^2}{2} \right), \quad V_{ov} = V_{SG} - |V_{tp}|$$

- **Active (Saturation) Region:**

$$\text{NMOS: } V_{DS} > V_{ov} \Rightarrow I_D = \frac{k'_n}{2} \frac{W}{L} V_{ov}^2, \quad V_{ov} = V_{GS} - V_{tn}$$

$$\text{PMOS: } V_{SD} > V_{ov} \Rightarrow I_D = \frac{k'_p}{2} \frac{W}{L} V_{ov}^2, \quad V_{ov} = V_{SG} - |V_{tp}|$$

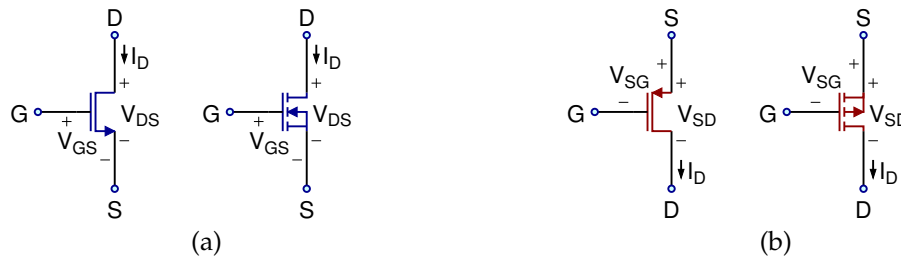


Figure 1: Circuit symbols for (a) NMOS Transistor (b) PMOS Transistor

MOSFET Characterization

Figure 2 shows a characterization circuit for an NMOS transistor. To obtain I_D as a function of V_{GS} , V_1 is swept while V_2 is kept constant. If V_1 is kept constant and V_2 is swept, I_D can be obtained as a function of V_{DS} .

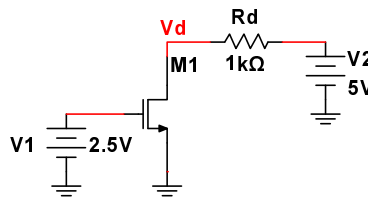


Figure 2: NMOS transistor characterization circuit

Characterization circuit for a PMOS transistor is shown in Fig. 3. Keeping V_2 constant and sweeping V_1 provides I_D as a function of V_{SG} . Sweeping V_2 while V_1 is kept constant provides the I_D vs. V_{SD} characteristics.

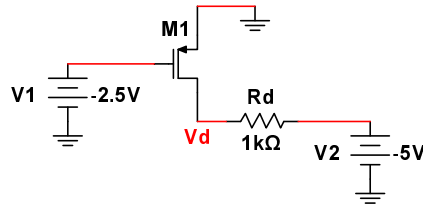


Figure 3: PMOS transistor characterization circuit

Figure 4(a) shows the drain current (I_D) of an NMOS transistor as a function of V_{GS} . Transistor parameters such as the threshold voltage (V_t) and the transconductance parameter ($k'W/L$ or β) can be obtained by taking the derivative of I_D with respect to V_{GS} , as depicted in Fig. 4(b). In this plot, $k'W/L$ (or β) is the slope of the line, whereas V_t is the intersection with the V_{GS} axis.

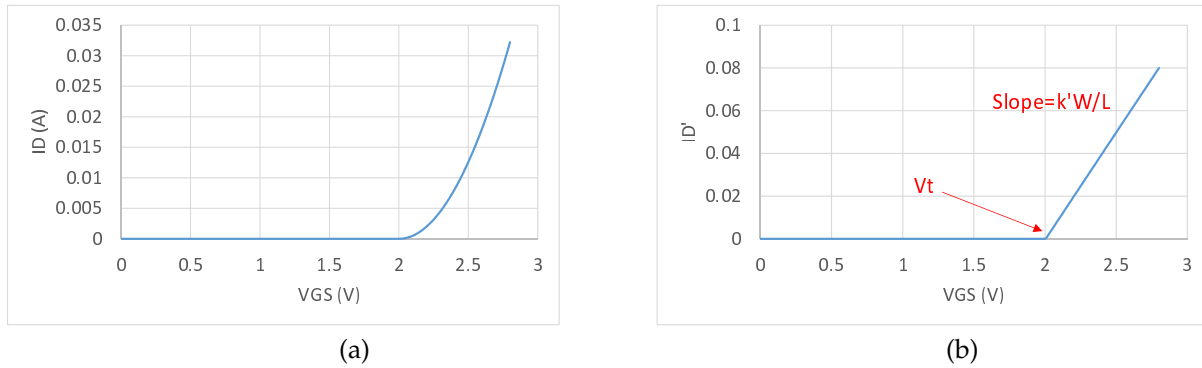


Figure 4: NMOS characterization (a) I_D vs. V_{GS} (b) $\frac{dI_D}{dV_{GS}}$ vs. V_{GS}

Simulations

For all simulations, provide screenshots showing the schematics and the plots with the simulated values properly labeled.

As the first step, install MOS transistor library (UsrComp_S.ECEN.usr) to your circuit simulator, details are provided in the simulator manual.

- Draw the schematics for the NMOS characterization circuit in Fig. 2 using the 2N7000G transistor.
 - Perform a **DC sweep** of V_1 from 0V to 2.5V while $V_2 = 5V$, and plot I_D and its derivative as a function of V_{GS} .
 - Find the threshold voltage V_t and the transconductance parameter $k' \frac{W}{L}$ (or β).
- Repeat (1) for the CD4007N transistor.
- Draw the schematics for the PMOS characterization circuit in Fig. 3 using the CD4007P transistor.
 - Perform a **DC sweep** of V_1 from -2.5V to 0V while $V_2 = -5V$, and plot I_D and its derivative as a function of V_{SG} .
 - Find the threshold voltage V_t and the transconductance parameter $k' \frac{W}{L}$ (or β).

Measurements

For all measurements, provide screenshots showing the plots with the measured values properly labeled.

- Build the NMOS characterization circuit in Fig. 2 using the 2N7000G transistor.
 - Apply a ramp signal from 0V to 2.5V at 1Hz for V_1 while $V_2 = 5V$. Export the voltage measurements from the **scope** to Excel, and plot I_D as a function of V_{GS} .
 - Plot the derivative of I_D as a function of V_{GS} and find V_t and $k' \frac{W}{L}$ as depicted in Fig. 4(b). In Excel, dI_D/dV_{GS} can be calculated as shown with the column **ID'** in Fig. 5, starting with the formula (B3-B2)/(A3-A2). However, due to noise in the measured data, taking the derivative without filtering can result in the **ID'** plot shown in Fig. 6(a). Using decimation provides filtering and reduces the noise in ID'. The column **ID' (decimated)** in Fig. 5 shows the starting formula (to be copied to all cells below), and the resulting plot is shown in Fig. 6(b). In this plot, a decimation factor of 300 is used. The corresponding V_{GS} should also be shifted as shown with the **VGS (adjusted)** column in Fig. 5.

	A	B	C	D	E
1	VGS	ID	ID'	VGS (adjusted)	ID' (decimated)
2	A2	B2	(B3-B2)/(A3-A2)	A152	(B302-B2)/(A302-A2)
3	A3	B3	(B4-B3)/(A4-A3)	A153	(B303-B3)/(A303-A3)

Figure 5: Implementation of derivation and decimation in Excel

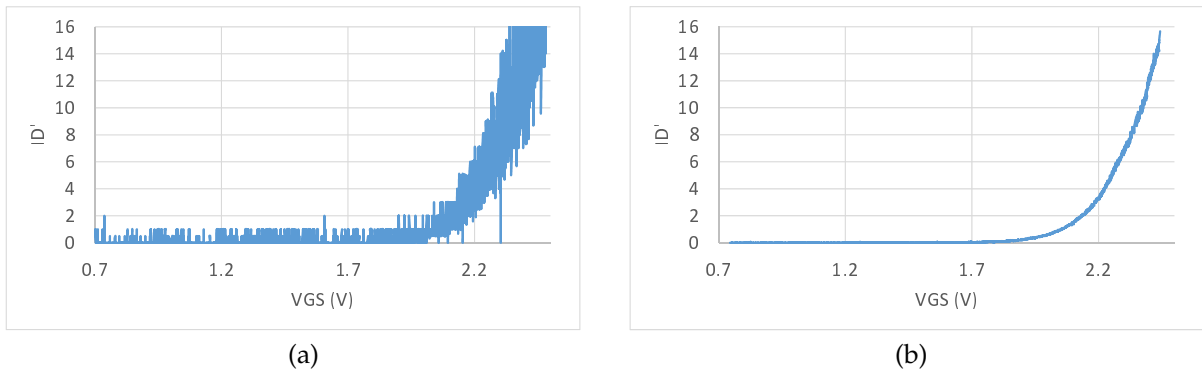


Figure 6: $\frac{dI_D}{dV_{GS}}$ vs. V_{GS} (a) with no filtering (b) after decimation

- Repeat (1) for the CD4007N transistor. See Fig. 7 for the internal schematics of CD4007 chip, connect pin 7 to GND and pin 14 to +5V supply voltage.

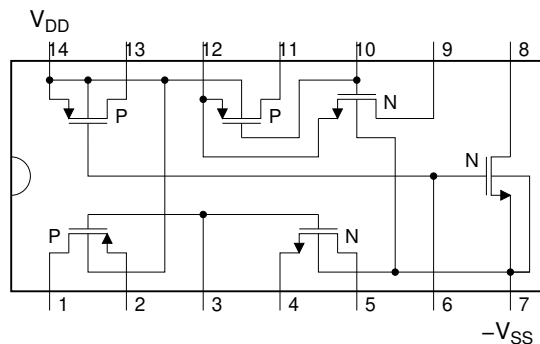


Figure 7: Schematic diagram of CD4007 chip

3. Build the PMOS characterization circuit in Fig. 3 using the CD4007P transistor, connect pin 7 to -5V supply voltage and pin 14 to GND.
 - (a) Apply a ramp signal from -2.5V to 0V at 1Hz for V_1 while $V_2 = -5V$. Export the voltage measurements from the **scope** to Excel, and plot I_D as a function of V_{SG} .
 - (b) Plot the derivative of I_D as a function of V_{SG} , and find V_t and $k' \frac{W}{L}$ as described in **1(b)**.

Report

1. Include schematics, simulation plots, and measurement plots.
2. Prepare a table showing simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Build the characterization circuits in Figs. 2 and 3 for 2N7000G, CD4007N and CD4007P transistors on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Using the characterization circuits, obtain V_t and $k' \frac{W}{L}$ for 2N7000G, CD4007N and CD4007P transistors as described.