Lab 3:
Second Order Circuit

Name: Wan-Yu Liao

ECEN 325 Section 514

TA: Mandela

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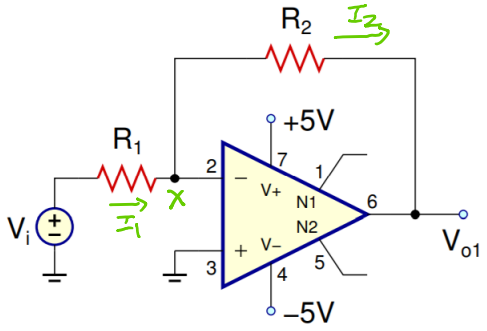
Calculation

1. Read the data sheet for the UA741 opamp and write down the typical values of the following parameters:

Supply Voltage:	5V to 15V -5V to -15V	Power Consumption:	50mW
Input Resistance:	2MΩ	Input Offset Voltage:	1mV
Output Resistance:	75Ω	Input Offset Current:	20nA
Voltage Gain:	106dB	Bandwidth:	1MHz
Slew Rate:	0.5V/μs		

2. Derive the voltage gains

Circuit A

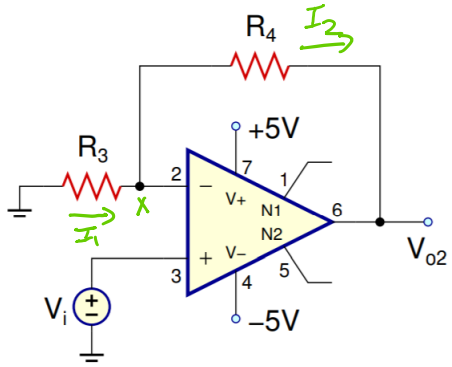


$V_x = 0 \qquad I_1 = I_2$

$$\frac{V_i - V_x}{R_1} = \frac{V_x - V_{o1}}{R_2}$$

$$\frac{V_{o1}}{V_i} = -\frac{R_2}{R_1}$$

Circuit B

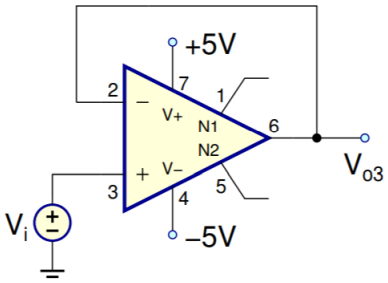


$$V_X = V_i$$

$$\frac{0 - V_X}{R_3} = \frac{V_X - V_{o2}}{R_4}$$

$$\frac{V_{o2}}{V_i} = 1 + \frac{R_4}{R_3}$$

Circuit C



$$V_{o3} = V_i$$

$$\frac{V_{o3}}{V_i} = 1$$

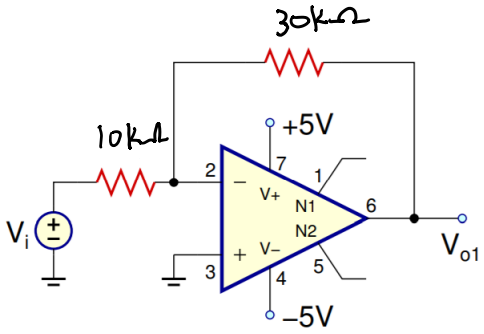
3. If R1 = R3 = 10kΩ, find R2 and R4 such that $V_{o1}/V_i = -3$ and $V_{o2}/V_i = 6$.

$$\frac{V_{o1}}{V_i} = -\frac{R_2}{R_1} \Rightarrow -3 = -\frac{R_2}{10k} \Rightarrow R_2 = 30k\Omega$$

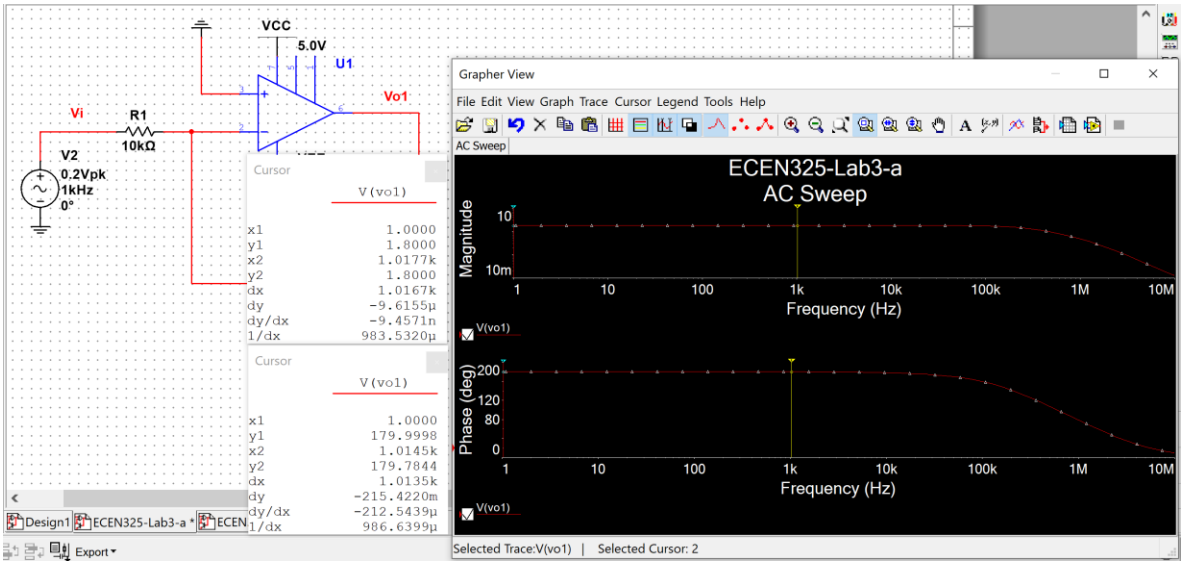
$$\frac{V_{o2}}{V_i} = 1 + \frac{R_4}{R_3} \Rightarrow 6 = 1 + \frac{R_4}{10k} \Rightarrow R_4 = 50k\Omega$$

Simulations

Circuit A

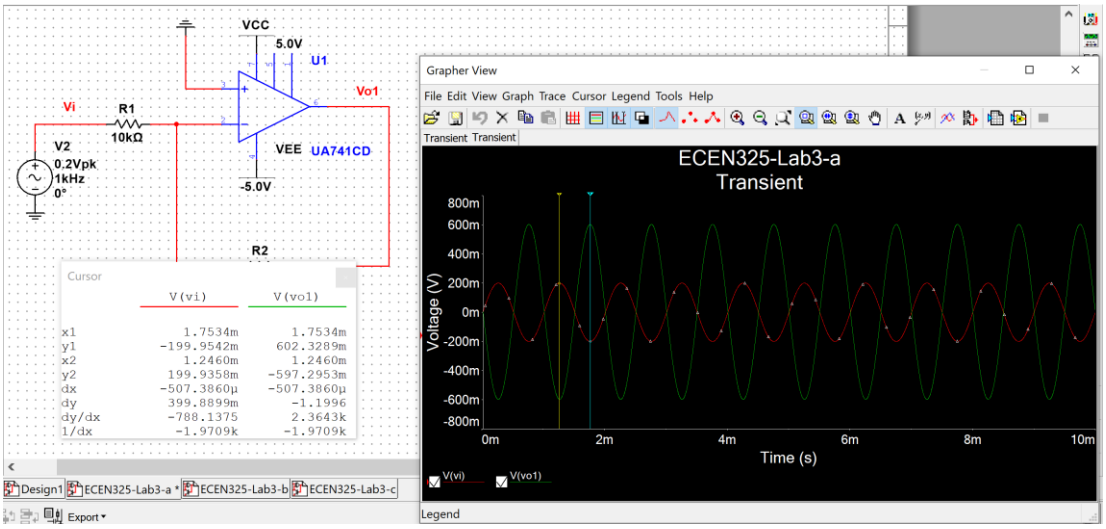


(a) Bode Plot



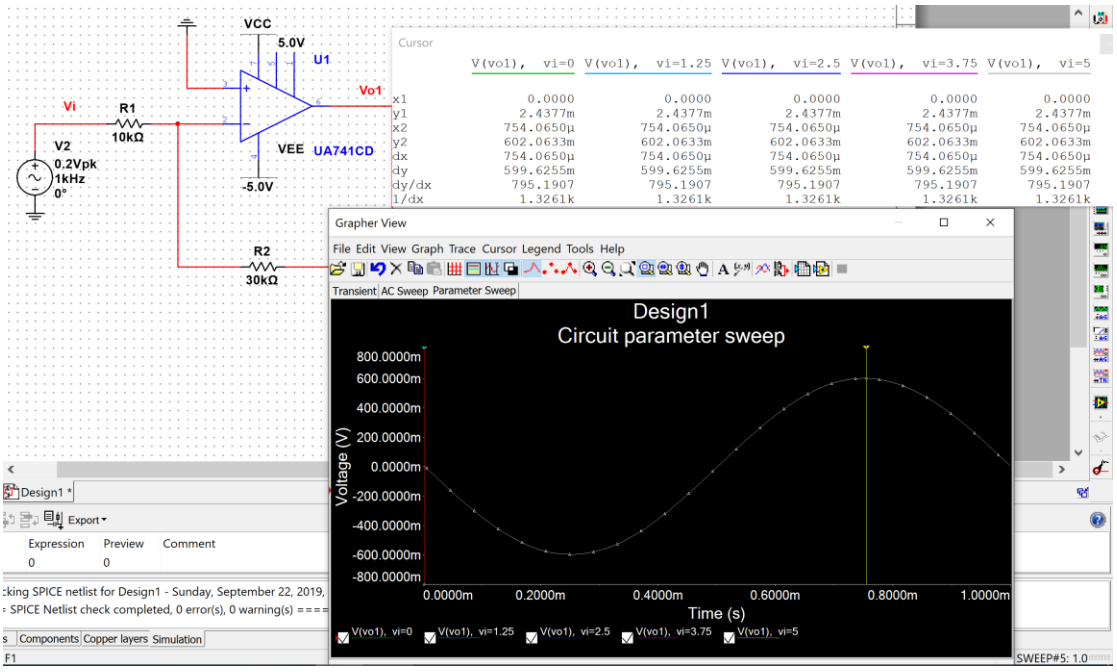
(b) Time-Domain Waveforms

This simulation is different from pre-lab because in the pre-lab, I connected the wrong vcc and vee to the op amp and I didn't get the correct graph.



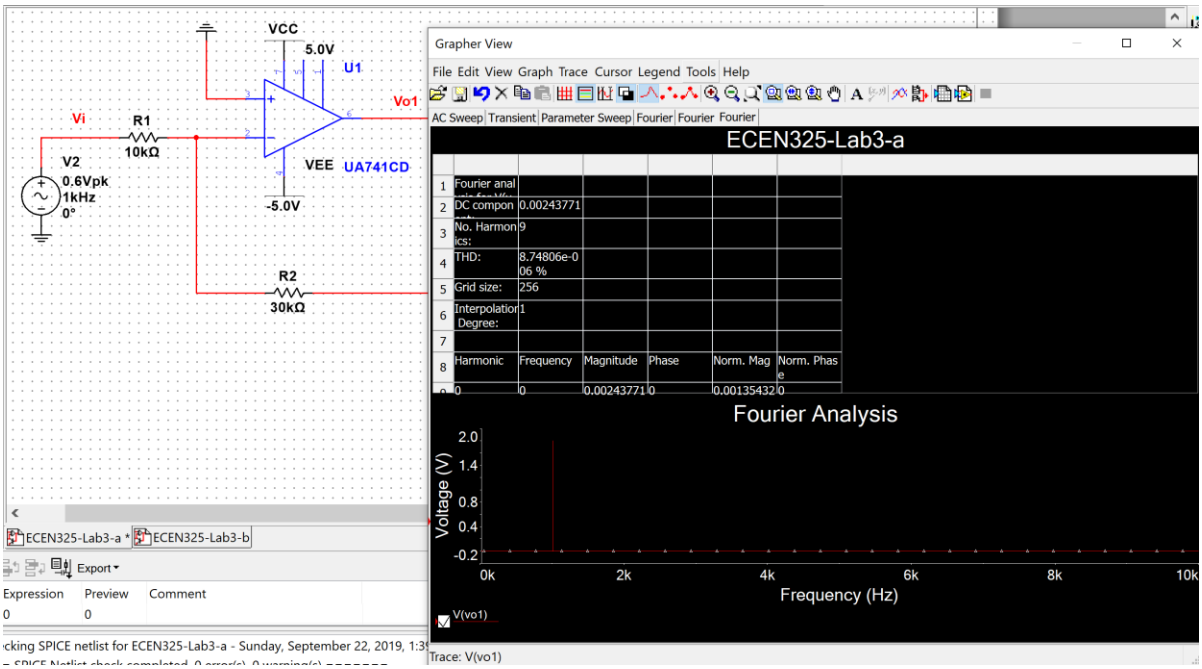
(c) Parameter Sweep

This graph is also different from the pre-lab. Maximum amplitude is 0.6V.

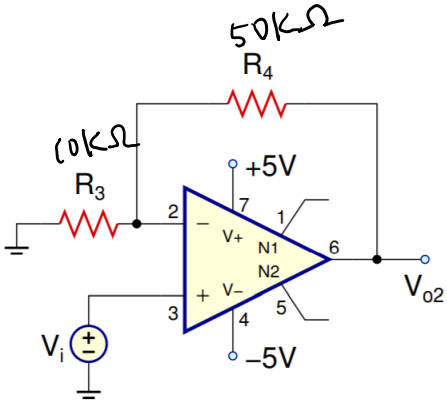


(d)

Applied $V_i(t) = 0.6 \sin(2\pi 1000t)$.

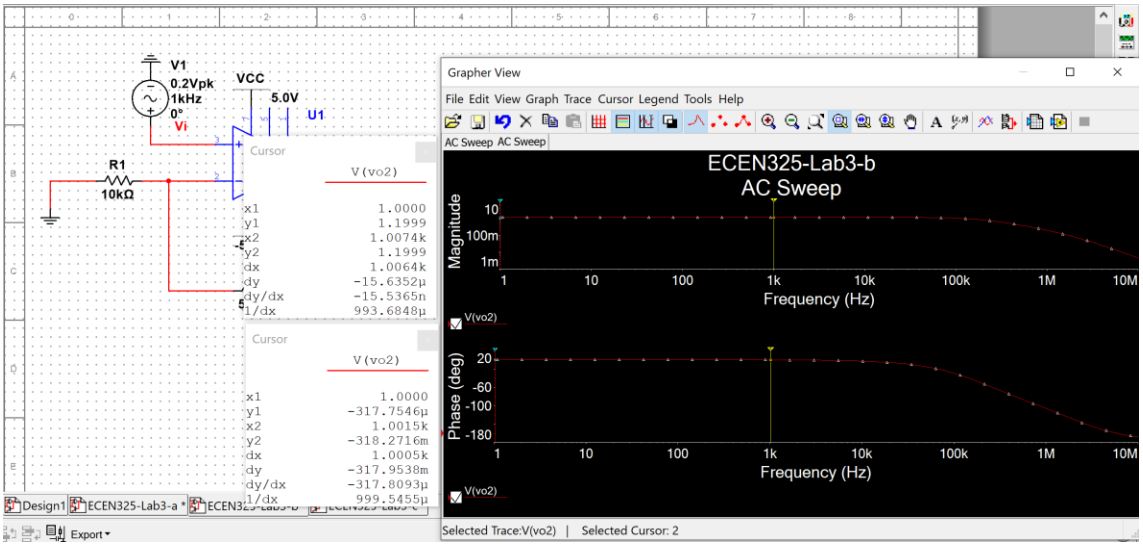


Circuit B

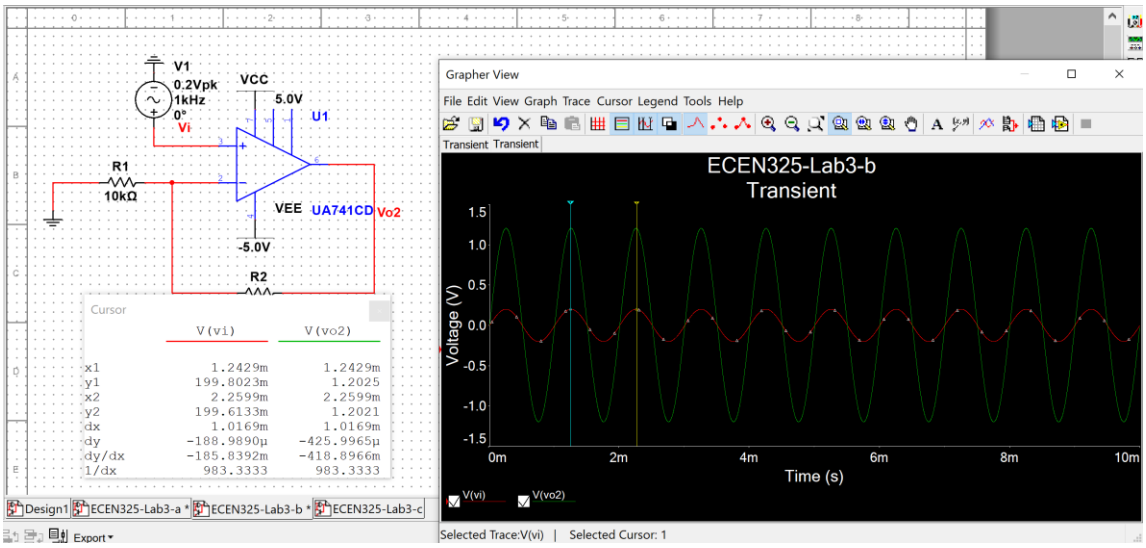


Simulation pictures for circuit B are all different from pre-lab because I used the wrong resistor value in pre-lab and connected the wrong vcc and vee in the pre-lab.

(a) Bode Plot

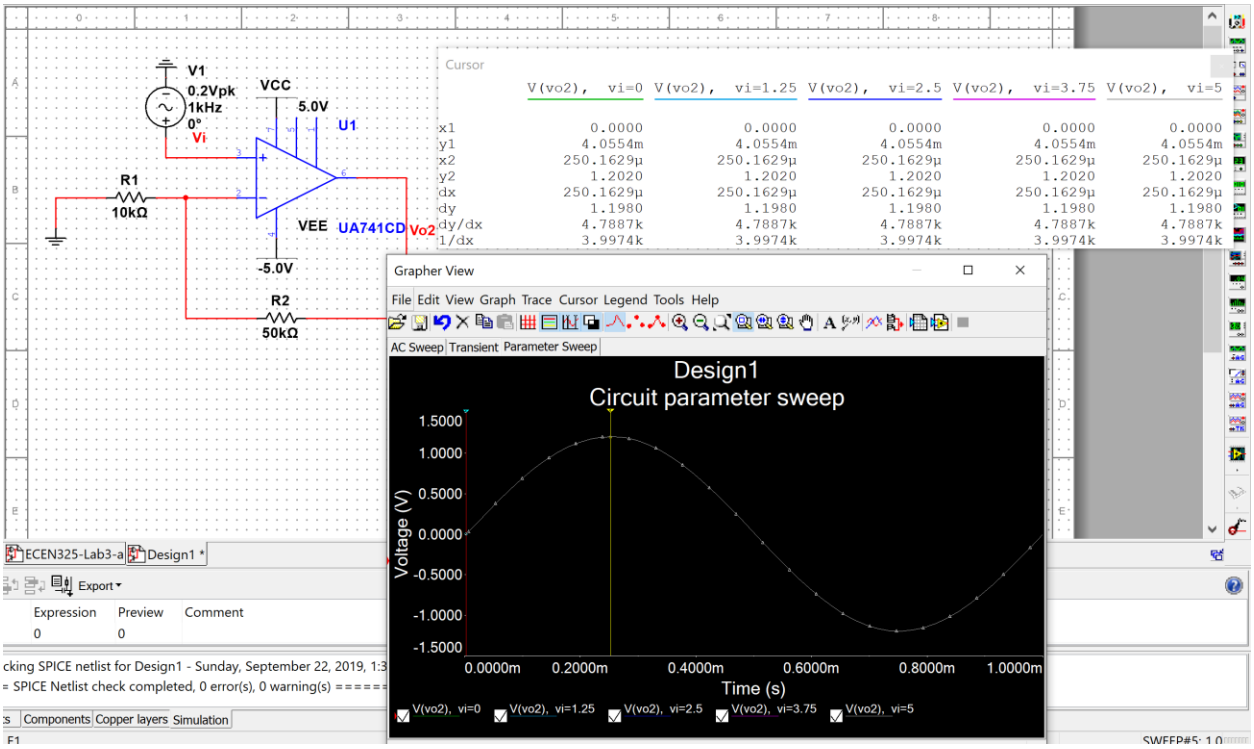


(b) Time-Domain Waveforms



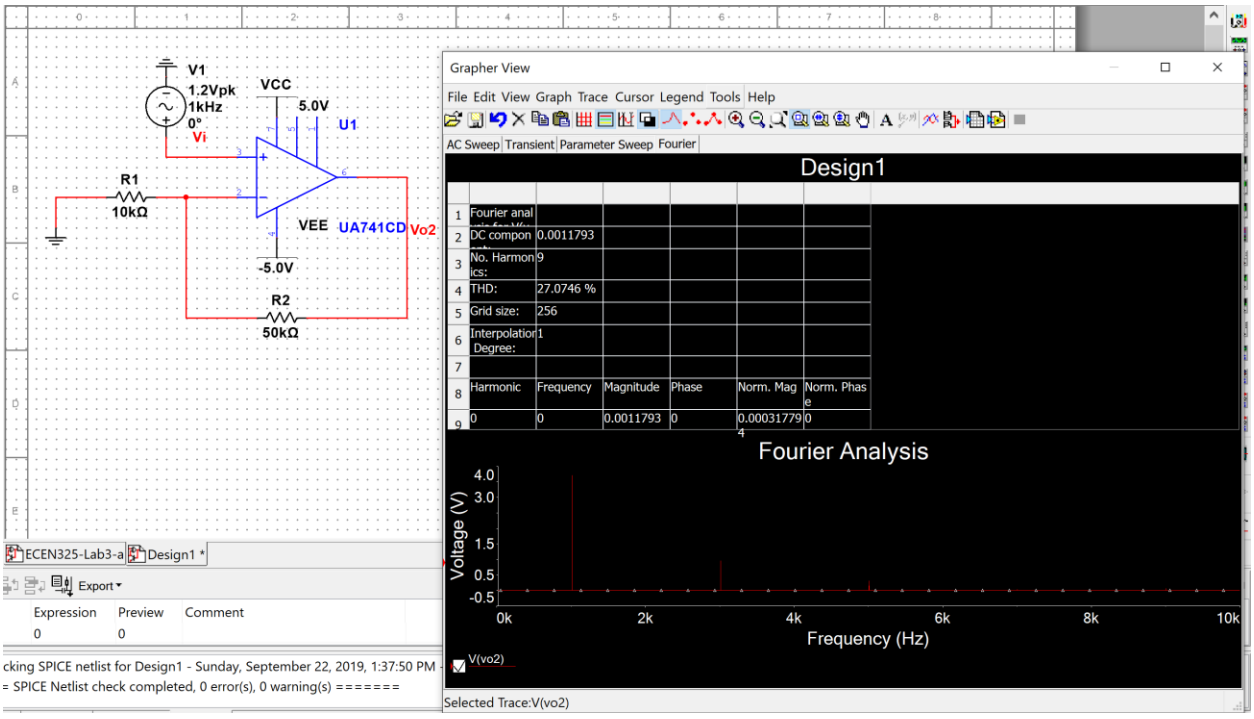
(c) Parameter Sweep

The max amplitude is about 1.2V.



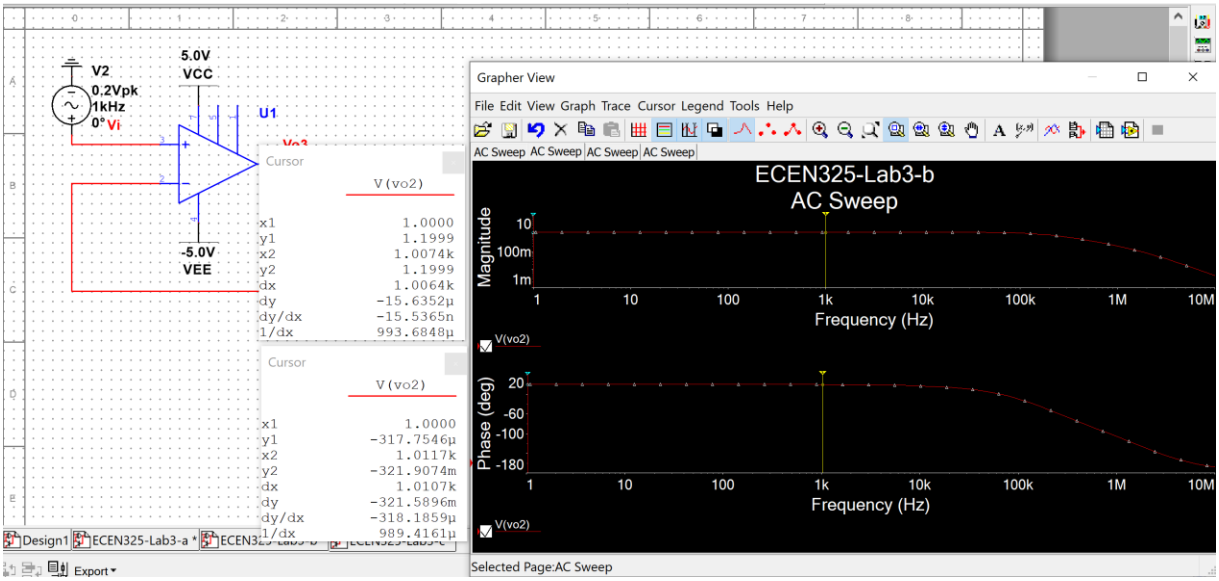
(d)

Applied $V_i(t) = 1.2 \sin(2\pi 1000t)$.



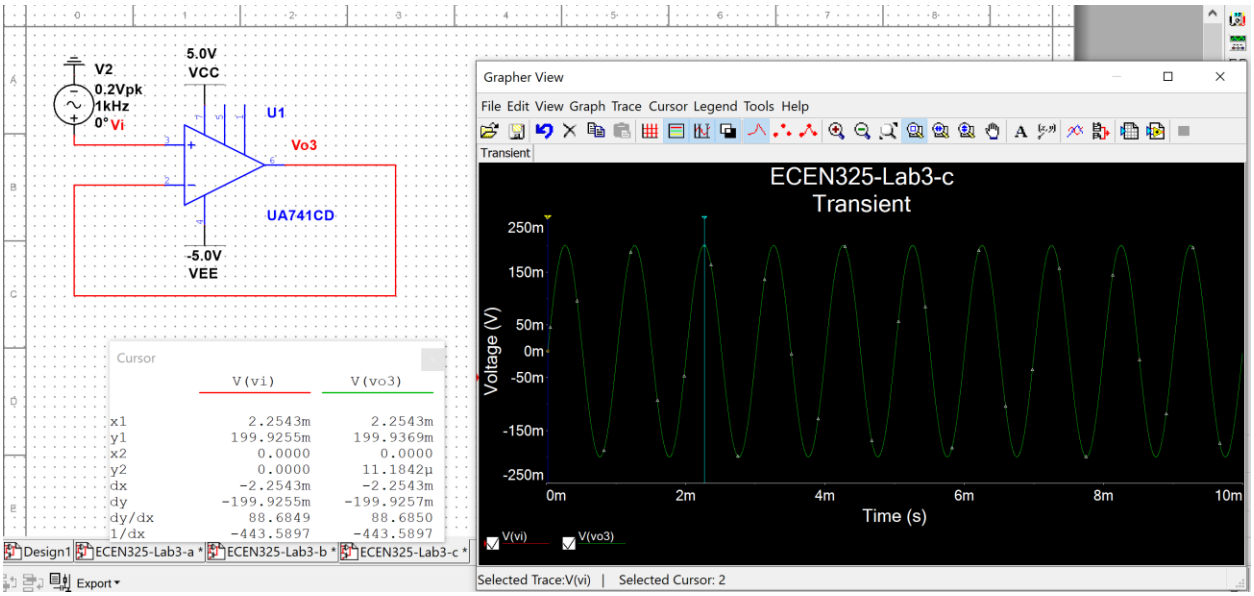
<u>Circuit C</u>

(a)



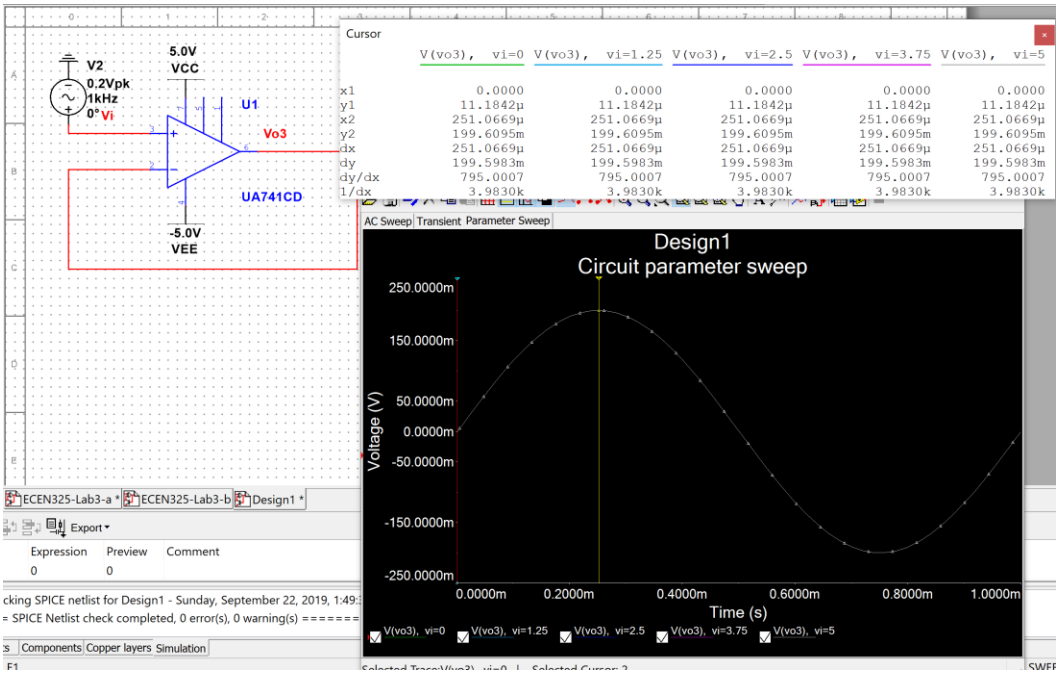
(b)

Time-Domain Waveform



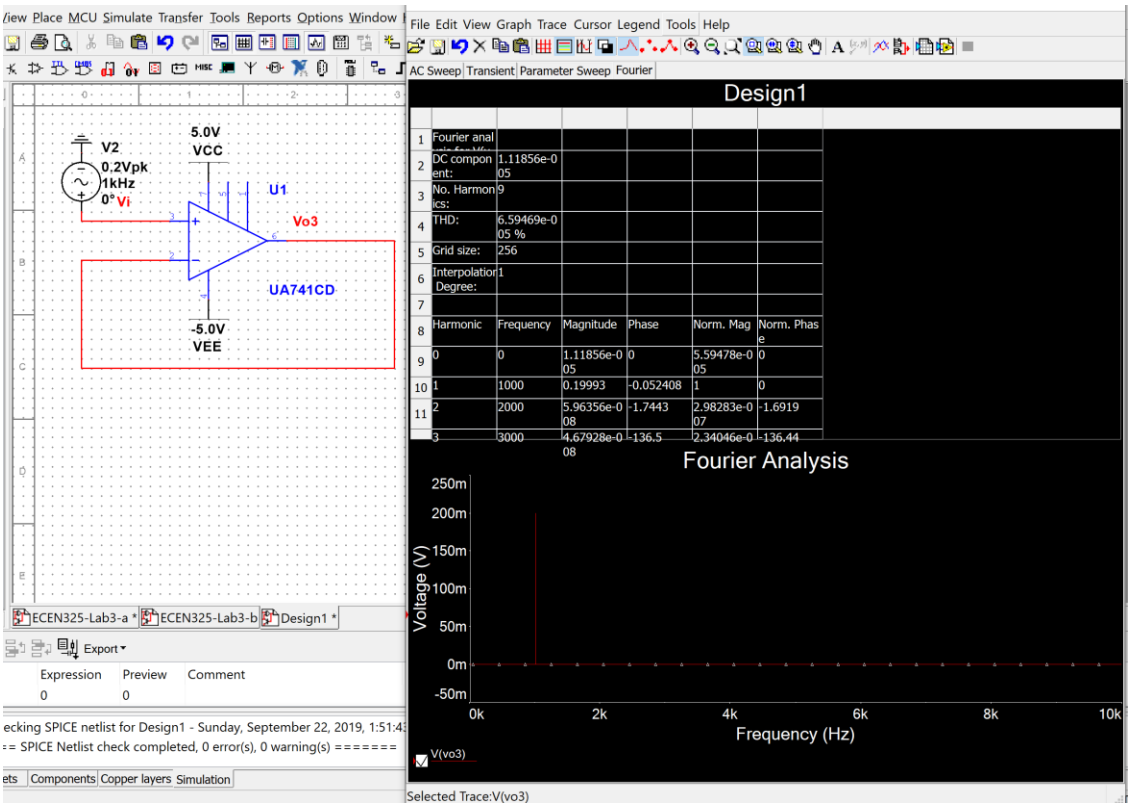
(c)

Max amplitude is about 0.2V.



(d)

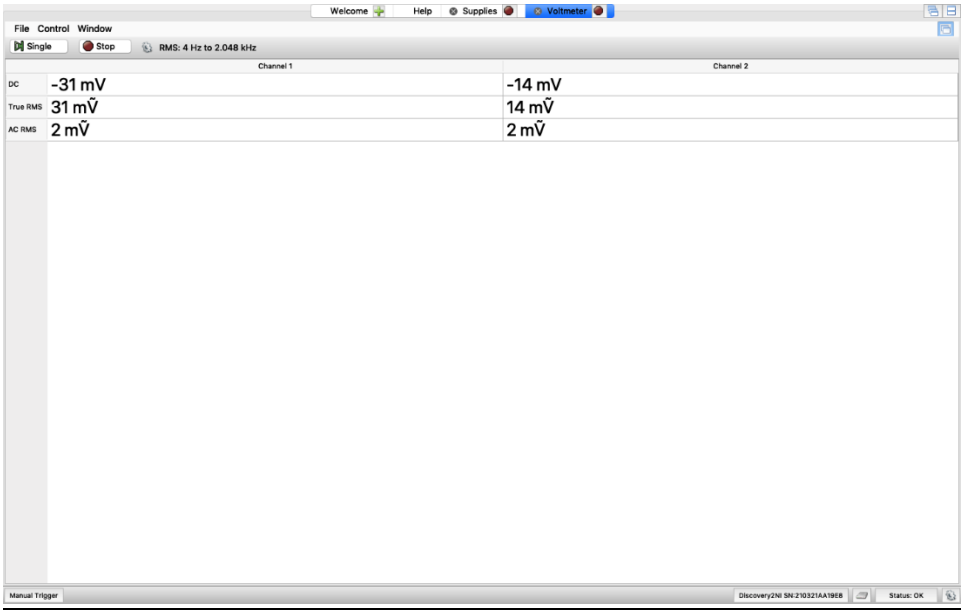
Applied $V_i(t) = 0.2 \sin(2\pi 1000t)$.



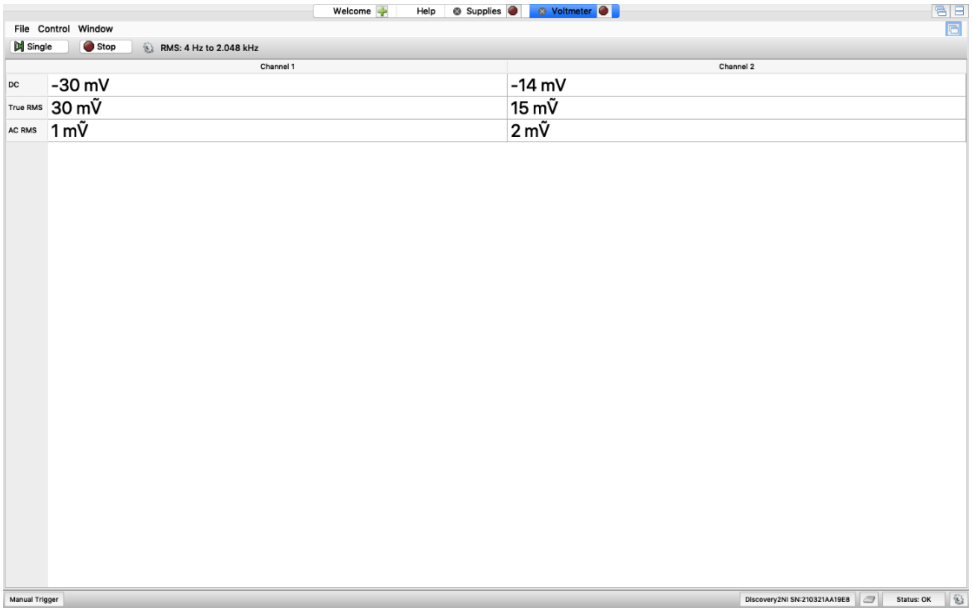
Measurement

Input Offset Current

Voltage Across Resistor @ Negative Terminal



Voltage Across Resistor @ Positive Terminal



I (negative terminal) = $-31*10^{-3}*10^{-5} = -31*10^{-8}$

I (positive terminal) = $-30*10^{-3}*10^{-5} = -30*10^{-8}$

Input offset = $1*10^{-8}$ = 100uA

DC Offset Voltage

Before placing the potentiometer:

Output voltage offset = 2mV

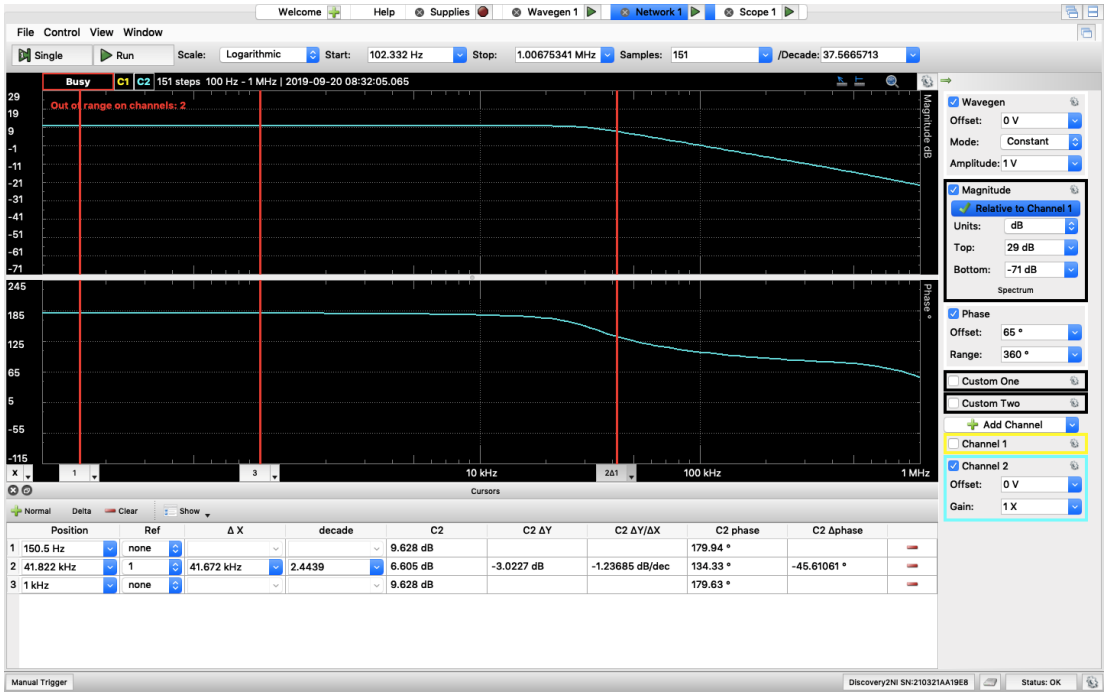
Input voltage offset = 2mv/6 = 0.33mV

After placing the potentiometer:

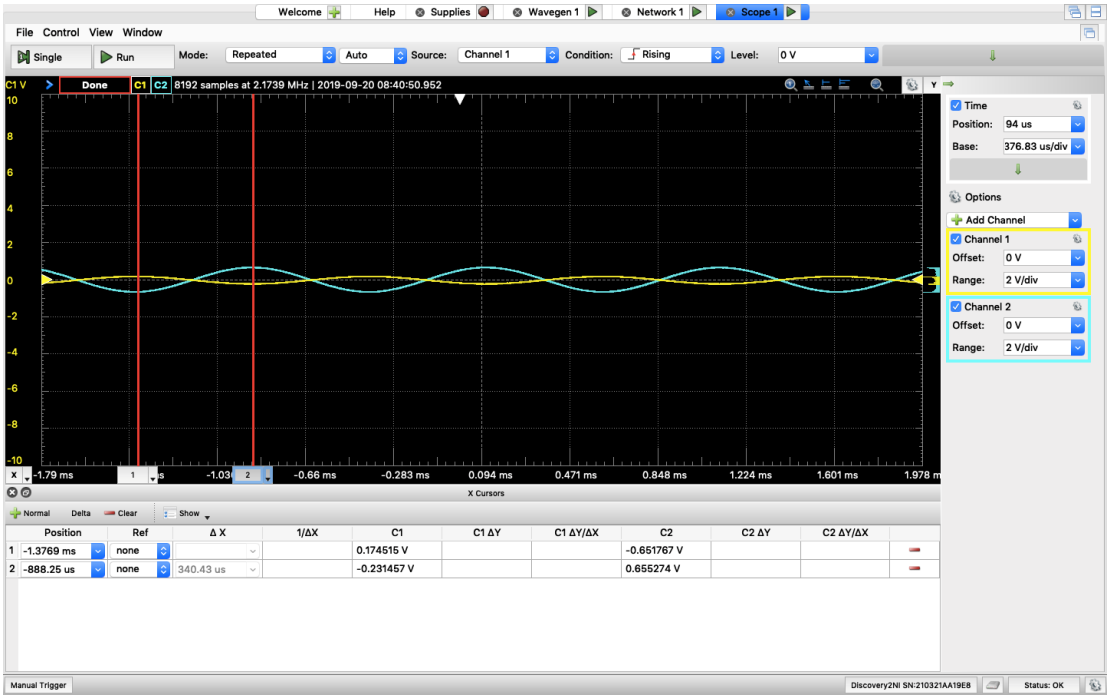
Output voltage = 1mV

Circuit A

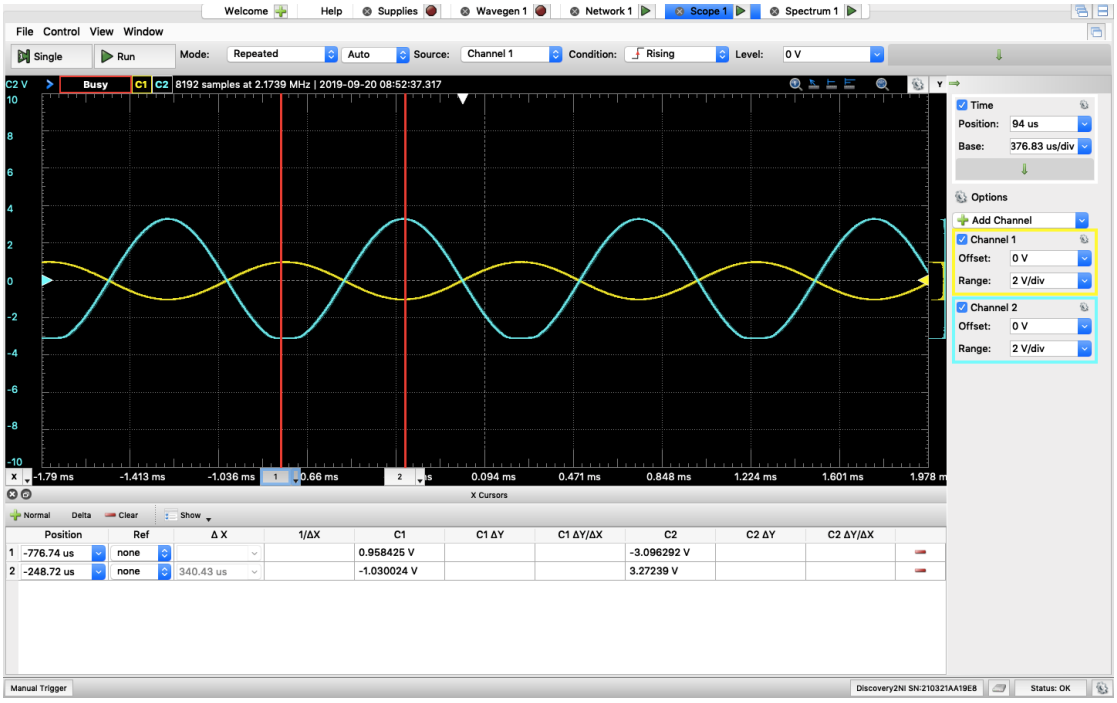
Bode Plot



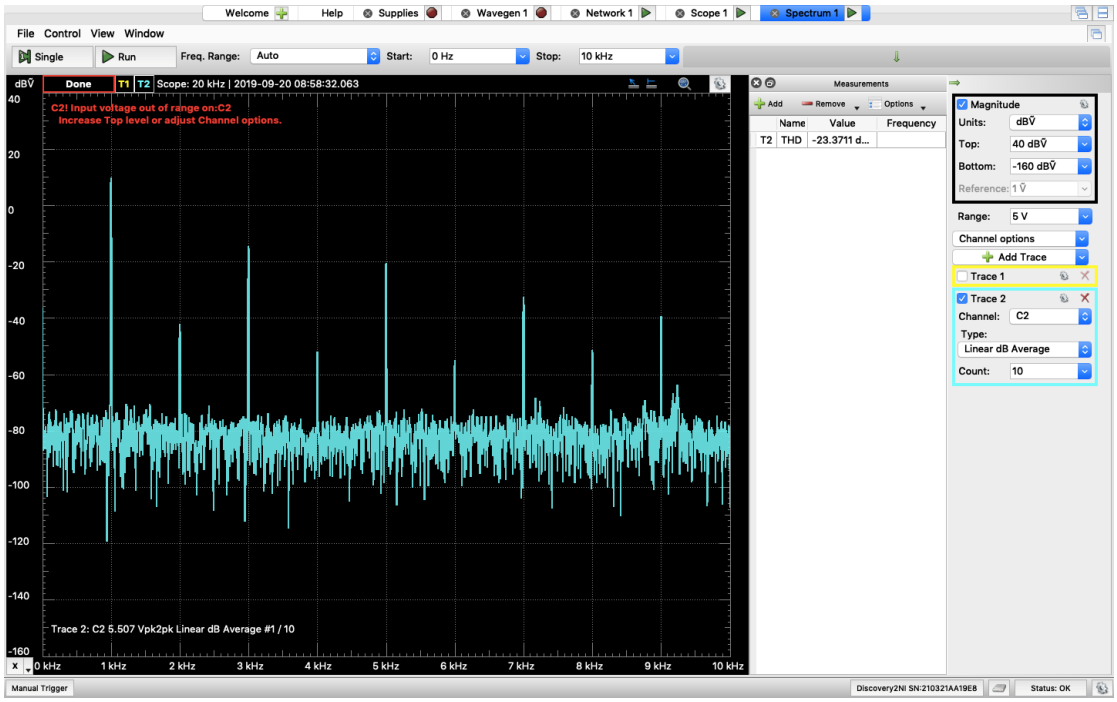
Time-Domain Waveform



Clipping Point

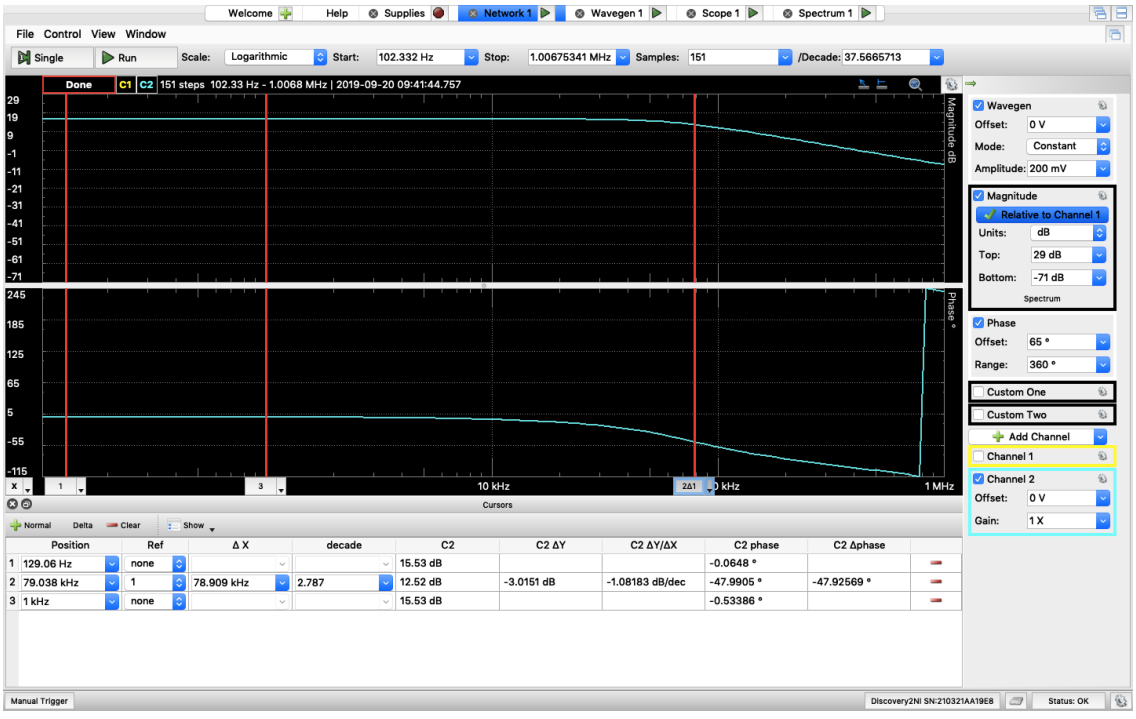


Total Harmonic Distortion

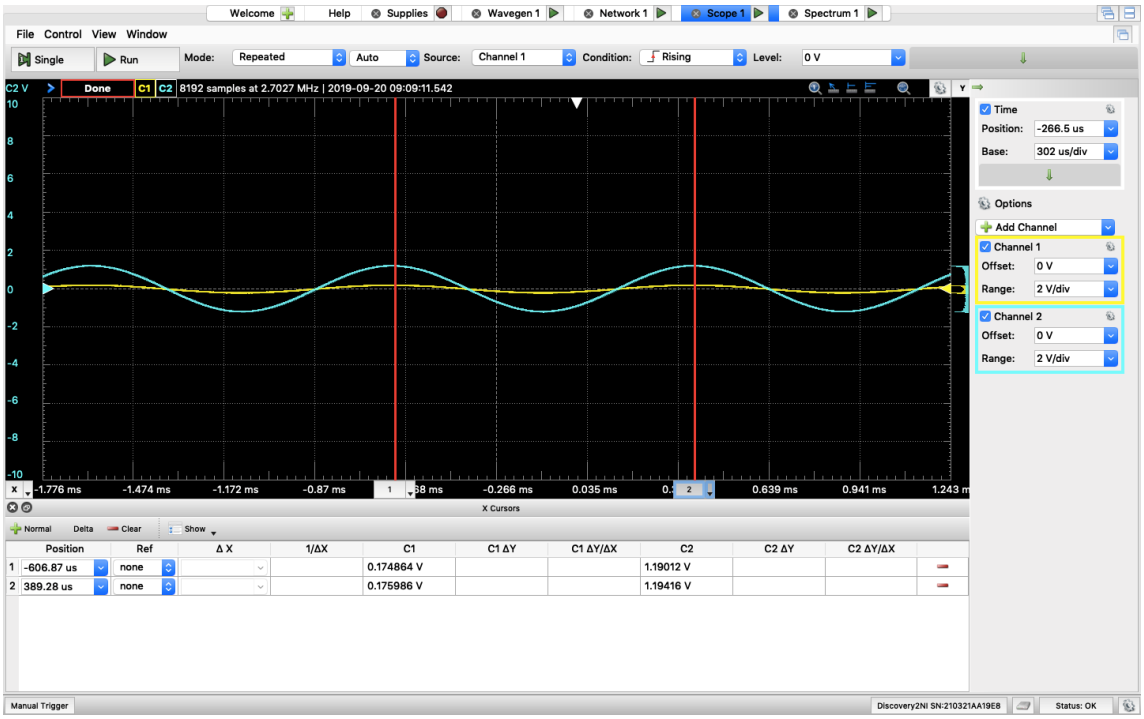


Circuit B

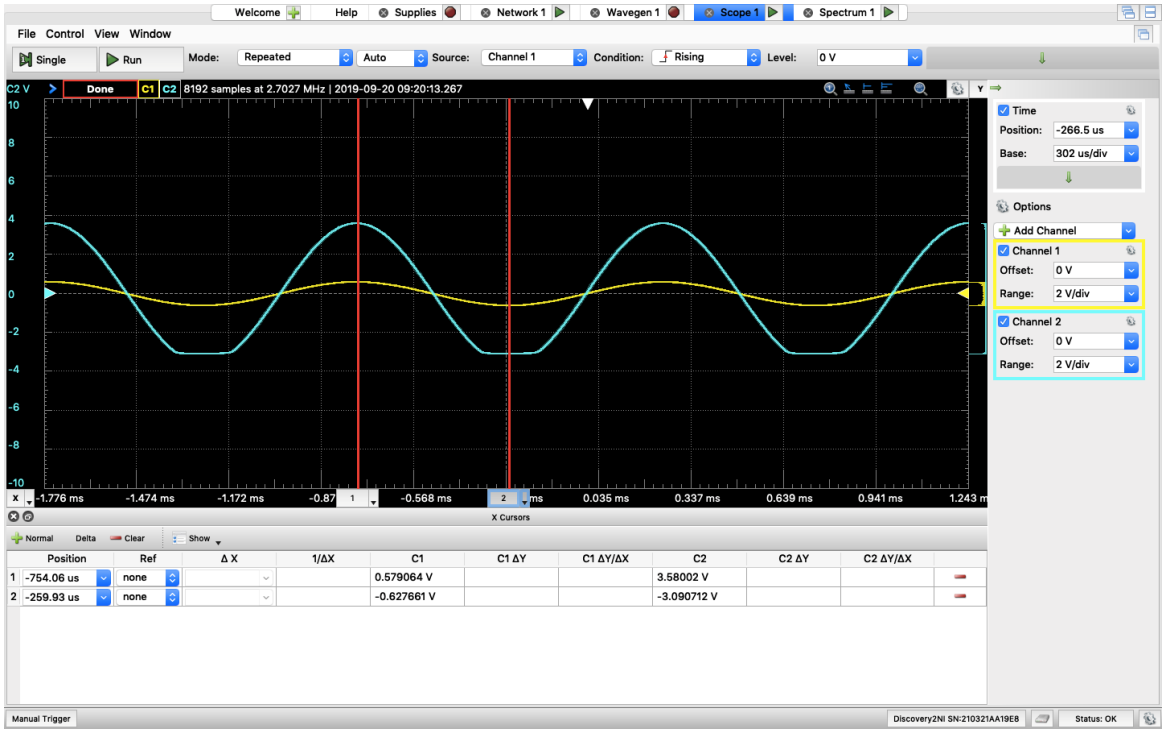
Bode Plot



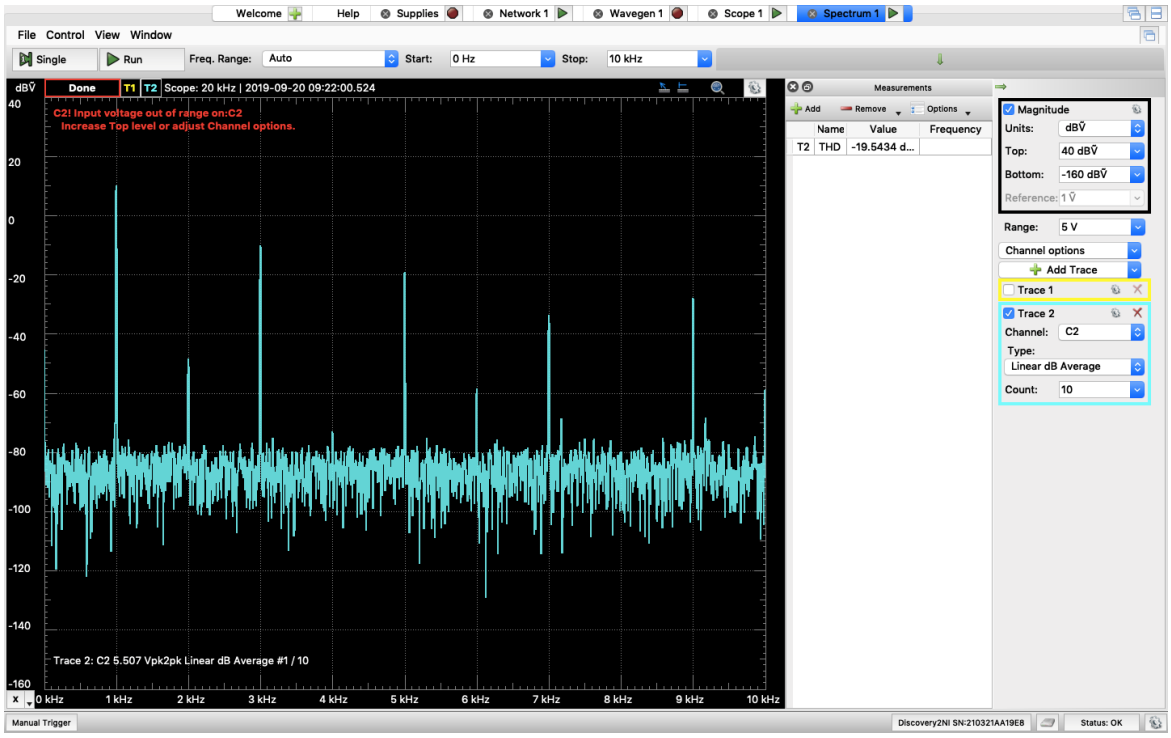
Time-Domain Waveform



Clipping Point

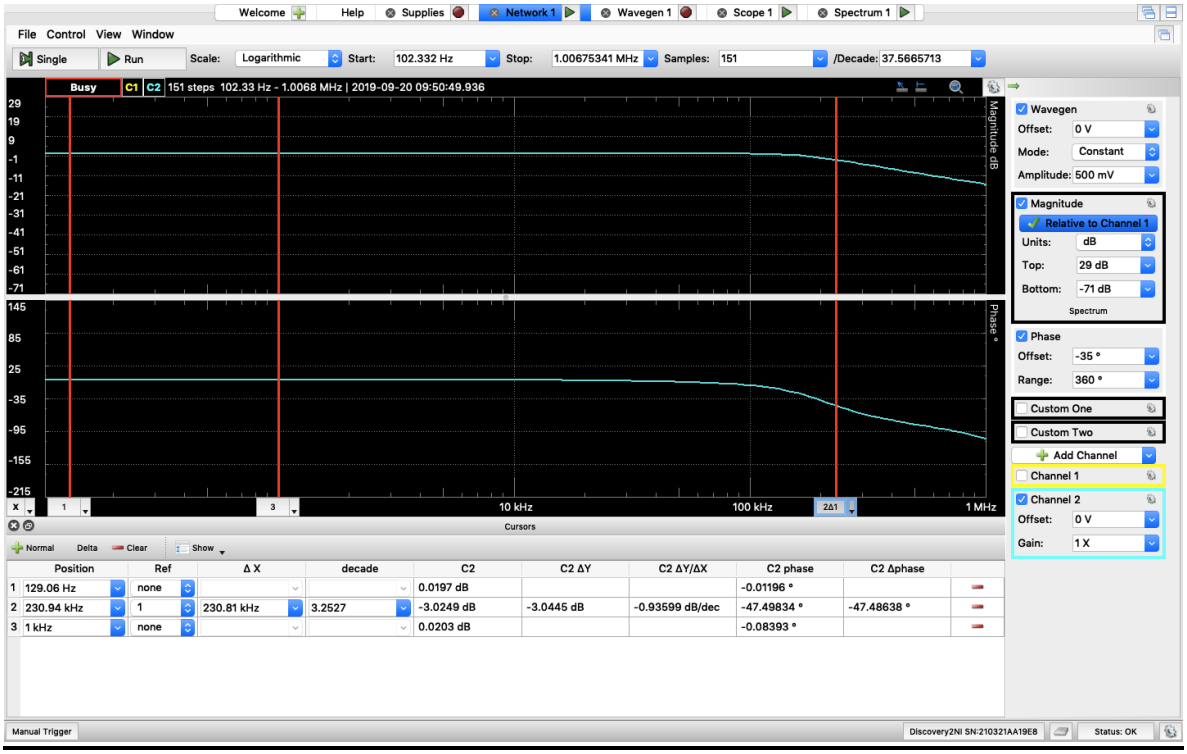


Total Harmonic Distortion

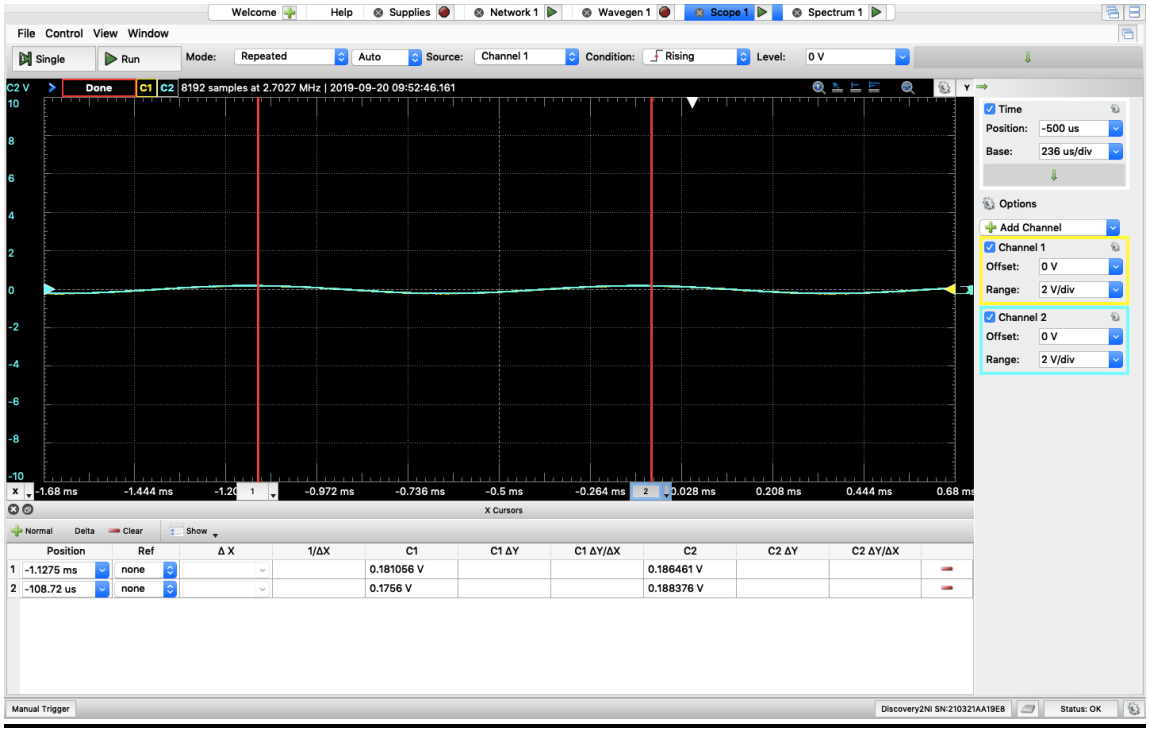


Circuit C

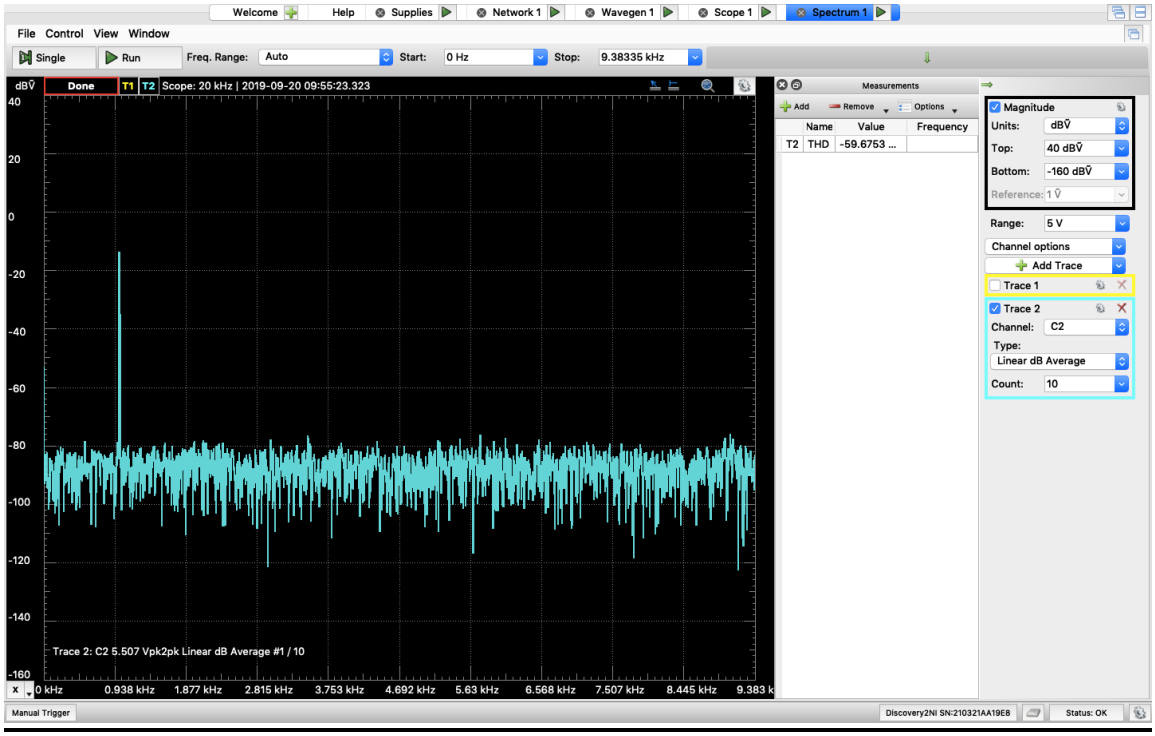
Bode Plot



Time-Domain Waveform



Total Harmonic Distortion



Tables

Data Sheet Value vs. Measured Value

	Data Sheet Value	Measured Value
Input Voltage Offset	1mV	0.33mV
Input Current Offset	TYP: 20nA MAX: 200nA	0.1nA

Calculated vs. Simulated vs. Measured

	V_o/V_i	|H|	∠H	$V_{i,\ max}$	THD%	DC Gain
Circuit A Calculated	**-3**					**3**
Circuit A Simulated	-602.3m/200.0m = **-3.01**	20log(1.8) = **5.1dB**	179.7°	0.6V	$8.75*10^{-6}$	**1.8**
Circuit A Measured	-0.652/0.174 = **-3.76**	**9.63dB**	179.63°	1V	0.0678	$10^{9.6/20}$ = **3.02**
Circuit B Calculated	**6**					**6**
Circuit B Simulated	1200m/199.6m = **6.01**	20log(1.2) = **1.58dB**	-0.322°	1.2V	27.1	**1.2**
Circuit B Measured	1.194/0.175 = **6.82**	**15.53dB**	-0.534°	0.6V	0.105	$10^{15/20}$ = **5.6**
Circuit C Calculated	**1**					**1**
Circuit C Simulated	199.94m/199.92m = **1.00**	20log(1.2) = **1.58dB**	-0.053°	0.2V	$6.59*10^{-5}$	**1.2**
Circuit C Measured	0.188/0.181 = **1.04**	**0.02dB**	-0.084°	0.2V	0.00104	$10^{0.0197/20}$ = **1.002**

Conclusion

The results of simulation are different from the results of calculation and measurement. It might because I used Vee for the negative power supply on simulation circuits or the values, I entered are wrong.

For the DC voltage offset part, after placing the potentiometer, the output voltage should be 0V but not 1mV. It might because I didn't turn the potentiometer to the right place.

For ideal amplifier, the Bode Plot should be a horizontal line. However, in reality, there are CMOS in the amplifier, and it is depended on A/s. Therefore, when the frequency gets very large, there is a pole that make the Bode plot goes down. That's the reason why in the measurement plots, the Bode plot for 3 circuits all decrease at the large frequency value.