ES7240

24-Bit, 192 kHz Stereo A/D Converter for PCM Audio

GENERAL DESCRIPTION

ES7240 is a high performance and low cost stereo analog to digital converter. ES7240 can accept I²S or Left Justified serial audio data format up to 24-bit word length. The device uses advanced multi-bit Δ-$\sum$ modulation technique to convert signal between analog and digital. The multi-bit Δ -$\sum$ modulator makes the device with low sensitivity to clock jitter and low out of band noise.

ORDERING INFORMATION

ES7240 -40°C ~ +85°C TSSOP-16

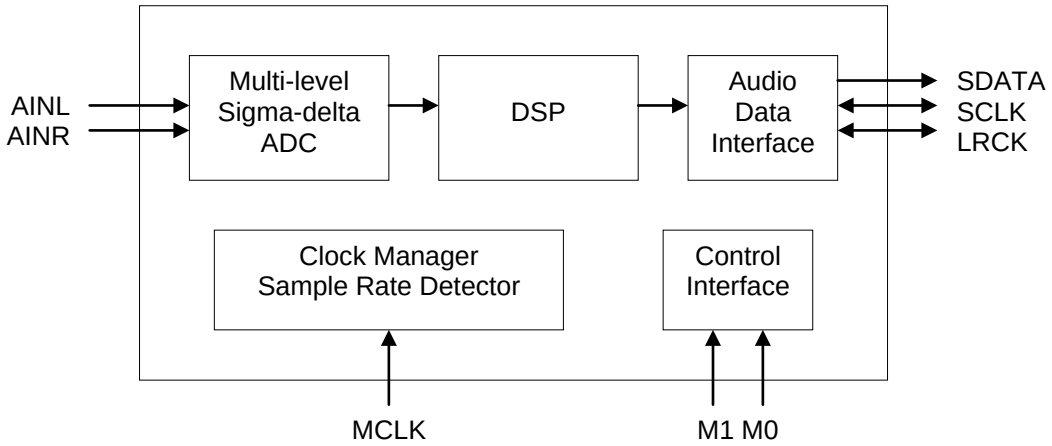
FEATURES

- 98 dB dynamic range
- -85 dB THD+N
- Up to 200 kHz sampling frequency
- I^2S or Left Justified audio data format, 16 to 24 bits
- VDDA and VDDD from 3V to 5.5V; VDDP from 1.4V to 5.5V
- Auto speed mode detection in slave mode; Auto MCLK divide detection in master mode

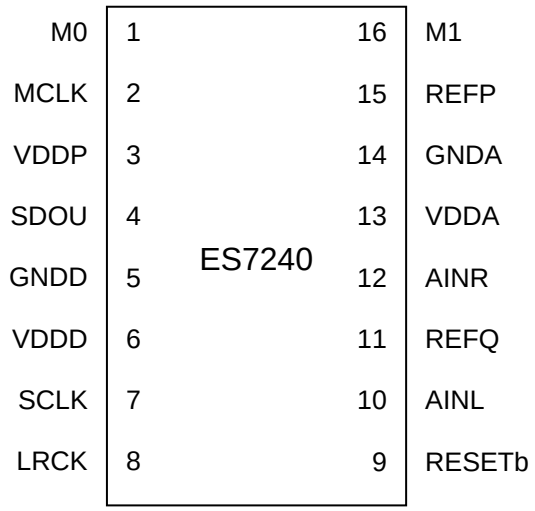
APPLICATIONS

- Digital Video Recorder
- Audio Recorder
- Digital Photo Frame
- LCD or Digital TV
- Set Top Box
- Car Audio
- A/V Receiver

BLOCK DIAGRAM



1. PIN DESCRIPTIONS



Pin Name	Pin number	Input or Output	Pin Description
M0, M1	1, 16	I	Mode selection
MCLK	2	I	Master clock
SCLK	7	I/O	Serial data bit clock
LRCK	8	I/O	Serial data left and right channel frame clock
SDOUT	4	O	Serial data output
RESETb	9	I	Active low chip reset
AINL, AINR	10,12	I	Analog left and right inputs
VDDP	3	I	Power supply for the digital input and output
VDDD/GNDD	6, 5	I	Digital power supply
VDDA/GNDA	13, 14	I	Analog power supply
REFP	15	O	Filtering capacitor connection
REFQ	11	O	Filtering capacitor connection

2. RECOMMENDED APPLICATION CIRCUIT

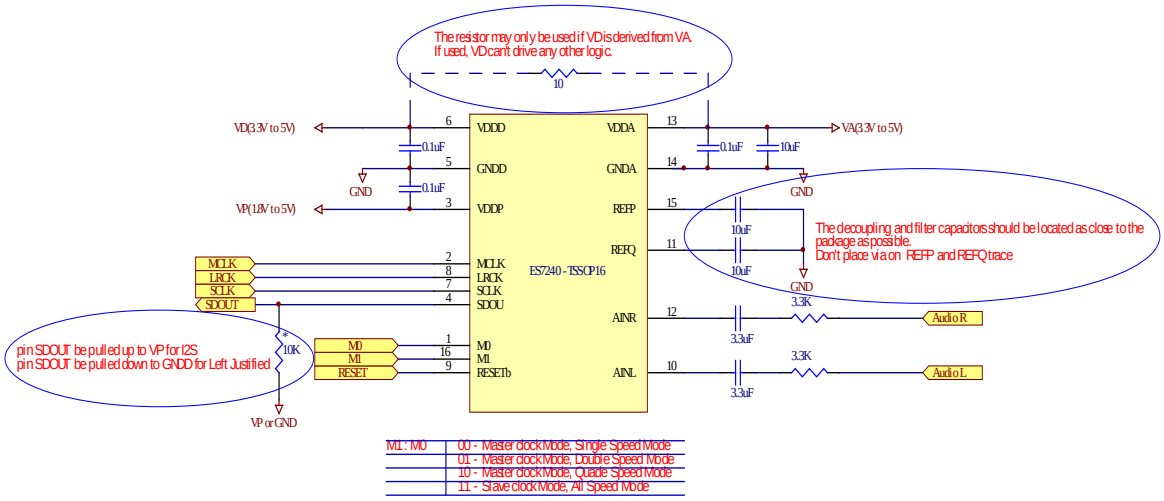


Figure 1 Recommended Application Circuit

3. APPLICATION DESCRIPTIONS

Master Clock Mode, Slave Clock Mode and Sampling Frequency

The device can work either in master clock mode or slave clock mode by setting mode control pins M1 and M0 according to Table 1.

Table 1 Mode Control

Pin	Input/Output	Pin Description
M1:M0	I	00 – master clock mode, single speed mode 01 – master clock mode, double speed mode 10 – master clock mode, quad speed mode 11 – slave clock mode, all speed modes

In master mode, LRCK and SCLK are derived internally from MCLK. The available MCLK/LRCK ratios are listed in Table 2. SCLK/LRCK ratio is always 64 in master mode.

In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with some specific rates. The device can auto detect MCLK/LRCK ratio according to Table 2. The device only supports the MCLK/LRCK ratios listed in Table 2. The LRCK/SCLK ratio is normally 64.

Table 2 Sampling Frequency and MCLK/LRCK Ratio

Speed Mode	MCLK/LRCK Ratio	Mater Clock Mode Sampling Frequency	Slave Clock Mode Fs Auto Detection Range
Single Speed	512	43kHz – 50kHz	8kHz – 50kHz
	256	8kHz – 50kHz	
Double Speed	256	86kHz – 100kHz	84kHz – 100kHz
	128	50kHz – 100kHz	
Quad Speed	128	172kHz – 200kHz	167kHz – 200kHz
	64*	100kHz – 200kHz	
*In Quad speed mode, 64 ratio only available in Master Mode			

According to the sampling rate, the device can work in three speed modes: single speed, double speed and quad speed. In master mode, mode pins M1 and M0 set the speed mode according to Table 1. In slave mode, the device can detect the speed mode automatically when the sampling rate falls into the auto detection ranges listed in Table 2.

Audio Data Output

ES7240 can accept I²S or Left Justified serial audio input data from 16-bit to 24-bit. The device can detect the data word length automatically. The relationship of SDATA, SCLK and LRCK with the two formats is shown through Figure 2 to Figure 3.

When device powers up, it will detect the logic level on SDOUT pin. If the logic level on SDOUT is high, ES7240 selects I²S format. If the logic level on SDOUT is low, ES7240 selects Left Justified format. SDOUT pin can be pull-up by a 10kΩ resistor to set I²S audio format, or pull-down by a 10 kΩ resistor to set Left Justified format.

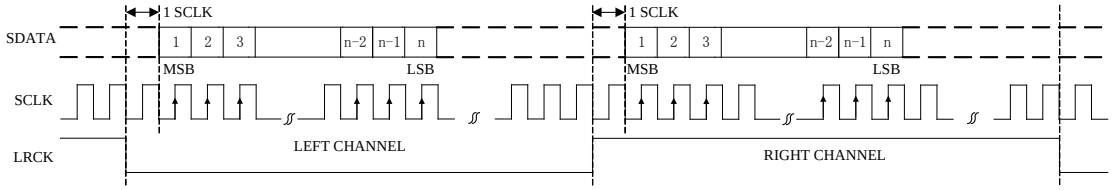


Figure 2 I²S Serial Audio Data Format Up To 24-bit

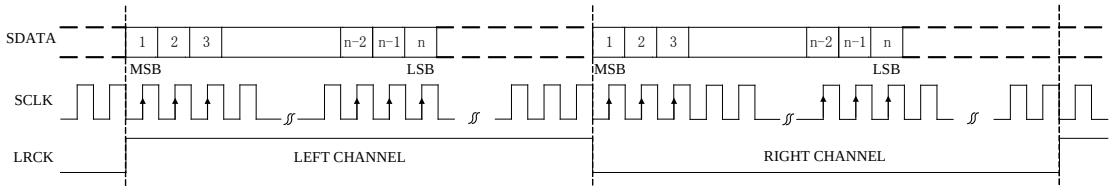


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

Power Up and Power Down

RESETb pin active low will put the device in power down mode. During power-up, RESETb pin should be hold at low level to keep the device in reset until the power supplies, clocks and mode selection pins are stable.

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

At or beyond this condition, operating continuously may cause permanent damage to the device. The performance and functions of the device are not guaranteed at these extremes.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+7.0V
Input Voltage Range	GNDD-0.3V	VDDP+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	3.0	3.3 or 5.0	5.5	V
VDDD	3.0	3.3	5.5	V
VDDP	1.4	3.3	5.5	V

Analog and Filter Characteristics and Specifications

Test conditions are as the following unless otherwise specify:
VDDA=5V, VDDD=3.3V, GNDA=0V, GNDD=0V, Ambient temperature=25°C,
Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256 or 128

PARAMETER	MIN	TYP	MAX	UNIT
Dynamic Range (Note 1)		98		dB
THD+N		-85		dB
Channel Separation (1KHz)		85		dB
Signal to Noise ratio		98		dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				

Passband	0		0.2083	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level (Note 2)		1		Vrms
Input Impedance		20		KΩ

Note
1. The value is measured used A-weighted filter. If not use, the result will decrease 2-3 dB.

Serial Audio Port Switching Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
MCLK Frequency			51.2	MHz
MCLK Duty Cycle		40	60	%
LRCK Frequency			200	KHz
LRCK Duty Cycle		40	60	%
SCLK Frequency			26	MHz
SCLK Pulse Width Low	T_{SCKL}	15		ns
SCLK Pulse Width High	T_{SCKH}	15		ns
SCLK Rising to LRCK Edge Delay	T_{LRH}	10		ns
SCLK Rising to LRCK Edge Setup Time	T_{RSU}	10		ns
SDATA Valid to SCLK Rising Setup Time	T_{SDS}	10		ns
SCLK Rising to SDATA Hold Time	T_{SDH}	10		ns

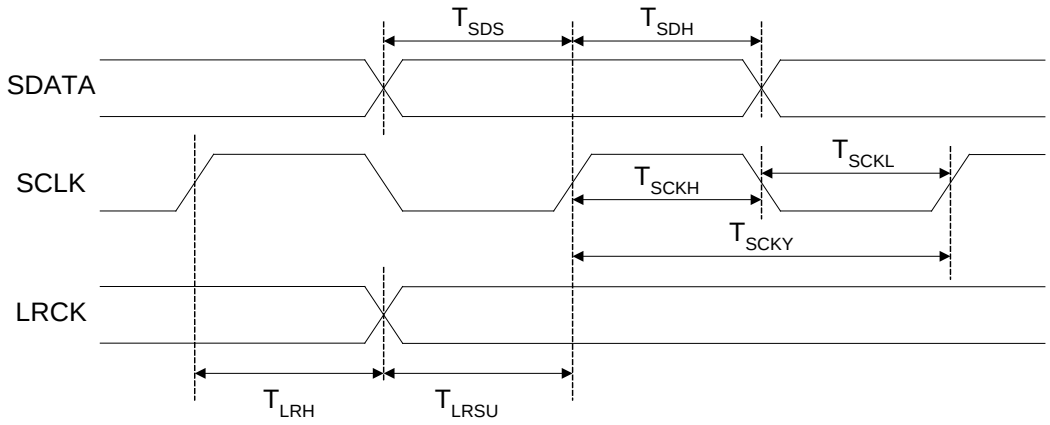


Figure 3 Serial Audio Port Timing

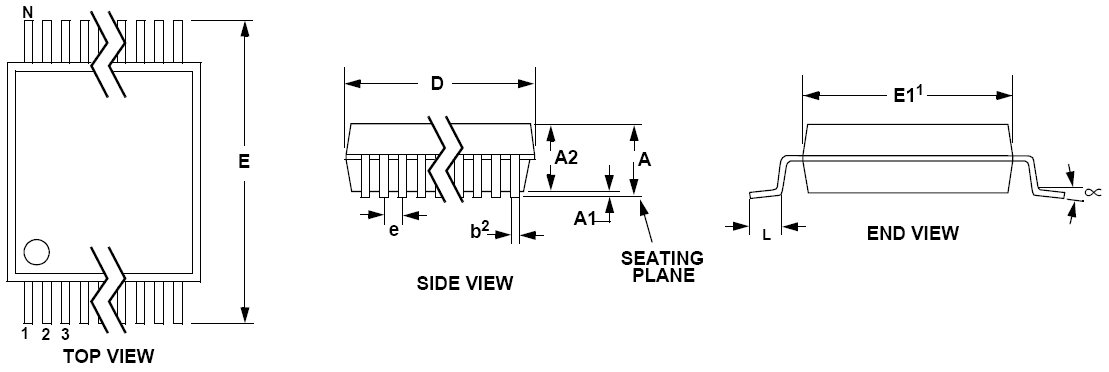
DC Characteristics and Specifications

PARAMETER		MIN	TYP	MAX	UNIT
Power Supply Current (Normal Operation Mode)					
VDDA=5V	IA		23.3		mA
VDDA=3.3V	IA		21.1		mA
VDDD, VDDP=5V	ID		32		mA
VDDD, VDDP=3.3V	ID		14		mA
Power Supply Current (Power Down Operation Mode)					
VDDA=5V	IA		1.5		mA
VDDA=3.3V	IA		1.2		mA

VDDD, VDDP=5V	ID		TBD		mA
VDDD, VDDP=3.3V	ID		1.1		mA
Digital Voltage Level					
Input High-level Voltage	VIH	0.7VDDP			V
Input Low-level Voltage	VIL			0.3VDDP	V
Output High-level Voltage	VOH	0.7VDDP			V
Output Low-level Voltage	VOL			0.1VDDP	V

5. PACKAGE INFORMATION

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
μ	0°	4°	8°	0°	4°	8°	

Note:
1. Reference JEDEC MO-153

6. CONTACT INFORMATION

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