1 Laboratory 6, Part I

Oscillator Design

Summary: For the first part of Laboratory 6 students will design their own 5.9 GHz oscillator. This is the most design intensive of the pre-project Laboratories. Students will have two weeks to design their oscillator, submitting their final designs by November 9th for fabrication.

1.1 Useful resources

https://www.rogerscorp.com/documents/725/acs/RO3200-Laminate-Data-Sheet-RO3203-RO3206-RO32
pdf

1.2 Preparation

1. You are now dangerous, you have built up your ability in MWO to develop individual circuit elements, and subsequently cascade them to determine the end-to-end performance of the ensemble. In addition, you have gathered an intuition in impedance matching. You mastered this all in Laboratory 4, now you will further refine your art.

2. We will use the design procedure described in class for our oscillators. It doesn't provide the best prediction of osillation frequency or output power but, provided you follow the recipe closely, almost guarantees oscillation.

3. The first step is to determine the bias your oscillator will operate with. For your amplifier designs you desired unconditional stability, now you desire the opposite, you want to find a bias that produces a $k \ll 1$ at your frequency of oscillation.

4. Using your class notes, select a bias, and corresponding S-parameters, that minimizes k. You may have to do this iteratively, checking the stability for various bias levels. I found that a collector bias of 2.5 V and 7.5 mA worked well. First, however, you need to convert the 2-port NXP S-parameters to 3-port S-parameters (relations provided at the back of this report), so you can properly de-stabilize your transistor. A short Matlab or Python script is likely in order. Use it to convert the 2-port S-parameters at a given bias to 3-port S-parameters and

write them into the appropriate Touchstone .s3p file format. This will provide you access to all terminals of the transistor.

5. Import your .s3p files into MWO to check the stability factor, k. Do this by creating a new schematic and import your .s3p file. Ground the port representing the base of the transistor. A small amount of inductance in series with the base of the transistor will help further enhance the instability.

6. With a small amount of base inductance I was able to obtain $k <= -.9$. Your schematic should look something like that shown in Figure 1. It might be helpful to add text to your schematic to keep track of the transistor terminals.

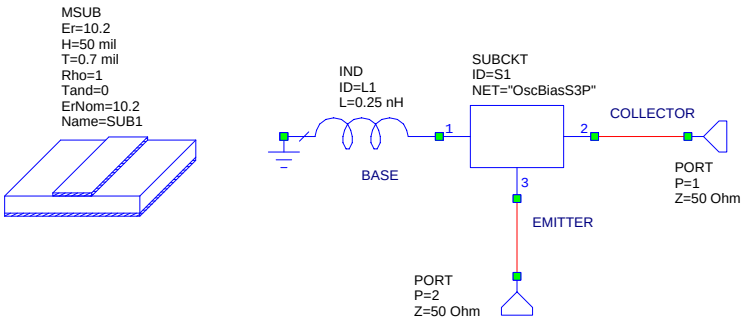

Figure 1: Adding inductance to the base of the transistor to improve its instability, after converting the transistor's .s2p file to .s3p format. The substrate definition is not necessary for this schematic, it was only included by default.

7. Now you need to embed around the transistor its packaging effects, and find a reasonable way to make a connection from the base to ground (assuming you chose this method), remembering we have to fight via inductance. The via inductance at 5.9 GHz is likely much larger than the optimal amount of base inductance you need.

8. Using the datasheet for the BFU730F transistor and your work in in Laboratory 4 as a guide, open up a new schematic and generate the various microstrip lines, steps, and transitions necessary to represent the footprint of the transistor, and connect it to the external world. The transistor has two emitter contacts. Because the packaging around the final transistor layout got very busy, I chose to only route out the larger of the two emitter pads, connecting the smaller to the former. I terminated the end of the smaller pad with a section of open transmission line.

9. Place your .s3p file for your transistor in the schematic view of your footrpint and wire it to the terminals. This will allow you to simulate the effects of the packaged device, the .s3p file will have no bearing on the layout.

10. Go to the layout window and snap together the various components. It should appear something like that shown in Figure 2. Note that I have connected the larger and shorter emitter pads together in the layout.

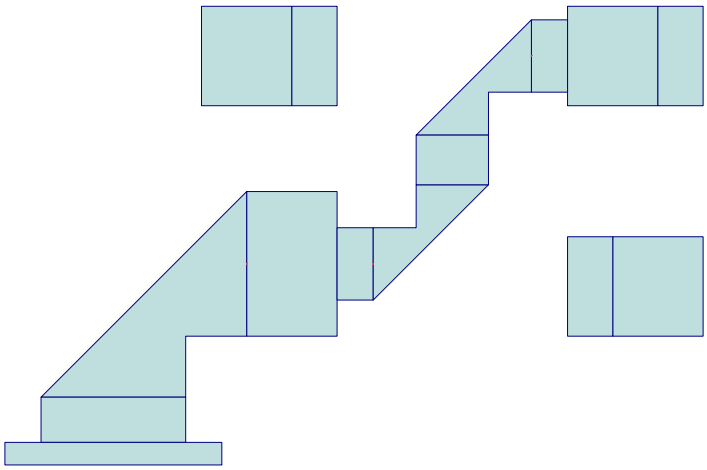

Figure 2: Layout of footprint for NXP BFU730F transistor. Base contact is at the upper left, collector at the lower right, and emitter terminal at the lower left.

11. You have now built out your first sub-circuit. Next, you will generate the remaining sub-circuits for the oscillator before combining them for the final artwork.

12. Now, you need to represent the base inductance of your initial stability simulation, with microstrip components, and add a bias network for the base. This is a little tricky, you need some inductance to ground, but at the same time, need to pass DC and have some decoupling at low frequency. My approach was to do the following, I added a narrow section of transmission line to the connection with the base, to synthesize some inductance. I then connected a microstrip-T, **Elements** $\Rightarrow$ **Microstrip** $\Rightarrow$ **Junctions** $\Rightarrow$ **MTEE** to the output of the line. To the the in-line output of the Tee, I connected a radial stub. The radial stub will provide a short to ground at the design frequency.

13. We need to make the orthogonal port of the Tee appear as an open. How do we do so? Correct, a high-impedance quarter-wave line terminated in a short.

14. Put in your high-impedance line and another Tee junction at its end. At this point, you will need to put in a decoupling capacitor (say 0402 10 pF), a via to ground, and provisions for your bias network. This itself will include a bias resistor, with the associated artwork, some more decoupling capacitance, a via, and a large pad for you to solder your DC connection to. You are dangerous, but have limited time, so I will show you what my circuitry looked like for the high-impedance line and above, shown in Figure 3. Note that I represented the DC pad as a wide, long, open line.

15. Make sure you have the vias represented exactly as shown, or it will be very hard to realize them when your circuit is fabricated.

16. Now assign your length of high-impedance line to the base, radial stub flare angle and radius, and length of shunt high-impedance lines as variables for tuning.

17. Open up a new schematic and import your sub-circuits for your transistor with footprint and base circuit that you just completed.

18. Place ports on the collector and emmitter and simulate your circuit.

19. Open up a new graph and plot out the stability factor and magnitude (linear) of S_{11} and S_{22}.

20. Now tune your variables so that the stability factor is minimized and the input and output match at 5.9 GHz are as great as possible in the positive sense (≥ 1). You will notice other frequencies where these conditions are met as well.

21. Which reflection coefficient is greater? For my circuit the collector was greater. This was the port I chose to make my load. The other port, the emitter, I chose to be my output.

22. When you are satisfied with the tuning, complete the layout of your base circuit. Mine appeared as shown in Figure 4. You will notice that I represented the short high-impedance line with a microstrip bend **Elements** $\Rightarrow$ **Microstrip** $\Rightarrow$ **Bends** $\Rightarrow$ **MCURVE**, this helped in the final layout of the completed oscillator, you may want to choose to do the same.

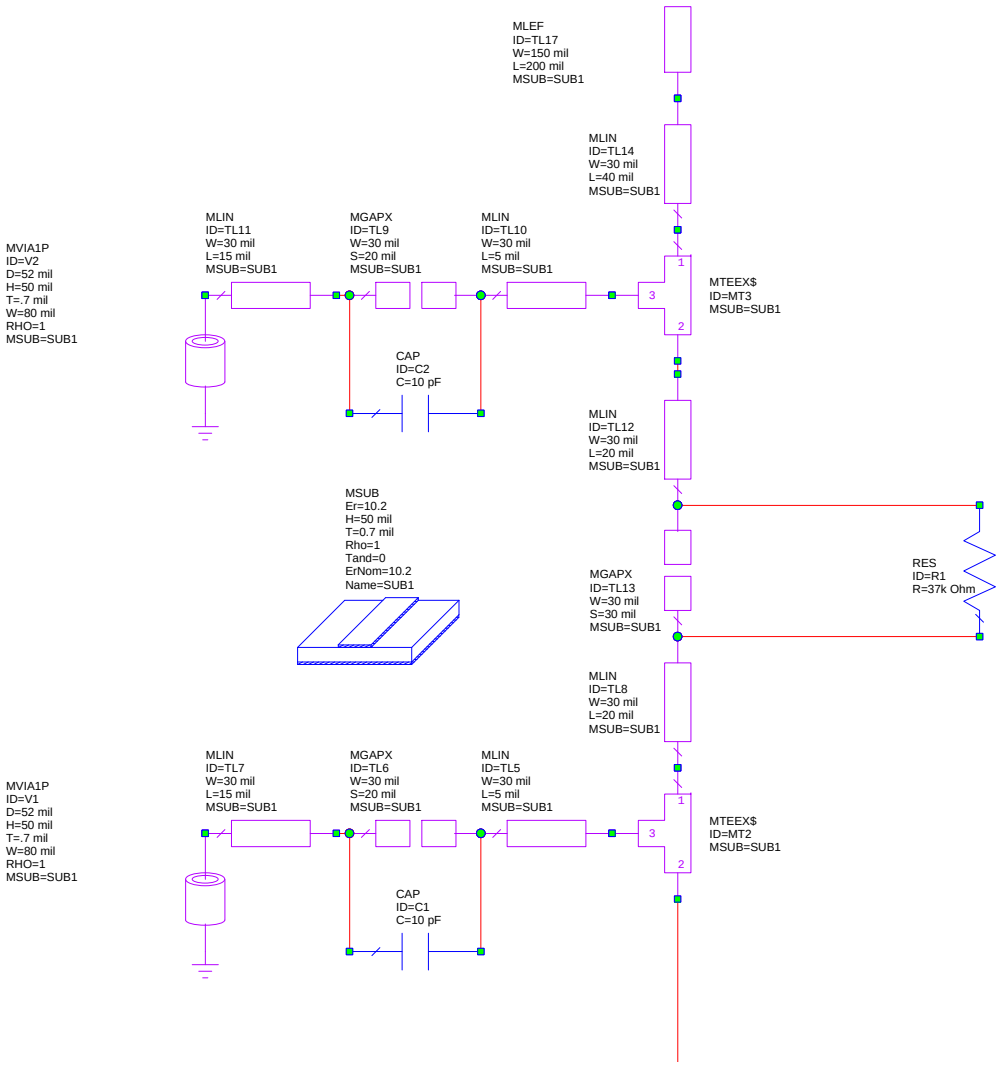

Figure 3: Schematic of bias circuit for the base. The high-impedance line feeding this network enters in from the bottom.

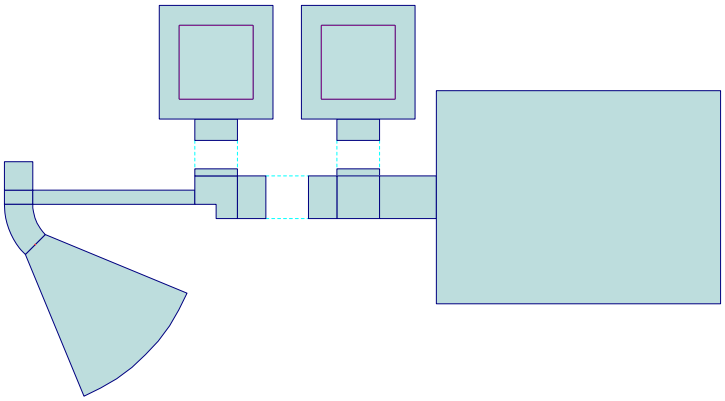

Figure 4: Layout of the base RF and DC bias circuitry. Connection to the base of the transistor is at the upper left. The DC connection is at the far right.

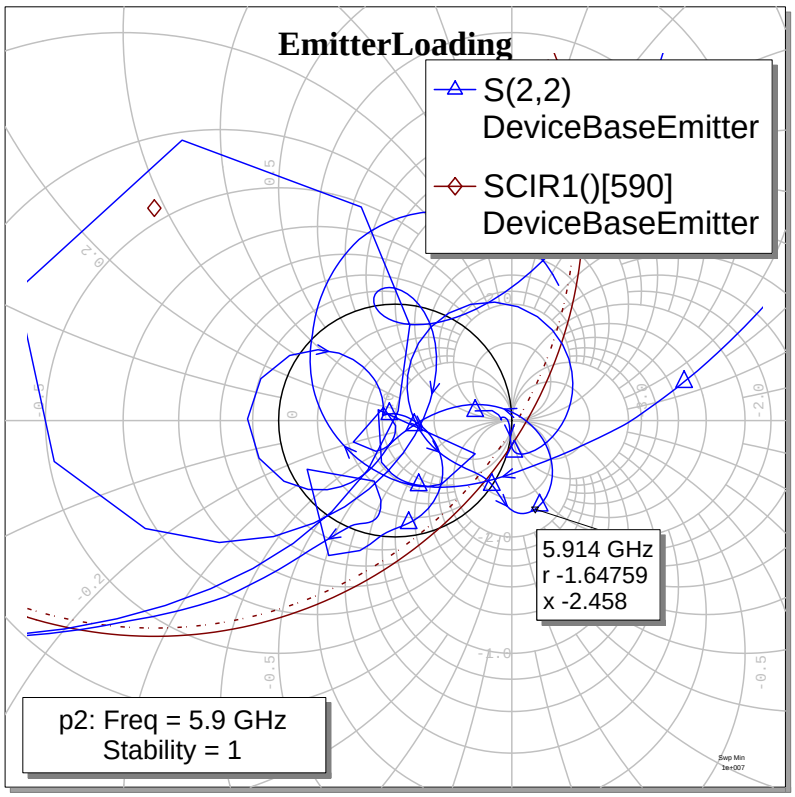

Figure 5: Simulating the effect of the output matching network, as viewed on the expanded Smith chart, port 2 is on the collector of the device. At 5.9 GHz the circuit is suitably unstable with only a small section of low impedance line in the output. The stability circle, plotted at 5.9 GHz, reveals that the entire interior of the normal, $\Gamma = 1$, Smith chart is unstable.

23. Open up a new schematic to design your next sub-circuit, the output network. Your output network has to serve two purposes. The first is to present the device the correct impedance transformation from 50 Ω to ensure oscillation. The second is to provide the necessary DC bias path.

24. I chose the emitter to be my output, and needed a small section of low impedance line to ensure oscillation for any termination at the output[1]. Because the emitter is grounded, I also had to provide a path to ground at DC, but have this path open at 5.9 GHz. To do so, I added a section of quarter wave, high impedance line in shunt with the output, with a via return to ground. I tuned the length of this line to ensure that it was open at 5.9 GHz as viewed by the output line. Finally, I placed a 10 pF cap at the output as a DC block to the output, but acting as a low impedance at 5.9 GHz (approximately -j2.7 Ω).

25. Complete your tuning and layout. When completed, assuming you used the same strategy as I did, it should appear something like that shown in Figure 6.

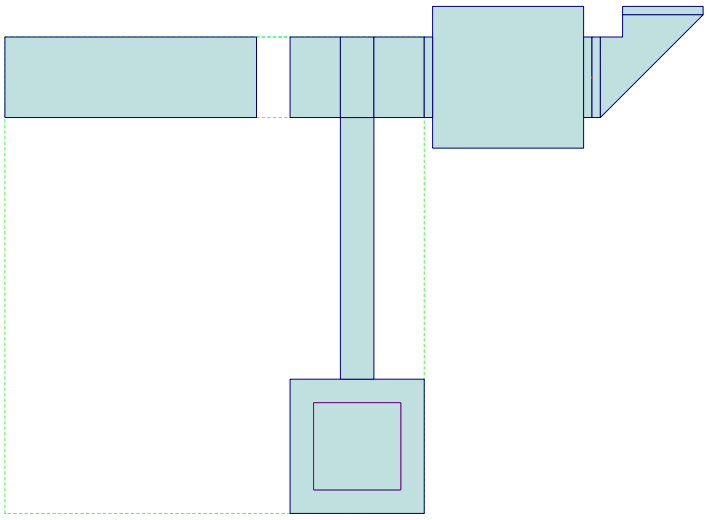

Figure 6: Layout of the output network. The network attaches to the emitter at the upper right, the output is at the middle left. The gap in the center is for an 0402 10 pF capacitor, serving as a DC block.

[1]Note that this is not strictly necessary. We only need to ensure we transform impedance seen by the output to an impedance within the instability circle. Having the circuit unstable over the entire Smith chart will desensitize us from manufacturing tolerances, aiding our chances of success.

26. The last network that remains to complete is your load network, or resonant circuit at the collector, and the necessary bias circuitry. To ensure oscillation at the frequency of interest, we will look at the input impedance to the collector at 5.9 GHz. It will be composed of a reactive component and a negative resistance, indicating that the circuit is cable of delivering power.

27. Create a new schematic and in it place the interconnection of sub-circuits you have already developed; the footprint of the device, the base network, and the emitter network.

28. Simulate the circuit and open up a new graph, where you will plot out the real and imaginary components of the impedance looking into the collector. I named my circuit *OSCILLATOR*, shown in Figure 7, and show the real and imaginary components of Z_{11} plotted in Figure 8.

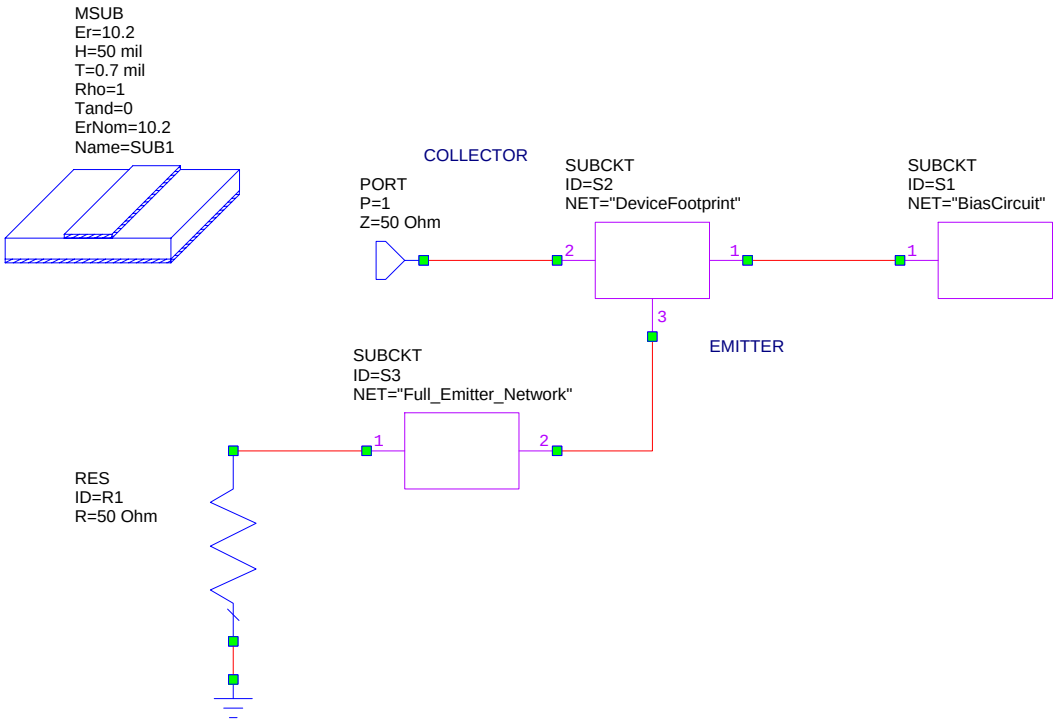

Figure 7: Schematic for generation of the load, or resonant network, attached to the collector.

29. We will ensure oscillation by presenting the collector with the conjugate imaginary compo-

nent of its input impedance at 5.9 GHz. The input impedance has a negative reactance, so a positive reactance (inductive) is required of this new network. Also, to ensure proper oscillator start up, we will add a value of resistance to this, roughly $1/3$ of the absolute value of the real component of the input impedance, looking into the collector.

30. Open up a new schematic to build out your collector network, to present the collector with the impedance value above. Assuming you also require inductance, add the necessary components, including gaps for surface mount components, to provide the collector with the correct impedance. To create an RF short for your series inductance and resistance, use a radial stub.

31. Tune your values of inductance, resistance, and stub length so that your collector network presents the necessary impedance. I have named my network *Collector Resonator*, its impedance response is plotted with that looking into the collector in Figure 8.

32. Once you are satisfied, you will need to place in the necessary bias for the collector. I did this by placing a microstrip tee between my inductor and resistance. Off the tee I placed a quarter wave section of high-impedance line. At the other end of the high-impedance line I placed a microstrip cross. Across the horizonal arms I placed some decoupling capacitance to ground with a via, and on the other a radial stub to ensure a low RF impedance (short) at 5.9 GHz.

33. On the fourth port of the microstrip cross, I placed a 100 Ω bias resistor for the collector and at its exit some more decoupling capacitance and a bias pad. The upper half of the bias circuit appears as shown in Figure 9.

34. Tune the line lenghts for the collector load network, to ensure the collector is presented with the appropriate impedance. Go to the layout window and snap your components together. It should appear something like that shown in Figure 10.

35. All the sub-circuits have now been completed. Create a final schematic and place in all of your sub-circuit building blocks, with one port at the emitter.

36. Complete the layout of your final circuit by snapping the building blocks together. You may need to go back and re-route some of your sub-circuits should conflicts arise (say if two radial stubs are too close together). The final layout should appear something like that shown in Figure 11.

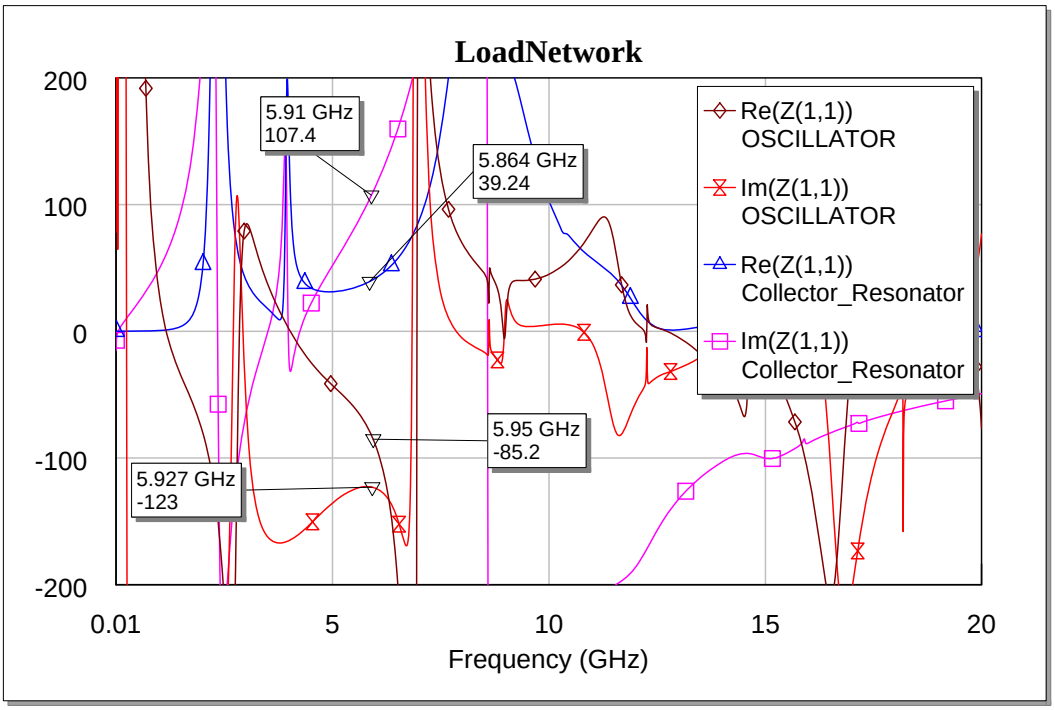

Figure 8: Input impedance of the collector, with previously designed networks at the transistor's base and emitter. Also shown are the values of impedance presented by the load network to be attached to the collector.

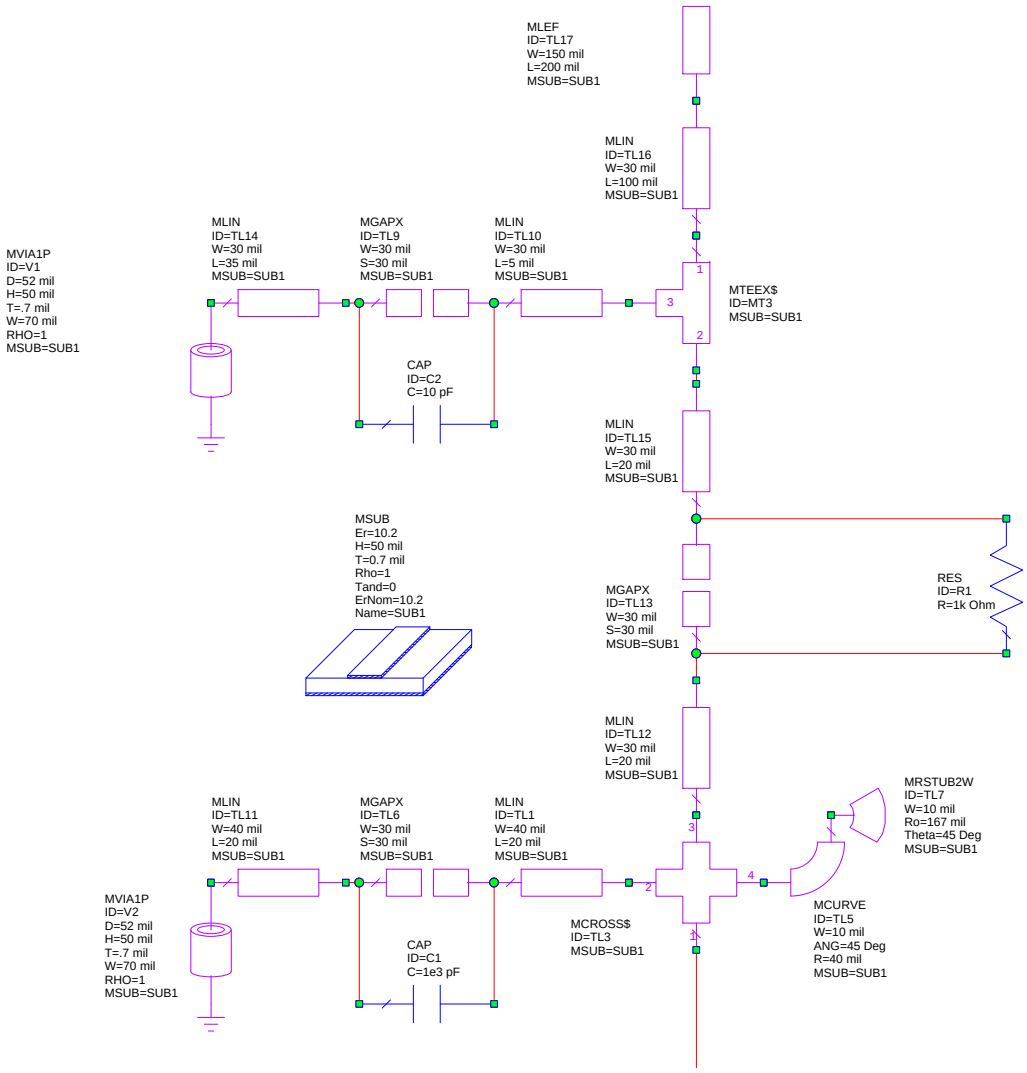

Figure 9: Collector load and bias circuit.

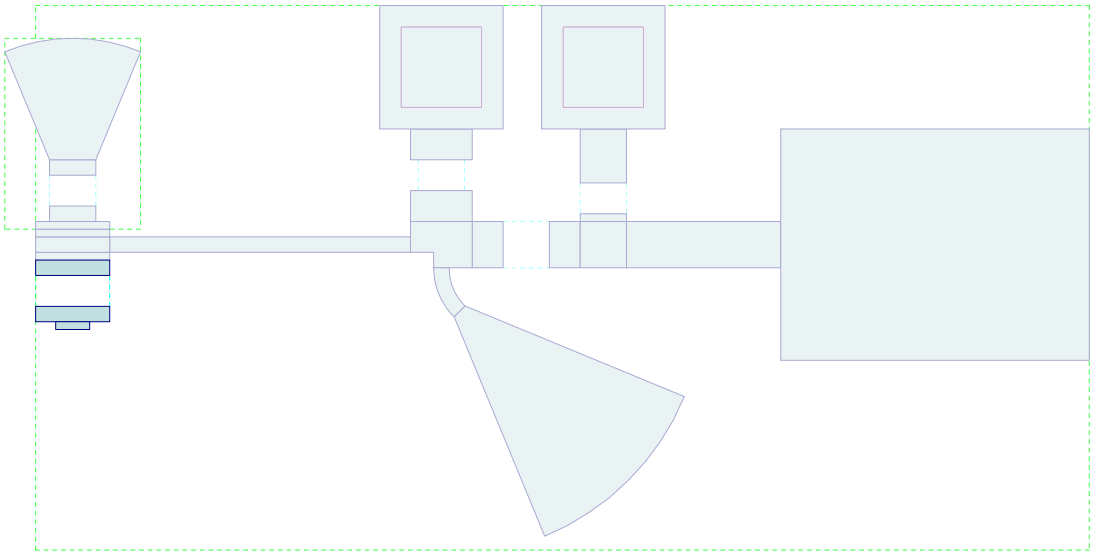

Figure 10: Collector bias circuit.

37. **Email your file to drussell@caltech.edu no later than Thursday at noon on November 9th.**

2 Conversion of 2-port to 3-port S-parameters

To convert your 2-port S-parameter files to a 3-port, freeing your emitter terminal from ground and allowing you access to all terminals of the transistor, use the relations below in a simple script.

$$\begin{bmatrix} S_{11}+\frac{\Delta_{11}\Delta_{12}}{4-\xi} & S_{12}+\frac{\Delta_{11}\Delta_{21}}{4-\xi} & \frac{2\Delta_{11}}{4-\xi} \\ S_{21}+\frac{\Delta_{22}\Delta_{12}}{4-\xi} & S_{22}+\frac{\Delta_{22}\Delta_{21}}{4-\xi} & \frac{2\Delta_{22}}{4-\xi} \\ \frac{2\Delta_{12}}{4-\xi} & \frac{2\Delta_{21}}{4-\xi} & \frac{\xi}{4-\xi} \end{bmatrix} \tag{2.1}$$

where

$$\xi = S_{11} + S_{12} + S_{22} + S_{21} \tag{2.2}$$

and

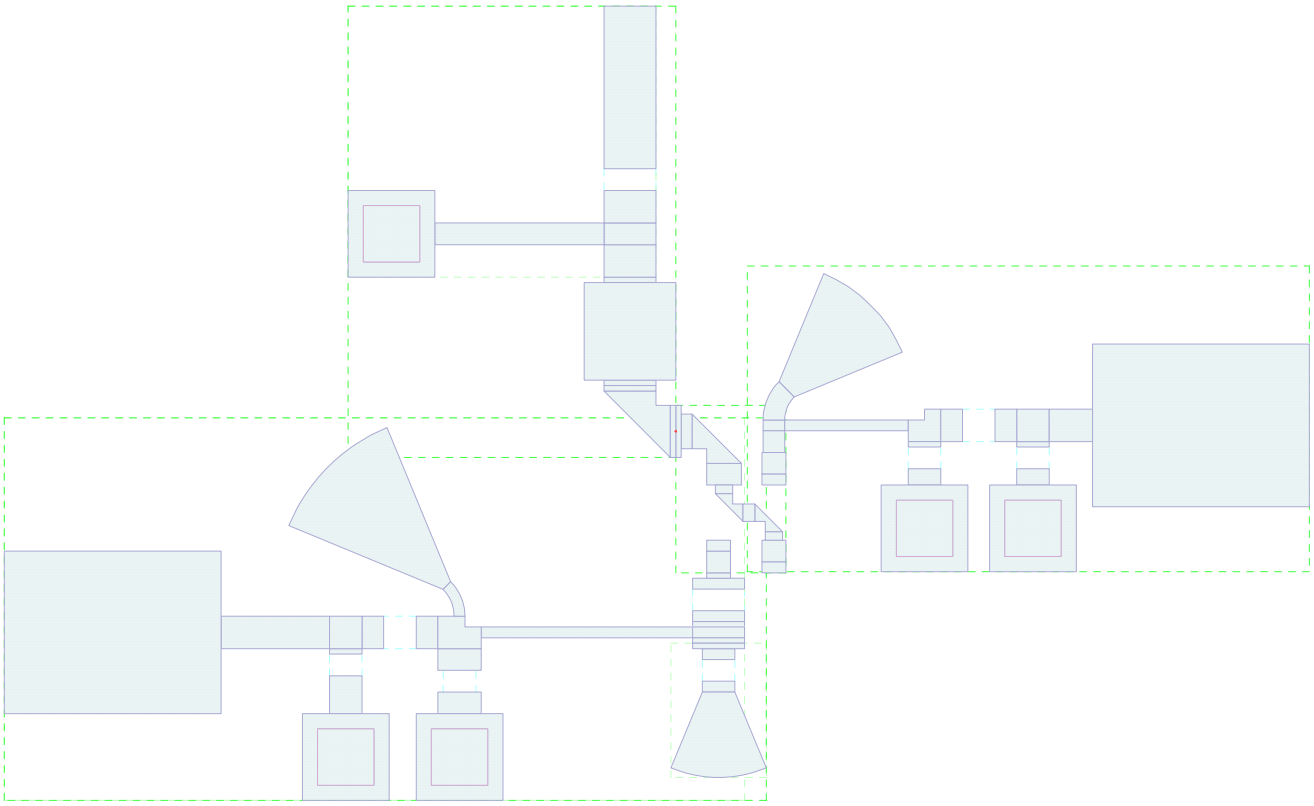

Figure 11: Layout of the completed oscillator. The output is at the top. Collector and base bias pads are at the left and right sides of the layout respectively.

$$\Delta_{11} = 1 - S_{11} - S_{12} \tag{2.3}$$

$$\Delta_{12} = 1 - S_{11} - S_{21}$$

$$\Delta_{21} = 1 - S_{12} - S_{22}$$

$$\Delta_{22} = 1 - S_{21} - S_{22}$$

In your script, include in a section to write your results to a .s3p file which you will import into MWO. My Matlab listing is shown below:

```
fileID = fopen('2V30mA.s3p','w');
fprintf(fileID,'%s\n','!3-port S-parameters');
fprintf(fileID,'%s %s %s %s %s %s\n','#', 'GHz', 'S', 'MA', 'R', '50');
for n=1:max(size(Freq))
   fprintf(fileID,'%f %f %f %f %f %f %f\n', Freq(n), abs(S11(n)),
       angle(S11(n))*180/pi, abs(S12(n)), angle(S12(n))*180/pi, abs(S13(n)),
       angle(S13(n))*180/pi);
   fprintf(fileID,'%f %f %f %f %f %f\n', abs(S21(n)), angle(S21(n))*180/pi,
       abs(S22(n)), angle(S22(n))*180/pi, abs(S23(n)), angle(S23(n))*180/pi);
   fprintf(fileID,'%f %f %f %f %f %f\n', abs(S31(n)), angle(S31(n))*180/pi,
       abs(S32(n)), angle(S32(n))*180/pi, abs(S33(n)), angle(S33(n))*180/pi);
end
```