Design and Optimization of Broadband Asymmetrical Multisection Wilkinson Power Divider

Homayoon Oraizi, *Senior Member, IEEE*, and Ali-Reza Sharifi

***Abstract*—In this paper, a numerical algorithm based on the method of least squares (MLS) is presented for the design and optimization of a Wilkinson power divider for arbitrary power division between its outputs in a specified frequency bandwidth incorporating source and load impedance matching. At first, its transmission, admittance, and scattering matrices are determined successively by considering the dispersion and dissipation models of substrate and metallic strips. An error function is then constructed for the desired output power division, maximum level of isolation between them, and the least amount of reflected power. Minimization of the error function with respect to the widths and lengths of strips and values of resistors provides their optimum values. A procedure is provided for the *initial* design and determination of *initial* values of parameters of a Wilkinson power divider based on the method of even- and odd-mode analysis. The optimum design of the Wilkinson power divider by the proposed MLS procedure is validated by available full-wave analysis software and fabrication and measurement of two samples.**

***Index Terms*—Computer-aided design (CAD), method of least squares (MLS), microwave components, optimization, power divider, Wilkinson power divider.**

I. Introduction

POWER dividers vary widely with particular advantages and disadvantages. The Wilkinson power divider was invented in 1960 [1] and has completely matched output ports with sufficiently high isolation between them. This device is also potentially lossless provided that no reflected power from output ports enters into it. This divider has wide applications in microwave circuits and antenna feeds, but it has a narrow bandwidth, which has the best performance at a center frequency. Several schemes have been devised to increase its bandwidth. The main proposal was made in 1968 [2], which used series connection of several sections having considerably increased bandwidth and high isolation between outputs for equal power division. A device for unequal power division between outputs was proposed in 1965 [3]. The even- and odd-mode analysis was employed for a single-section Wilkinson power divider. A procedure based on the even- and odd-mode analysis was used for the design of a three-port multisection power divider with unequal output powers in 1971 [4]. It should be noted that the even- and odd-mode method of analysis is useful for axially symmetric circuits. It is not applicable to asymmetrical circuits, which are tackled in this paper. However, the method devised for determination of scattering matrix elements was applicable for the case of neglecting dispersion and dissipation effects. In recent years, several schemes have been proposed to decrease the size of transmission lines in order to facilitate their application in microwave integrated circuits (MICs) and monolithic microwave integrated circuits (MMICs) [5], [6]. A power divider was proposed and fabricated using lumped components and compensation capacitors for increasing frequency bandwidths [7].

In this paper, a design and optimization procedure based on the method of least squares (MLS) is proposed to increase the bandwidth of a Wilkinson power divider. First, the even- and odd-mode analysis is used to determine the *initial* element sizes (namely, the widths and lengths of metallic strips and values of resistors) of a multisection Wilkinson power divider for arbitrary power division together with source and load impedance matching in a specified frequency bandwidth. Second, the design optimization for the asymmetrical Wilkinson power divider is achieved by a proposed procedure based on the MLS.

The dispersion and dissipation models of microstrips are also incorporated into the proposed procedure.

In Section II, the Wilkinson power divider is divided into two networks. First, their transmission and admittance matrices are determined, and then the scattering matrix of the device is calculated. Finally, an error function is constructed over the required frequency bandwidth to provide the required power division between output ports and minimize the reflected power from the input port and maximize the isolation among output ports. The error function depends on the metallic strip widths and lengths and values of resistors. Minimization of the error determines their optimum design values.

However, any minimization routine requires initial values of variables to begin the algorithm. Procedures for evaluation of initial values of metallic strip widths (or their characteristic impedances) and their lengths and the values of resistors are provided in Section III. These procedures may be considered as an approximate design method for the Wilkinson power divider.

In Section IV, the computer implementation of the proposed MLS design and optimization method is described. Several design examples are presented, together with the description of input parameters and output values and diagrams.

In Section V, the MLS optimum design, simulation by Microwave Office, fabrication, and measurements of two samples of Wilkinson power dividers are described. The performance of the dividers by the three methods (i.e., MLS, software, and measurements) are compared, which indicate the efficacy of the proposed design and optimization method of least squares. In Section VI, the conclusions of this paper are presented. An abstract of the MLS algorithm for design and optimization of Wilkinson power dividers is described in [8].

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The authors are with the Department of Electrical Engineering, Iran University of Science and Technology, Narmak, Tehran 16844, Iran (e-mail: h_oraizi@IUST.ac.ir; alireza_sharifi@ee.iust.ac.ir).

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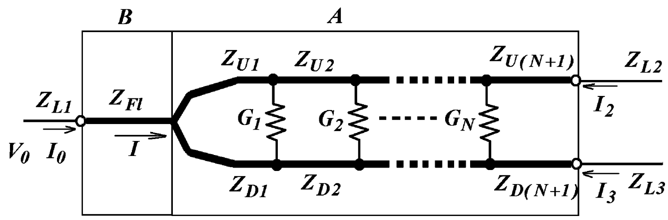


Fig. 1. Multisection Wilkinson power divider.

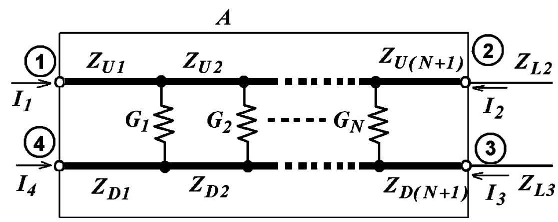


Fig. 2. Converting the three-port network in Fig. 1 to a four-port network.

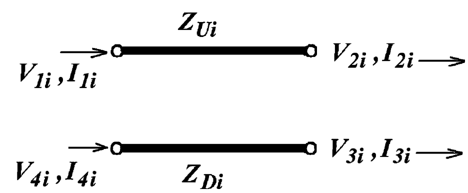


Fig. 3. Two parallel transmission lines.

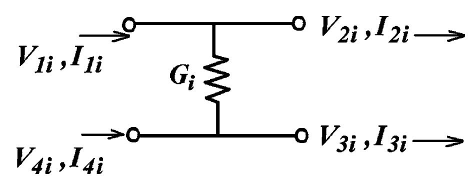


Fig. 4. Resistor connected to parallel transmission lines on both sides.

It should be noted that the available commercial microwave software packages such as HFSS and Microwave Office are mainly devised for the analysis of microwave structures. Their applications for design and synthesis in combination with optimization routines (such as the Genetic Algorithm) are, at best, a blind process and very time-consuming with respect to machine CPU time and skilled manpower effort. Design tasks that are time-consuming may disrupt the overall schedule of a project. The design and optimization of microwave circuits and components are too complicated and involved to be set aside in favor of the commercial analysis software. Development of effective design and optimization procedures for microwave circuits and components are desirable and required now, as they were before the availability of commercial software packages. The discipline of optimization is of serious interest in other fields of science and engineering.

The proposed procedure based on the MLS designs and optimizes an asymmetrical multisection Wilkinson power divider and determines its configuration for any specification of arbitrary power division ratio between its outputs and complex impedance matching among its input and output ports (namely, source and load impedances) in a specified frequency bandwidth. Therefore, the significance of the design method is the provision of arbitrary power division, impedance matching, and the realization of the broadest possible bandwidth. Furthermore, the available design methods for the Wilkinson power divider are not developed to minimize insertion loss, realization of arbitrary phase difference between output ports, and complex impedance matching among input and output ports in a specified frequency bandwidth. Such specifications may be readily incorporated into the design procedure by the MLS.

II. Design and Optimization Procedure for a Wilkinson Power Divider

Here, an error function is constructed based on the MLS for the optimum design of an asymmetrical multisection Wilkinson power divider.

A. Determination of Scattering Matrix

Consider a multisection Wilkinson power divider shown in Fig. 1, which is to provide an arbitrary power division between its outputs over a specified frequency bandwidth with different source and load impedances connected to its ports. In this paper, Z_{Ui} and Y_{Ui} denote the characteristic impedance and admittance of the ith section of the upper transmission line, respectively, and Z_{Di} and Y_{Di} denote those of the ith section of the lower transmission line, respectively. Also, G_i denotes the conductance inserted between the ith section of the upper and lower transmission lines of the divider.

The optimum design procedure requires determination of the widths and lengths of metallic strips and values of resistors of the divider. An error function is constructed according to the specifications, which depends on the geometrical configuration and above parameters of the divider, and its minimization determines their optimum values. Now, the power divider is separated into two networks, called A and B, depicted in Fig. 1.

The three-port network A is shown as a four-port network in Fig. 2, which is a tandem connection of network blocks consisting of two adjacent transmission lines shown in Fig. 3 in series with shunt conductances (G_i) shown in Fig. 4. Consequently, the transmission matrix of the two adjacent lines "as a four-port network" in Fig. 3 is stated in (1), shown at the bottom of the following page, where subscript k indicates the kth discrete frequency in the bandwidth, $\gamma_{Ui,k}$ and $\gamma_{Di,k}$ are the propagation constants of the upper and lower transmission lines of the ith section, respectively, and l_{Ui} and l_{Di} are the lengths of upper and lower transmission lines of the ith section, respectively. The transmission matrix of ith section in (1) is denoted by $[P]_{i,k}$.

The transmission matrix of the shunt conductance of the four-port network in Fig. 4 is determined as follows:

$$\begin{bmatrix} V_{i1} \\ V_{4i} \\ I_{1i} \\ I_{4i} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ G_i & -G_i & 1 & 0 \\ -G_i & G_i & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix}. \tag{2}$$

Its transmission matrix in (2) is denoted by $[G]_i$. Consequently, the $ABCD$ matrix of the four-port network A in Fig. 2 is [9]–[11]

$$[TA]_k = \left(\prod_{i=1}^{N}[P]_{i,k} * [G]_i\right) * [P]_{N+1,k} \tag{3}$$

and its corresponding transmission equation may be written as follows:

$$\begin{aligned}\begin{bmatrix} V_1 \\ V_4 \\ I_1 \\ I_4 \end{bmatrix} &= [TA]\begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix} \\ &= \begin{bmatrix} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{bmatrix}\begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix} \\ &= \begin{bmatrix} [C11] & [C12] \\ [C21] & [C22] \end{bmatrix}\begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix}\end{aligned} \tag{4}$$

where the block $ABCD$ matrices $[C11], \ldots,$ are defined above. Now, the admittance matrix of the four-port network A in Fig. 2 may be written as

$$\begin{aligned}\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} &= \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \\ &= \begin{bmatrix} [D11] & [D12] \\ [D21] & [D22] \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}\end{aligned} \tag{5}$$

where the block admittance matrices $[D11], \ldots,$ are defined above. The admittance matrix may then be expressed in terms of the transmission matrices [12]

$$\begin{aligned}&\begin{bmatrix} [D11] & [D12] \\ [D21] & [D22] \end{bmatrix} \\ &\quad = \begin{bmatrix} [C22][C12]^{-1} & [C21] - [C22][C12]^{-1}[C11] \\ -[C12]^{-1} & [C12]^{-1}[C11] \end{bmatrix}.\end{aligned} \tag{6}$$

The input node of network A in Fig. 1 is at the same potential as input ports 1 and 4 in Fig. 2

$$V_1 = V_4 = V \tag{7}$$

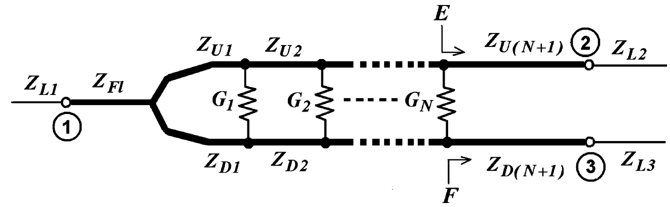


Fig. 5. N-section Wilkinson power divider.

and the input current into node 1 of network A in Fig. 1 is equal to the sum of input currents into input ports 1 and 2 in Fig. 2

$$I = I_1 + I_4. \tag{8}$$

Therefore, the admittance matrix of the three-port network A in Fig. 1 may be obtained from the admittance matrix of the four-port network in (6) as

$$\begin{bmatrix} I \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y_{11}+Y_{14}+Y_{41}+Y_{44} & Y_{12}+Y_{42} & Y_{13}+Y_{43} \\ Y_{21}+Y_{24} & Y_{23} & Y_{24} \\ Y_{31}+Y_{34} & Y_{32} & Y_{33} \end{bmatrix} \cdot \begin{bmatrix} V \\ V_2 \\ V_3 \end{bmatrix}. \tag{9}$$

The transmission matrix of network B in Fig. 1 is

$$\begin{aligned}\begin{bmatrix} V_0 \\ I_0 \end{bmatrix} &= \begin{bmatrix} \cosh\gamma_1 l_1 & Z_{0,1}\sinh\gamma_1 l_1 \\ Y_{0,1}\sinh\gamma_1 l_1 & \cosh\gamma_1 l_1 \end{bmatrix}\begin{bmatrix} V \\ I \end{bmatrix} \\ \gamma_1 &= \alpha_1 + j\beta_1 \\ \Rightarrow \quad \begin{bmatrix} V \\ I \end{bmatrix} &= \begin{bmatrix} \cosh\gamma_1 l_1 & -Z_{0,1}\sinh\gamma_1 l_1 \\ -Y_{0,1}\sinh\gamma_1 l_1 & \cosh\gamma_1 l_1 \end{bmatrix}\begin{bmatrix} V_0 \\ I_0 \end{bmatrix} \\ &= \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix}\begin{bmatrix} V_0 \\ I_0 \end{bmatrix}.\end{aligned} \tag{10}$$

Now, by combining (9) and (10), the overall transmission matrix of network in Fig. 1 may be derived in (11), shown at the bottom of the following page, since $t_{11}t_{22} - t_{12}t_{21} = 1$ for reciprocal systems. t_{11}, t_{12}, t_{21}, and t_{22} are defined by (10). Finally, the scattering matrix of the divider may be obtained from its admittance matrix as [12]

$$[S] = ([YT] + [YL])^{-1}([YL] - [YT]) \tag{12}$$

$$\begin{bmatrix} V_{1i} \\ V_{4i} \\ I_{1i} \\ I_{4i} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_{Ui,k} l_{Ui}) & 0 & Z_{Ui,k}\sinh(\gamma_{Ui,k} l_{Ui}) & 0 \\ 0 & \cosh(\gamma_{Di,k} l_{Di}) & 0 & Z_{Di,k}\sinh(\gamma_{Di,k} l_{Di}) \\ Y_{Ui,k}\sinh(\gamma_{Ui,k} l_{Ui}) & 0 & \cosh(\gamma_{Ui,k} l_{Ui}) & 0 \\ 0 & Y_{Di,k}\sinh(\gamma_{Di,k} l_{Di}) & 0 & \cosh(\gamma_{Di,k} l_{Di}) \end{bmatrix}\begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix} \tag{1}$$

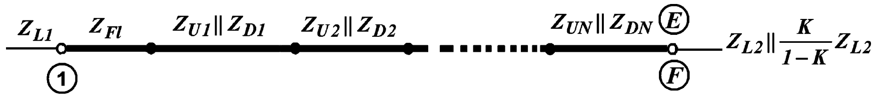


Fig. 6. Equivalent circuit of Fig. 5 when it is excited from port 1.

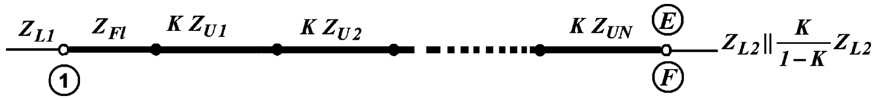


Fig. 7. Equivalent circuit of Fig. 6.

where YT is defined in (11) and YL is the load admittance matrix defined as follows:

$$[YL] = \begin{bmatrix} Y_{L1} & 0 & 0 \\ 0 & Y_{L2} & 0 \\ 0 & 0 & Y_{L3} \end{bmatrix}.$$

It is worth noting that the above analysis may consider any asymmetrical network in which the upper section is different from its lower section. Similarly, the above analysis may proceed by considering network B consisting of the three-port network from Z_{L1} to G_1.

B. Construction of the Error Function

Assume that the input power at port 1 should be divided between ports 2 and 3 in the ratio of $K : (1-K)$, where the input reflection coefficient should be as low as possible and the isolation among its output ports should be as high as possible. The error function may be constructed by

$$\begin{aligned}\varepsilon = wt1\sum_k P_{1,k} + wt2\sum_k [P_{2,k} - KP_{\text{tot},k}]^2 \\ + wt3\sum_k [P_{3,k} - (1-K)P_{\text{tot},k}]^2 \\ + wt4\sum_k |S23_k|^2 \end{aligned} \tag{13}$$

where $wt1$, $wt2$, $wt3$, and $wt4$ are weighting functions which may, in general, be functions of frequency in the specified bandwidth. Some of the weighting factors may be set equal to zero, depending on the requirements and convergence of the problem. The total output power from the divider ports is defined by

$$P_{\text{tot},k} = P_{1,k} + P_{2,k} + P_{3,k} \tag{14}$$

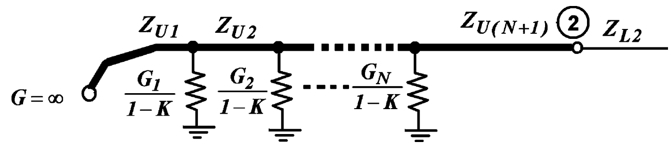


Fig. 8. Upper half of the circuit in Fig. 5 when excited from the output port.

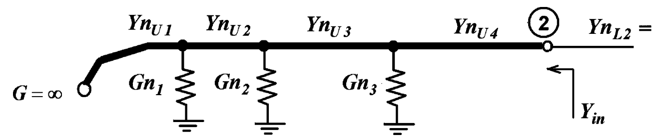


Fig. 9. Network of Fig. 8 when $N = 3$.

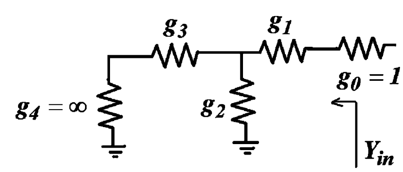


Fig. 10. Single-ended low-pass filter of order 3.

where the reflected power from input port 1 and transmitted powers from output ports 2 and 3 at the kth frequency are

$$\begin{cases} P_{1,k} = \dfrac{1}{2}\dfrac{|S_{11,k}|^2}{Z_{L1}} \\ P_{2,k} = \dfrac{1}{2}\dfrac{|S_{21,k}|^2}{Z_{L2}} \\ P_{3,k} = \dfrac{1}{2}\dfrac{|S_{31,k}|^2}{Z_{L3}}. \end{cases} \tag{15}$$

The coding of computer programs for the above formulation of the MLS design and optimization procedure is quite simple and straightforward, despite its seemingly complex appearance.

$$\begin{bmatrix} I_0 \\ I_2 \\ I_3 \end{bmatrix} = \frac{1}{(t_{22}-y_{11}t_{12})}\begin{bmatrix} (y_{11}t_{11}-t_{21}) & y_{12} & y_{13} \\ y_{21} & y_{22}(t_{22}-y_{11}t_{12})+y_{21}t_{12}y_{12} & y_{23}(t_{22}-y_{11}t_{12})+y_{21}t_{12}y_{13} \\ y_{31} & y_{32}(t_{22}-y_{11}t_{12})+y_{31}t_{12}y_{12} & y_{33}(t_{22}-y_{11}t_{12})+y_{31}t_{12}y_{13} \end{bmatrix}\begin{bmatrix} V_0 \\ V_2 \\ V_3 \end{bmatrix} = [YT]\begin{bmatrix} V_0 \\ V_2 \\ V_3 \end{bmatrix} \tag{11}$$

TABLE I
INPUT VALUES AND RESULTS OF THE COMPUTER PROGRAM FOR THE FIRST EXAMPLE

Input values								
er=10.5	h=1.27 mm	Loss tan.=.002	fL=1 GHz	K(freq. div.)=15	fu=5 GHz	Sigma=57e6 (S/m)	N=4	
P2/P3=2	ZL1= 50 Ohms	ZL2= 50 Ohms	ZL3= 75 Ohms	Select=2	MinW=0.01mm	Error-Bop=0.2613	Error-Aop=0.010583	
Initial values (mm)			***Values before optimization (mm)***			***Values after optimization (mm)***		
W-fL= 2.43	L-fL= 6.72	G(1)= 0.0102	W-fL= 2.4252	L-fL= 6.72	G(1)= 0.0102	W-fL= 1.456	L-fL= 8.74250	G(1)=0.00995
WU(1)= 1.16	LU(1)= 7.18	G(2)= 0.0109	WU(1)= 1.1578	LU(1)= 7.18	G(2)= 0.0109	WU(1)=0.65267	LU(1)= 9.1537	G(2)=0.00527
WU(2)= 1.16	LU(2)= 7.18	G(3)= 0.0072	WU(2)= 1.1578	LU(2)= 7.18	G(3)= 0.0072	WU(2)=0.97162	LU(2)= 9.0870	G(3)=0.00281
WU(3)= 1.16	LU(3)= 7.18	G(4)= 0.0026	WU(3)= 1.1578	LU(3)= 7.18	G(4)= 0.0026	WU(3)=1.38930	LU(3)= 8.7865	G(4)=0.00122
WU(4)= 1.16	LU(4)= 7.18		WU(4)= 1.1578	LU(4)= 7.18		WU(4)=1.61160	LU(4)= 8.5696	
WU(5)= 1.16	LU(5)= 6.94		WU(5)=0.15316	LU(5)= 6.94		WU(5)=1.32950	LU(5)= 13.880	
WD(1)= 0.15	LD(1)= 7.18		WD(1)=0.15316	LD(1)= 7.18		WD(1)=0.12263	LD(1)= 9.1537	
WD(2)= 0.15	LD(2)= 7.18		WD(2)=0.15316	LD(2)= 7.18		WD(2)=0.17984	LD(2)= 9.0870	
WD(3)= 0.15	LD(3)= 7.18		WD(3)=0.15316	LD(3)= 7.18		WD(3)=0.15248	LD(3)= 8.7865	
WD(4)= 0.15	LD(4)= 7.18		WD(4)=0.15316	LD(4)= 7.18		WD(4)=0.13209	LD(4)= 8.5696	
WD(5)= 1.54	LD(5)= 6.94		WD(5)=0.45948	LD(5)= 6.94		WD(5)=0.37072	LD(5)= 13.880	

TABLE II
INPUT VALUES AND RESULTS OF THE COMPUTER PROGRAM FOR SECOND EXAMPLE

Input values								
er=10.5	h=1.27 mm	Loss tan.=.002	fL=1 GHz	K(freq. div.)=15	fu=18 GHz	Sigma=57e6 (S/m)	N=6	
P2/P3=1	ZL1= 50 Ohms	ZL2= 50 Ohms	ZL3= 50 Ohms	Select=2	MinW=0.01mm	Error-Bop=0.5412	Error-Aop=0.03151	
Initial values (mm)			***Values before optimization (mm)***			***Values after optimization (mm)***		
W-fL= 1.99	L-fL= 1.94	G(1)= 0.0155	W-fL= 1.9948	L-fL= 1.94	G(1)= 0.0155	W-fL= 1.4138	L-fL= 4.0955	G(1)= 0.006721
WU(1)= 0.5	LU(1)= 2.09	G(2)= 0.0098	WU(1)=0.50062	LU(1)= 2.09	G(2)= 0.0098	WU(1)= 0.36064	LU(1)= 2.9030	G(2)=0.0035816
WU(2)= 0.5	LU(2)= 2.09	G(3)= 0.0155	WU(2)=0.50062	LU(2)= 2.09	G(3)= 0.0155	WU(2)= 0.38982	LU(2)= 2.6703	G(3)=0.0024025
WU(3)= 0.5	LU(3)= 2.09	G(4)= 0.0067	WU(3)=0.50062	LU(3)= 2.09	G(4)= 0.0067	WU(3)= 0.35816	LU(3)= 2.6645	G(4)=0.0020528
WU(4)= 0.5	LU(4)= 2.09	G(5)=0.0076	WU(4)=0.50062	LU(4)= 2.09	G(5)=0.0076	WU(4)= 0.2702	LU(4)= 2.7050	G(5)=0.0016783
WU(5)= 0.5	LU(5)= 2.09	G(6)=0.0014	WU(5)=0.50062	LU(5)= 2.09	G(6)=0.0014	WU(5)= 0.26602	LU(5)= 2.5794	G(6)=0.0014458
WU(6)= 0.5	LU(6)= 2.09		WU(6)=0.50062	LU(6)= 2.09		WU(6)= 0.24084	LU(6)= 2.4972	
WU(7)= 0.5	LU(7)= 2.09		WU(7)=0.50062	LU(7)= 2.09		WU(7)= 0.32136	LU(7)= 2.3811	
WD(1)= 0.33	LD(1)= 2.09		WD(1)=0.33374	LD(1)= 2.09		WD(1)= 0.08081	LD(1)= 2.9030	
WD(2)= 0.33	LD(2)= 2.09		WD(2)=0.33374	LD(2)= 2.09		WD(2)= 0.09385	LD(2)= 2.6703	
WD(3)= 0.33	LD(3)= 2.09		WD(3)=0.33374	LD(3)= 2.09		WD(3)= 0.16879	LD(3)= 2.6645	
WD(4)= 0.33	LD(4)= 2.09		WD(4)=0.33374	LD(4)= 2.09		WD(4)= 0.38686	LD(4)= 2.7050	
WD(5)= 0.33	LD(5)= 2.09		WD(5)=0.33374	LD(5)= 2.09		WD(5)= 0.57844	LD(5)= 2.5794	
WD(6)= 0.33	LD(6)= 2.09		WD(6)=0.33374	LD(6)= 2.09		WD(6)= 1.1008	LD(6)=2.4972	
WD(7)= 0.33	LD(7)= 2.09		WD(7)=0.33374	LD(7)= 2.09		WD(7)= 1.6762	LD(7)=2.3811	

III. DETERMINATION OF INITIAL VALUES OF DIVIDER PARAMETERS

Any minimization routine for the error function requires initial values of its variables, which here are the geometrical dimensions of metallic strips (the width and length of each section) and values of resistors.

A. Initial Values of Metallic Strip Widths

Here, we use the even- and odd-mode analysis to provide an initial design for the Wilkinson power divider and thus obtain the initial values of its configuration.

In order to minimize the power loss in resistors of the Wilkinson power divider, we try as far as possible to make the voltages on the upper and lower transmission lines equal (see Fig. 5). Since the power in upper branch is $K/(1-K)$ times that in the lower one, the admittances in the upper branch are selected equal to $K/(1-K)$ times that in the lower one. Since, in general, the load admittance of port 2 is not proportional to that of port 3 in the ratio of $K/(1-K)$, the characteristic admittance of the output line sections are chosen in such a way that the admittances seen from points E and F in Fig. 5 be in the ratio of $Y_E/Y_F = K/(1-K)$ [3].

Consequently, in the general case that $Y_{L2} \neq (K/(1-K))Y_{L3}$, the initial characteristic admittance of output line sections are selected as

$$\begin{aligned} Y_{U(N+1)} &= Y_{L2} \\ Y_{D(N+1)} &= \sqrt{Y_{L3} \times \frac{1-K}{K} Y_{L2}}. \end{aligned}$$

When the divider is excited at its input port 1, the points on the upper and lower branches at equal distances from its input should be at equal potentials, and the two terminals of resistors would be at the same potentials; they could be short circuited. Therefore, the upper and lower branches will be parallel, and the equivalent circuit will be as in Fig. 6.

Assuming that the admittances of the lower branch are $(1-K)/K$ times the upper one, their parallel combination is

$$Y_{Ui} \| Y_{Di} = Y_{Di} + Y_{Ui} = \frac{1-K}{K} Y_{Ui} + Y_{Ui} = \frac{1}{K} Y_{Ui}$$

or

$$Z_{Ui} \| Z_{Di} = K Z_{Ui}. \tag{16}$$

Consequently, the equivalent circuit of Fig. 7 results.

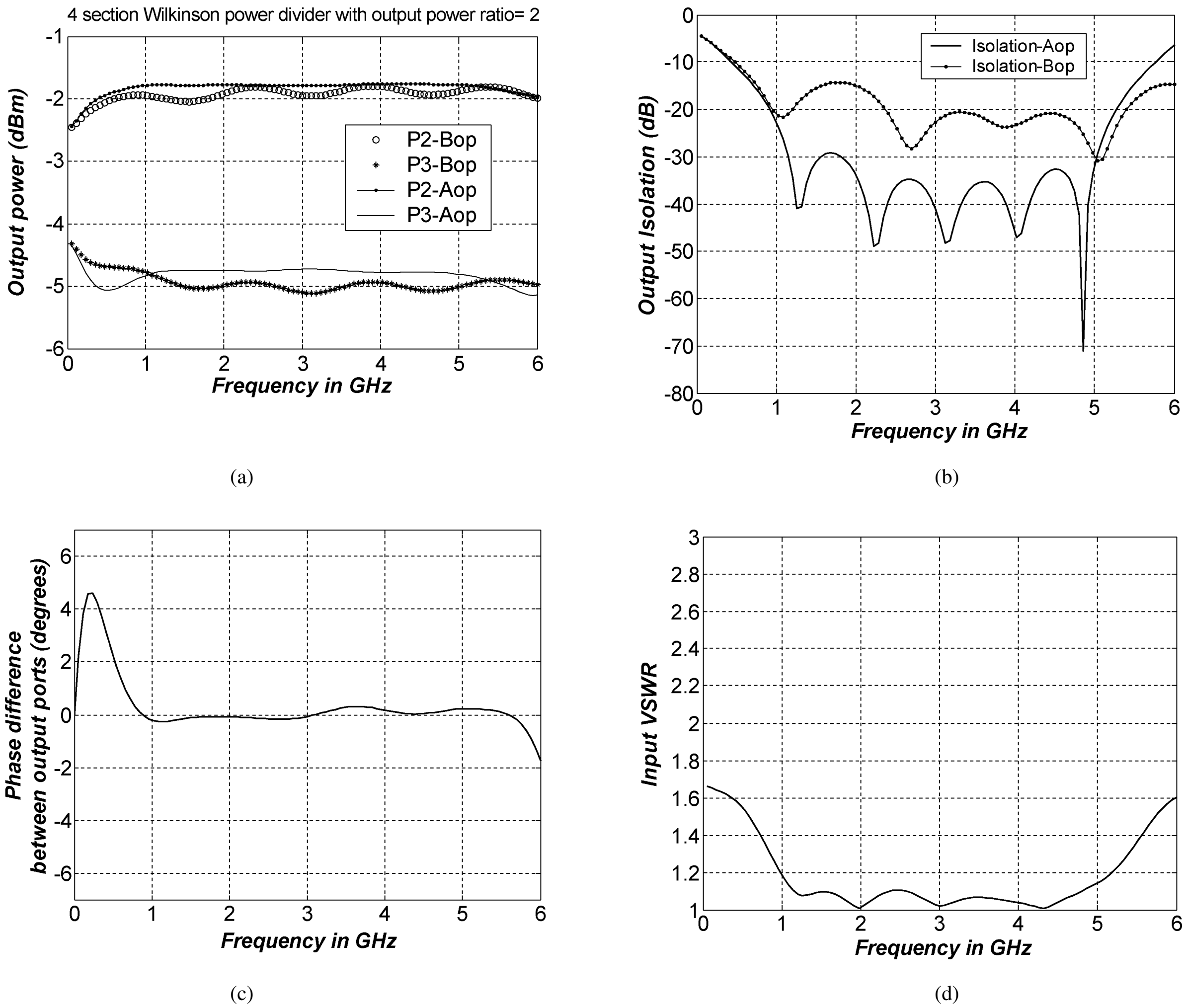


Fig. 11. (a) Output powers of a four-section 1.7-dB power divider with unequal impedances. (b) Isolation between output ports. (c) Phase difference between outputs. (d) Input VSWR.

A simple impedance-matching problem then appears, where the input impedance Z_{L1} should be matched to the output impedance $[Z_{L2}||(K/(1-K))Z_{L2} = KZ_{L2}]$ through the transmission line. There are many selections of the step characteristic impedances depending on the desired accuracy. However, here we select an approximate value for all of the sections, which is equal to the average value of Z_{L1}, KZ_{L2}.

Having determined the characteristic impedances of steps in the equivalent circuit in Fig. 7, the initial values for the widths of the step lines of the upper and lower branches may be calculated by closed formulas. The characteristic impedances of the $(N+1)$th section in the upper branch is selected as Z_{L2} and that in the lower branch is selected to match Z_{L3} to $(K/(1-K))Z_{L2}$.

B. Initial Values of the Strip Lengths

The best solution of strip length is $\lambda/4$ at the center frequency. However, to keep the length of the divider short, the initial length of the strip sections in the upper and lower branches may be taken equal to $3\lambda/16$ at the center frequency (f_0) or

$$L = \frac{3c}{16 f_0 \sqrt{\varepsilon_{\mathrm{ref}}(f_0)}} \tag{17}$$

where c is the speed of light, in free space, and $\varepsilon_{\mathrm{ref}}(f_0)$ is the effective dielectric constant at (f_0).

For the MLS design and optimization algorithm, the step lengths on the upper and lower branches may be kept independent, and their resulting values may become quite different. This situation may cause problems in fabrication and applications and may increase power loss in the resistors and may introduce considerable phase difference between the upper and lower branches of the divider. For such reasons, it is advisable to keep their lengths equal by imposing constraints on their lengths.

C. Initial Values for Resistors

Suppose that the output ports of the power divider are excited by an odd mode. The divider may then be divided into two parts along its electrical axis, where the voltage is zero. The upper part is shown in Fig. 8. The initial values of characteristic impedances of transmission lines were estimated in Section III-B. For the case of $Z_{L2} = ((1-K)/K)Z_{L3}$ and odd-mode excitation of output ports (e.g., as in Fig. 8), the initial values of resistors may be selected in such a way that the input impedance at port 2 is equal to Z_{L2}, at least at the center frequency [13].

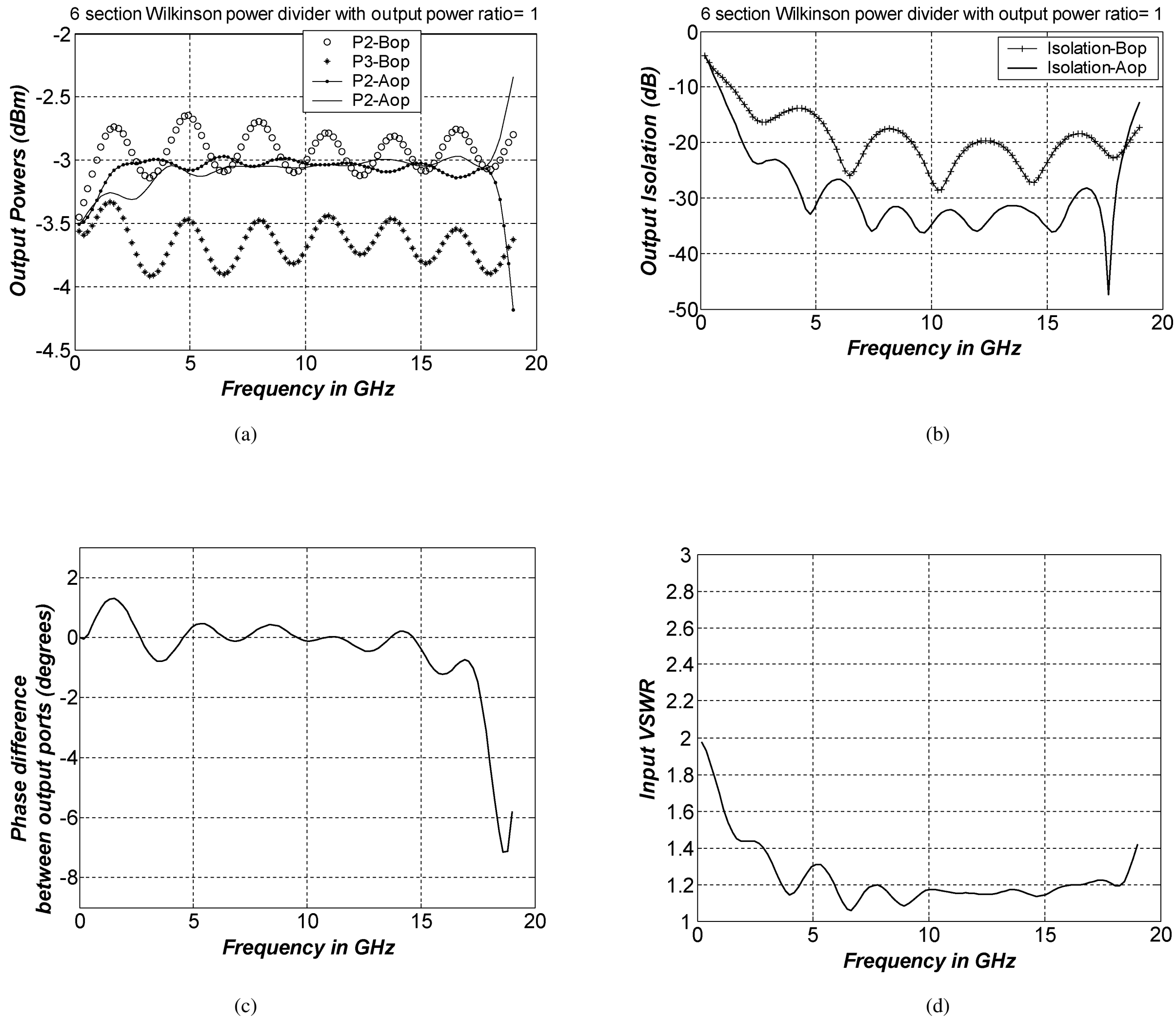


Fig. 12. (a) Output powers for a six-section power divider with equal. power division and equal impedances. (b) Isolation between output ports. (c) Phase difference between outputs. (d) Input VSWR.

For example, consider a three-section $(N = 3)$ divider. The impedances and admittances are normalized with respect to Z_{L2} and Y_{L2}, respectively. The lines are specified by their characteristic admittances, as shown in Fig. 9.

If the lengths of transmission lines are equal to $\lambda/4$, then the input admittance at port 2 is

$$Y_{\text{in}} = \frac{Yn_{U4}^2}{Gn_3 + \frac{Yn_{U3}^2}{Gn_2 + \frac{Yn_{U2}^2}{Gn_1}}} \tag{18}$$

and the input impedance is

$$Z_{\text{in}} = \frac{Gn_3}{Yn_{U4}^2} + \frac{1}{\frac{Gn_2 Yn_{U4}^2}{Yn_{U3}^2} + \frac{Yn_{U2}^2 Yn_{U4}^2}{Gn_1 Yn_{U3}^2}} \tag{19}$$

where the characteristic admittances of lines are Yn_{U2}, Yn_{U3}, and Yn_{U4}, which were calculated earlier. Now, the value of Gn_1, Gn_2, and Gn_3 should be determined so that the normalized input impedance at port 2 is approximately equal to 1. The above expression is in the form of continued fractions. On the other hand, a single-port low-pass filter of order 3 has a configuration similar to that in Fig. 10 [14], where the series elements are denoted by impedances and the shunt elements are denoted by admittances. Therefore, the input impedance is

$$Z_{\text{in}} = g_1 + \frac{1}{g_2 + \frac{1}{g_3}} \tag{20}$$

which should be equal to 1 for impedance matching. This expression is also in the form of continued fractions. There are tables in references [14], which provide the values of g_1, g_2, and g_3 for filters of different orders. In order to determine the values of elements Gn_1, Gn_2, and Gn_3, for example, the expressions

TABLE III
INPUT VALUES AND RESULTS OF THE COMPUTER PROGRAM FOR THE FIRST FABRICATED SAMPLE

Input values								
er=10.5	h=1.27 mm	Loss tan.=.002	fL=1 GHz	K(freq. div.)=15	fu=2 GHz	Sigma=57e6 (S/m)	N=3	
P2/P3=1	ZL1= 50 Ohms	ZL2= 50 Ohms	ZL3= 75 Ohms	Select=2	MinW=0.01mm	Error-Bop=0.63574	Error-Aop=0.0050387	
Initial values (mm)			***Values before optimization (mm)***			***Values after optimization (mm)***		
W-fL= 1.99	L-fL= 13.72	G(1)= 0.0184	W-fL= 1.9948	L-fL= 13.72	G(1)= 0.0184	W-fL=1.2701	L-fL=13.9107	G(1)=0.0085108
WU(1)= 0.5	LU(1)= 14.54	G(2)= 0.0058	WU(1)= 0.50062	LU(1)= 14.54	G(2)= 0.0058	WU(1)=0.22433	LU(1)=15.0719	G(2)=0.0038415
WU(2)= 0.5	LU(2)= 14.54	G(3)= 0.0061	WU(2)= 0.50062	LU(2)= 14.54	G(3)= 0.0061	WU(2)=0.57244	LU(2)=12.0157	G(3)=0.0023324
WU(3)= 0.5	LU(3)= 14.54		WU(3)= 0.50062	LU(3)= 14.54		WU(3)=0.81925	LU(3)=14.1069	
WU(4)= 1.39	LU(4)= 14.19		WU(4)= 1.3894	LU(4)= 14.19			LU(4)=20.6174	
WD(1)= 0.33	LD(1)= 14.54		WD(1)=0.33374	LD(1)= 14.54		WD(1)=0.34306	LD(1)=15.0719	
WD(2)= 0.33	LD(2)= 14.54		WD(2)=0.33374	LD(2)= 14.54		WD(2)=0.38634	LD(2)=12.0157	
WD(3)= 0.33	LD(3)= 14.54		WD(3)=0.33374	LD(3)= 14.54		WD(3)=0.69109	LD(3)=14.1069	
WD(4)= 0.59	LD(4)= 14.19		WD(4)=0.58241	LD(4)= 14.19		WD(4)=0.46161	LD(4)=20.6174	

in (19) and (20) are equated. For the example of $N = 3$, the values of Gn_i are obtained as

$$
\begin{cases}
g_1 = \dfrac{Gn_3}{Yn_{U4}^2} \Rightarrow Gn_3 = g_1 Yn_{U4}^2 \\
\qquad \Rightarrow G_3 = (1-K) Y_{L2} g_1 Yn_{U4}^2 \\
g_2 = \dfrac{Gn_2 Yn_{U4}^2}{Yn_{U3}^2} \Rightarrow Gn_2 = \dfrac{g_2 Yn_{U3}^2}{Yn_{U4}^2} \\
\qquad \Rightarrow G_2 = (1-K) Y_{L2} \dfrac{g_2 Yn_{U3}^2}{Yn_{U4}^2} \\
g_3 = \dfrac{Yn_{U2}^2 Yn_{U4}^2}{Gn_1 Yn_{U3}^2} \Rightarrow Gn_1 = \dfrac{Yn_{U2}^2 Yn_{U4}^2}{g_3 Yn_{U3}^2} \\
\qquad \Rightarrow G_1 = (1-K) Y_{L2} \dfrac{g_3 Yn_{U2}^2 Yn_{U4}^2}{Yn_{U3}^2}.
\end{cases} \tag{21}
$$

Consequently, a short computer program may be written to calculate the values of resistors for a power divider having N sections. Similar operation may be done for $Z_{L2} \neq ((1 - K)/K) Z_{L3}$.

IV. COMPUTER PROGRAM IMPLEMENTATION

Here, the computer program and some sample examples are described. The "Fmincon" function of MATLAB software is used for optimization of the error function [15]. Fmincon uses a sequential quadratic programming (SQP) method. In this method, a QP subproblem is solved at each iteration. Fmincon, uses the Broyden, Fletcher, Goldfarb, and Shanno (BFGS) quasi-Newton method with a mixed quadratic and cubic line search procedure.

There is a class of algorithms that is based on Newton's method, but which does not require calculation of second derivatives. These are called quasi-Newton (or secant) methods. They update an approximate Hessian matrix at each iteration of the algorithm. The update is computed as a function of the gradient. The quasi-Newton method that has been most successful in published studies is the BFGS update.

Conjugate gradient methods and quasi-Newton methods are of the best favored methods that use gradient information. The BFGS quasi-Newton method requires more computation in each iteration and more storage than the conjugate gradient methods, although it generally converges in fewer iterations.

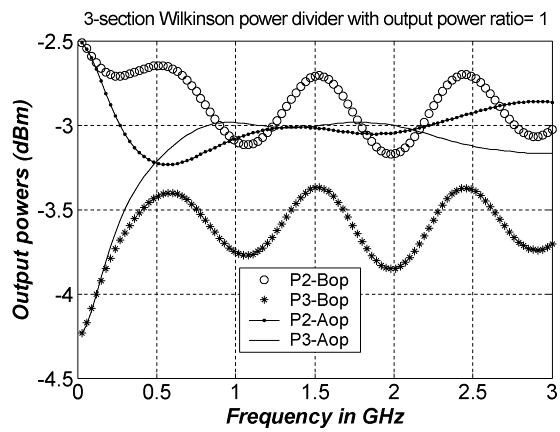


Fig. 13. Computed output power curves of fabricated sample 1.

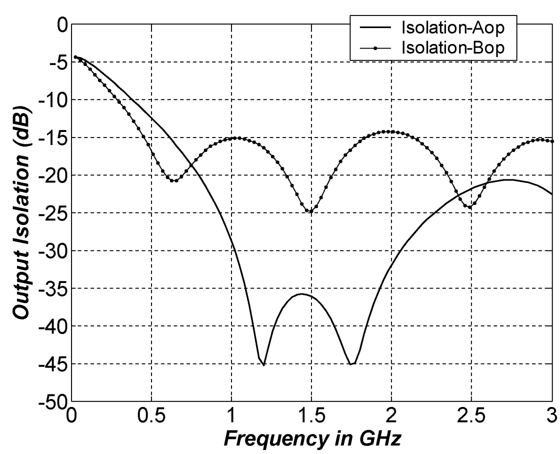


Fig. 14. Computed isolation before and after optimization for sample 1.

Input data such as substrate parameters, required frequency bandwidth, power division ratio, and source and load impedances of Wilkinson power divider are entered and written in printouts. The initial values of the divider configuration are then calculated by the computer program and are printed in the initial values column of output tables. The lengths of the strips are kept fixed, one step of the optimization is performed on the widths of the strips, and the resulting values are printed in the second column of the output tables entitled "*values before optimization.*" Curves for output powers and isolation between output ports are also plotted and denoted by "Bop." The value of the

TABLE IV
INPUT VALUES AND RESULTS OF THE COMPUTER PROGRAM FOR SECOND FABRICATED EXAMPLE

Input values								
er=10.5	h=1.27 mm	Loss tan.=.002	fL=1 GHz	K(freq. div.)=15	fu=2 GHz	Sigma=57e6 (S/m)	N=3	
P2/P3=2	ZL1= 50 Ohms	ZL2= 50 Ohms	ZL3= 50 Ohms	Select=2	MinW=0.01mm	Error-Bop=0.61716	Error-Aop=0.0080514	
Initial values (mm)			*Values before optimization (mm)*			*Values after optimization (mm)*		
W-fL= 2.43	L-fL= 13.58	G(1)= 0.0202	W-fL= 2.4252	L-fL= 13.58	G(1)= 0.0202	W-fL=1.3471	L-fL=8.7903	G(1)=0.0096216
WU(1)=1.16	LU(1)= 14.45	G(2)= 0.0045	WU(1)= 1.1578	LU(1)= 14.45	G(2)= 0.0045	WU(1)=0.51678	LU(1)=15.0896	G(2)=0.0037803
WU(2)= 1.16	LU(2)= 14.45	G(3)= 0.0067	WU(2)= 1.1578	LU(2)= 14.45	G(3)= 0.0067	WU(2)=1.1279	LU(2)=8.1054	G(3)=0.0036282
WU(3)= 1.16	LU(3)= 14.45		WU(3)= 1.1578	LU(3)= 14.45		WU(3)=1.4199	LU(3)=13.5657	
WU(4)= 2.2	LU(4)= 13.87		WU(4)= 2.203	LU(4)= 13.87		WU(4)=2.7966	LU(4)=19.4318	
WD(1)= 0.15	LD(1)= 14.45		WD(1)=0.15316	LD(1)= 14.45		WD(1)=0.17775	LD(1)=15.0896	
WD(2)= 0.15	LD(2)= 14.45		WD(2)=0.15316	LD(2)= 14.45		WD(2)=0.2082	LD(2)=8.1054	
WD(3)= 0.15	LD(3)= 14.45		WD(3)=0.38221	LD(3)= 14.45		WD(3)=0.33071	LD(3)=13.5657	
WD(4)= 1.16	LD(4)= 13.87		WD(4)=0.45948	LD(4)= 13.87		WD(4)=0.12483	LD(4)=19.4318	

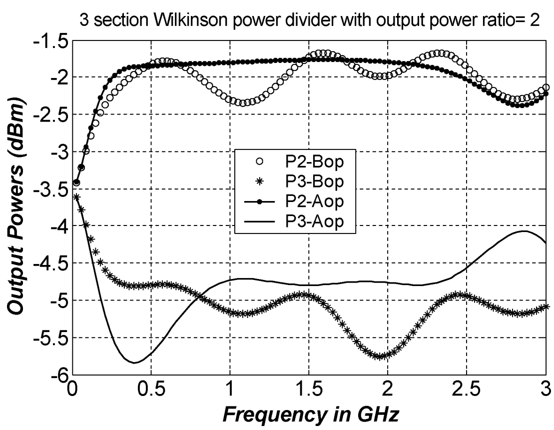


Fig. 15. Computed output power curves of fabricated sample 2.

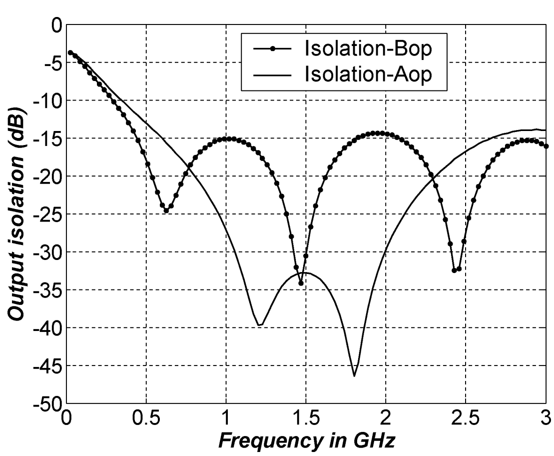


Fig. 16. Isolation before and after optimization for fabricated sample 2.

error function in this step is also printed. After this step, optimization is performed on all of the element values such as lengths and widths of strips and resistors, and their optimum values are obtained. They are printed in the third column of computer printout entitled "*values after optimization*" and are plotted with the notation "Aop."

In mass production, standard resistors in chip form should be used. Since the calculated resistors may not be equal to standard values, they are replaced with their nearest standard values, and error function is optimized again with respect to strip widths and lengths.

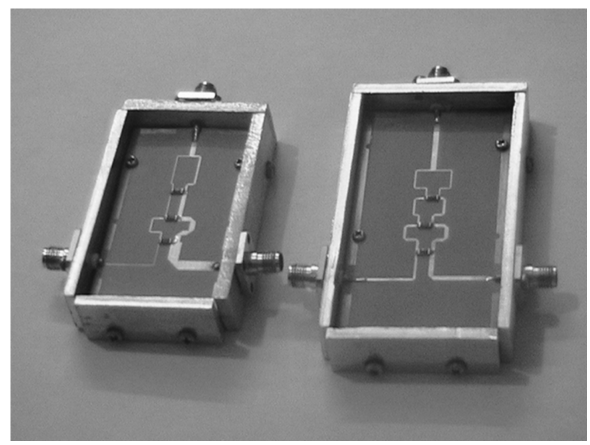
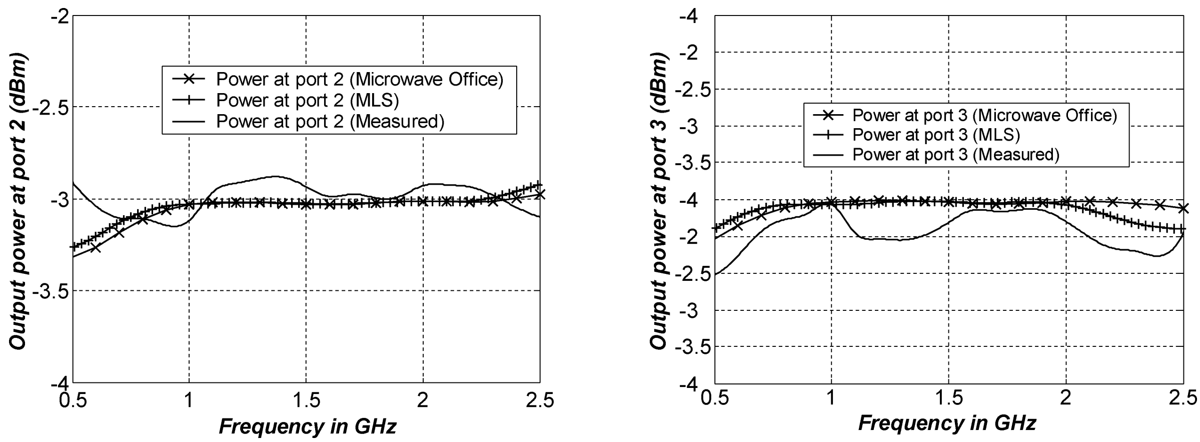


Fig. 17. (*left*) Fabricated power divider in example 2. (*right*) Fabricated power divider in example 1.

Tables I and II and Figs. 11 and 12 show results of the executed computer programs for two sample examples. In all of the tables, the input parameters are written as "*input values*" as follows:

ε_r	dielectric constant;
h	substrate thickness in millimeters;
Loss tan	substrate loss tangent;
fL	lower bound of the frequency bandwidth;
K	number of divisions of the frequency bandwidth;
fu	upper bound of the frequency bandwidth;
C	the amount of power which is transferred to port 2 in decibels;
Z_{L1}	Impedance of port 1 in ohms;
Z_{L2}	Impedance of port 2 in ohms;
Z_{L3}	Impedance of port 3 in ohms;
Sigma	conductivity of strips;
N	number of sections of divider;
Select	the model of dispersion selected; if Select $=0$, then no dispersion is considered, and, if Select $=2$, then the Kirschning and Jansen model is adopted [16];



(a)

(b)

Fig. 18. (a) Comparison of output power at port 2 for sample 1, as obtained by Microwave Office software, measurements, and MLS design algorithm. (b) Comparison of output power at port 3 for sample 1, as obtained by Microwave Office software, measurements and MLS design algorithm.

MinW	minimum of strip widths in millimeters;
Error-Bopt	value of error function before optimization;
Error-Aopt	value of error function after optimization.

In the *"input values"* column, the initial values of widths and lengths of strips (in mm) and conductance of resistors in siemens are shown. In the column *"values before optimization"*, the program output after one step of optimization is shown while the transmission-line lengths are kept fixed. In the column *"values after optimization"*, after several steps of optimization, the strip widths, lengths, and resistor values are shown.

For the first example, we consider a four-section Wilkinson power divider with an unequal power-division ratio of $P_2/P_3 = 2$ and unequal source and load impedances of $Z_{L1} = 50\ \Omega$, $Z_{L2} = 50\ \Omega$, and $Z_{L3} = 75\ \Omega$, respectively in the frequency band 1–5 GHz. Fig.11 (a) and (b) shows the power outputs and isolation between output ports, before and after optimization, respectively. Fig. 11 (c) and (d) shows the phase difference between output ports and VSWR at the input port, after optimization, respectively. Table I shows the input values and the results of the computer program for this example. This four-section divider (for unequal power division and unequal source and load impedances) has a usable bandwidth of $f_2/f_1 = 5$, VSWR < 1.10 and isolation > 30 dB. In comparison, a similar four section hybrid designed in [2] (for equal power division and equal source and load impedances) has a bandwidth of $f_2/f_1 = 4$, VSWR< 1.10 and isolation > 26 dB.

For the second example, we consider a six-section Wilkinson power divider with equal power division ratio $(P_2/P_3 = 1)$ and equal source and load impedances of $Z_{L1} = Z_{L2} = Z_{L3} = 50\,\Omega$, in the frequency band 1–18 GHz. The initial values for the configuration of the Wilkinson power divider may be selected in a quite arbitrary manner, so that the performance of the MLS design and optimization procedure may be highlighted. Therefore, for the case of equal power division between outputs (for the ratio $K = 0.5$) in this example, the initial values for WD and WU are not selected equal to show the capabilities of the design procedure.

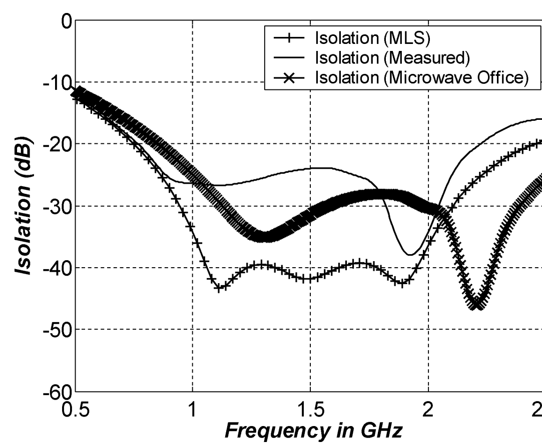


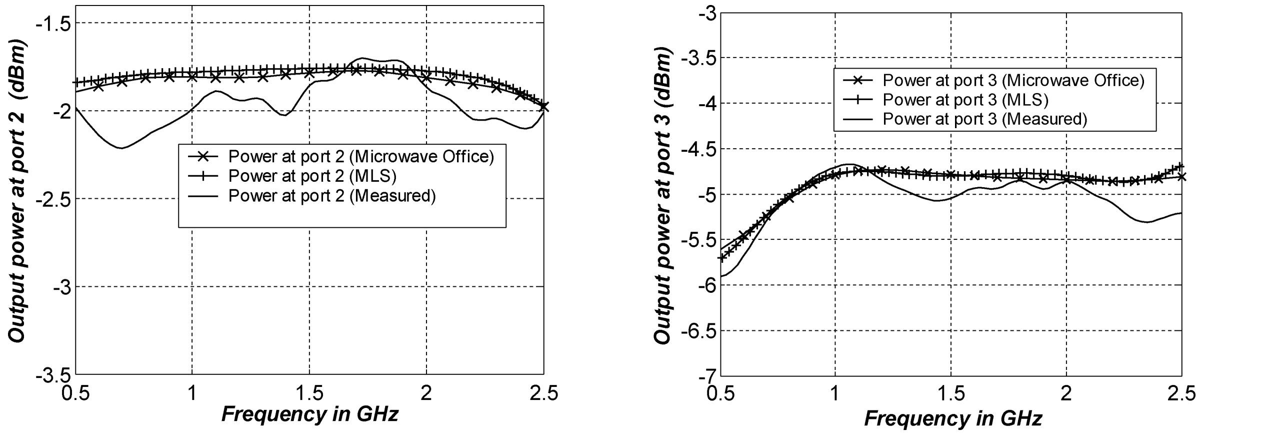
Fig. 19. Comparison among measurement results, as obtained by Microwave Office software, and MLS algorithm for isolation for sample 1.

Fig. 12(a) and (b) shows the output powers and isolation between output ports before and after optimization, respectively. Fig. 12(c) and (d) shows the phase difference between output ports and VSWR at the input port, respectively. Table II shows the input values and the results of computer program for this example.

V. Fabrication and Measurments

Two samples of Wilkinson power divider are designed, fabricated, and measured. In the MLS design and optimization computer program, the minimum microstrip widths are specified here as 100 μm for ease of fabrication, and some restrictions are imposed on consecutive microstrip widths to decrease the effects of discontinuities and phase difference between output ports [17].

The first sample is a three-section power divider with equal power division ratio and source and load impedances of $Z_{L1} = 50\ \Omega$, $Z_{L2} = 50\ \Omega$, and $Z_{L3} = 75\ \Omega$, in the L-band for the frequency range of 1–2 GHz. The MLS design and optimization



(a) (b)

Fig. 20. (a) Comparison among measurement results, as obtained by Microwave Office software, and MLS algorithm for output power at port 2 for sample 2. (b) Comparison among measurement results, as obtained by Microwave Office software, and MLS algorithm for output power at port 3 for sample 2.

provides the printouts shown in Table III, and Fig. 13 shows the output powers before and after optimization. The isolation between output ports before and after optimization is shown in Fig. 14.

However, the resistor values of $R1 = 117.5\ \Omega$, $R2 = 260.3\ \Omega$, and $R3 = 428.7\ \Omega$ determined by the MLS algorithm are not standard values. They should be replaced by their nearest standard values. Consequently, the following standard resistor values are selected: $R1 = 120\ \Omega$, $R2 = 270\ \Omega$, and $R3 = 470\ \Omega$. (Of course, resistor tolerance values should be considered.) Actual values of sample resistors to be used in fabrication may be measured. The widths and lengths of strips are then obtained by the algorithm for fixed standard resistors.

The second sample is a three-section divider with an unequal power division ratio of $P_2/P_3 = 2$, and equal source and load impedances of $Z_{L1} = Z_{L2} = Z_{L3} = 50\ \Omega$, in the L-band. The MLS design and optimization are similar to those of the first sample. Table IV provides the relevant data for the second sample. The resistor values are obtained as $R1 = 103.9\ \Omega$, $R2 = 264.5\ \Omega$, and $R3 = 275.6\ \Omega$. They are replaced by the nearest standard values of $R1 = 100\ \Omega$, $R2 = 270\ \Omega$, and $R3 = 270\ \Omega$. The above-mentioned procedure of optimization is repeated. Figs. 15 and 16 show the divider output powers and isolation between output ports for the second sample, respectively.

Pictures of the two fabricated power dividers are shown in Fig. 17. Both fabricated samples are tested by the network analyzer (HP-8510). These dividers are also analyzed by the Microwave Office software.

The results of MLS design and optimization, Microwave Office software simulation, and measurements of the first fabricated sample for output power at ports 2 and 3 are shown in Fig. 18(a) and (b), respectively. The isolation between output ports 2 and 3 as obtained by the MLS algorithm, software, and measurements are shown in Fig. 19. It is seen that the proposed method of least squares for the design and optimization of the Wilkinson power divider is very well verified by Microwave Office and fabrication and measurements.

The results of the second fabricated sample for output powers from ports 1 and 2 and isolation between them as computed by

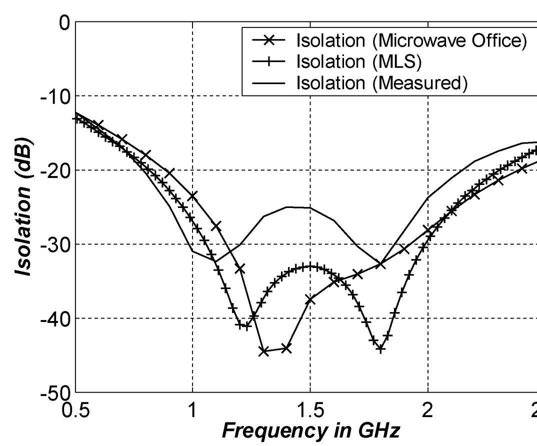


Fig. 21. Comparison of isolation among measurement results, as obtained by Microwave Office software, and MLS algorithm for sample 2.

the MLS design algorithm and Microwave Office software and measurements are depicted in Figs. 20 and 21, respectively.

The magnitude of ripples in the measured output power values is at most 0.4 dB, which is quite small. However, the difference between the computer and measured values of the power-divider characteristics may be attributable to the approximations made in the theoretical analysis and simulation and to the isolation resistors and fabrication of the divider and the measurement setup (such as connectors). Furthermore, the effects of step discontinuities on the metal strips of the microstrip are reduced by imposing some constraints on the relative variations of strip widths.

VI. Conclusion

A design and optimization procedure based on the MLS is introduced for a multisection Wilkinson power divider for any power division ratio, broadband frequency bandwidth, and incorporation of impedance matching, namely arbitrary source and load impedances. The method of design may be applied to any asymmetric divider. The design method proceeds by dividing the input port into two ports and considering the divider as a series connection of sections of two parallel transmission lines and conductances. The transmission matrix of the divider is then obtained which leads to its scattering matrix. An error function is then constructed on the desired frequency bandwidth in terms of the required output powers at the ports and isolation between output ports. This error function depends on the geometry of the divider (namely, widths and lengths) of strips and values of resistors. The minimization of the error provides the optimum design of the divider in terms of the values of widths and lengths of strips and resistor values. The length of transmission-line sections in the upper and lower sections of the divider may be considered unequal. The applicability of the proposed MLS design procedure for Wilkinson power divider is verified by comparison with full-wave analysis software such as Microwave Office (which is not suitable or adequate for design and synthesis) and actual fabrication and measurements.

An advantage of the proposed design and optimization method for the Wilkinson power divider is that a specification for an arbitrary phase difference between its outputs in a frequency bandwidth and minimization of the insertion loss may be incorporated into the expression of the error function.

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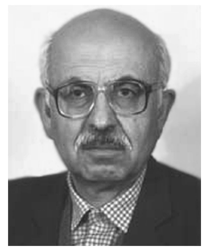

Homayoon Oraizi (SM'98) was born on April 24, 1942, in Isfahan, Iran. He received the B.E.E. degree from the American University of Beirut, Beirut, Lebanon, in 1967, and the M.Sc. and Ph.D. degrees in electrical engineering from Syracuse University, Syracuse, NY, in 1969 and 1973, respectively.

From 1973 to 1974, he taught at Khajeh-Nassir Tousi University of Technology, Tehran, Iran. From 1974 to 1985, he was with the Communication Division, Iran Electronics Industries, Shiraz, Iran, as a Systems Engineer, Supervisor, and Head of the Systems Engineering Department, where he was engaged in various aspects of technology transfer mainly in the field of HF/VHF/UHF communication systems. In 1985, he joined the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran, as an Assistant Professor. In 1994, he was promoted to Associate Professor and, in 1999, to Professor of electrical engineering. He teaches various courses in electromagnetics engineering, supervises B.Sc., M.Sc., and Ph.D. theses and dissertations and has served as the Head of the Communication Groups for one two-year term. He also spent a six-month sabbatical leave at Tsukuba University, Ibaraki, Japan. from August 2004 to February 2005. He has written and translated several text books in Farsi such as *Electromagnetics* (Iran Univ. Sci. Technol., vol. 1, "Electrostatics," 2nd ed., 2001; vol. 2, "Magnetostatics," 2nd ed., 2005), *Fields and Waves* (Iran Univ. Sci. Technol., 2nd ed., 2006), *Antenna Analysis and Design* (Iran Univ. Sci. Technol., 3rd ed., 2005) (which was recognized as the book of the year 1996 in Iran), and *Time Harmonic Electromagnetic Fields* (Iran Univ. Sci. Technol., 1st ed., 1999). His research interests are in the area of numerical methods for antennas, microwave devices, and radio wave propagation. He has conducted and completed many projects in the industry and university, He has also authored or coauthored over 100 papers in international journals and conferences. He was listed in *Who's Who in the World* in 1999.

Prof. Oraizi was the recipient of a fellowship presented by the Japan Society for the Promotion of Science to spend a two-month term from July to August 2003 at Tsukuba University.

Ali-Reza Sharifi was born in Iran, in 1979. He received the B.Sc. degree from Shahid Beheshti University, Tehran, Iran, in 2001, the M.Sc. degree from Iran University of Science and Technology, Tehran, Iran, in 2004, and is currently working toward the Ph.D. degree at Iran University of Science and Technology, all in electrical engineering.

His research interests are in various areas of electrical engineering. such as high-frequency circuit design and the application of numerical methods in electromagnetic, antennas, microwave circuits, and photonics. He has completed several projects on electronic and communication circuits.