USRP-2940 Features

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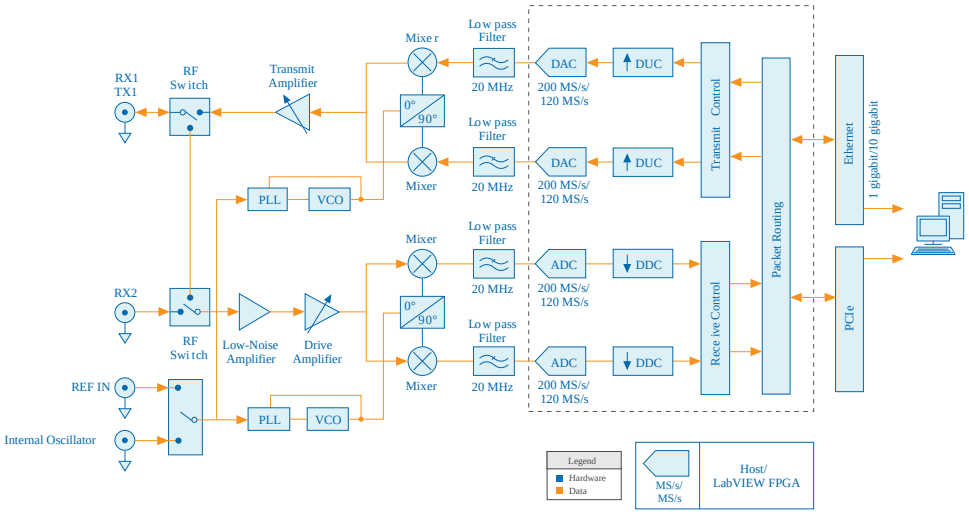
Contents

USRP-2940 40 MHz Block Diagram

Signals received by the USRP-294040 MHz are amplified, downconverted, filtered, digitized, and decimated before being passed to the host computer. Signals transmitted by the USRP-294040 MHz are upsampled, reconstructed, filtered, upconverted, and amplified before being transmitted.

Note The signal path is duplicated for each of the two channels.



Note The area within the dotted line indicates the processing on the FPGA when you use NI-USRP with the default FPGA image. When you use LabVIEW FPGA, you control the processing on the FPGA.

The following lists describe the individual blocks:

Note The RF switch allows transmit and receive operations to occur on the same shared antenna. On this device, one antenna is designated receive-only.

Receive Path:

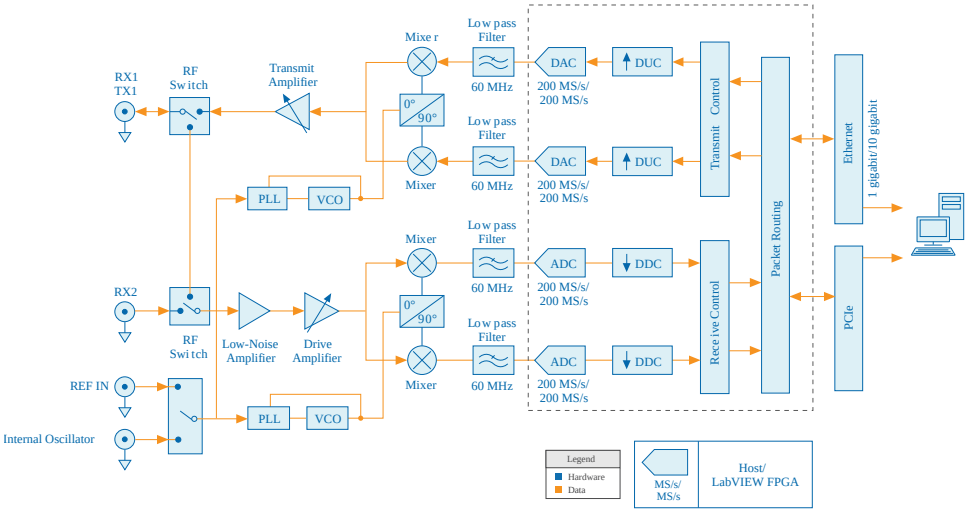
- The low-noise amplifier and drive amplifier amplify the incoming signal.
- The phase-locked loop (PLL) controls the voltage-controlled oscillator (VCO) so that the device clocks and local oscillator (LO) can be frequency-locked to a reference signal.
- The mixer downconverts the signals to the baseband in-phase (I) and quadrature (Q) components.
- The lowpass filter reduces noise and high frequency components in the signal.
- The analog-to-digital converter (ADC) digitizes the I and Q data.
- The digital downconverter (DDC) mixes, filters, and decimates the signal to a user-specified rate.
- The downconverted samples are passed to the host computer over a standard gigabit Ethernet connection.

Transmit Path:

- The host computer synthesizes baseband I/Q signals and transmits the signals to the device over a standard gigabit Ethernet connection.
- The digital upconverter (DUC) mixes, filters, and interpolates the signal to 400 MS/s.
- The digital-to-analog converter (DAC) converts the signal to analog.
- The lowpass filter reduces noise and high frequency components in the signal.
- The mixer upconverts the signals to a user-specified RF frequency.
- The PLL controls the VCO so that the device clocks and LO can be frequency-locked to a reference signal.
- The transmit amplifier amplifies the signal and transmits the signal through the antenna.

USRP-2940 120 MHz Block Diagram

Signals received by the USRP-2940120 MHz are amplified, downconverted, filtered, digitized, and decimated before being passed to the host computer. Signals transmitted by the USRP-2940120 MHz are upsampled, reconstructed, filtered, upconverted, and amplified before being transmitted.



Note The area within the dotted line indicates the processing on the FPGA when you use NI-USRP with the default FPGA image. When you use LabVIEW FPGA, you control the processing on the FPGA.

The following lists describe the individual blocks:

Note The RF switch allows transmit and receive operations to occur on the same shared antenna. On this device, one antenna is designated receive-only.

Receive Path:

- The low-noise amplifier and drive amplifier amplify the incoming signal.

- The phase-locked loop (PLL) controls the voltage-controlled oscillator (VCO) so that the device clocks and local oscillator (LO) can be frequency-locked to a reference signal.
- The mixer downconverts the signals to the baseband in-phase (I) and quadrature (Q) components.
- The lowpass filter reduces noise and high frequency components in the signal.
- The analog-to-digital converter (ADC) digitizes the I and Q data.
- The digital downconverter (DDC) mixes, filters, and decimates the signal to a user-specified rate.
- The downconverted samples are passed to the host computer over a standard gigabit Ethernet connection.

Transmit Path:

- The host computer synthesizes baseband I/Q signals and transmits the signals to the device over a standard gigabit Ethernet connection.
- The digital upconverter (DUC) mixes, filters, and interpolates the signal to 400 MS/s.
- The digital-to-analog converter (DAC) converts the signal to analog.
- The lowpass filter reduces noise and high frequency components in the signal.
- The mixer upconverts the signals to a user-specified RF frequency.
- The PLL controls the VCO so that the device clocks and LO can be frequency-locked to a reference signal.
- The transmit amplifier amplifies the signal and transmits the signal through the antenna.