

# **CSE-315 Microprocessor**

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# 1 Chapter-9 : 8086/8088 specification

- virtually no differences between these two microprocessors. Both are packaged in 40-pin dual in-line package.
- **8086**:16 bit microprocessor with a 16bit data bus(A0-A15)  
**8088**:16 bit microprocessor with a 8bit data bus(A0-A7)  
major difference between 8086 and 8088.
- Minor differences  
**8086**: $M/\overline{IO}$ ; **8088**: $IO/\overline{M}$   
PIN34:-**8086**: $\overline{BHE}$ /S7; **8088**:SS0
- power supply requirements:  
+5v with a supply voltage tolerance of  $\pm 10\%$   
both 32F to 180F  
8086 and 8088 have 340 and 360 mA.

**figures in the book**

## 1.1 Pin Connection

- **AD7-AD0**:
  - 8088 address/data bus lines
  - multiplexed address data bus
  - rightmost 8 bits of the memory address or I/O port whenever  $ALE=1$  or  $ALE=0$
  - high impedance state during hold acknowledge.

- **A15-A8:**
  - 8088 address bus
  - high impedance state during hold acknowledge.
- **AD15-AD8:**
  - 8086 address/data bus lines.
  - contains address bits when ALE=1
  - high impedance state during hold acknowledge.
- **A19/S6-A16/S3:**
  - multiplexed address/data bus lines
  - high impedance state during hold acknowledge.
- **S6:** always 0
- **S5:** indicated the condition of **IF** flag

S4	S3	indicate segment accessed during current bus cycle
0	0	extra segment
0	1	stack segment
1	0	code or no segment
1	1	data segment

- $\overline{RD}$  : if it is 0 then the data bus becomes receptive to data from memory or i/o devices connected to the system.
- high impedance state during hold acknowledge.
- **READY:**

- enters into wait state and remains idle if 0
- no effect on operations of microprocessor if this pin is in logic state 1.
- **INTR:**
  - used to request a h/w interrupt.
  - if INTR=1 when IF=1 then microprocessor enters an interrupt acknowledge cycle after completion of current instruction
- **NMI:**
  - non maskable interrupt pin.
  - similar to INTR except do not check IF flag.
- **$\overline{\text{TEST}}$  :**
  - an input that is tested by **wait** instruction. -if it is 0, the **WAIT** functions as **NOP**.
  - if 1 then **WAIT** waits for  **$\overline{\text{TEST}}$**  to become logic 0.

## 2 Chapter-9 : 8086/8088 specification

- **NMI:**
  - non-maskable interrupt pin
  - similar to INTR except that NMI does not check IF flag.
- **RESET:**
  - causes the microprocessor to reset if this pin remains high for a minimum of 4 clocking periods.
  - whenever the microprocessor gets reset, it begins executing instructions at memory location FFFF0H and disables future interrupts by clearing IF.
- **CLK:**
  - provides the base timing signal to the microprocessor.
  - clock signal must have at least 33% duty cycle(high for  $\frac{1}{3}$  rd and low for  $\frac{2}{3}$  of the period)
- **VCC**
  - power supply input
  - provides +5V
- **GND:-** 2 pins, both must be connected to ground.
- **MN/ $\overline{MX}$ :**-selects either minimum mode or maximum mode operations of microprocessor.
- **$\overline{BHE}$ /**S7****-both high enable. -use in 8086 to enable the most significant data bus bits(D15-D8) during a read or write

-the state of S7 is always a logic1

## 2.1 Minimum Mode Pins

–  $\text{IO}/\overline{\text{M}}$  or  $\text{M}/\overline{\text{IO}}$

-selects memory or i/o -indicates that microprocessors address bus contains either a memory address or an i/o port address.  
-high impedance state during a hold acknowledge.

–  $\overline{\text{WR}}$ :

-indicates that microprocessor is outputting data to a memory or io device.  
-data bus contains valid data for memory or io during the time, WR remains 0.

–  $\overline{\text{INTA}}$ :

-a response to the INTR input pin.  
-used to gate the interrupt vector number onto the data bus in response to an interrupt request.

–  $\overline{\text{ALE}}$ :

-address latch enable.  
-indicates that the microprocessor address/data bus contains address information.  
-the address can be a memory address or an i/o port.  
-does not float during a hold acknowledge.

–  $\text{DT}/\overline{\text{R}}$ : - data transmit or receive.

-indicates that microprocessors data bus is transmitting( $\text{DT}/\overline{\text{R}}=1$ )



or receiving( $DT/\overline{R}=(DT/\overline{R}=0)$ ) data.

-used to enable external data bus buffers.

– **DEN**:-data bus enable

-activates external data bus buffers.

– **HOLD**: - requests a direct memory access (DMA).

-if it is logic 1, microprocessor stops executing s/w and places its address, data and control bus at high impedance state.

-if it is a logic 0, the microprocessor executes s/w normally.

– **HLDA**: - hold acknowledge

-indicates that the microprocessor has entered the hold state.

–  $\overline{SS0}$  - equivalent to the S0 pin in the maximum mode operation.

-it is combined with  $IO/\overline{M}$  and  $DT/\overline{R}$  to decode function of the current bus cycle.

$IO/\overline{M}$	$DT/\overline{R}$	$\overline{SS0}$	<b>function</b>
0	0	0	interrupt acknowledge
0	0	1	memory card
0	1	1	memory write
0	1	1	halt
1	0	0	opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	passive/inactive

Table 1: bus cycle status(8088)[minimum mode]

$\overline{IS2}$	$\overline{S1}$	$\overline{S0}$	<b>function</b>
0	0	0	interrupt acknowledge
0	0	1	I/O card
0	1	1	I/O write
0	1	1	halt
1	0	0	opcode fetch
1	0	1	memory read
1	1	0	memory write
1	1	1	passive

Table 2: bus control functions generated by the bus controller 8088[maximum mode]

### 3 8086/8088 hardware specifications

**Maximum Mode Pins:** for using with external co-processors

- $\overline{S2}, \overline{S1}, \overline{S0}$  - indicate the function of current bus cycle.  
-normally decoded 8288 bus controller.
- $\overline{R1}/\overline{GT1}$  and  $\overline{R0}/\overline{GT0}$  - request/grant pins  
-requests direct memory access(DMA)  
-used to both request and grant DMA operation.
- $\overline{LOCK}$  - used to lock peripheral off the system.
- **OS1 and OS2** - queue status bit.  
-show status of the internal instruction queue.  
-accessed by numeric co-processor(8087)

QS1	QSA	Function
0	0	queue is idle
0	1	first byte of opcode
1	0	queue is empty
1	1	subsequent byte of opcode

### 3.1 clock generator-8284A

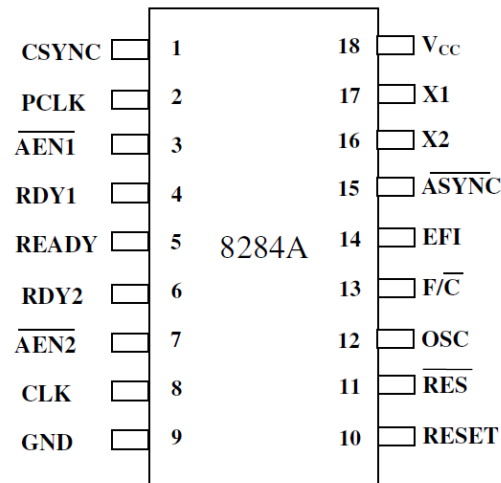


Fig1. Pin diagram of the 8284A clock generator

Figure 1: 8284A clock generator

- **Basic functions:**

- clock generation
- RESET synchronization
- READY synchronization
- TTL-level peripheral clk signals

- **pin functions**

- **AEN1 and AEN2 (address enable)** - qualify the bus ready signals RDY1 and RDY2 respectively.
- wait states are generated by the READY pin of microprocessor, which is controlled by  $\overline{AEN1}$  and  $\overline{AEN2}$

- **RDY1 and RDY2** - Bus ready inputs.
  - cause wait states in conjunction with  $\overline{AEN1}$  and  $\overline{AEN2}$  pins.
- **$\overline{ASync}$**  : - READY synchronization.
  - selects either one or two stages of synchronization for RDY1 and RDY2 inputs.
- **READY** - an output pin that connects to microprocessors READY input.
  - synchronized with RDY1 and RDY2 inputs.
- **X1 and X2:** - crystal oscillator pins.
  - connect to an external crystal which is used as the timing source for the clock generator and all its functions.
- **F/ $\overline{C}$**  - Frequency/crystal select input.
  - chooses the clocking source.
  - if it is held high, an external clock is provided to the EFI pin.
  - if it is held low, the internal crystal oscillator provides the timing signal.
- **EFI:** - External Frequency Input.
  - supplies timing whenever F/ $\overline{C}$  is held high.
- **CLK:** - clock output pin, which provides clock input to microprocessor and other components.
  - output signal is  $\frac{1}{3}$  of crystal or EFI input freq. and has a duty cycle of 33%(as required by 8086/8088).

- **PCLK:** - peripheral clock.
  - $\frac{1}{6}$  of the crystal or EFI input freq. and has a 50% duty cycle.
- **OSC:** - oscillator output.
  - at same freq. as the crystal or EFI input.
  - provides an EFI input to other 8284A in a multi-processor system.
- **$\overline{\text{RES}}$ :** - reset input.
  - often connected to an RC network that provides power on resetting.
- **RESET:** - reset output.
  - connected to microprocessors RESET input pin.
- **CSYNC:** - clock synchronization.
  - used whenever the EFI input provides synchronization in a multi-processor system.
  - if the internal oscillator is used, this pin must be grounded.



## 4.2 operation of the RESET section

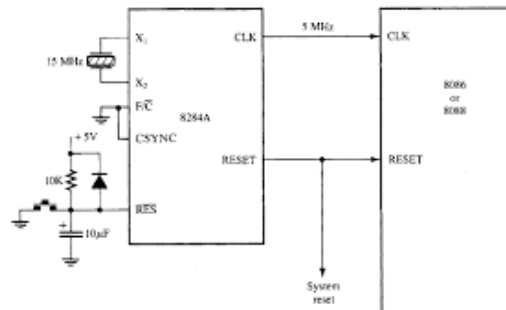


Figure 3: RESET operation of 8284A clock generator

- $\overline{\text{RES}}$  goes through a **Schmitt Trigger** and a **D-type** flip-flop, which ensures meeting timing requirements of microprocessors RESET input.
- the circuit applies RESET to microprocessor at a negative edge(1-0) and the microprocessor samples the RESET the signal at the positive edge(0-1).
- when power is first applied to the system, the RC circuit provides a logic 0 to  $\overline{\text{RES}}$
- after a short time  $\overline{\text{RES}}$  becomes logic 1, as the capacitor charges to +5v through the resistor.
- a push button allows the microprocessor to be reset by an operator.
- correct RESET timing requires the RESET input to become a logic 1 no later than 4 clock cycles after the power is applied, and held high for at least 50 micro-seconds.



- RESET goes high in 4 clock by FF. RESET stays high for 50 microseconds by RC.

### 4.3 Bus buffering and latching

- the address/data bus on the microprocessor is multiplexed(shared) to reduce the # of pins, which, on the other hand, burdens with the task of extracting or de-multiplexing info from these pins.
- Why not leave the buses multiplexed??  
memory and i/o require that the address remains valid and stable throughout a read or write cycle. If the buses are multiplexed , the address can get changed causing read or write in wrong locations.
- All computer systems have 3 types of buses:
  1. Address bus: provides memory address or i/o port of #s
  2. Data bus: transfers data between microprocessor and memory and i/o.
  3. control bus: provides control signals to memory and i/o.

**Basic of de-multiplexing- images in the lecture**

## 5 Demultiplexing 8088

9th image, figure would added later

- 74LS373 latches(OE for output enable and G or LE for latch enable inside) are used to demultiplex address data bus connections and address/status bus connections.
- 74LS373 passes inputs to outputs like wires when ALE is logic 1; when ALE returns to logic 0, the latches remember the inputs at the time of the change to logic 0.

### 5.1 Demultiplexing 8086

9th image, figure would added later

- Difference from 8088, AD15-AD8 and  $\overline{BHE}/S7$
- $\overline{BHE}$  selects a high order memory bank in a 16-bit memory system in 8086.

## 5.2 Buffered System

- If more than 10 unit loads are attached to any bus pins, the entire microprocessor system must be buffered(Buffer provides amplification in a digital circuit to drive output loads enabling more TTL unit loads to be driven.)
- The demultiplexed pins are already buffered by the 74LS373 latches.
- A fully buffered signal will introduce a timing delay which causes no difficulty unless memory or i/o devices are used that function at near the maximum speed of the bus.

## 5.3 Fully buffered 8088

image from 10th image

microprocessor	74LS244(octal buffer)	74LS245(octal bidirectional bus buffer)	74LS373
8088	2	1	2
8086	1	2	3

## 6 Memory Interfaces

- 4 common types of memory: ROM, flash memory(EEPROM), static random access memory(SRAM) and dynamic random access memory(DRAM).
- pin connections common to all memory devices: address inputs, data inputs(inputs/outputs), some type of selection input and at least one control input used to select a read or write operation.
- control connections:  
ROM-only one control input( $\overline{OE}$  or  $\overline{G}$ )-output enable and gate.  
RAM-one  $R/\overline{W}$  or 2 ( $\overline{WE}/\overline{W}$  and  $\overline{OE}/\overline{G}$ )-control input do not get activated at the same time.

### 6.1 ROM memory(nonvolatile memory)

- permanently stores programs that are resident to the system and must not change when power supply is disconnected(permanently programmed)
- EPROM(erasable programmable rom): programmed using a device called EPROM programmer; erasable if exposed to high-intensity uv light for about 20 minutes or less.
- PROM(programmable ROM): programmed by burning open tiny Ni-Chrome or Silicon Oxide fuses. Once programmed, it can't be erased
- Read Mostly Ram(RMM) or flash memory or EEPROM(electrically erasable programmable rom) or EAROM(electrically altered rom) or

NOVRAM(non-volatile ram). Electrically erasable, however, needs more time to erase than a normal RAM.

- delays in operation of an EPROM:

$t_{acc}$ : address to output delay.

$t_{OH}$ : address to output hold.

$t_{co}$ : chip select to output delay.

$t_{OF}$ : chip deselect to output float.

**timing digram of eprom- page12**

## **6.2 Static Memory or Static RAM(SRAM) or Volatile memory**

- Retain data as long as DC power is applied (no data without power)
- Difference between ROM and RAM:  
RAM-¿written under normal operation; ROM-¿programmable outside the computer and is normally read.

## **6.3 DRAM**

- DRAM is essentially same as SRAM, except that it retains data for only 2 or 4ms on an integrated capacitor.
- After 2 or 4ms, the contents of DRAM must be completely rewritten(refreshed) because the capacitors(which store logic 1/0) lose their charges.

- Refreshing also occurs during a write, a read or during a special refresh cycle.

## 7 Lecture 7

### 7.1 Dynamic RAM (DRAM)

- Have much larger sizes compared to SRAM. Its obvious disadvantage is requirement of many address pins. To reduce the number of address pins, the address inputs are multiplexed.
- Example of multiplexed address pins: 64k X 4 DRAM

**image from image13**

A0-A7 : Address inputs

$\overline{CAS}$  : Column Address Strobe

DQ1-DQ4 : Data-in/Data-out

$\overline{G}$  : Output enable

$\overline{RAS}$  : Row Address Strobe

VDD : +5v supply

VSS : Ground

$\overline{W}$  : Write enable

- Here for 64k, 16 address pins are required. However, 8 address pins are used through multiplexed
  - At first, A0-A7 are stored in internal row latch as row address through enabling  $\overline{RAS}$

- Next A8-A15 are stored in internal column latch as column address through enabling  $\overline{CAS}$

- Address multiplexer of 65k X 4

**image from image13**

- If  $\overline{RAS}$  is 0, then 'A' pins get connected and A0-A7 are stored in the **Internal Row Address** latch
- The Internal Row Address latch is edge triggered and so the row address get captured into the latch before the address changes to column address.
- If  $\overline{RAS}$  is 1, then the 8-pins get connected and A8-A15 are stored in Internal Column Address Latch

## 7.2 Address Decoding

- Decoding address sent from microprocessor is necessary, as without it, only one memory device can be connected to a microprocessor.
- Another reason of decoding is possible mismatch(or difference) between the # of connections in microprocessor and memory.