CSE-315 Microprocessor

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1 Chapter-9 : 8086/8088 specification

- virtually no differences between these two microprocessors. Both are packaged in 40-pin dual in-line package.
- **8086:**16 bit microprocessor with a 16bit data bus(A0-A15)
  8088:16 bit microprocessor with a 8bit data bus(A0-A7)
  major difference between 8086 and 8088.
- Minor differences
  8086:M/$\overline{IO}$;**8088:**IO/$\overline{M}$
  PIN34:-**8086:**$\overline{BHE}$/S7;**8088:**SS0
- power supply requirements:
  +5v with a supply voltage tolerance of $+-10\%$
  both 32F to 180F
  8086 and 8088 have 340 and 360 mA.

figures in the book

1.1 Pin Connection

- **AD7-AD0:**

  -8088 address/data bus lines

  -multiplexed address data bus

  -rightmost 8 bits of the memory address or I/O port whenever ALE=1 or ALE=0

  -high impedance state during hold acknowledge.

- **A15-A8:**

  -8088 address bus

  -high impedance state during hold acknowledge.

- **AD15-AD8:**

  -8086 address/data bus lines.

  -contains address bits when ALE=1

  -high impedance state during hold acknowledge.

- **A19/S6-A16/S3:**

  -multiplexed address/data bus lines

  -high impedance state during hold acknowledge.

- **S6:** always 0

– **S5:** indicated the condition of **IF** flag

S4	S3	indicate segment accessed during current bus cycle
0	0	extra segment
0	1	stack segment
1	0	code or no segment
1	1	data segment

– -$\overline{RD}$: if it is 0 then the data bus becomes receptive to data from memory or i/o devices connected to the system.
-high impedance state during hold acknowledge.

– **READY:**
-enters into wait state and remains idle if 0
-no effect on operations of microprocessor if this pin is in logic state 1.

– **INTR:**
-used to request a h/w interrupt.
-if INTR=1 when IF=1 then microprocessor enters an interrupt acknowledge cycle after completion of current instruction

– **NMI:**

-non maskable interrupt pin.

-similar to INTR except do not check IF flag.

– $\overline{\textbf{TEST}}$:

-an input that is tested by **wait** instruction. -if it is 0, the **WAIT** functions as **NOP**.

-if 1 then **WAIT** waits for $\overline{\textbf{TEST}}$ to become logic 0.