CSE-315 Microprocessor

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1 Chapter-9 : 8086/8088 specification

- virtually no differences between these two microprocessors. Both are packaged in 40-pin dual in-line package.
- **8086:**16 bit microprocessor with a 16bit data bus(A0-A15)
  8088:16 bit microprocessor with a 8bit data bus(A0-A7)
  major difference between 8086 and 8088.
- Minor differences
  8086:M/$\overline{IO}$;**8088:**IO/$\overline{M}$
  PIN34:-**8086:**$\overline{BHE}$/S7;**8088:**SS0
- power supply requirements:
  +5v with a supply voltage tolerance of $+-10\%$
  both 32F to 180F
  8086 and 8088 have 340 and 360 mA.

figures in the book

1.1 Pin Connection

- **AD7-AD0:**

  -8088 address/data bus lines

  -multiplexed address data bus

  -rightmost 8 bits of the memory address or I/O port whenever ALE=1 or ALE=0

  -high impedance state during hold acknowledge.

- **A15-A8:**

  -8088 address bus

  -high impedance state during hold acknowledge.

- **AD15-AD8:**

  -8086 address/data bus lines.

  -contains address bits when ALE=1

  -high impedance state during hold acknowledge.

- **A19/S6-A16/S3:**

  -multiplexed address/data bus lines

  -high impedance state during hold acknowledge.

- **S6:** always 0

– **S5:** indicated the condition of **IF** flag

S4	S3	indicate segment accessed during current bus cycle
0	0	extra segment
0	1	stack segment
1	0	code or no segment
1	1	data segment

– -$\overline{RD}$: if it is 0 then the data bus becomes receptive to data from memory or i/o devices connected to the system.
-high impedance state during hold acknowledge.

– **READY:**
-enters into wait state and remains idle if 0
-no effect on operations of microprocessor if this pin is in logic state 1.

– **INTR:**
-used to request a h/w interrupt.
-if INTR=1 when IF=1 then microprocessor enters an interrupt acknowledge cycle after completion of current instruction

– **NMI:**

-non maskable interrupt pin.

-similar to INTR except do not check IF flag.

– $\overline{\textbf{TEST}}$:

-an input that is tested by **wait** instruction. -if it is 0, the **WAIT** functions as **NOP**.

-if 1 then **WAIT** waits for $\overline{\textbf{TEST}}$ to become logic 0.

2 Chapter-9 : 8086/8088 specification

- **NMI:**

  -non-maskable interrupt pin

  -similar to INTR except that NMI does not check IF flag.

- **RESET:**

  -causes the microprocessor to reset if this pin remains high for a minimum of 4 clocking periods.

  -whenever the microprocessor gets reset, it begins executing instructions at memory location FFFF0H and disables future interrupts by clearing IF.

- **CLK:**

  -provides the base timing signal to the microprocessor.

  -clock signal must have at least 33% duty cycle(high for $\frac{1}{3}$ rd and low for $\frac{2}{3}$ of the period)

- VCC

  -power supply input

  -provides +5V

- **GND:**- 2 pins, both must be connected to ground.

- **MN/**$\overline{MX}$:-selects either minimum mode or maximum mode operations of microprocessor.

- $\overline{BHE}$**/S7**-both high enable. -use in 8086 to enable the most significant data bus bits(D15-D8) during a read or write
  -the state of S7 is always a logic1

2.1 Minimum Mode Pins

- **IO/**$\overline{M}$ **or M/**$\overline{IO}$
  -selects memory or i/o -indicates that microprocessors address bus contains either a memory address or an i/o port address.
  -high impedance state during a hold acknowledge.

- $\overline{WR}$**:**
  -indicates that microprocessor is outputting data to a memory or io device.
  -data bus contains valid data for memory or io during the time, WR remains 0.

- $\overline{INTA}$**:**
  -a response to the INTR input pin.
  -used to gate the interrupt vector number onto the data bus in response to an interrupt request.

– $\overline{ALE}$**:**

-address latch enable.

-indicates that the microprocessor address/data bus contains address information.

-the address can be a memory address or an i/o port.

-does not float during a hold acknowledge.

– **DT/**$\overline{R}$**:** - data transmit or receive.

-indicates that microprocessors data bus is transmitting(DT/$overline R$=1) or receiving(DT/$overline R$=(DT/$overline R$=0) data.

-used to enable external data bus buffers.

– **DEN:**-data bus enable

-activates external data bus buffers.

– **HOLD:** - requests a direct memory access (DMA).

-if it is logic 1, microprocessor stops executing s/w and places its address, data and control bus at high impedance state.

-if it is a logic 0, the microprocessor executes s/w normally.

– **HLDA:** - hold acknowledge

-indicates that the microprocessor has entered the hold state.

– $\overline{SS0}$ - equivalent to the S0 pin in the maximum mode operation.

-it is combined with IO/$\overline{M}$ and DT/$\overline{R}$ to decode function of the current bus cycle.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	**function**
0	0	0	interrupt acknowledge
0	0	1	memory card
0	1	1	memory write
0	1	1	halt
1	0	0	opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	passive/inactive

Table 1: bus cycle status(8088)[minimum mode]

IO/$\overline{S2}$	DT/$\overline{S1}$	$\overline{S0}$	**function**
0	0	0	interrupt acknowledge
0	0	1	I/O card
0	1	1	I/O write
0	1	1	halt
1	0	0	opcode fetch
1	0	1	memory read
1	1	0	memory write
1	1	1	passive

Table 2: bus cycle status(8088)[minimum mode]