Digital Implementation of a New PWM Switching Scheme for Modular Structured Multilevel Voltage Source Inverter

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Abstract

This work proposes a new switching scheme for the cascaded multilevel inverter that can be suitably implemented using digital technique. Unlike other schemes, the proposed method is based on the symmetric regular sampling unipolar PWM with a single carrier and multiple modulating signals. Non-transcendental trigonometric equations that define the switching instants of the multilevel inverter are derived. This algorithm is implemented using a low-cost fixed-point micro controller on an experimental five-level cascaded inverter test-rig.

Nomenclature

MVSI	Multilevel Voltage Source Inverter
MSMI	Modular Structured Multilevel Inverter
N	number of output voltage levels (N) of the cascaded inverter
M	number of H-bridge module (M)
f_o	frequency of the output of the cascaded inverter
f_c	switching frequency or carrier frequency
A_m	amplitude of the modulation signal
m_f	modulation frequency ratio
m_i	modulation index

Introduction

In recent years, the electrical and machinery industries have begun to demand for power conversion equipment in the range of several Megawatts to be connected to a medium voltage network (2.3-6.9kV). Typical applications are the electric train, heavy-duty ac drives, conveyer belts, and unified power-flow controllers. However, power (semiconductor) switches with the suitable switching frequency at ratings above 5kV are rare; hence it is difficult to achieve inverter output voltage which is compatible to the medium voltage grid [1]. One approach is to utilise the multilevel voltage source inverter (MVSI) structure. Multilevel inverter is an array of power semiconductor switches and capacitor voltage sources, which is switched in a manner that an output voltage of stepped waveform is generated. For the normal two-level voltage source inverter, the maximum voltage output level is determined by the voltage blocking capability of each power switch. In contrast, for MVSI, the stress on each switch can be reduced in proportional to the number of output voltage levels. Thus with MVSI, higher input DC link voltage can be utilised using lower rated power switches.

Besides this important point, there are other advantages of the MVSI. It is possible to remove the expensive and bulky step-up transformer for applications that does not require galvanic isolation. Furthermore MVSI is known to improve harmonics performance, resulting in reduced switching losses. This is particularly crucial for high power application as increased power losses can complicate thermal management system design. With several levels in output waveform constructed using MVSI, the dV/dt on each power switch is reduced and so thus the EMI problem.

MVSI topologies

The development of MVSI began in the early 1980's when Nabae *et al.* [2] proposed the neutral-point clamped (NPC) pulse width modulation (PWM) inverter. Since then several multilevel topologies have evolved; most common are the NPC or Diode-Clamped Multilevel Inverter [2-4], Flying-Capacitor Multilevel Inverter [5] and Modular Structured Multilevel Inverter [6]. In addition there are emerging multilevel topologies such as the asymmetric hybrid cells [7] and soft-switching multilevel inverters [8]. A brief description of the three main MVSI topologies is given below.

Diode-Clamped Multilevel Inverter (DCMI)

The DCMI uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. An example of a single-phase four-level DCMI and its output voltage waveform is shown in Figs.1 and 2. To produce N-levels of the phase voltage, the DCMI requires N-1 capacitors on the dc bus. Thus for a four-level inverter, the dc bus consists of three capacitors C_1, C_2 and C_3. For a dc bus voltage of Vdc, the voltage across each capacitor is Vdc/3. Consequently the voltage stress for each power device is limited to Vdc/3, through the clamping diodes.

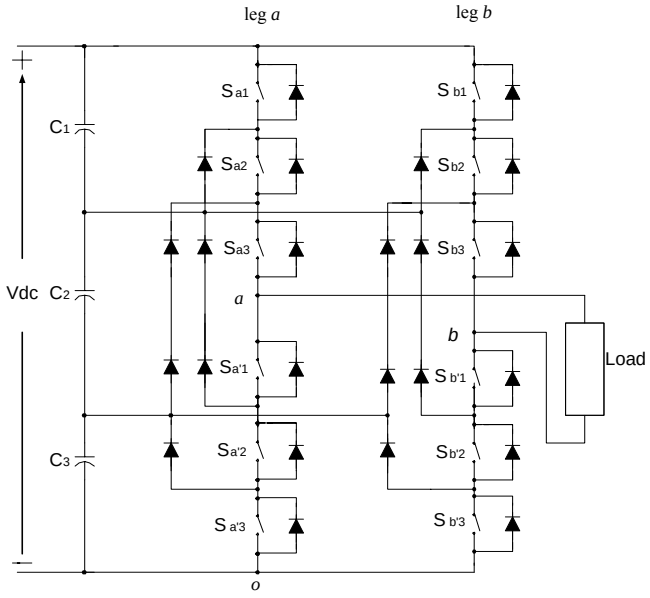


Fig. 1 A single phase four level DCMI

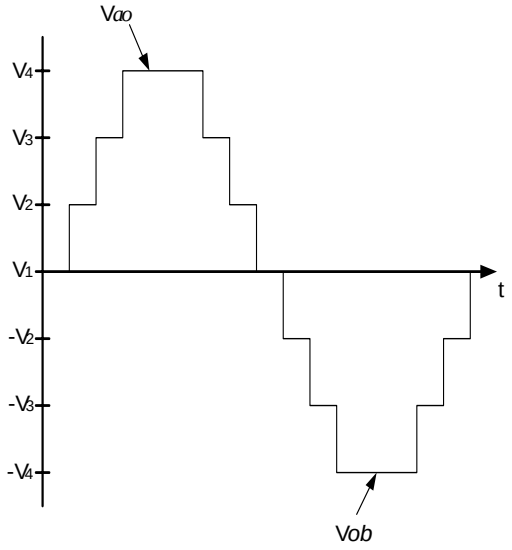


Fig. 2 Output voltage waveform

Although each power switch only required to block a voltage level of $V_{dc}/3$, each clamping diodes need to have different voltage ratings for reverse voltage blocking. Assuming that each blocking diode voltage rating is the same as the power switches, the relationship between the diodes and the output voltage levels is expressed as (N-1)×(N-2)]. This represents a quadratic increase with respect to N, and for high level inverters, the system impractical to implement. Furthermore, the voltage unbalance problem across the capacitor make this topology is unattractive to handle real power flow control.

Flying-capacitor multilevel inverter (FCMI)

Fig. 3 illustrates the fundamental building block of a single-phase four-level FCMI. The voltage level defined is similar to that of the DCMI. To generate N-level staircase output voltage, N-1 capacitors on the dc bus are needed. It is obvious that two inner-loop balancing capacitors for phase leg *a*, C_{a1} and C_{a2} are independent from those for phase leg *b*. Both phase leg share the same dc link capacitors, C_1, C_2 and C_3.

The advantage of this topology is that it eliminates the clamping diode problems present in the DCMI. In addition, the large amount of capacitance provide extra ride through capabilities during power outage. Similar to DCMI, the harmonic content is proportional with the level of the inverter, thus it's possible to avoid the output filters. Furthermore, this topology naturally limits the dV/dt stress across the devices and introduces additional switching states that can be used to maintain the charge balance in the capacitors. However, FCMI has several technical difficulties that complicate its practical application for-high power converters. To maintain the charge balance in the capacitors, the dc-link capacitors need a controller, thus adding complexity to the control of the overall circuit. Furthermore, an excessive number of storage capacitors are required when the number of inverter level is high. Therefore it is more difficult to package the bulky capacitors.

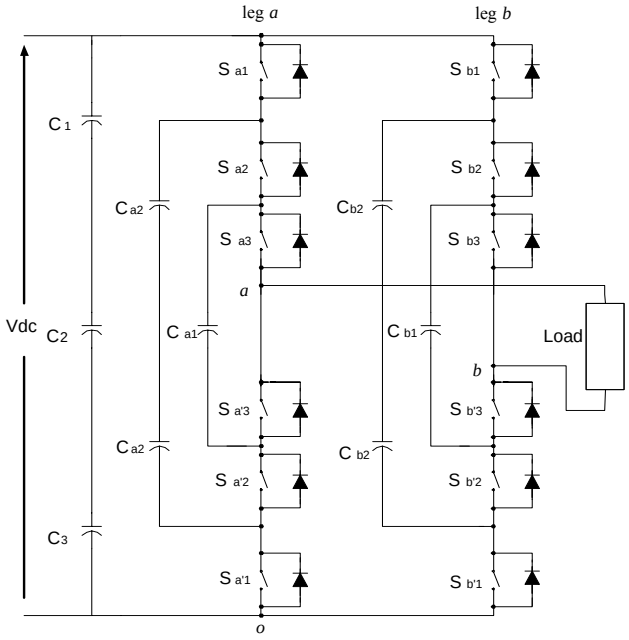


Fig. 3 Circuit of a single phase four level FCMI

Modular structured multilevel inverters (MSMI)

The MSMI, shown in Fig. 4, utilises separate dc sources to construct the multilevel phase voltage by means of H-bridges inverter modules. Due to its modular structure, it is also known as the cascaded MVSI. It inherits several advantages over other multilevel topologies in terms of circuit modularity, protection and packaging. In addition the cascaded structure requires the least number of components among all multilevel topologies to achieve the same output voltage levels. Furthermore it does not suffer the voltage-balancing problem as experienced by the DCMI. The MSMI inverter is well suited for renewable energy applications because naturally, renewable energy sources provide separate dc sources. This topology will be discussed in more details in the following sections.

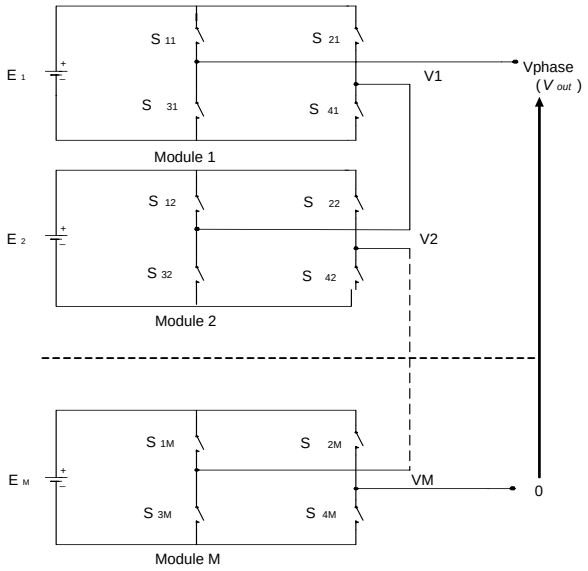


Fig. 4 Structure of a MSMI

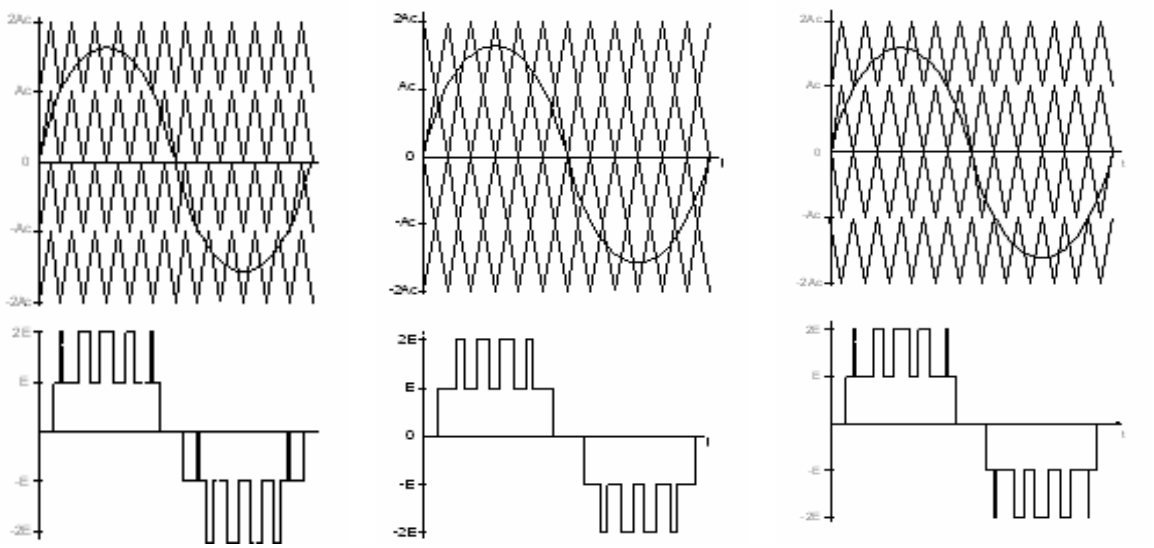
MVSI modulation techniques

In general, the modulation control of MVSI is more complicated than the two-level VSI due to the need to cater for the transitions between the voltage levels (or steps). This was demonstrated by previous works, for example [5, 9-12]. Efforts form these researchers have established the sinusoidal natural sampling PWM (SPWM) as the most popular modulation method. Other modulation methods such as the space vector PWM modulation (SVPWM) [13] and harmonics elimination PWM (HEPWM) [14-15] has also been applied to multilevel topologies for specific applications.

The SPWM for MVSI is based on the intersection of a single sinusoidal reference with N-1 triangular carrier signals. The resulting intersection points become the switching instants of the PWM pulses. As far as the carrier signals alignment is concerned, three carrier phase shifting (or commonly known as the disposition method) schemes are suggested:

- Phase disposition (PD) where all the carrier signals are in phase,
- Alternative phase opposition disposition (APOD) where the carrier signals above the zero line of sinusoidal modulating waveform are 180 out of phase with those below the zero line, and
- Phase disposition (POD), where each carrier signal is phase shifted by 180 from its adjacent carriers.

Figs. 5(a) to 5(c) show these disposition techniques. Each of these variations has particular harmonic benefits, which have been argued extensively in [11].



(a) APOD (b) POD (c) PD

Fig. 5 Phase disposition of the five level MVS

While the literature on the modulation techniques for MVSI can be considered extensive, there seems to be inadequate description on how such scheme can be implemented effectively on a digital system. For the multi carrier schemes described in [16], digital implementation results in an inherent "jump" in more than one level of the output voltage during level transitions. The level jumps seriously distort the output voltage waveform, thus degrading its harmonics spectra. The same authors proposed software solutions to check and then to avoid these undesired conditions. However the correction scheme is rather complicated and its practical implementation can be quite cumbersome.

This work attempts to propose an alternative switching scheme for the MSMI that utilizes the symmetric regular sampling unipolar PWM. Unlike other schemes, the proposed method is based on the intersection of a single carrier waveform with multiple modulating signals. It was discovered that by using this technique, switching transitions can be programmed effectively using a simple fixed-point microprocessor. It was also observed that the level jumping problem vanished. To the benefit of the readers, the paper begins by outlining the principle of the modulation and the derivation trigonometric equations that define the switching instant. To determine the effectiveness of the algorithm, a Matlab-Simulink simulation is carried out. Finally, to validate workability of the proposed scheme, a single-phase five-level MSMI is built and tested.

The proposed Modulation Scheme

Modulation principle

The proposed scheme is implemented on a MSMI. For convenience, an N-level, single-phase MSMI is redrawn as Fig 6. The ac output voltage of each module is connected in series to form an output voltage, V_{out}. The number of H-bridge module (M), depends on the number of levels (N) required and can be written as:

$$M=\frac{N-1}{2} \tag{1}$$

It is usually assumed that N is odd, as this would give an integer-valued M. By different combinations of the four switches, S_{1M} through S_{4M}, each module can generate three different voltage outputs, i.e. +E, E, and 0. The total output voltage is then constructed by the sum of the output voltage from each module. For example, a five level inverter would have an output levels of +2E, +E, 0, E, and –2E.

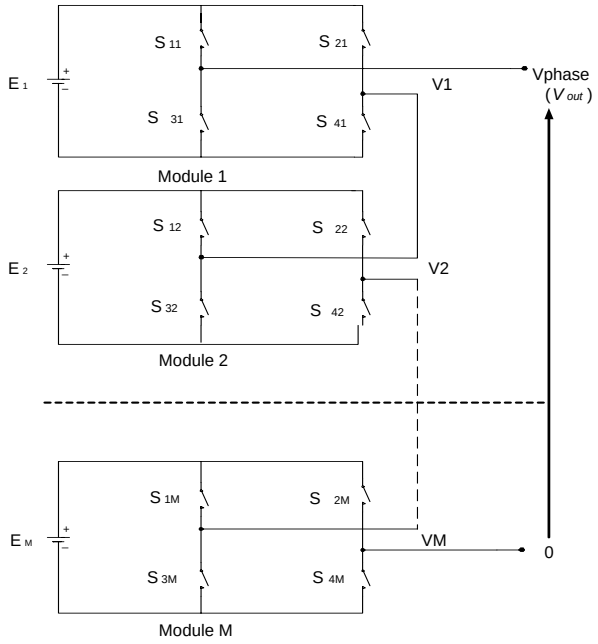


Fig. 6 MSMI Structure

The proposed modulation scheme is based on the classical unipolar, symmetric PWM switching technique. The method compares several modified sinusoidal modulation signals $s_u(k)$ with a single triangular carrier signal $c(k)$ as shown in Fig. 7. Each of these modified modulation signals have the same frequency (f_o) and amplitude (A_m). The carrier signal is a train of triangular waveform with frequency f_c and amplitude A_c. Equations (2) and (3) define the modulation index and ratio for N-level inverter with M number of modules:

$$m_i = \frac{A_m}{A_c} \cdot \frac{1}{\frac{(N-1)}{2}} = \frac{A_m}{MA_c} \tag{2}$$

$$m_f = f_c / f_o \tag{3}$$

The variable k represents a position of each modulated width pulses, initiated from k= 1,2,3…m_f/2. Intersection between the modified modulation signals and the carrier signal defines the switching instant of the PWM pulses.

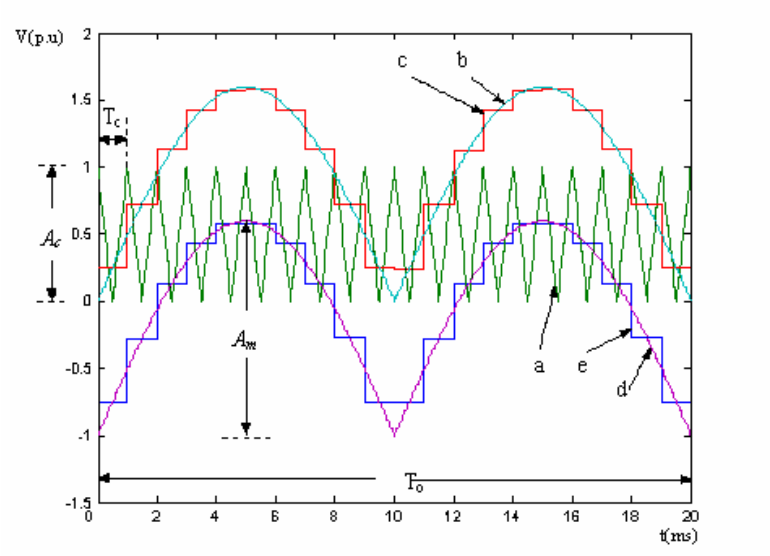


Fig. 7 The modified sinusoidal modulation signals with a single carrier signal. Waveform labels: (a) Carrier signal $c(k)$, (b) Absolute sinusoidal modulation signal $m_1(t)$, (c) Modified sinusoidal modulation signal $s_1(k)$ of $m_1(t)$, (d) Shifted absolute sinusoidal modulation signal $m_2(t)$, (e) Modified sinusoidal modulation signal $s_2(k)$ of $m_2(t)$.

To illustrate the principle of the proposed scheme, a five-level inverter at $m_i = 0.4$ and m_i=0.8 for E=100V is shown in Figs 8 and 9, respectively. For clarity, a low value of m_f, i.e 20 is arbitrary chosen. For a five level output, two modulation signals namely $s_1(k)$ and $s_2(k)$ and single triangular carrier $c(k)$ are involved in the modulation process. Signal $s_2(k)$ is actually $s_1(k)$ that shifted down by the amplitude of triangular carrier signals A_c. In general signal $s_{u+1}(k)$ is shifted down by A_c from $s_u(k)$. The PWM pulses $V_1(k)$ is generated from the comparison between $s_1(k)$ and $c(k)$, while $V_2(k)$ is from comparison between $s_2(k)$ and $c(k)$. The comparison is designed such that if $s_1(k)$ is greater than $c(k)$, a pulse-width $V_1(k)$ is generated; if $s_2(k)$ is greater than $c(k)$, $V_2(k)$ is generated. On the other hand if there is no intersection, then $V_1(k)$ and $V_2(k)$ remain at 0. It can be seen in Fig. 6 that for the case of $m_i \leq 0.5$, only $s_1(k)$ and carrier signal $c(k)$ is involved in the modulation process. There is no intersection for $s_2(k)$. Therefore, the output pulse $V_2(k)$ is zero. The output voltage V_{out}, which is the sum of $V_1(k)$ and $V_2(k)$, is then similar to the conventional three-level unipolar PWM case. For m_i>0.5, as depicted in Fig. 7, both modulating signal, i.e. $s_1(k)$ and $s_2(k)$ intersect the carrier and therefore V_1 and V_2 pulses are generated. As a result, a multilevel output voltage V_{out} is formed.

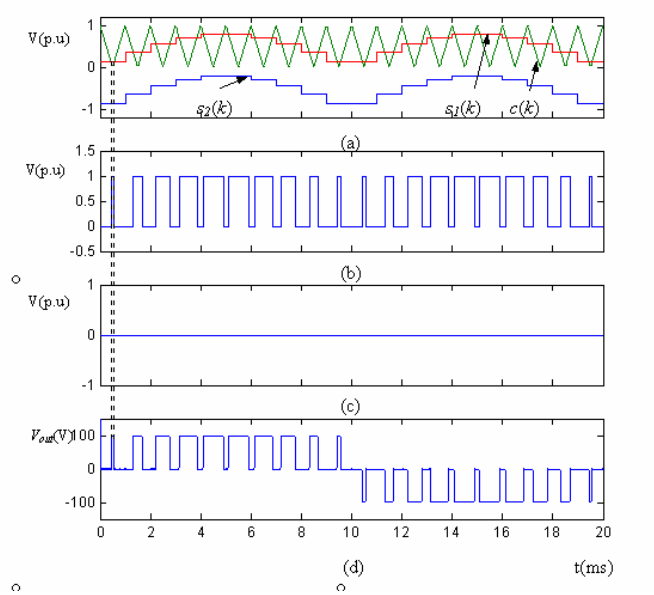


Fig. 8 Proposed modulation scheme for $m_i = 0.4$, $m_f = 20$.Traces: (a) Modulation signals and carrier signal (b) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform

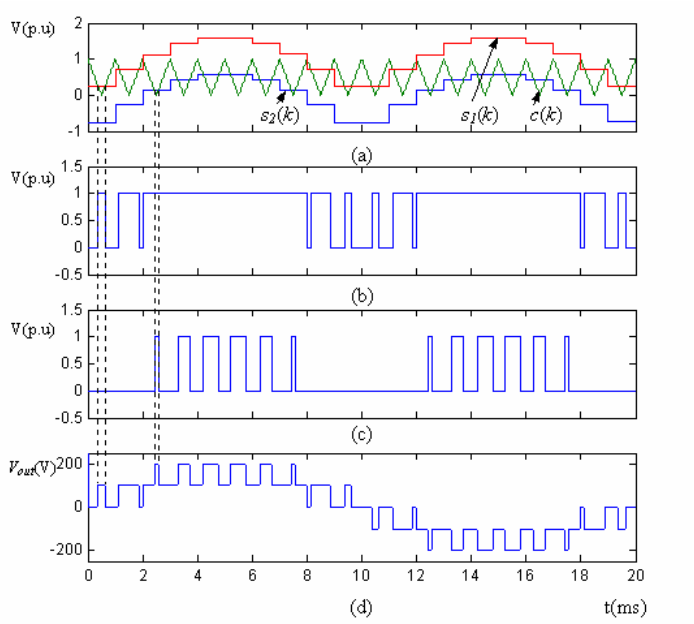


Fig. 9 Proposed modulation scheme for $m_i = 0.8$, $m_f = 20$. Traces: (a) Modulation signals and carrier signal; (b) PWM pulses produced from comparison between $s_1(k)$ and $c(k)$, $V_1(k)$; (c) PWM pulses produced from comparison between $s_2(k)$ and $c(k)$, $V_2(k)$; (d) PWM output waveform.

For a N-level inverter there are M modulating waveform, which corresponds to M number of H-bridge modules. The *n*th level transitions occur at:

$$m_i = \frac{n}{\mathrm{M}} \quad ; n = 1 \ldots M \text{ -} 1 \tag{4}$$

For example for a 9 level inverter, N=9; therefore M=4. The transition occurs when the modulation index m_i reaches 0.25, 0.5 and 0.75. Note that the definition of modulation index used in this discussion is given by Equation (2).

Derivation of the switching angle equations

It can be seen that the k^{th} rising edge is defined as the intersection of the negative slope carrier $c^-(k)$ and two set of modulating signals $s_1(k)$ and $s_2(k)$. Since the waveform is symmetrical, the intersection of the positive slope carrier $c^+(k)$ and the modulating signals is not required. It can be deduced from the rising edge equations, i.e. the intersection between $c^-(k)$ and $s_1(k)$ or $s_2(k)$ as shown in Fig. 10.

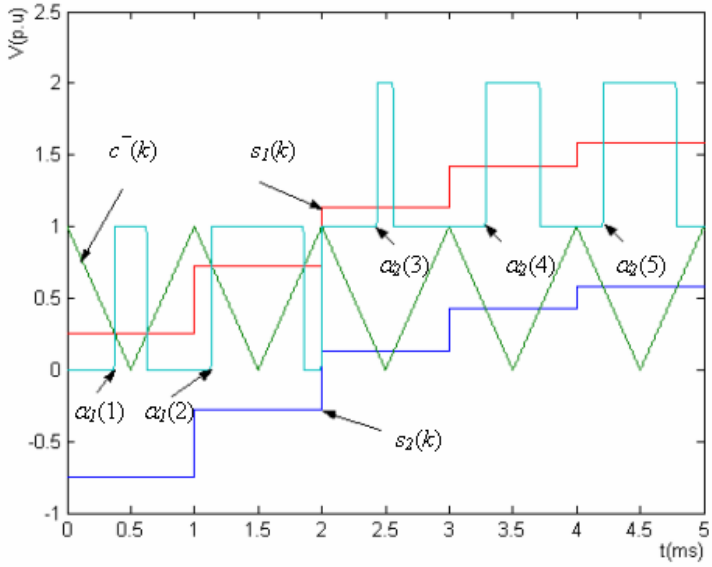


Fig. 10 Intersection between single carrier and modified sinusoidal modulation signals

The straight-line equation for the carrier wave is denoted by $c^-(k)$ for the negative slope. It can be expressed as:

$$c^-(k) = \left(\frac{-A_c}{\frac{T_c}{2}} \right) \alpha_k + hA_c; \quad k = 1,2,3....; h = 1,3,5.... \tag{5}$$

Where f_c is a carrier frequency and f_o is a modulating signal frequency. The symmetric regular sampled modulation signals $s_1(k)$ and $s_2(k)$ can be expressed as:

$$s_1(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] \text{ and } s_2(k) = A_m \sin\left[\omega(i) + \frac{\pi}{m_f}\right] - A_c \tag{6}$$

Where $i = 0,1,2...\frac{m_f}{2}$-1 when $s_1(k)$ and $s_2(k)$ intersects with $\bar{c}(k)$. The angular frequency ω, in (6) is represented by $2\pi/m_f$. Using the arithmetic regression and the k^{th} raising edge ($\alpha_1(k)$) of PWM signal $V_1(k)$ is produced by the intersection between $s_1(k)$ and $\bar{c}(k)$, i.e.:

$$\left(\frac{-A_c}{\frac{T_c}{2}}\right)\alpha_1(k) + hA_c = A_m \sin\left(\omega(i) + \frac{\pi}{m_f}\right); \quad h = 2k-1 \text{ and } i = k-1 \tag{7}$$

Solving, this rising edge kth transition point $\alpha_1(k)$ is represented by:

$$\alpha_1(k) = \frac{T_c}{2}\left[(2k-1) - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{8}$$

Using the same method, i.e. the intersection between $s_2(k)$ with $\bar{c}(k)$, every rising edge $\alpha_2(k)$ of PWM signal $V_2(k)$ can be expressed as:

$$\alpha_2(k) = \frac{T_c}{2}\left[2k - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{9}$$

Equations (8) and (9) can be generalized to produce a general switching angle for an N-level inverter:

$$\alpha_u(k) = \frac{T_c}{2}\left[(2k+u-2) - \frac{A_m}{A_c}\sin\left(\omega(k-1) + \frac{\pi}{m_f}\right)\right] \tag{10}$$

Where $u=1,2..$M and $\mathrm{M}=\frac{\mathrm{N}-1}{2}$. Equation (10) can be used to generate the k^{th} PWM pulses for a cascaded inverter of any level N. Note that the variable u corresponds to the particular H-bridge module that the switching will be subjected on. It follows that α_u is the switching angle for the k^{th} pulse of a particular bridge module. It can also be noted that this equation (10) is non-transcendental. All the variables at the

right hand side of this equation are known and therefore the switching angles can be calculated directly. Its practical implementation using digital technique is therefore quite straightforward.

Simulation of a Five Level MSMI

To obtain an insight on the proposed modulation scheme, a MATLAB-Simulink simulation of a five-level MSMI, shown in Fig. 11 is carried out. The DC source is set to 100V. The fundamental and switching frequency is set to 50HZ and 1Khz, respectively. This corresponds to m_r of 20.

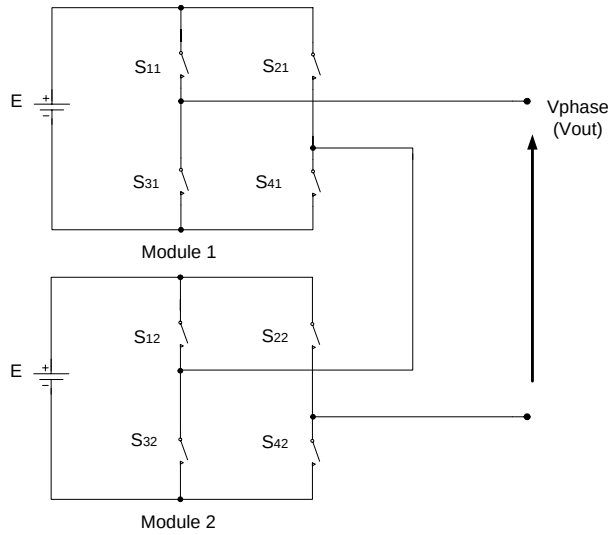


Fig. 11 Single phase five level MSMI.

Simulink block diagram to generate PWM signals $V_1(k)$ and $V_2(k)$ is shown in Fig. 12. To produce a five level inverter with m_i greater than 0.5, two modulation signals are required namely, $s_1(k)$ and $s_2(k)$. Signal $s_1(k)$ is created after symmetric regular sampled passed through absolute block (Abs) while signal $s_2(k)$ is formed when $s_1(k)$ is subtracted with the amplitude of carrier signal. For simulation purpose, amplitude of carrier signal $c(k)$ is set to 1 p.u.

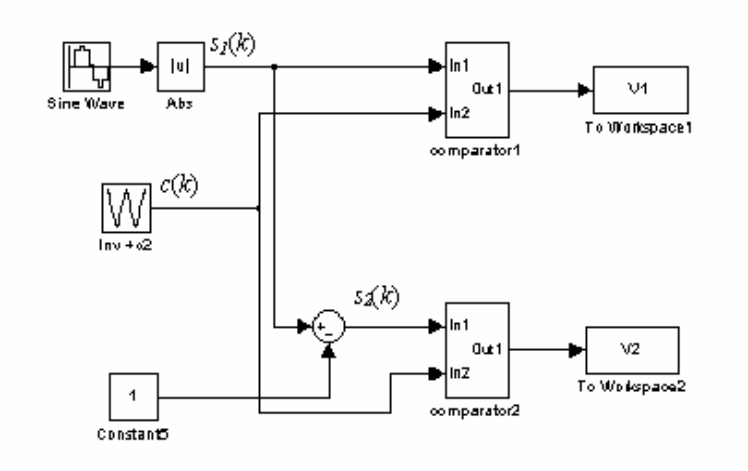
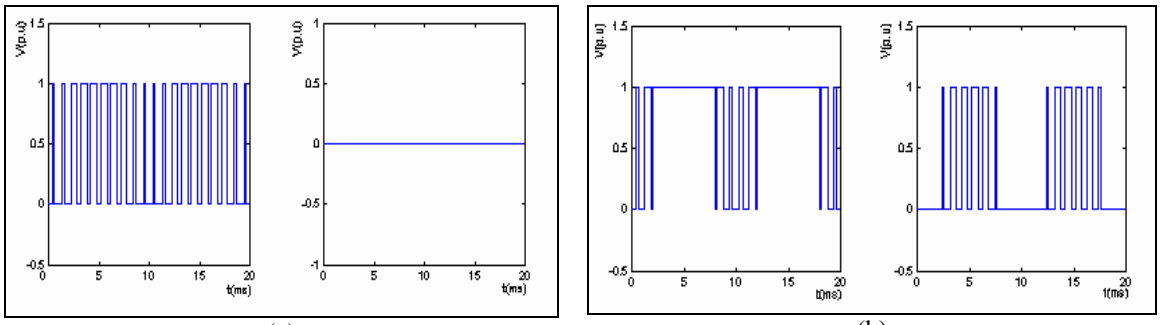


Fig. 12 Simulink block diagram for PWM signal generation

Each modulation signals $s_1(k)$ and $s_2(k)$ is separately compared to a single carrier signal $c(k)$ using comparator 1 and 2. The output signals $V_1(k)$ and $V_2(k)$ obtained after this comparison are shown in Fig. 13. However it has to be noted that if m_i less than 0.5, only $V_1(k)$ is generated while $V_2(k)$ is always zero as shown in Fig. 15(a). This is because the intersection occurred only between $s_1(k)$ and $c(k)$, while for $s_2(k)$, it is not intersected at all.



(a) (b)

Fig.13 Simulation result of PWM signals generation with (a) $m_i \leq 0.5$, (b) $m_i > 0.5$

For a five-level MSMI, there are 16 different switches configurations for the gating signals. For this work, the selected switching state configuration is shown in Table 1. The selection is advantageous because only one pair of the power devices in each module needs to be switched at high frequency. Another pair is commutated at the fundamental frequency. In effect, the overall switching losses of the inverter are reduced.

Table 1 Selected switching state for a five-level MSMI

Load Voltage	+2E	+E	0	0*	-E	-2E
S_{11}	ON	ON	ON	OFF	OFF	OFF
S_{21}	OFF	OFF	ON	OFF	ON	ON
S_{31}	OFF	OFF	OFF	ON	ON	ON
S_{41}	ON	ON	OFF	ON	OFF	OFF
S_{12}	ON	ON	ON	OFF	OFF	OFF
S_{22}	OFF	ON	ON	OFF	OFF	ON
S_{32}	OFF	OFF	OFF	ON	ON	ON
S_{42}	ON	OFF	OFF	ON	ON	OFF

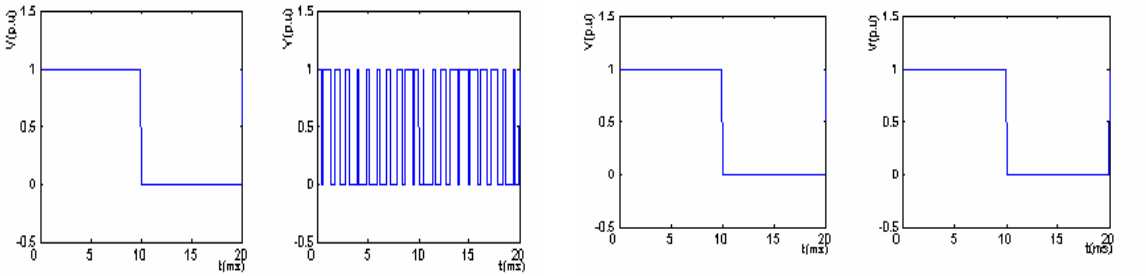
0 indicates the switching state at zero load voltage for positive half cycle and 0* indicates the switching state at zero load voltage for negative half cycle.

As shown in Table 1, $S_{11}$and S_{12} is the same signal. The same is true for their compliment, i.e. S_{31} and S_{32}. This configuration also shows that for each module, the lower switch is always complement with the upper switch. Equations below illustrate the relationship among the switches:

$$\begin{aligned} S_{11} &= S_{12} = \overline{S_{31}} = \overline{S_{32}} \\ S_{21} &= \overline{S_{41}} \\ S_{22} &= \overline{S_{42}} \end{aligned} \tag{11}$$

From Equation (11), it can be concluded that with the selected switches configuration, three signals are sufficient to produce all gating signals for five-level MSMI ($m_i > 0.5$). However for a three-level output ($m_i \leq 0.5$), only two signals, i.e. the fundamental frequency square wave and $V_1(k)$. The remaining signal ($V_2(k)$), is automatically set to zero. Furthermore, to produce PWM gating signal for switches S_{21} and S_{22}, $V_1(k)$ and $V_2(k)$ are EXOR-ed with the fundamental frequency square wave.

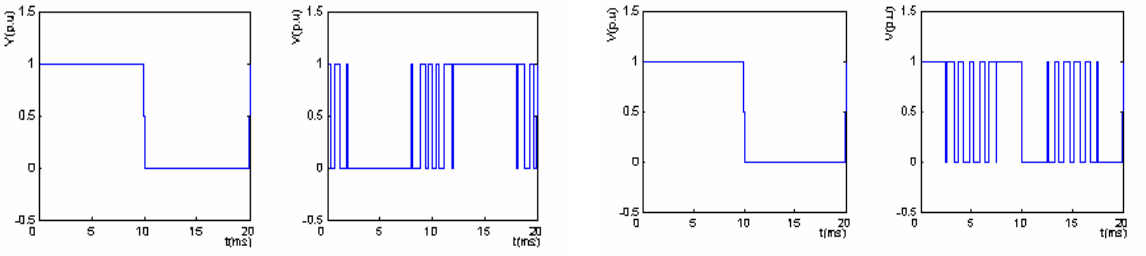
Fig. 14 shows gating signals for switches S_{11}, S_{21}, S_{12} and S_{22} for $m_i = 0.4$ and $m_f = 20$. Note that switch S_{21} is the only PWM signals that is switched at high frequency. The switching frequency of the switch is proportional to modulation ratio m_f. Gating signals for switches S_{22}, S_{11} and S_{12} is the same 50Hz square wave that is used in EXOR-ed process. The gating signals for S_{31}, S_{41}, S_{32} and S_{42} are not shown, as they are the complements of S_{11}, S_{21}, S_{12} and S_{22}, respectively. All gating signals in the figure indicate that with the selected switching configuration applied to the MSMI, only two switches, i.e. S_{21} and S_{41} are switched at high frequency. The remaining six switches S_{11}, S_{31}, S_{12} S_{22}, S_{32} and S_{42} are switched at fundamental frequency. For this reason it is possible to use lower cost switch for the latter six switches.



Gating signal for S_{11} Gating signal for S_{21} Gating signal for S_{12} Gating signal for S_{22}

Fig. 14 Gating signals of five-level MSMI with $m_i = 0.4$ and $m_f = 20$.

Fig. 15 shows gating signals for $m_i = 0.8$ and $m_f = 20$. For this case, four switches S_{21}, S_{41}, S_{22} and S_{42} are switched at high frequency. The remaining four switches S_{11}, S_{31} and their complements are switched at fundamental frequency.

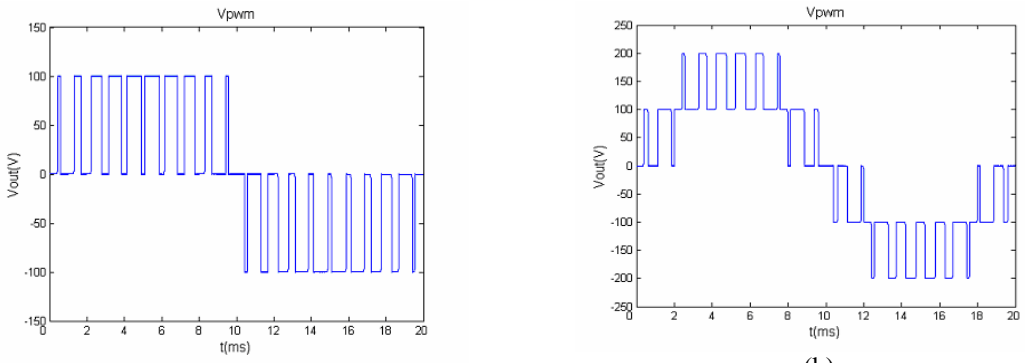


Gating signal for S_{21} Gating signal for S_{21} Gating signal for S_{12} Gating signal for S_{22}

Fig. 15 Gating signals of five-level MSMI with $m_i = 0.8$ and $m_f = 20$

To obtain the output voltage, all gating signals S_{11}, S_{21}, S_{31}, S_{41}, $S1_2$, S_{22}, S_{32} and S_{42} are connected to their respective power switches.

Fig. 16 shows the inverter output waveform for m_i=0.4 and $m_i = 0.8$, respectively.



(a) (b)

Fig. 16 Output voltage waveform: (a) $m_i = 0.4$ and $m_f = 20$ (b) $m_i = 0.8$ and $m_f = 20$

Hardware Implementation

Generation of PWM waveform

A five-level 250 Watts experimental rig is built to prove the effectiveness of the proposed modulation technique. The inverter input voltages are fixed at 100V dc for each H-bridge module with pure resistive load. The PWM signal generation is performed by the SIEMENS SAB-C167CR-LM fixed-point microcontroller. Integrated on-chip peripherals such as Serial Port, bi-directional Parallel Port, Timers, PWM module and Peripheral Interfaces units make the interfacing task much easier and with higher reliability. To obtain a five-level output voltage as described in the simulation section, three signals need to be generated, namely the fundamental frequency square wave, the PWM signal $V_1(k)$ and the PWM signal $V_2(k)$. These signals are generated using on chip PWM module. The PWM module eliminates the requirement for complicated external timers. It allows the generation of up to four independent PWM signals. The standard PWM is selected to generate fundamental frequency square wave, meanwhile the symmetrical PWM is dedicated to generate V_a and V_b.

Overall functional block diagram

The functional block diagram of the microcontroller ports, its associated logic gates, IGBT gate driver and power circuit are shown in Fig. 17. The PWM signals ($V_1(k)$ and $V_2(k)$) and 50 Hz square wave are generated by the PWM module and latched out via C167 microcontroller parallel ports P7.0, P7.1 and P7.3, respectively. The fast external interrupt signal for P7.2, which operates as input trigger for P7.1 is activated via port P.2.9. The enable signals for IGBT gate drive are also supplied by microcontroller via ports P2.0 through P2.3.

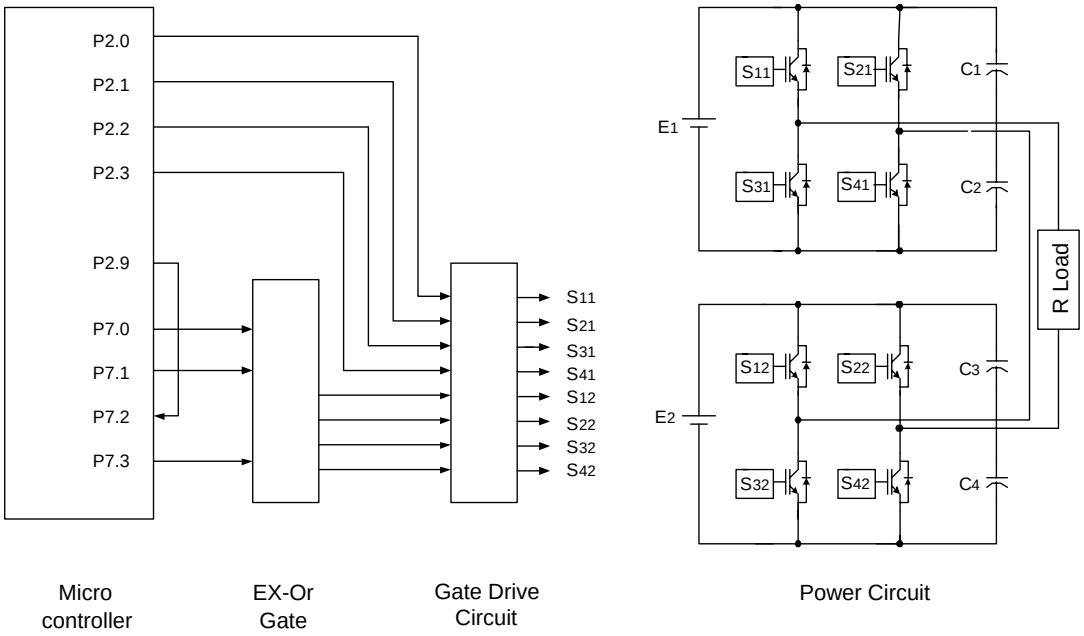
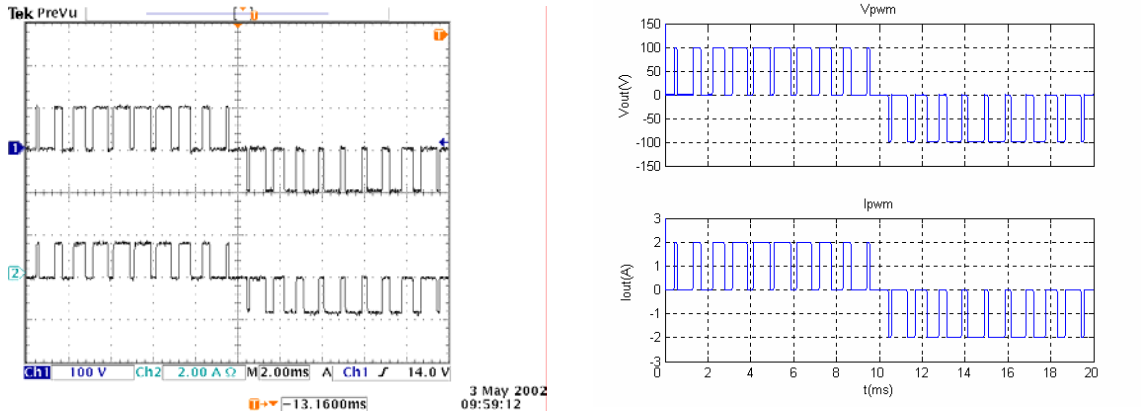


Fig. 17 Functional block diagram of the inverter system.

As illustrated in Fig. 17, two modules of cascaded power circuit are required for a five-level inverter. Both modules are connected in series and constructed from IGBT switches and dc link capacitors. Power switches used for the inverter are type IRG430CKD IGBTs, manufactured by International Rectifier.

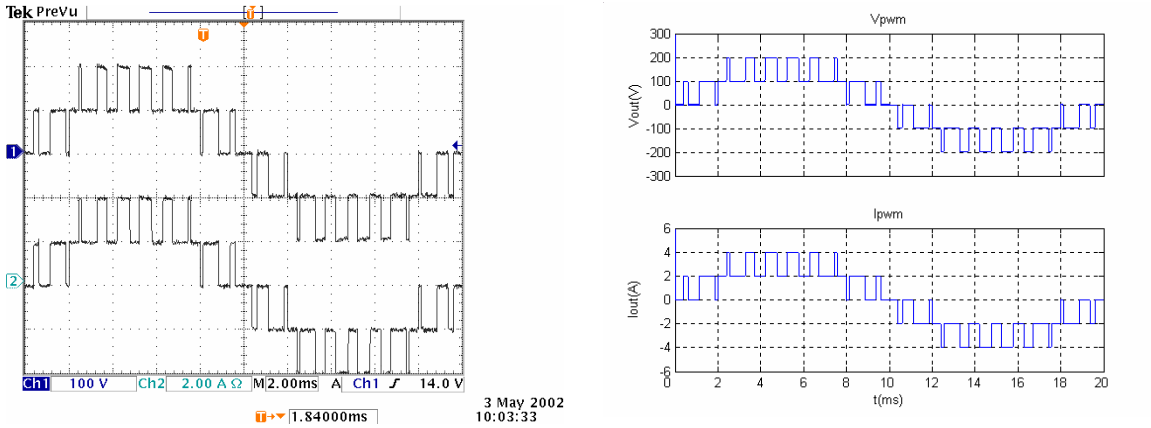
Results

Fig. 18 shows the oscillogram of the output voltage and current of the inverter for $m_i = 0.4$ and $m_f = 20$. For comparison, the MATLAB simulation results are shown side-by side. As can be observed, the output voltage is similar to a three-level inverter, because $m_i < 0.5$. For $m_i = 0.8$ and $m_f = 20$ shown in Fig. 19, the five-level PWM waveform is obtained. Clearly the output voltage is consistent with the theoretical prediction.



(a) (b)

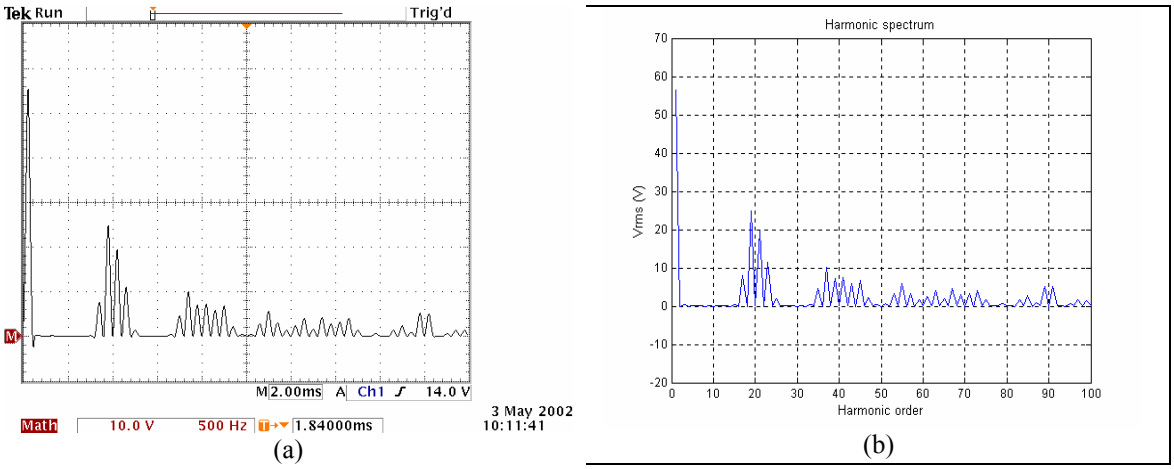
Fig. 18 Output waveforms for $m_i = 0.4$; $m_f = 20$ (a): Practical result (b) MATLAB simulation
Top trace: output voltage. vertical scale 100V/div.bottom trace: output current.
Vertical scale 2A/div. horizontal scale 2ms/div.



(a) (b)

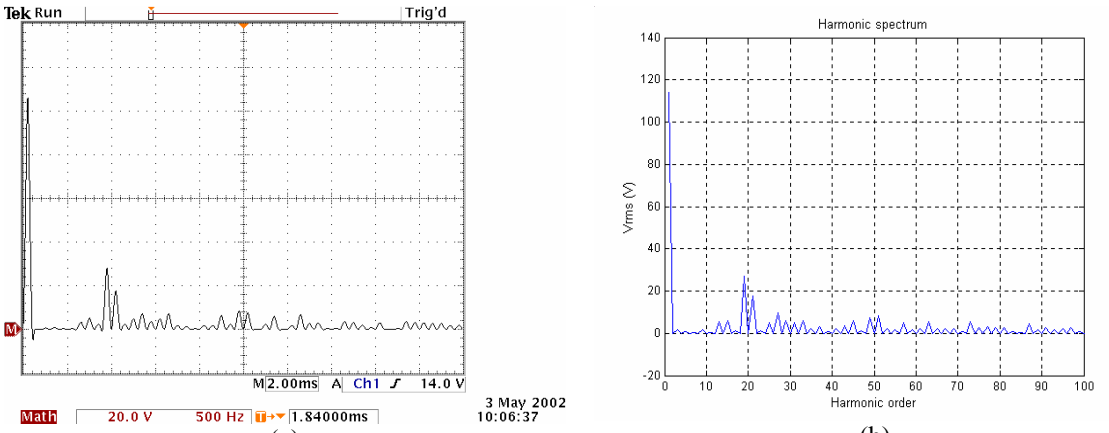
Fig. 19 Output waveform for $m_i = 0.8$; $m_f = 20$ (a): Practical result. (b) MATLAB simulation
Top trace: Output voltage. vertical scale 100V/div., bottom trace: Output current.
Vertical scale: 2A/div., horizontal scale 2ms/div.

For the case of $m_f = 20$ and $m_i = 0.4$, the output voltage harmonic spectrum are shown in Fig. 20, while for the case of $m_f = 20$; $m_i = 0.8$ it is illustrated in Fig. 21. As can be seen, the magnitude of the fundamental voltage for the latter case is doubled but the harmonics remain about the same. As a result, the ratio of its harmonics to a normalised fundamental is approximately half of the former.



(a) (b)

Fig. 20 Harmonics of output voltage for $m_i = 0.4$; $m_f = 20$ (a): Practical. (b) MATLAB simulation
Vertical scale 10V/div. , horizontal scale 500Hz/div.



(a) (b)

Fig. **21** Harmonics f output voltage for $m_i = 0.8$; $m_f = 20$ (a): Practical. (b) MATLAB simulation
Vertical scale 10V/div., horizontal scale 500Hz/div

Fig. 22 shows the comparison the harmonic profile of the proposed modulation technique with the POD scheme (using symmetrical regular sampling PWM). It can be observed that the proposed technique produces identical spectra to the POD scheme for all major harmonics. It can be suggested that both strategies produce harmonic components of the same magnitude and frequencies despite the obvious difference between the two modulation principles.

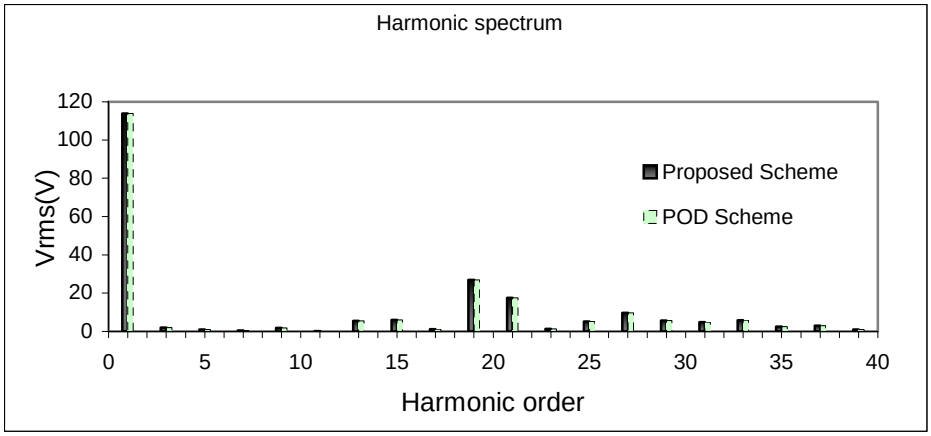
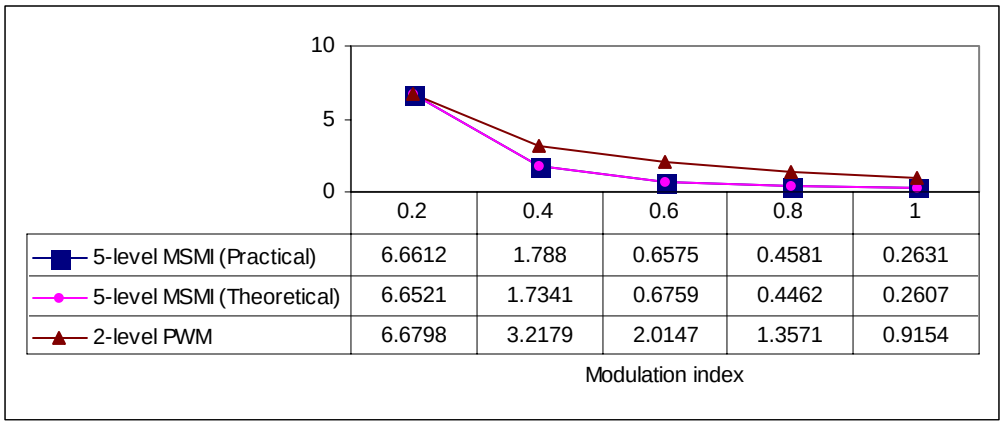


Fig. 22 Comparison of harmonic spectrum between the proposed scheme and POD scheme

Fig. 23 shows the comparison of the THD between a five-level single-phase MSMI and a conventional two-level inverter configuration. The figure shows that for both cases, a poor THD are obtained when the inverter operated at low modulation index. This is to be expected because at $m_i \leq 0.5$, the cascaded inverter essentially behaves like a conventional three-level inverter. A better THD is obtained when the inverter operated at higher modulation index, particularly when $m_i > 0.5$. For example, at modulation index equals 1.0, it was found that THD is three times superior compared to a conventional two-level inverter.



	0.2	0.4	0.6	0.8	1
5-level MSMI (Practical)	6.6612	1.788	0.6575	0.4581	0.2631
5-level MSMI (Theoretical)	6.6521	1.7341	0.6759	0.4462	0.2607
2-level PWM	6.6798	3.2179	2.0147	1.3571	0.9154

Fig. 23 Variation of THD for five-level and two-level SPWM inverter configuration

Conclusions

This paper presents a new switching scheme for the modular structured multilevel inverter. The proposed scheme is based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. Mathematical equations that define the PWM switching instants are derived. Due to the non-transcendental nature of the equation, digital implementation is possible. A low power inverter test rig is built and the PWM algorithm is programmed using a low-cost fixed-point microcontroller. Several tests to quantify the performance of the inverter with the proposed modulation scheme are carried out. The results were compared with MATLAB simulation and are found to be in very close agreement.

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