NCTU-CS Digital System Lab.

LAB 04 – Circle

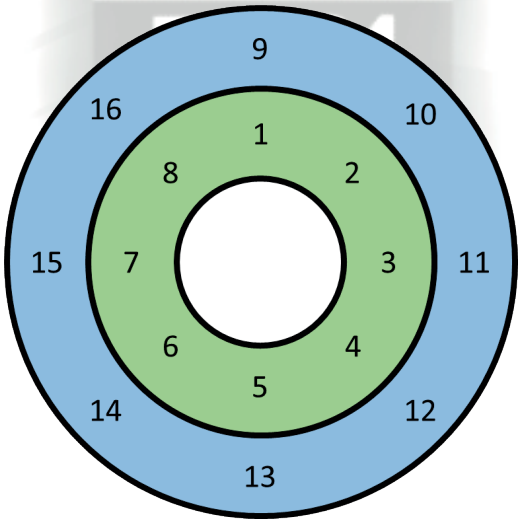
Design: CIRCLE

Data Preparation

Extract LAB data for TA's directory.
% **tar xvf ~2016dlabta05/Lab04.tar**

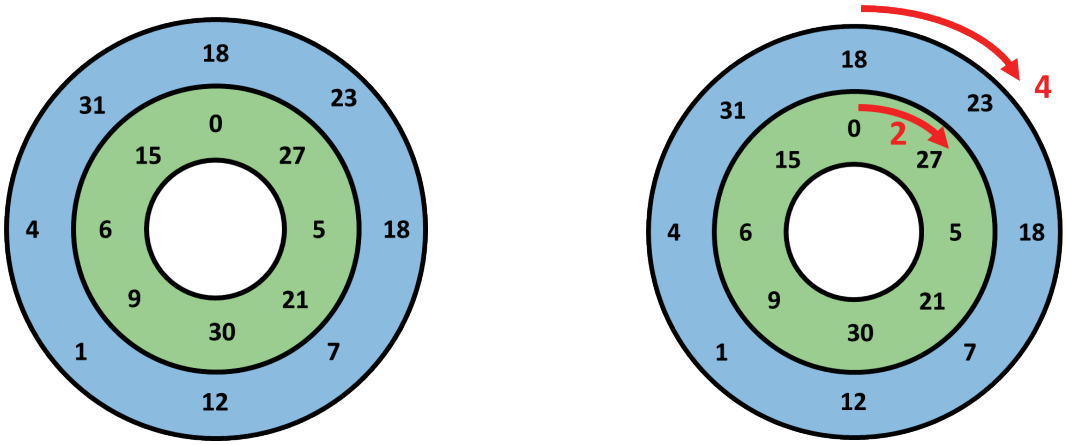
Design Description

There are two concentric circles with 16 positions, as the following figure shows. You will get 16 values for each position from input sequence. And there are two numbers for you at the same time to turn each circle clockwise. After finishing the turning task, two values should be sum for eight radius directions. Finally, **sort** the eight values in order of size. You should **output the eight values** from the **minimum** to the **maximum**.



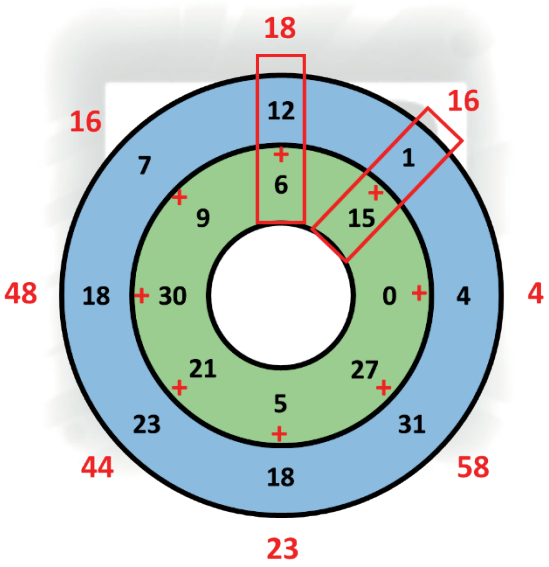
Example：

Input:



The circle 1 is 2, and circle 2 is 4.

After rotation:



The sum of each direction are 18、16、4、58、23、44、48、16

And the sorted sequence for output are 4、16、16、18、23、44、48、58

Inputs

1. Sixteen input data for **in** will be input in 16 continuous cycles while **in_valid** is high
2. **circle 1** and **circle 2** valid only at the first input cycle.
3. All signal are unsigned integer.

4. Input information :.

Input port	Bit Width	Description
in	5 bits	16 values for each position
circle1	3 bits	Number of turns for circle 1
circle2	3 bits	Number of turns for circle 2
in_valid	1 bit	High when **in** is valid
clk	1 bit	Clock
rst_n	1 bit	**Synchronous *active-low*** reset

Outputs

1. Your answer should be output at out for **8 cycle**.
2. Output information :

Output port	Bit Width	Description
out	6 bit	8 values after sorting
out_valid	1 bit	High when **out** is valid

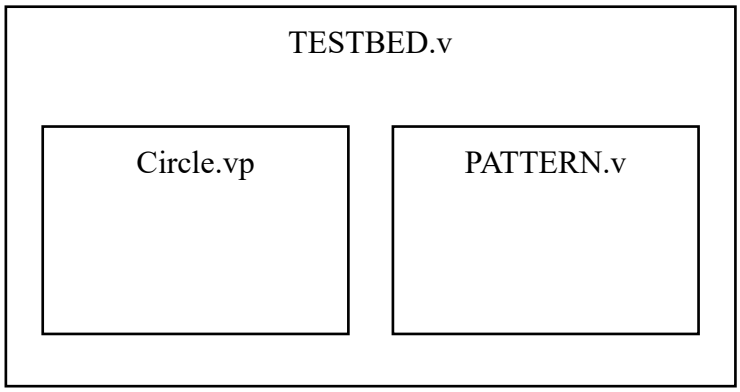
Specifications

1. Top module name : Circle (File name : Circle.vp)
2. The clock period is 4 ns.
3. It is a **synchronous reset** and **active-low** architecture. Signal out and out_valid should be zero after reset.
4. All inputs will be given at negative edge of clk, and all output is synchronized at positive edge of clk.
5. The latency should not be **more than 100.**
6. Grading policy:

   Pattern: 80%

   Question: 20%

Block Diagram



Note

1. Simulation step:
   - Put your Pattern and Testbench in 00_TESTBED
   - Go to 01_RTL and simulation to check Pattern :

     ./01_run to run 1 correct and 7 in correct designs

     Or **./01_run_1** to run the correct design only
   - Clear up : ./09_clean_up
2. Please add your student ID and name to the file name of .v file before upload file on e3 platform:
   Pattern_0556123_陳小明.v
3. Sample waveform: