Computer Organization, Spring 2017

Lab 5: Pipeline CPU I

Due : 2017/05/28

1. Goal

In this lab, please modify the single cycle processor designed in lab4 to a pipelined processor. And you don't have to consider the hazard issue.

2. Demands

A. Please use ModelSim or Xilinx as your HDL simulator.

B. One person form a group. Please attach your names and student IDs as comments in the top of each file. (Ex. Lab5_0416001.zip) The type of compressed file must be "zip". Other form of file will get -10%. The assignment you upload on E3 must have the form of "Lab5_student ID.zip".

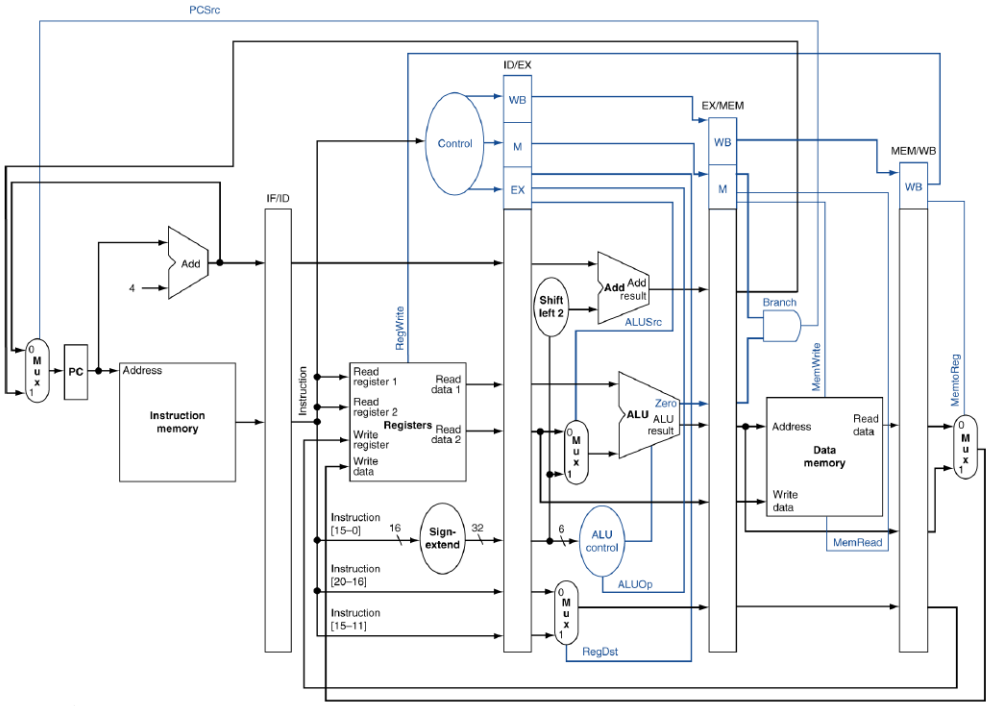
C. Reg_file(negative-edge triggered), Program_Counter, and TestBench are supplied.

D. For each pipeline register, it should contain the fields for data and control signals.

E. Instruction set: we will test part of the instructions which have been implemented in previous lab : add, addi, sub, and, or, nor, lui, sll, slt, lw, sw, beq, bne. We will not test "jump" instruction in this lab but will test it in the next lab. And we will not test "jal","jr" in lab5 and lab6. You may remove the circuits for jr and jal in your design.

3. Pipelined CPU

a. Architecture diagram



According to the above diagram, in this lab you should implement a five-stage pipelined processor with IF, ID, EX, MEM, and WB stages. You should insert a pipeline register between each two stages. Each pipeline register should contain the fields for data and control signals. The pipeline registers are written when the positive clock edge occurs.

b. The description of pipeline stage

The function of each stage is described as follows:

IF stage: In this stage, the processor fetches an instruction from the instruction memory and performs PC + 4.

ID stage: In this stage, the processor decodes the instruction to generate the control signals, reads two source registers, and generates the sign-extended immediate value.

EX stage: In this stage, ALU_Ctrl generates control signals for function units according to ALUOp. At the same time, Register Write ID and branch target are also determined in this stage.

MEM stage: In this stage, the processor accesses data memory according to the control signals. The modification of PC from branch taken instruction is also performed in this stage.

WB stage: In this stage, the processor will write the value into register file according to the control signal when negative clock edge occurs.

c. Description of pipeline register

Please design four pipeline registers. Each pipeline register must be "positive-edge triggered", has default value 0.Then, insert these pipeline registers into your single-cycle CPU designed in Lab4 to accomplish the pipelined CPU required in this lab.

DO NOT set any delay time for the sequential circuits of the pipelined registers designed by you.

4. Test

There are 2 test patterns, CO_P5_test_data1.txt, CO_P5_test_data2.txt.

The default pattern is the first one.

5. Grade

a. Total score: 100pts. COPY WILL GET A 0 POINT!

b. Instruction score: 80 pts.

c. Report: 20pts –format is in CO_document.

6. Hand in your assignment

Please upload the assignment to the E3.

Put all of *.v source files and report into same compressed file.

(Use Lab5_student ID to be the name of your compressed file)

7. Q&A

If you have any question, just send email to TAs.