# NCTU-CS Digital System Lab.

# LAB 02 - CONVCOR

**Design: Convolution and correlated sum** 

# **Data Preparation**

Extract LAB data from TA's directory.
 % tar xvf ~2016dlabta05/Lab02.tar

## **Design Description and Examples**

Correlation and Convolution are basic operations that we will perform to extract information from images. In this practice, we need to compute convolution and correlation sum for A and B, which has three entries, respectively. Two calculation operates as following:

Input:

for convolution operation

$$In_a \circ In_b = \sum_{k=-\infty}^{\infty} a_k * b_{n-k}$$

 $\underline{Output}: \quad a_0b_0 \qquad \qquad a_0b_{1} + a_1b_0 \qquad a_0b_{2} + a_1b_{1} + a_2b_0 \qquad a_1b_{2} + a_2b_1 \qquad \quad a_2b_2$ 

for correlation sum

 $a_0 a_1 a_2$   $\times \times \times$   $\overline{b_0} \overline{b_1} \overline{b_2}$   $a_0 \overline{b_0} + a_1 \overline{b_1} + a_2 \overline{b_2}$ 

Output:

These two different calculation modes are selected by the signal, MODE. MODE0 is the convolution of A and B. MODE1 is the correlation sum of two matrices.

Your goal is to compute matrices by above rules and output the correct answer.

Signal	Description
MODE	MODE=0: convolution of A and B
	MODE=1: correlation sum of A and B

#### **Inputs**

- Three input data for in\_a[15:0] and in\_b[15:0] each will be sequentially input in 3 continuous cycles while in\_ valid is high.
- 2. You will receive 3 inputs of 16-bits **signed complex numbers** for **in\_a[15:0]** and **in\_b[15:0]**, respectively. The former 8 bits are the real part of each number. Last 8 bits are the image part otherwise. Two parts of this complex number all are **twos-complement representation**.

Ex: Bits format of  $in_a0=a_1a_2a_3a_4a_5a_6a_7a_8+(a_9a_{10}a_{11}a_{12}a_{13}a_{14}a_{15}a_{16})i$ 

- 3. **in\_mode** define which calculation should be done at *first* cycle.
- 4. All inputs will be changed at clock *negative* edge.

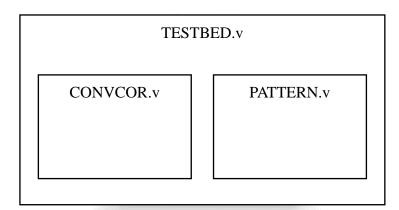
#### **Outputs**

- Your answer should be output at out[35:0] for only 5 cycle when MODE = 0;
  Whereas, output at out[35:0] for only 1 cycle when MODE = 1.
- 2. **out[35:0]** is signed complex number, also. The former 18 bits are the real part, and last 18 bits are the image part otherwise.
- 3. **out\_valid** should be low and **out** should be set to zero after initial reset.
- 4. **out\_valid** is set to be high when output value is valid.
- 5. All outputs are synchronized at clock *positive* edge.
- 6. Test pattern will check whether your answer is correct or not at clock **negative edge** when **out\_valid** is high.

#### **Specifications**

- 1. Top module name : **CONVCOR** (File name : **CONVCOR.v**)
- 2. Input pins: clk, rst\_n, in\_valid, in\_a[15:0], in\_b[15:0], in\_mode.
- 3. Output pins: out\_valid, out[35:0].
- 4. **out\_valid** should not be raised when **in\_valid** is high (in\_a and in\_b is transferring).
- 5. It is **active-low synchronous** reset.
- 6. The latency of your design in each pattern should not be larger than 100 cycles.

### **Block Diagram**



#### Note

- 1. Simulation step:
  - Put your design in 01\_RTL
  - Simulation to check design : ./01\_run.f
  - Show waveto debug: nWave&
  - Clear up : ./09\_clean\_up
- 2. Please add your student ID to the file name of .v file before upload file on e3 platform:

CONVCOR\_0556123.v

3. Sample waveform:

