NCTU-CS Digital System Lab.

Online Test 01

Data Preparation

1. Extract LAB data from TA's directory.
   % tar xvf ~2016dlabtestta05/Online_Test1.tar

Design Description and Examples

Design two mode:

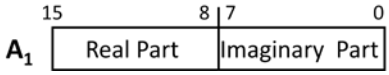
Input：

In: A_0 A_1 B_0 B_1

Mode 0：

Four inputs A_0, A_1, B_0, B_1 which get from **in** port by 4 cycles are 16-bits **signed complex numbers**. For each input, the former 8 bits are the real part of each number and last 8 bits are the image part otherwise. Two parts of this complex number, real part and image part, all are **twos-complement representation**. First two inputs belong to A series, and the last two inputs belong to B series, otherwise.

Ex:



You should complex conjugate A series first, and convolute with B series then.

$$\bar{A} \circ B = \sum_{k=-\infty}^{\infty} \bar{A}_k * B_{n-k}$$

$0\ \bar{A}_0\ \bar{A}_1$ $\quad$ $\bar{A}_0\ \bar{A}_1$ $\quad$ $\bar{A}_0\ \bar{A}_1$
$\times\ \times\ \times$ $\quad$ $\times\ \times$ $\quad$ $\times$
$B_1\ B_0\ 0$ $\quad$ $B_1\ B_0$ $\quad$ $B_1\ B_0$

Output： $\bar{A}_0\ B_0$ $\quad$ $\bar{A}_0\ B_1 + \bar{A}_1\ B_0$ $\quad$ $\bar{A}_1\ B_1$

Mode1:

You should cut each input **a set of 4 bits.** Each set is representing the range of 4bits numbers: 0~15. Find the maximum and minimum set and output sequentially **max, min value** and **max minus(-) min** in 3 continuous cycles:

A_0 : 1111_0100_1101_1101 A_1 : 1011_1101_0101_0011

B_0 : 1000_0010_1000_0100 B_1 : 0001_1010_0110_1001

A_0 : 1111 0100 1101 1101 A_1 : 1011 1101 0101 0011

B_0 : 1000 0010 1000 0100 B_1 : 0001 1010 0110 1001

Output： Max: **15**(1111) Min: **1**(0001) Max – Min: **14**

You should output sequentially in 3 continuous cycles：15 1 14

Your goal is to compute these operations by above rules and output the correct answer.

Inputs

1. Four input data for **in[15:0]** each will be sequentially input in **4 continuous** cycles while **in_ valid** is high.
2. **in_mode** valid at the ***first*** input cycle.
3. All inputs will be changed at clock ***negative*** edge.

Input Signals	**Bit Width**	**Description**
clk	1	clock
rst_n	1	synchronous active-high reset
in	16	4 of 16 bit inputs
in_valid	1	high when **in** is valid
in_mode	1	select the operations should be compute by two MODE discuss above

Outputs

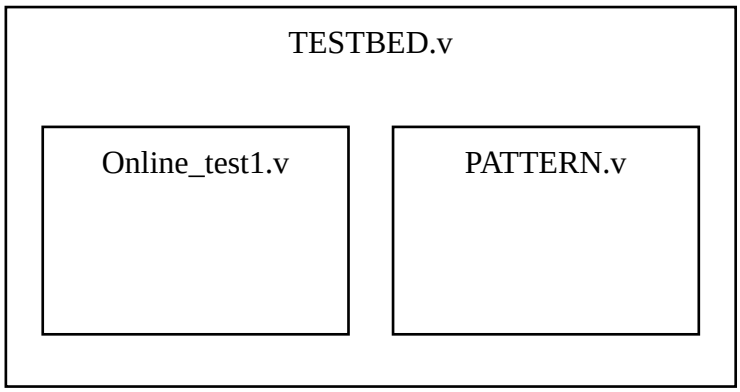
1. Your answer should be output at **out[35:0]** for **only 3 cycle** when **MODE = 0**; Whereas, output at **out[35:0]** for **only 3 cycle** when **MODE = 1**.
2. For **mode 0**, **out[35:0]** is signed complex number, also. The former 18 bits are the real part, and last 18 bits are the image part otherwise.
3. For **mode 1**, **out[35:0]** is unsigned integer.
4. **out_valid** should be low and **out** should be set to zero after initial reset.
5. **out_valid** should be set to high when output value is valid.
6. All outputs are synchronized at clock ***positive*** edge.
7. Test pattern will check whether your answer is correct or not at clock **negative edge** when **out_valid** is high.

Output Signals	Bit Width	Description
out	36	output result
out_valid	1	high when **out** is valid

Specifications

1. Top module name : **Online_test1** (File name : **Online_test1.v**)
2. Input pins: **clk , rst_n , in_valid , in[15:0], in_mode**.
3. Output pins: **out_valid , out[35:0]**.
4. **out_valid** should not be raised when **in_valid** is high (when **in** data is transferring).
5. It is **active-high synchronous** reset.
6. The latency of your design in each pattern should not be larger than 1000 cycles.

Block Diagram



Note

1. Simulation step:
   - Put your design in 01_RTL
   - Simulation to check design : ./01_run.f
   - Show wave to debug: nWave &
   - Go to folder 02_SYN/ and check synthesis：./01_run_dc
   - Clear up : ./09_clean_up
2. Please add your student ID and name to the file name of .v file before upload file on e3 platform:
   Online_test1_0556123_陳小明.v
3. Sample waveform: