NCTU-CS Digital System Lab.

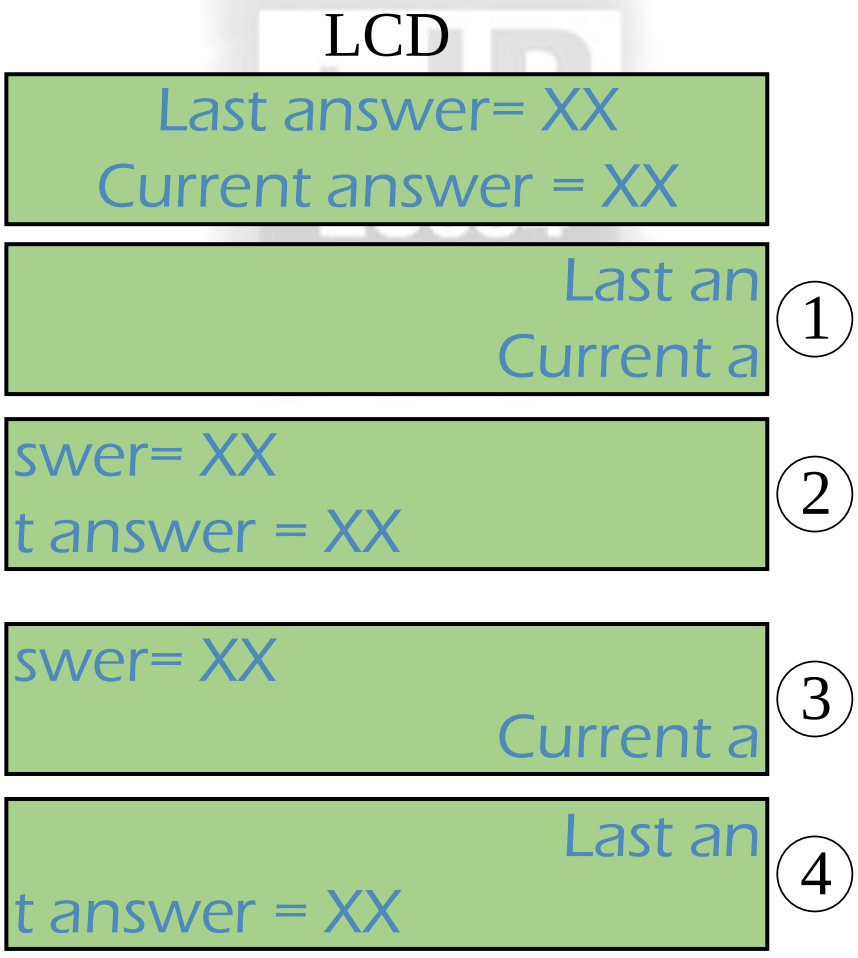
LAB 08 – FPGA_LCD

Data Preparation

Prepare following files by yourselves:
LCD.v
LCD.ucf

Design Description

According to the LAB07 (LED, BUTTON, SWITCH, IP)_Calculator, show the result of each calculations. And you should do as the same as follow:



1. From right to left ***or***
2. From left to right

Bonus

3. Up: From left to right
   Down: From right to left
4. UP: From right to left
   Down: From left to right

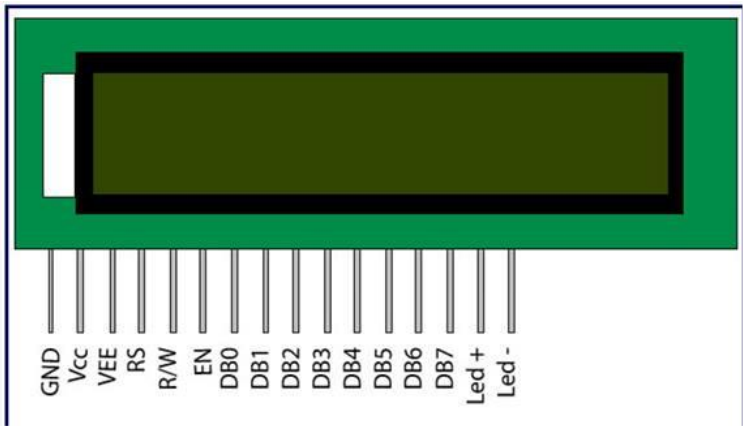
Input:

Name	Location	Function
BTN_SOUTH	K17	Reset
BTN_WEST	D18	Square root
BTN_NORTH	V4	Multiplication
BTN_EAST	H13	Addition
SW0	L13	2^0
SW1	L14	2^1
SW2	H18	2^2
SW3	N17	2^3

Output:

Name	Location	Function
LED0	F12	Specify as the answer[7:0] Ex. LED0 => answer[0]
LED1	E12	
LED2	E11	
LED3	F11	
LED4	C11	
LED5	D11	
LED6	E9	
LED7	F9	
LCD_E	**M18**	**R/W Enable pulse** **0: disabled** **1: R/W op enabled**
LCD_RS	**L18**	**Register Select** **0: instruction register during write operations. Busy Flash during read op.** **1: data for R/W op.**
LCD_RW	**L17**	**R/W Control** **0: Write, LCD accepts data** **1: Read, LCD presents data**
SF_D11	**M15**	**Data bit DB7**

SF_D10	**P17**	**Data bit DB6**	**Shared with StrataFlash pins SF_D<11:8>**
SF_D9	**R16**	**Data bit DB5**	
SF_D8	**R15**	**Data bit DB4**	



Specifications

1. Top module name : LCD.v (File name : LCD.v)
2. All outputs are synchronized at clock positive edge.
3. It is **asynchronous**, **active-high** reset architecture.
4. Square root should use IP.
5. Reset means calculate restart.
6. All numbers are unsigned and integer.

Grading Policy

Function Validity: 80%

Questions: 20%

Bonus: 10%

Note

1. Name to the file name of .v file and .rar file before upload file on e3 platform:
   LCD_0556123_陳小明.v

   LCD_0556123_陳小明.rar