# NCTU-CS Digital System Lab.

# LAB 03 – Image Processor

## Design: IMPOR

### Data Preparation

Extract LAB data for TA's directory.
% tar xvf ~2016dlabta06/Lab03.tar

### Design Description

You are design an image processor. There will be 9 cycles of pixel value for input sequence after image processor raise the ready signal. After receive input, image processor should raise the ready signal. And the mode signal will indicate that operation should image processor do on input. **Image processor should output the pixel values of image after several operations when mode is 0**. And image processor will raise the ready to receive next input.

### Example

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

Assume this is 9 pixel input at first.

**Mode 1**

| | | |
|---|---|---|
| 3 | 2 | 1 |
| 6 | 5 | 4 |
| 9 | 8 | 7 |

**Mode 2**

| | | |
|---|---|---|
| 7 | 8 | 9 |
| 4 | 5 | 6 |
| 1 | 2 | 3 |

**Mode 3(left rotate)**

| | | |
|---|---|---|
| 3 | 6 | 9 |
| 2 | 5 | 8 |
| 1 | 4 | 7 |

**Mode 4(right rotate)**

| | | |
|---|---|---|
| 7 | 4 | 1 |
| 8 | 5 | 2 |
| 9 | 6 | 3 |

**mode 5 : the first column plus 1**

| | | |
|---|---|---|
| 2 | 2 | 3 |
| 5 | 5 | 6 |
| 8 | 8 | 9 |

**mode 6 : the second column plus 1**

**mode 7 : the third column plus 1**

## Inputs

1. All signal are unsigned integer.
2. Input information :.

| Input port | Bit number | Value |
|---|---|---|
| **in** | 3 bits | 0 ~ 7 |
| **mode** | 3 bits | 0 ~ 7 |
| **in_valid** | 1 bit | 0 ~ 1 |
| **clk** | 1 bit | 0 ~ 1 |
| **rst_n** | 1 bit | 0 ~ 1 |

## Outputs

1. You should set ready signal low when your design is processing image.
2. Output information :.

| Output port | Bit number | Value |
|---|---|---|
| **out** | 3 bit | 0 ~ 7 |
| **out_valid** | 1 bit | 0 ~ 1 |
| **ready** | 1 bit | 0 ~ 1 |

## Specifications

1. Top module name : IMPOR (File name : IMPOR.v)
2. The clock period is 4 ns.
3. It is an asynchronous reset and active-low architecture. Signal out and out_valid should be zero after reset.
4. Signal out and out_valid should be zero when in_valid is high.
5. All inputs will be given at negative edge of clk, and all output is synchronized at positive edge of clk.
6. The latency is determined by the period time between every input and input to output, and it should not be more than 12.
7. The synthesis result of data type cannot include any latch.
8. Slack should be non-negative.
9. The gate level simulation cannot include any timing violation.
10. if the pixel is 7.plus 1 still 7 in this lab.
11. When ready is high.our input will give at next negedge.

## Note

1. Grading policy:
RTL and Gate-level simulation correctness: 70%
Performance: 30%
- Latency 10%
- Area 20%
2. Template folders and reference commands:
01_RTL/ (RTL simulation) ./01_run
02_SYN/ (Synthesis) ./01_run_dc
(Check the design if there's latch or not in syn.log)
(Check the design's timing in /Report/IMPOR.timing)
03_GATE / (Gate-level simulation) **./01_run**

**Block Diagram**