NCTU-CS Digital System Lab.

LAB 01 – ALU(9/23)

Design: ALU

Data Preparation

Extract LAB data for TA's directory.
140.113.208.231 port22

% tar xvf ~2016dlabta02/lab01.tar

Design Description

You have to design a with following four modes :

(A) MODE == 0 :
OUT = A + B

(B) MODE == 1 :
OUT = A &B

(D) MODE == 2 :
if(A > B) OUT = 1
else OUT = 0

(E) MODE == 3:
OUT = A>>B

You need to use **continuous assignment** and **procedural assignment** to design this ALU:

Continuous assignment
e.g. assign c = a * b ;

Procedural assignment
e.g. always@(*) begin
…
end

Inputs

1. The signal A, B are signed 4-bit numbers.
2. The signal MODE is unsigned 2-bit number.

Outputs

The signal OUT is signed 8-bit number.

Specifications

1. The module name : ALU (File name : ALU.v)
2. Input pins : A[3:0], B[3:0], MODE[1:0]
3. Output pins : OUT[7:0]
4. You need to upload your design **continuous version** and **procedural** version respectively.

Note

1. Put your design in 01_RTL
2. Simulation to check design : ./01_run.f
3. Show wave to debug : nWave &
4.Clear up : ./09_clean_up

Block Diagram