NCTU-CS Digital System Lab.

Online Test (12/18)

Design: **TIMER**

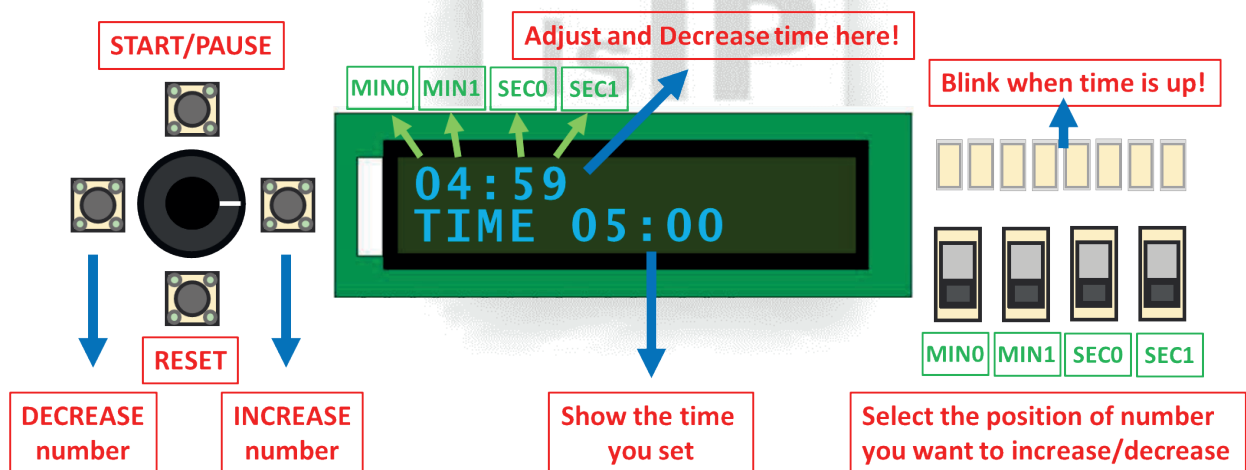### Data Preparation

Prepare following files by yourselves:

TIMER.v

TIMER.ucf

Design Description and Examples

You should design a countdown timer on the FPGA

There are 4 buttons, 4 switches, LCD and 8 LEDs will be used.

Input:

Name	Location	Function
BTN_SOUTH	K17	Reset
BTN_WEST	D18	Decrease the number of position you select
BTN_NORTH	V4	Start/Pause timer
BTN_EAST	H13	Increase the number of position you select
SW0	L13	Position SEC1
SW1	L14	Position SEC0
SW2	H18	Position MIN1
SW3	N17	Position MIN0

Output:

Name	Location	Function	
LED0	F12	Blink together when time is up	
LED1	E12		
LED2	E11		
LED3	F11		
LED4	C11		
LED5	D11		
LED6	E9		
LED7	F9		
LCD_E	M18	R/W Enable pulse 0: disabled 1: R/W op enabled	
LCD_RS	L18	Register Select 0: instruction register during write operations. Busy Flash during read op. 1: data for R/W op.	
LCD_RW	L17	R/W Control 0: Write, LCD accepts data 1: Read, LCD presents data	
SF_D11	M15	Data bit DB7	Shared with StrataFlash pins SF_D<11:8>
SF_D10	P17	Data bit DB6	
SF_D9	R16	Data bit DB5	
SF_D8	R15	Data bit DB4	

For example:

Step 1:

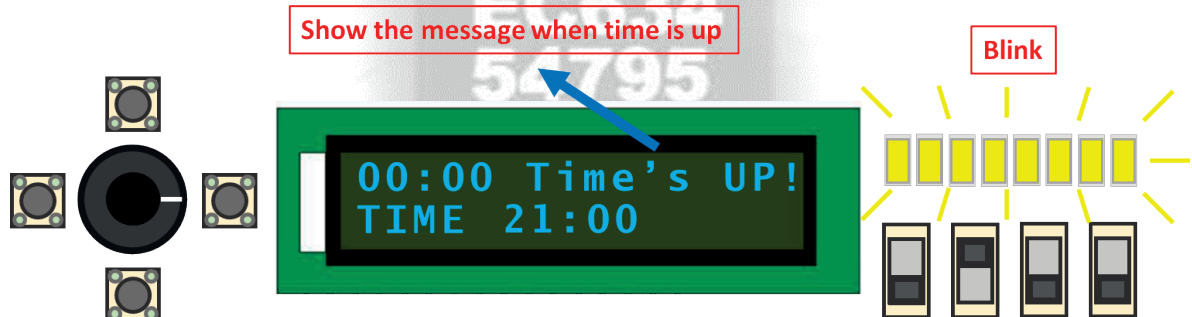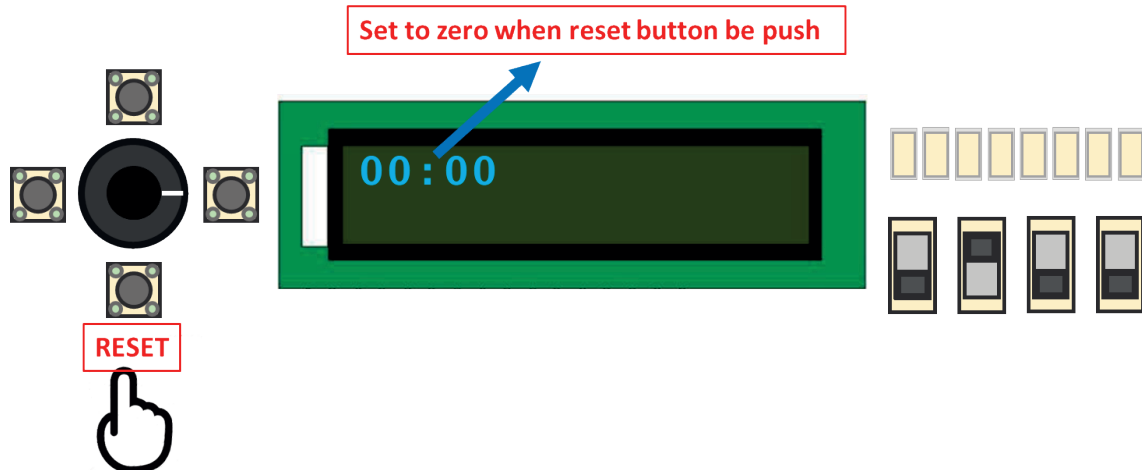Turn on MIN1 switch(SW2), and press increase button(BTN_EAST).

Adjust time

MIN1

21:00

MIN1
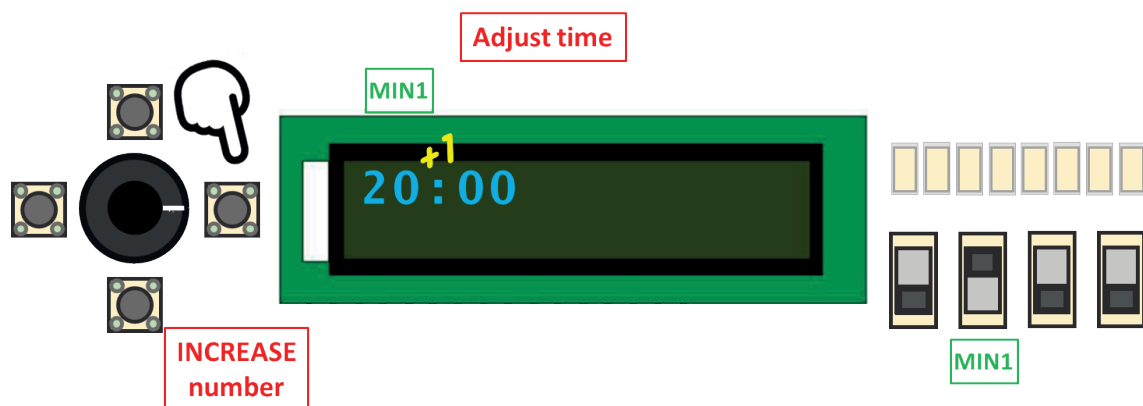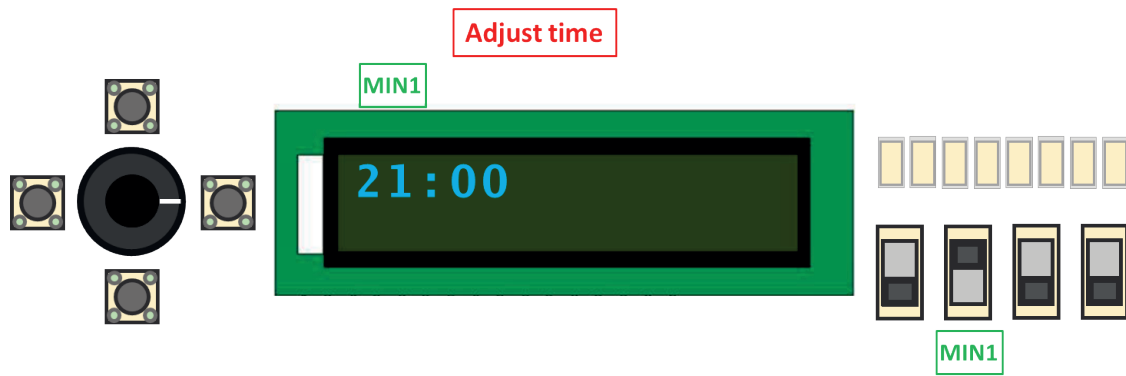
Step2: Press start/pause (north) button to start the timer.

START/PAUSE

Start to decrease time

20:59
TIME 21:00

Show up the time you set

When time is up.

Show the message when time is up

Blink

00:00 Time's UP!
TIME 21:00
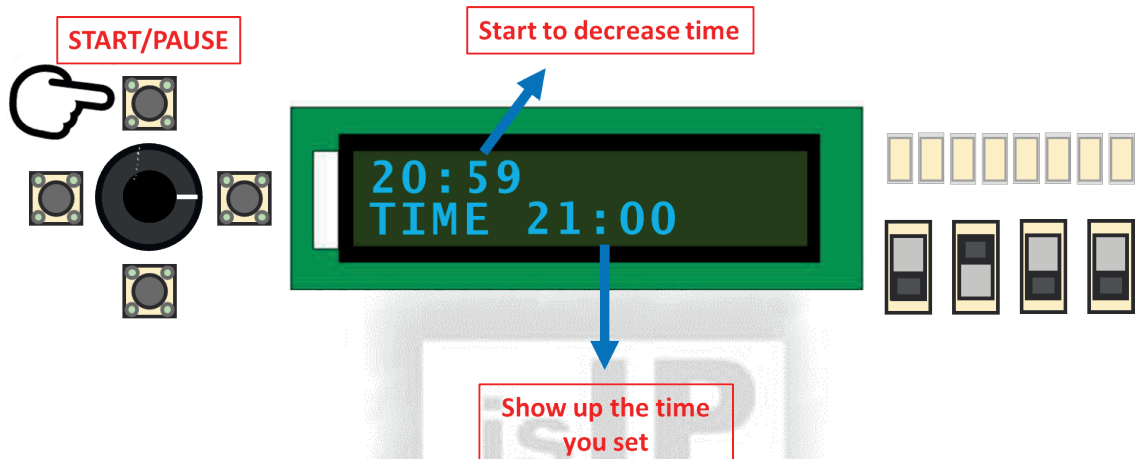
Step3: Press reset button to restart.

Set to zero when reset button be push

00:00

RESET

Specifications

1. All outputs are synchronized at clock positive edge.

2. It is asynchronous, active-high reset architecture.

3. Reset means TIMER restart (All number should be set to ZERO).

4. The decrease rate is the same as actual timer.

5. The left two digits are minutes part, and right two digits are seconds part.

6. The max number of two parts is 59

Grading Policy

Function Validity: 80%

Questions: 20%

Note

Name to the file name of .v file and .rar file before upload file on e3 platform:

LCD_0556123_陳小明.v

LCD_0556123_陳小明.rar