## 74LVC138A

# 3-to-8 line decoder/demultiplexer; inverting

Rev. 5 — 19 October 2011

Product data sheet

## 1. General description

The 74LVC138A is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address <u>inputs (A0, A1 and A2)</u> and, when enabled, provides eight mutually exclusive outputs ( $\overline{Y0}$  to  $\overline{Y7}$ ) that are LOW when selected.

There are three enable inputs: two active LOW ( $\overline{E}1$  and  $\overline{E}2$ ) and one active HIGH (E3). Every output will be HIGH unless  $\overline{E}1$  and  $\overline{E}2$  are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LVC138A devices and one inverter. The 74LVC138A can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

### 2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ♦ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



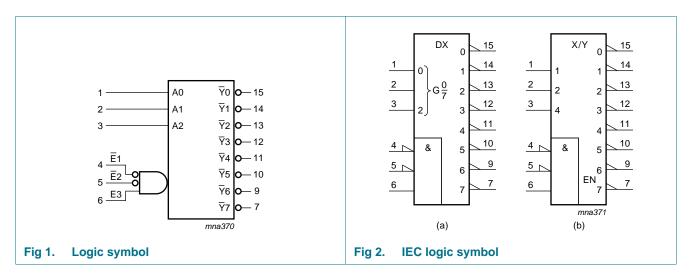
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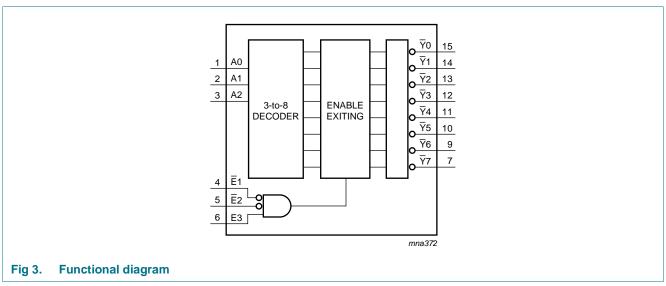
## **Ordering information**

**Ordering information** Table 1.

Type number	Package			
	Temperature range	Name	Description	Version
74LVC138AD	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC138ADB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC138APW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC138ABQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 $\times$ 3.5 $\times$ 0.85 mm	SOT763-1

## **Functional diagram**





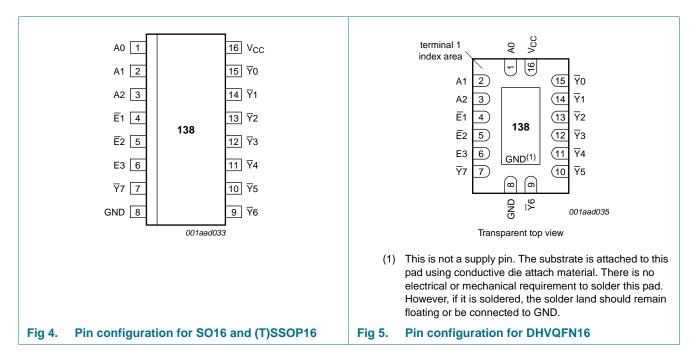
74LVC138A

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### 3-to-8 line decoder/demultiplexer; inverting

## 5. Pinning information

### 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
E1	4	enable input (active LOW)
E2	5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
<del>Y</del> [0:7]	15, 14, 13, 12, 11, 10, 9, 7	output
$V_{CC}$	16	supply voltage

3-to-8 line decoder/demultiplexer; inverting

## 6. Functional description

Table 3. Function table [1]

Input						Outp	ut						
E1	E2	E3	A0	A1	A2	<u>Y</u> 0	<u>Y</u> 1	<u>Y</u> 2	<u>Y</u> 3	<u>Y</u> 4	<u>Y</u> 5	<u>Y</u> 6	<del>Y</del> 7
Н	Χ	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
Χ	Н	Х	Х	Х	X	Н	Н	Н	Н	Н	Н	Н	Н
Χ	Χ	L	Х	Х	X	Н	Н	Н	Н	Н	Н	Н	Н
	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
			Н	L	L	Н	L	Н	Н	Н	Н	Н	Н
			L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
			Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
			L	L	Н	Н	Н	Н	Н	L	Н	Н	Н
			Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
			L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
			Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
VI	input voltage		[ <u>1]</u> –0.5	+6.5	V
I <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
Vo	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
I <sub>O</sub>	output current	$V_O = 0 V to V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb}$ = -40 °C to +125 °C	[3] _	500	mW

<sup>[1]</sup> The minimum input voltage ratings may be exceeded if the input current ratings are observed.

<sup>[2]</sup> The output voltage ratings may be exceeded if the output current ratings are observed.

<sup>[3]</sup> For SO16 packages: above 70 °C the value of P<sub>D</sub> derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P<sub>D</sub> derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P<sub>D</sub> derates linearly with 4.5 mW/K.

3-to-8 line decoder/demultiplexer; inverting

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
	rate	V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	85 °C	-40 °C to	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	٧
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_{O} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	$V_{CC} = 3.6 \text{ V}; V_{I} = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ

## 3-to-8 line decoder/demultiplexer; inverting

 Table 6.
 Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	85 °C	-40 °C to	+125 °C	Unit	
			Min	Typ[1]	Max	Min	Max		
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	10	-	40	μΑ	
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	-	5000	μΑ	
Cı	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF	

<sup>[1]</sup> All typical values are measured at  $V_{CC}$  = 3.3 V (unless stated otherwise) and  $T_{amb}$  = 25 °C.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C to	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	An to Yn; see Figure 6	[2]		1		1		
		$V_{CC} = 1.2 \text{ V}$		-	14	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.5	5.2	11.5	0.5	12.7	ns
			1.5	3.0	6.5	1.5	7.3	ns	
		$V_{CC} = 2.7 \text{ V}$		1.5	3.2	6.8	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.7	5.8	1.0	7.5	ns
		E3 to $\overline{Y}$ n; see Figure 6	[2]						
		V <sub>CC</sub> = 1.2 V		-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.0	5.5	11.4	1.0	12.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.5	3.2	6.5	1.5	7.1	ns
		$V_{CC} = 2.7 \text{ V}$		1.5	3.3	6.8	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.9	5.8	1.0	7.5	ns
		En to Yn; see Figure 7	[2]						
		V <sub>CC</sub> = 1.2 V		-	15	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.0	5.6	11.5	1.0	12.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.8	3.3	6.5	1.8	7.3	ns
		$V_{CC} = 2.7 \text{ V}$		1.5	3.4	6.4	1.5	8.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.9	5.8	1.0	7.5	ns
t <sub>sk(o)</sub>	output skew time		[3]	-	-	1.0	-	1.5	ns

### 3-to-8 line decoder/demultiplexer; inverting

**Dynamic characteristics** ...continued Table 7.

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions		<b>-40</b>	°C to +8	5 °C	-40 °C to	Unit	
				Min	Typ[1]	Max	Min	Max	
$C_PD$	power dissipation	$V_I = GND$ to $V_{CC}$	[4]						•
capacitance		V <sub>CC</sub> = 1.65 V to 1.95 V		-	9.9	-			pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	15.8	-			pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	21.1	-			pF

- [1] Typical values are measured at  $T_{amb} = 25$  °C and  $V_{CC} = 1.2$  V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

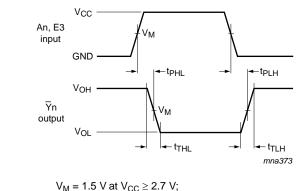
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 

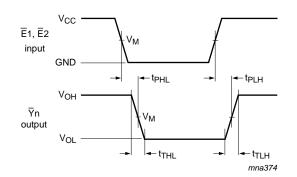
## 11. Waveforms



 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 V$ ;

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

The inputs An, E3 to outputs Yn propagation Fig 6. delavs



 $V_M = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V};$ 

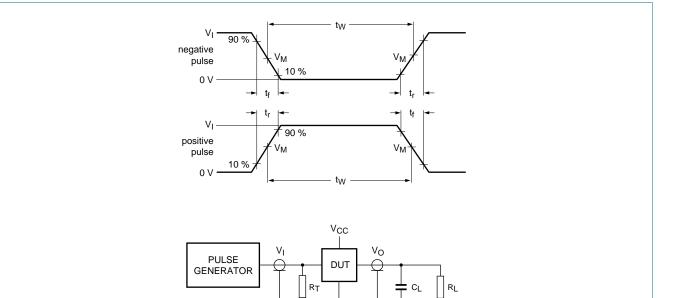
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 V$ ;

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

The inputs En to outputs Yn propagation Fig 7. delavs

## 3-to-8 line decoder/demultiplexer; inverting

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Test data is given in Table 8. Definitions for test circuit:

R<sub>L</sub> = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 8. Test circuit for measuring switching times

Table 8. Test data

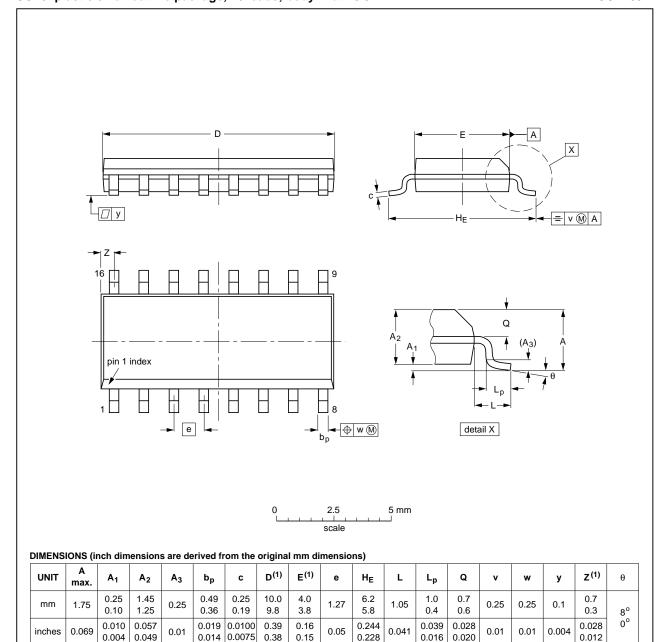
Supply voltage	Input		Load				
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>			
1.2 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ			
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ			
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2 ns	30 pF	500 Ω			
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			

### 3-to-8 line decoder/demultiplexer; inverting

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			<del>99-12-27</del> 03-02-19

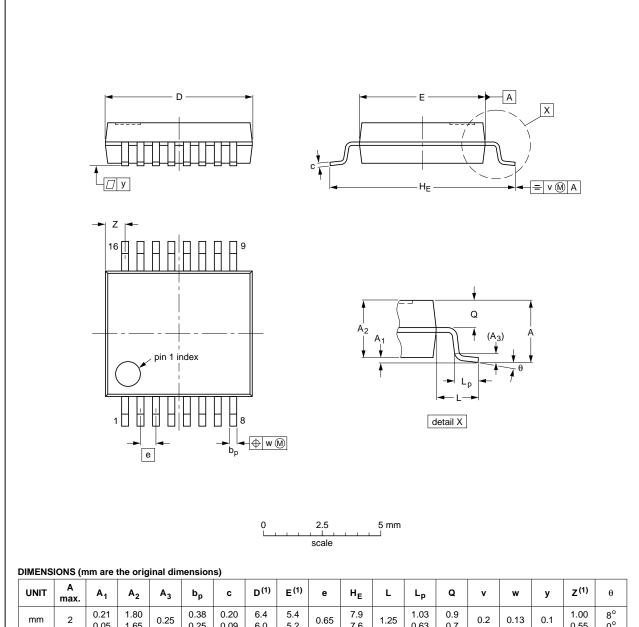
Fig 9. Package outline SOT109-1 (SO16)

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3-to-8 line decoder/demultiplexer; inverting

## SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	U	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT338-1		MO-150				<del>99-12-27</del> 03-02-19	

Fig 10. Package outline SOT338-1 (SSOP16)

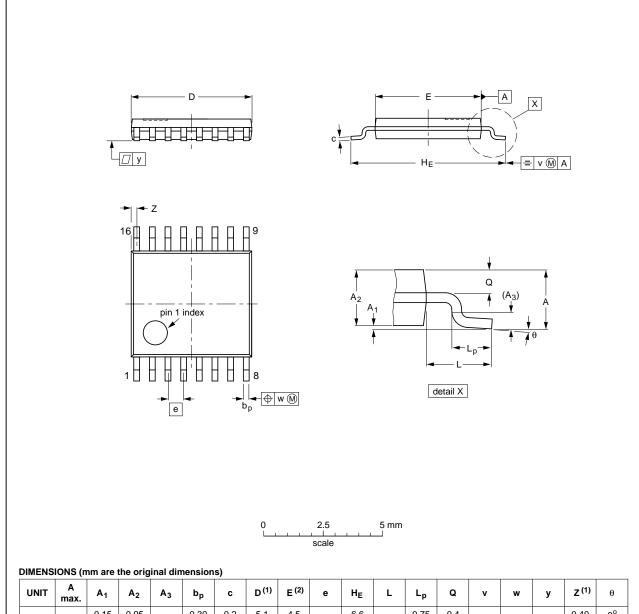
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3-to-8 line decoder/demultiplexer; inverting

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	REFER	EUROPEAN	ISSUE DATE		
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	MO-153				<del>99-12-27</del> 03-02-18
	IEC	IEC JEDEC		IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION

Fig 11. Package outline SOT403-1 (TSSOP16)

74LVC138A

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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

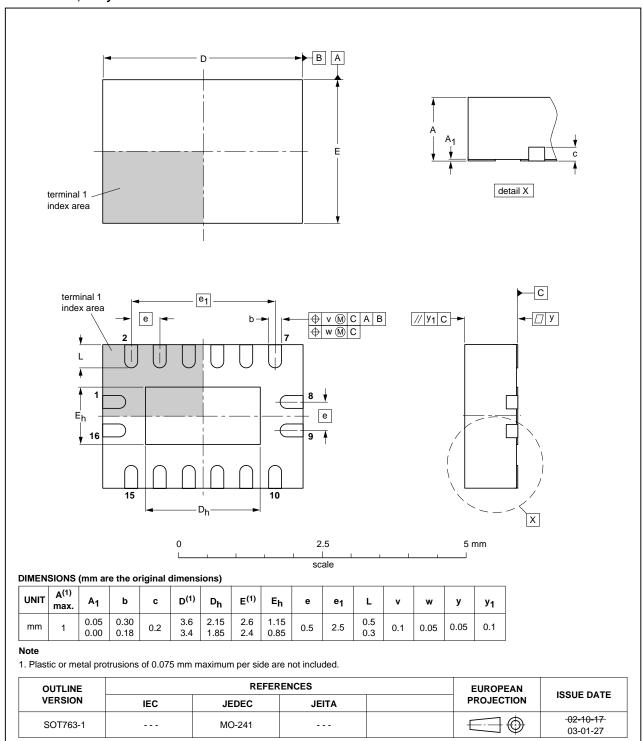


Fig 12. Package outline SOT763-1 (DHVQFN16)

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## 3-to-8 line decoder/demultiplexer; inverting

## 13. Abbreviations

#### Table 9. **Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

## Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC138A v.5	20111019	Product data sheet	-	74LVC138A v.4
Modifications:	<ul> <li>The format of of NXP Semic</li> </ul>	this data sheet has been red onductors.	esigned to comply with	the new identity guidelines
	<ul> <li>Legal texts ha</li> </ul>	ve been adapted to the new	company name where	appropriate.
	• Table 4, Table	5, Table 6, Table 7 and Table	e 8: values added for lo	ower voltage ranges.
74LVC138A v.4	20030506	Product specification	-	74LVC138A v.3
74LVC138A v.3	20020312	Product specification	-	74LVC138A v.2
74LVC138A v.2	19980428	Product specification	-	74LVC138A v.1
74LVC138A v.1	-	-	-	-

#### 3-to-8 line decoder/demultiplexer; inverting

## 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 3-to-8 line decoder/demultiplexer; inverting

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## 3-to-8 line decoder/demultiplexer; inverting

## 17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
7	Limiting values	4
8	Recommended operating conditions	5
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	7
12	Package outline	ç
13	Abbreviations 1	3
14	Revision history 1	3
15	Legal information 1	4
15.1	Data sheet status	4
15.2	Definitions1	4
15.3	Disclaimers	
15.4	Trademarks1	5
16	Contact information 1	5
17	Contonte 1	6

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