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Homework #1

5-1:

A computer uses a memory unit with 256K words of 32 bits each. A binary instruction is stored in one word of memory. The instruction has fours parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code, the register code and the address part?

- The operation code must have 7 bits
- The register code must have 6 bits
- The address must have 18 bits

5-2:

What is the difference between a direct and an indirect address instruction?

- A direct address specifies the location where the operand is stored while an indirect address specifies where the address for the operand can be found.

5-3:

The following control inputs are active in the bus system shown in Fig. 5-4. For each case, specify the register transfer instructions that will be executed during the next clock transition.

a. IR <- M[AR]
b. PC <- TR
c. DR <- AC, M[AR] <- AC
d. AC <- AC + DR

5-4:

The following register transfers are to be executed in the system of Fig. 5-4. For each transfer, specify the binary value that must be applied to the select inputs, the register whose LD control input must be active (if any) and the memory read/write operation (if needed) and the operation in the adder and logic circuit (if any).

AR <- PC

a. Select Inputs: 010, LD of AR, no memory read/write, no operation.

IR <- M[AR]

b. Select inputs: 111, LD of IR, memory read, no operation.

M[AR] <- TR

c. Select inputs: 110, no LD required, memory write, no operation.

AC <- DR, DR <- AC

d. Select inputs: 100, LD of AC and DR, no memory read/write, move DR to AC.

5-5:

Explain why each of the following microoperations cannot be executed during a single clock pulse in the system shown in Fig. 5-5. Specify a sequence of microoperations that will perform the operation.

IR <- M[PC]

a. The address stored in PC will first need to be moved to AR to accomplish this operation. Because the memory and PC cannot both use the bus at the same time, this operation must be split across two clock pulses.

   The following operations could be performed instead:
   AR <- PC
   IR <- M[AR]

AC <- AC + TR

b. The value stored in TR cannot be added to the value in AC unless the value is in register DR. This is because of no direct connection between TR and the Adder/Logic unit.

   The following operations could be performed instead:
   DR <- TR
   AC <- AC + DR

DR <- DR + AC (AC does not change)

c. The resulting value from the addition will change the value in AC, therefore, to perform this operation without changing the value of AC, the value will first have to be temporarily stored.

   The following operations could be performed instead:
   TR <- AC
   AC <- AC + DR, DR <- TR
   DR <- AC, AC <- DR

5-6:

Consider the instruction formats of the basic computer shown in Fig. 5-5 and the list of instructions in Table 5-2. For each of the following 16-bit instructions, give the equivalent four-digit hexadecimal code and explain in your own words what it is that the instruction is going to perform.

0001 0000 0010 0100

a. The above binary string represents the hexadecimal code 1024. This represents the ADD instruction in direct mode. This instruction tells the computer to take the value inside memory location 024 and add it to AC.

1011 0001 0010 0100

b. The above binary string represents the hexadecimal code B124. This represents the STA instruction in indirect mode. This instruction tells the computer to store the contents of AC into the memory location specified by the address found at location 124.

0111 0000 0010 0000

c. The above binary string represents the hexadecimal code 7020. This represents the INC instruction. This instruction tells the computer to increment the value inside of AC.

5-7:

What are the two instructions needed in the basic computer in order to set the E flip-flop to 1?

- CLE – This instruction clears E.
- CME – Complement E, this instruction inverts the now 0 bit to 1.

5-9:

The content of AC in the basic computer is hexadecimal A937, and the initial value of E is 1. Determine the contents of AC, E, PC, AR, and IR in hexadecimal after the execution of the CLA instruction. Repeat 11 more times, starting from each one of the register-reference instructions. The initial value of PC is hexadecimal 021.

	AC	*E*	*PC*	*AR*	*IR*
Initial	A937	1	021	-	-
CLA	0	1	022	800	7800
CLE	A937	0	022	400	7400
CMA	56C8	1	022	200	7200
CME	A937	0	022	100	7100
CIR	D49B	1	022	080	7080
CIL	526F	1	022	040	7040
INC	A938	1	022	020	7020
SPA	A937	1	022	010	7010
SNA	A937	1	023	008	7008
SZA	A937	1	022	004	7004
SZE	A937	1	022	002	7002
HLT	A937	1	022	001	7001

5-10:

An instruction at address 021 in the basic computer has I = 0, an operation code of the AND instruction, and an address part equal to 083_{16}. The memory word contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR. Repeat the problem six more times starting with an operation code of another memory-reference instruction.

	PC	*AR*	*DR*	*AC*	*IR*
Initial	021	-	-	A937	-
AND	022	083	B8F2	A832	0083
ADD	022	083	B8F2	6229	1083
LDA	022	083	B8F2	B8F2	2083
STA	022	083	-	A937	3083
BUN	083	083	-	A937	4083
BSA	084	084	-	A937	5083
ISZ	022	083	B8F3	A937	6083

5-11:

Show the contents in hexadecimal of registers PC, AR, DR, IR, and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each clock pulse.

	PC	*AR*	*DR*	*IR*	*SC*
Initial	7FF	-	-	-	0
T_0	7FF	7FF	-	-	1
T_1	800	7FF	-	EA9F	2
T_2	800	A9F	-	EA9F	3
T_3	800	C35	-	EA9F	4
T_4	800	C35	FFFF	EA9F	5
T_5	800	C35	0000	EA9F	6
T_6	801	C35	0000	EA9F	0

5-12:

The content of PC in the basic computer is $3AF_{16}$. The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

What is the instruction that will be fetched and executed next?

- The next instruction in IR will be 932E. This is an indirect ADD instruction at memory location 32E.

Show the binary operation that will be performed in AC when the instruction is executed.

- When the operand is fetched (at memory location 9AC) 8B9F will be added to the current value of AC which is 7EC3. The following operation will result:

  0111 1110 0110 0011 + 1000 1011 1001 1111 = 0000 1010 0000 0010 (Binary)

  7EC3 + 8B9F = 0A02 (Hexadecimal)