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Engineering – 303

Lab 7

3/15/2017

Introduction/Description

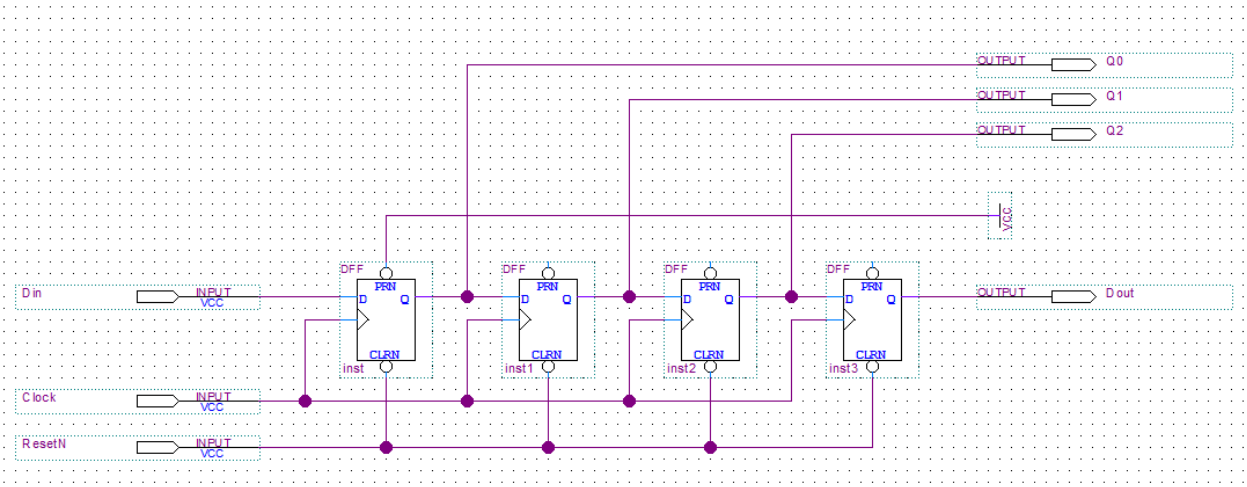
The goal of this lab was to design and implement several circuits that are capable of holding more than a single bit in their memory. By building on the previous lab we were able to take the same idea and expand the design to hold more in its register, thus making it a much more useful circuit. In this lab, we were supposed to build a total of four circuits. The first one was called a 4-bit Shift Register which was capable of holding 4 bits in memory and shifted them through the register as the clock progresses. Next, we built a 4 bit binary counter which counted from zero to fifteen. Then, we were told to make a circuit that would perform the same task of the 4-bit Shift Register with the added addition of parallel load, which takes the value of the inputs and places them in memory. Lastly, we implemented a 16-bit Shift/Parallel register with hex display output.

Design

Part 0 – 4-Bit Shift Register

In the first part of the lab, we implement a design for a 4-bit shift register. Although we successfully designed a shift register in the previous lab we used one already programmed into Quartus to avoid unforeseen errors. In this design, we simply took the included 1-bit positive edge flip-flop and daisy chained four of them together to make a 4-bit register.

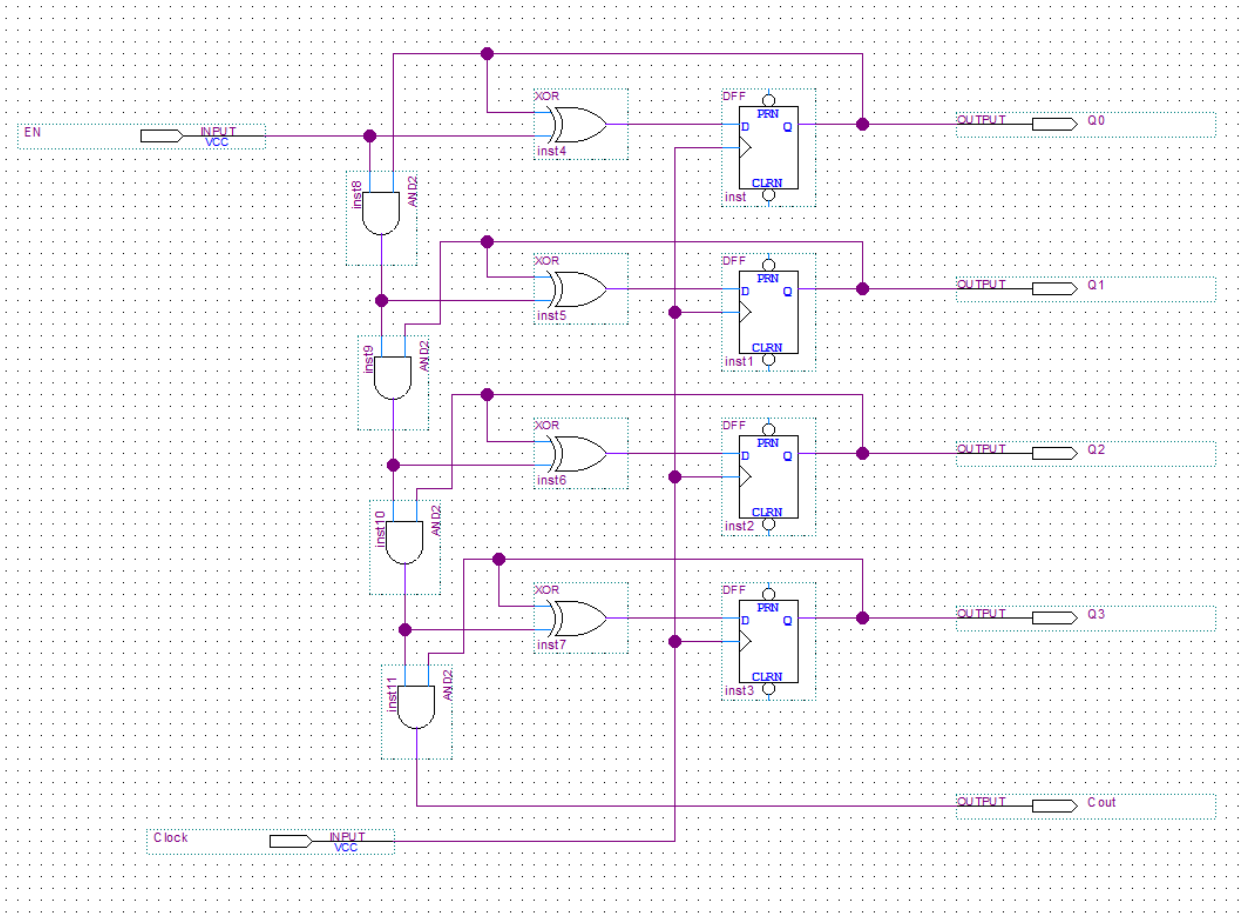
Here is the Block Diagram design for the 4-bit Shift Register.



Part 1 – 4-Bit Synchronous Binary Counter

In this section of the lab, I was instructed to implement a design that was capable of counting from zero to fifteen. At fifteen the circuit outputs a binary 1 and the circuit resets the count back to zero and starts over. This circuit performs this task indefinitely.

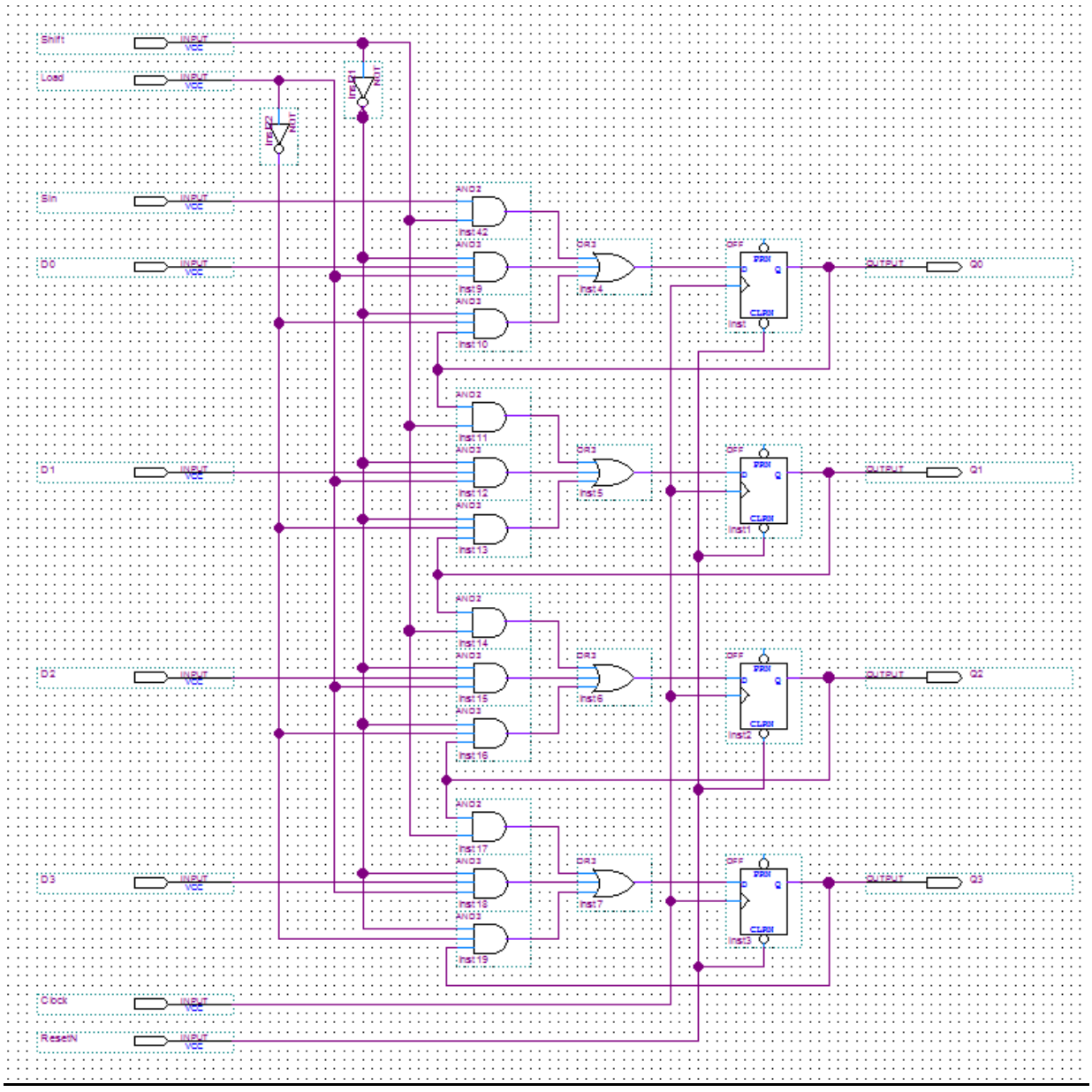
Here is the Block-Diagram Design for the circuit.



Part 2 – 4-Bit Shift Register with Parallel Load

In this part of the lab, we designed a 4-bit shift register with parallel load. This design adds the ability for the circuit to be able to load a maximum of 4 bits into its register. When the circuits Load input is a binary 1 the circuit is in parallel load mode. When the circuits Shift is a binary 1 and Load is a binary 0 then the circuit performs just as the 4-bit shift register would that was created earlier in the lab.

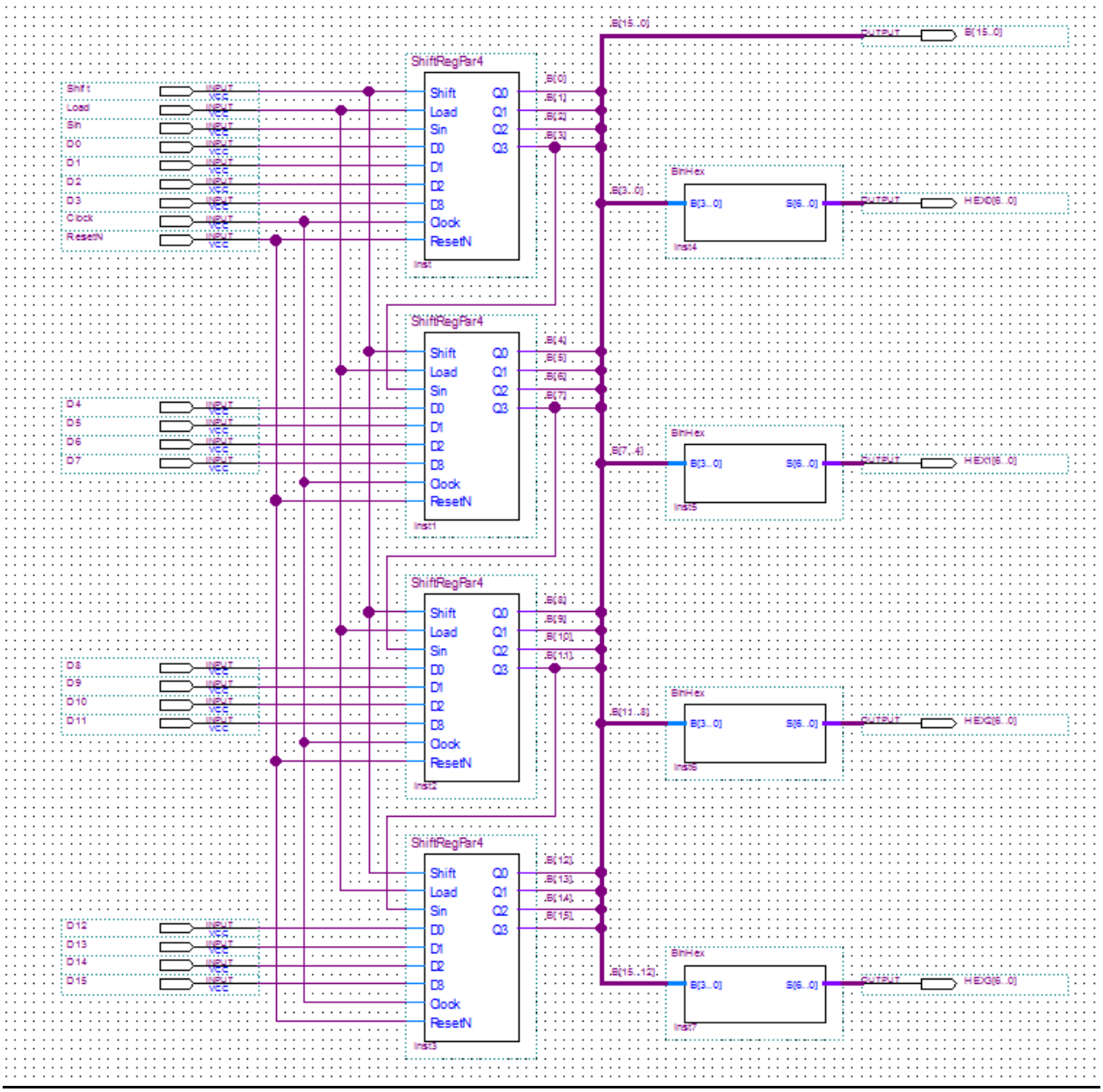
Here is the Block-Diagram design for the 4-Bit Shift Register with Parallel Load.



Part 3 – 16-Bit Shift/Parallel Register with HEX Displays

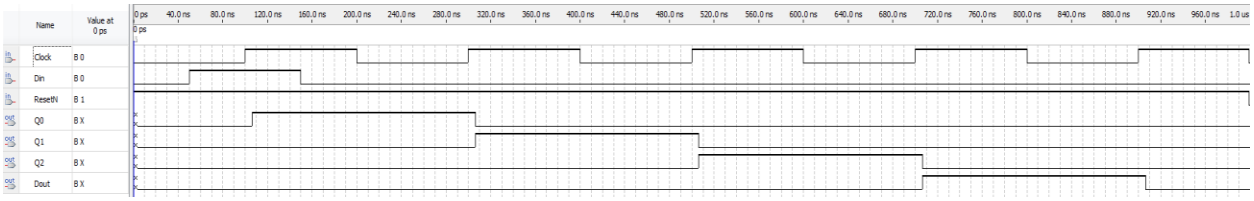
In the last part of the lab, I was told to take my recently designed 4-bit shift/parallel load register and use it to create a 16-bit shift/parallel load register with hex displays. This was done my simply daisy chaining the 4-bit registers to create a 16-bit register and then attaching a hex display module from lab 4.

Here is the Block-Diagram for the 16-Bit Shift/Parallel Register

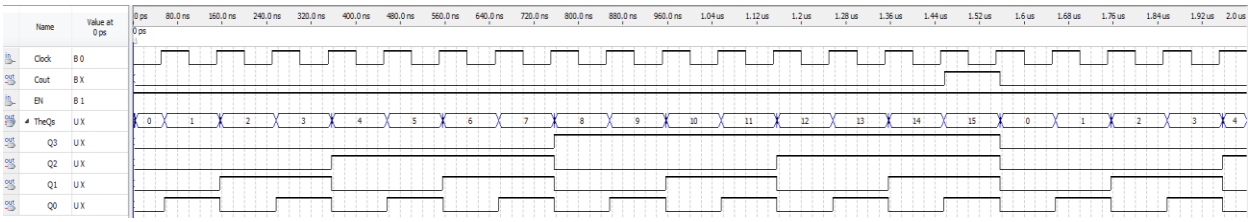


Testing

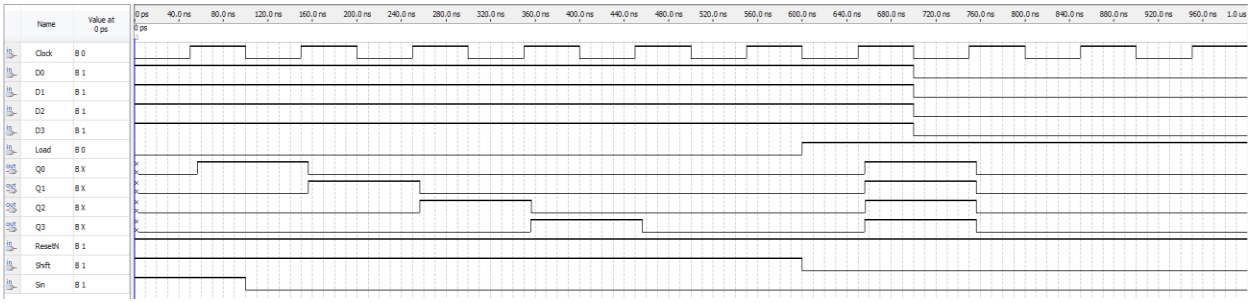
When testing the 4-bit Shift Register that we made in the lab I encountered no problems and it performed as expected for every single input combination.



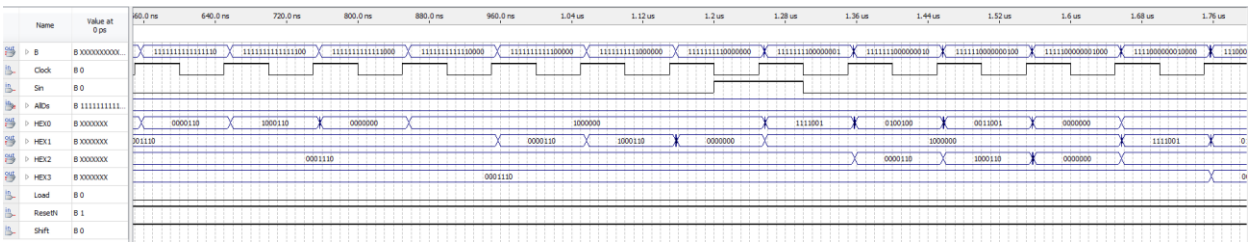
When testing the 4-bit Synchronous Binary Counter I encountered no problems and it performed as expected for every single input combination.



When testing the 4-bit Shift/Parallel Register I encountered no problems and it performed as expected for every single input combination.



When testing the 16-bit Shift/Parallel Register with Hex display I encountered no problems and it performed as expected for every single input combination.



Conclusion

In this lab, I learned how to take the few simple memory circuits that I created in lab 6 and turn them into larger designs that are capable of holding more than a single bit in their memory. I also learned that these circuits are capable of being used several different ways. For example, the shift register grabs one input at a time and gradually moves it down the register till it exits the circuit. The parallel register grabs a set of inputs and stores them for later use. If I was to perform this lab again I would strive to understand the theory behind the circuits a little better. Overall I enjoyed this lab and it was interesting to see how these circuits performed when they were expanded to hold more than one bit.