Quinn Roemer

Engineering – 303

Lab 11

3/28/2017

Introduction/Description

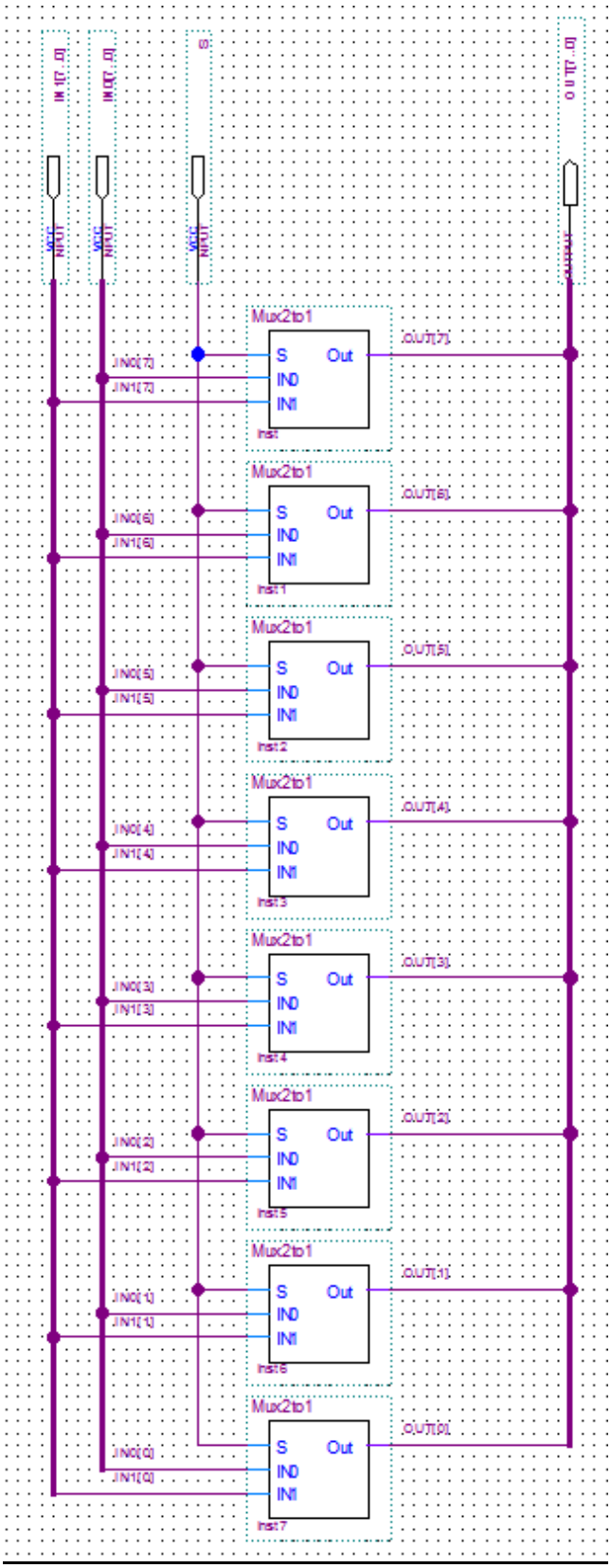
The goal of this lab was to implement several designs that would be used to create the Functional Unit of our Central Processing Unit. This Functional Unit is capable of manipulating a total of 8 bits. And contains an ALU capable of performing simple arithmetic and logic operations and a Shifter which is capable of reorganizing the bits inputted to it. In this lab, I was instructed to create a total of 5 circuits on my journey to an operational functional unit. Also, this lab built upon the previous lab by using several circuits from that lab in its design.

Design

Part 0 – 8 bit 2 to 1 Mux

The first circuit that I implemented was called an 8 bit 2 to 1 Mux. This circuit essentially looked at two 8 bit binary numbers. It then chooses one of those binary numbers based on a selection input. This chosen binary number was then outputted. Please note, for this circuit and all other circuits in this lab no truth tables, kmaps were created.

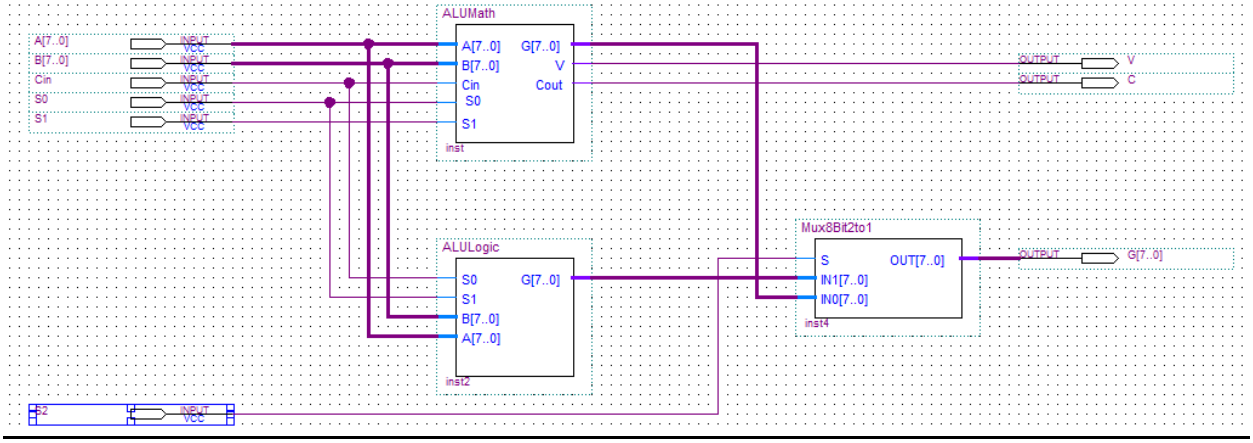
Here is the Block-Diagram design for the 8 bit 2 to 1 Mux.



Part 1 – The ALU Stage.

In this part of the lab, I was instructed to create the ALU of the Function Unit. To do this I would have to combine the Math Unit and the Logic Unit from the previous lab into one circuit.

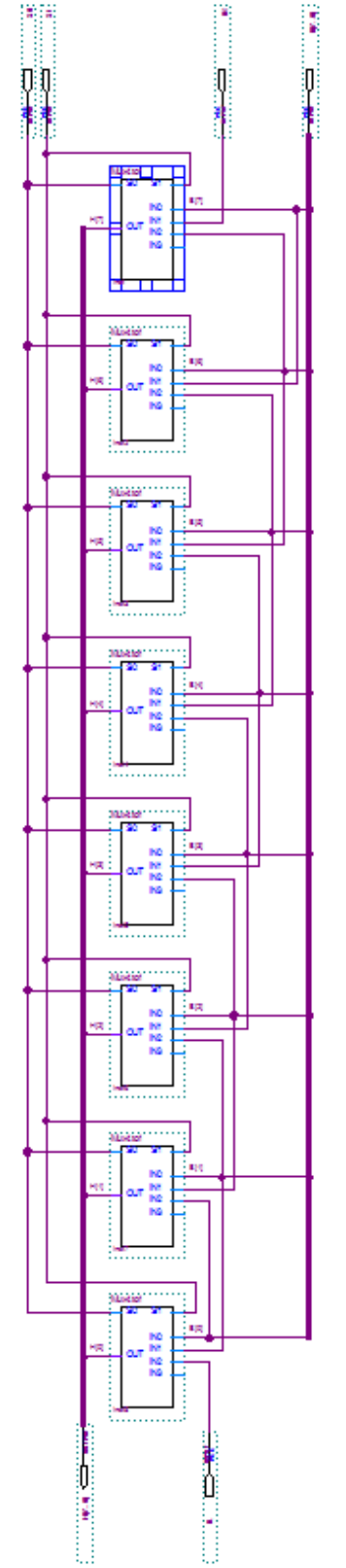
Here is the Block-Diagram for the ALU Stage.



Part 2 – A Shifter.

The next circuit in the lab was a shifter capable of shifting the contents of an 8-bit input. Depending on the selection signal the circuit would either do nothing, shift 1 place, shift 2 places, or shift 3 places.

Here is the Block-Diagram for the Shifter.



Part 3 – A Zero Detect Module.

In part 3 of the lab, I was told to create a circuit that would examine an 8-bit output and send a signal of binary 1 if all bits in the input were zero. Note, this circuit was created using Verilog.

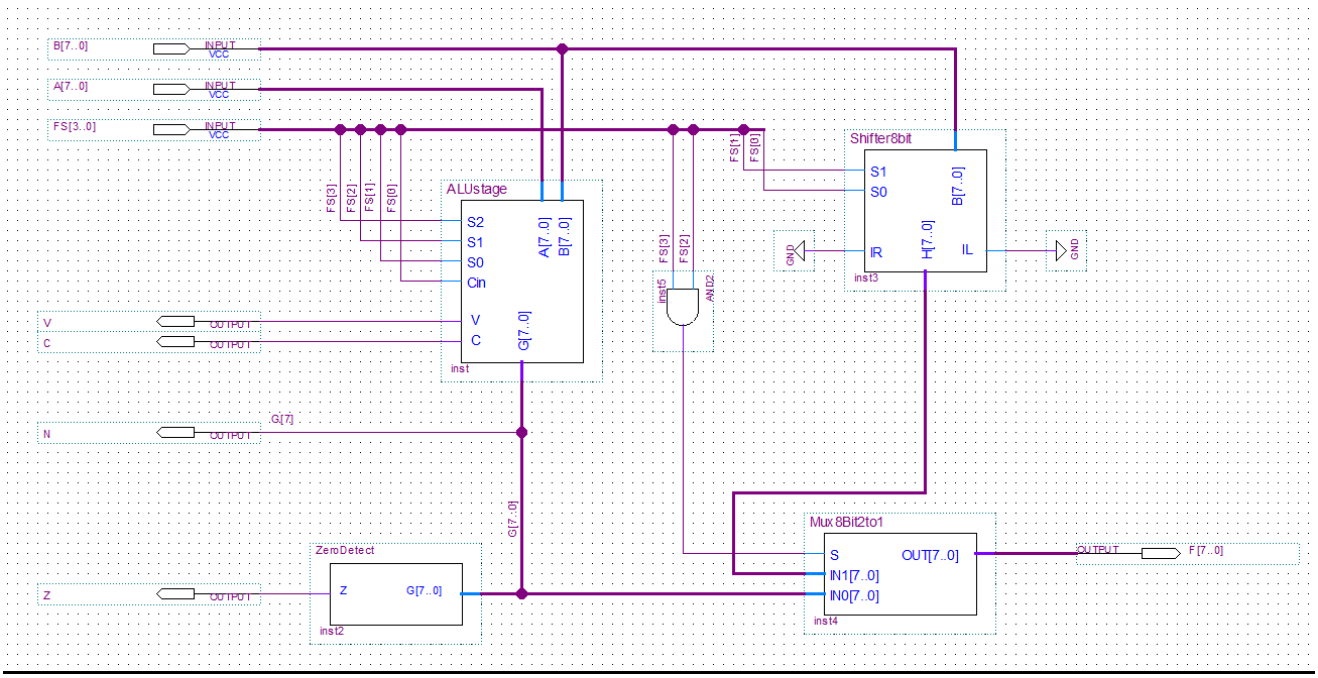
Here is the Verilog Design for the Zero Detect Module.

```
1   //A Verilog module that will detect when all 8 bits of its input is zero.
2
3   module ZeroDetect (G, Z);
4
5   input [7:0] G; //The 8 bit bus.
6   output Z;      //A single bit output.
7
8   assign Z = ~G[7] & ~G[6] & ~G[5] & ~G[4] & ~G[3] & ~G[2] & ~G[1] & ~G[0];
9
10  endmodule
```

Part 4 – The Function Unit.

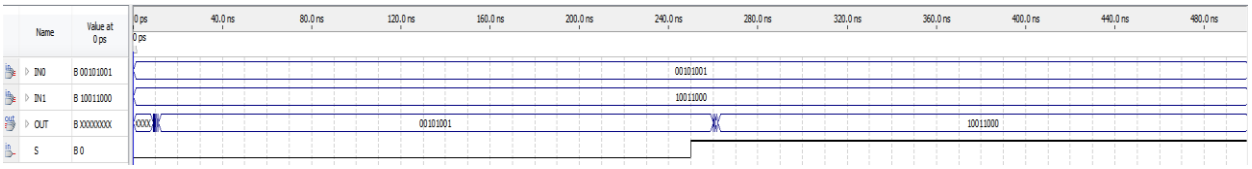
In the last part of the lab, I was instructed to implement the design for the Function Unit. This design incorporated all of the previous circuits in this lab into one big circuit that could perform many different tasks based on a selection signal.

Here is the Block-Diagram for the Function Unit.

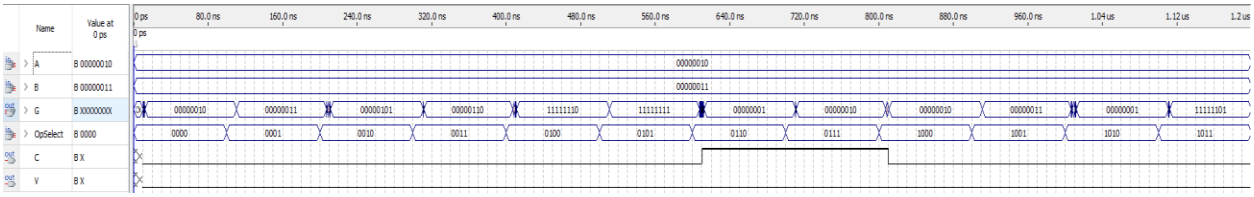


Testing

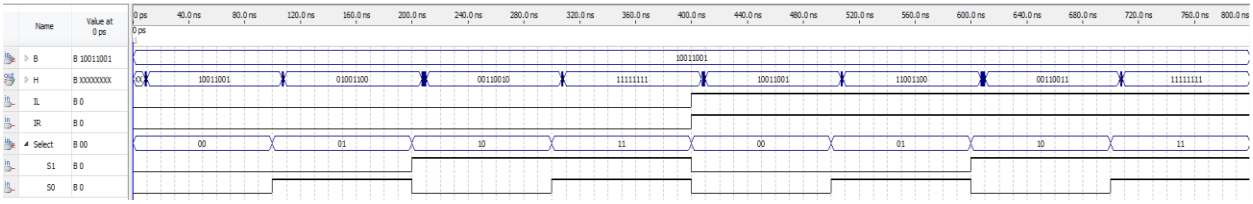
When testing the 8 bit 2 to 1 Mux I encountered no problems and it performed as expected for every single input combination.



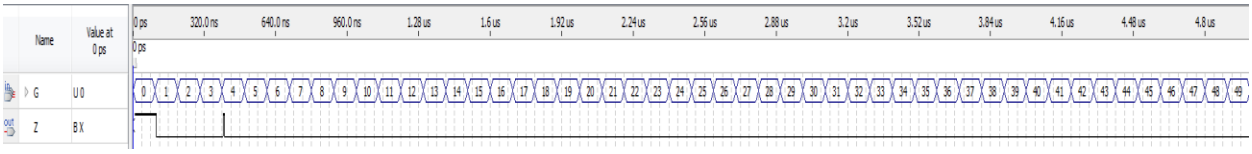
When testing the ALU stage I encountered no problems and it performed as expected for every single input combination.



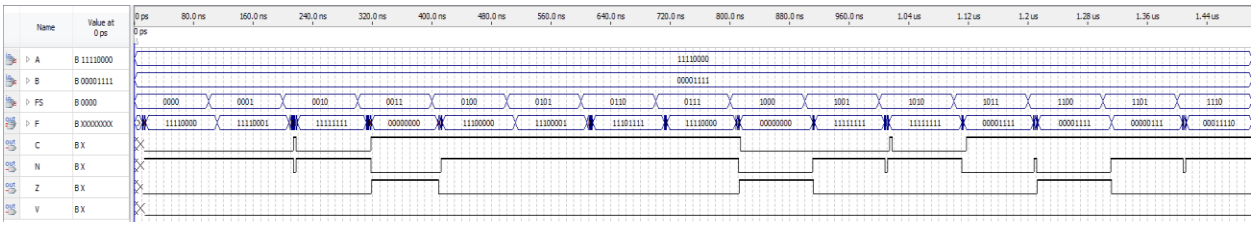
When testing the Shifter I encountered one small problem. When trying to compile the circuit I did not realize I forgot to lab one of the wires coming out of the bus wire. This caused the software to give me several errors. However, once I realized the error and corrected it, the circuit performed as expected for every single input combination.



When testing the Zero Detect Unit I encountered no problems and it performed as expected for every single input combination.



When testing the Function Unit I encountered no problems and it performed as expected for every single input combination.



Conclusion

In this lab, I learned how to create many of the individual parts contained in our Function Unit for our CPU. I learned that the function unit is only a collection of circuit all tied together. They each perform their individual tasks and at the end, the correct output is chosen based on the selection signal. Also, I learned that all of the wires that come out of a bus wire need to be labeled. Otherwise, the compiler will have trouble figuring out which wire goes where. Overall, this lab proved to be enjoyable and I am excited that we are finally taking steps toward creating our CPU.