Quinn Roemer

Engineering - 303

Lab 1

1/25/17

Introduction/Description

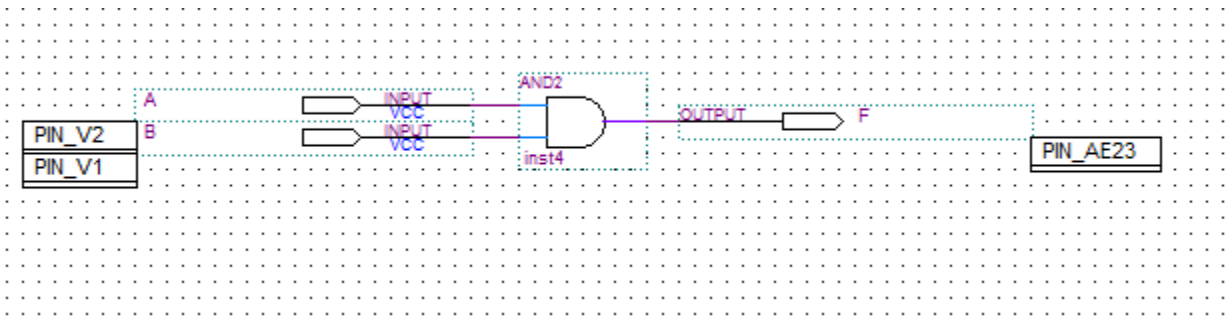
The purpose of this lab was to learn how to design simple circuits in Quartus using Verilog and Block-Diagrams. I was supposed to learn how to design, compile, and simulate circuits that were inputted into Quartus through various methods.

Design

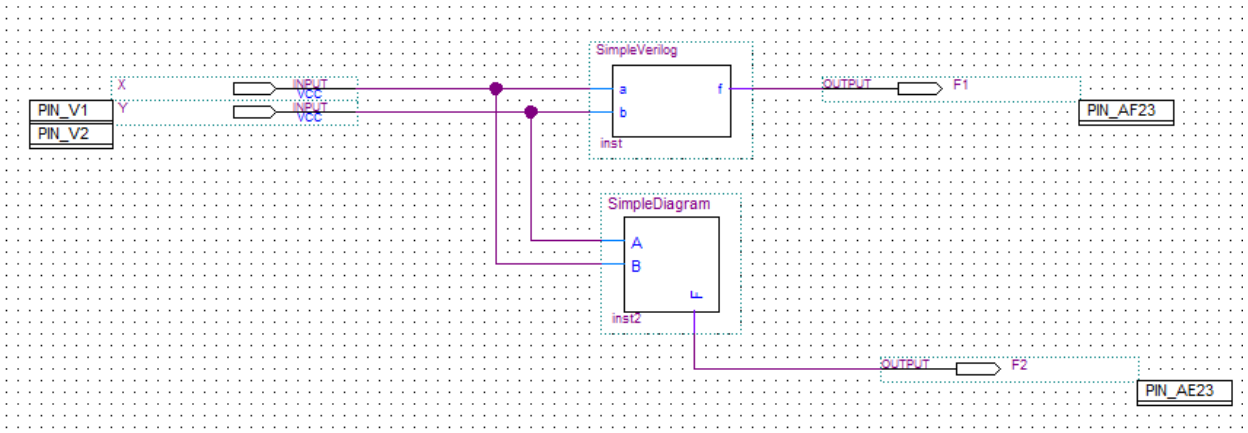
In the first part of the lab I was supposed to design a simple AND circuit in Verilog by following the included instructions in the lab.

```
1   module SimpleVerilog (a, b, f);
2
3   input a, b;
4   output f;
5
6   assign f = a & b;
7
8   endmodule
```

In the second part of the lab I was supposed to design a simple AND circuit in a Block-Diagram by following the included instructions in the lab.



In the third part of the lab I was supposed to take the two circuit designs that I created in the two earlier parts of the lab and use them to create a hierarchical design by including them both in a circuit.



Here is a truth table that encompasses the first two circuits designed in the lab.

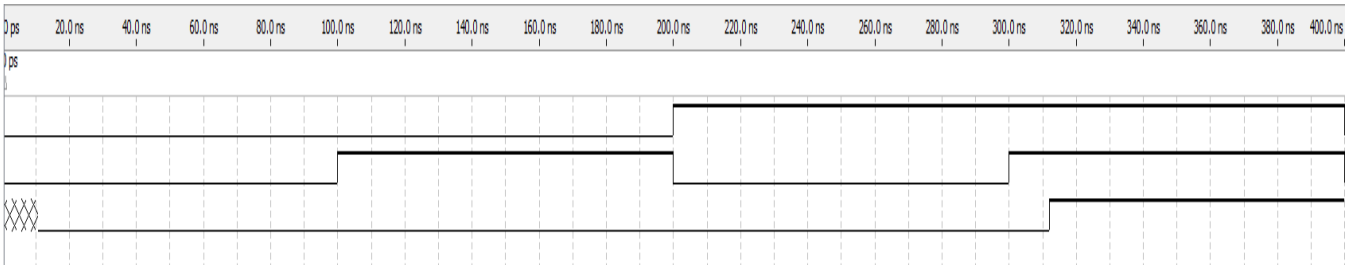
Input A	Input B	Output F
0	0	0
0	1	0
1	0	0
1	1	1

Here is a truth table that encompasses the last circuit designed in the lab.

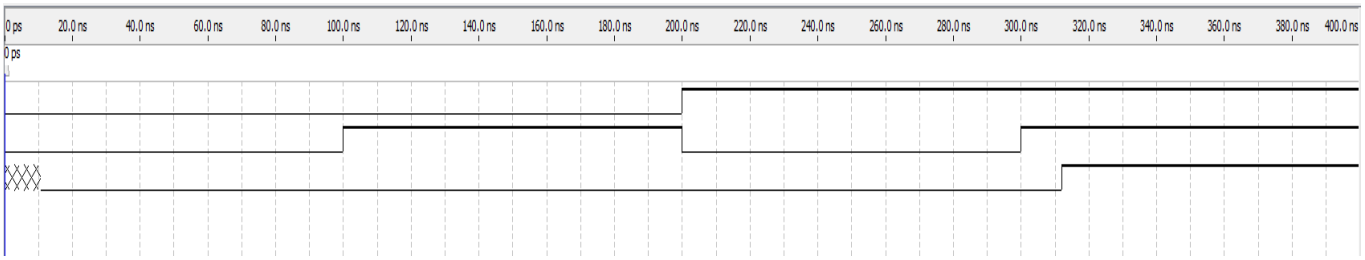
Input X	Input Y	Output F1	Output F2
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

Testing

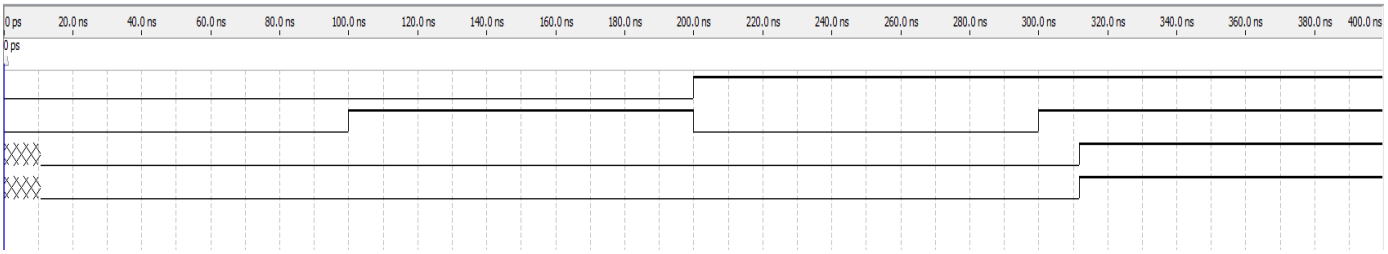
When testing the AND circuit created in Verilog I encountered no problems and it worked as expected for every single input combination.



When testing the AND circuit created by using a Block-Diagram I encountered no problems and it worked as expected for every single input combination.



When testing the hierarchical circuit created in part 3 of the lab I encountered no problems and it worked as expected for every single input combination.



Conclusion

This lab effectively taught me how to create, compile, and simulate simple circuit designs in Quartus. I believe I performed the lab correctly and do not need to change my approach in using Quartus. I have no suggestions to improve the designs that were created in the labs.