CSE2312-002, 004 (Fall 2021)
Homework #2

Notes:
With this homework, we move from abstract processor concepts to the ARM processor as used on the RPi when running Rasbian operating system.

All numbers are in base-10 unless otherwise noted.

If part of a problem is not solvable, explain why in the answer area.

The target date to complete this homework set is September 21, 2021.

This homework set will not be graded, but please solve all of the problems to prepare for the quizzes and exams.

1. For each of the following operations, show the value of R0 in base-10 unsigned representation (e.g., If R0 = 16384, then R0 LSR #1 = 8192).

In the questions below, it using arithmetic operations on unsigned numbers is noted as abnormal.

For these questions, assume that the register R0 contains an unsigned 32-bit integer (e.g., uint32_t) with a value of 2048 (0x00000800).

a. R0 LSR #8: 8

b. R0 LSR #9: 4

c. R0 LSR #10: 2

d. R0 LSR #11: 1

e. R0 LSR #12: 0

f. R0 LSL #20: 2,147,483,648

g. R0 LSL #21: 0

h. R0 LSL #22: 0

i. R0 ASR #8: 8 (abnormal ASR usage)

For these questions, assume that the register R0 contains an unsigned 32-bit integer (e.g., uint32_t) with a value of 3758096384 (0xE0000000).

j. R0 LSL #1: 3,221,225,472

k. R0 LSR #1: 1,879,048,192

l. R0 ASR #1: 4,026,531,840 (abnormal ASR usage)

2. For each of the following operations, show the value of R0 in base-10 signed representation (e.g., If R0 = -64, then R0 ASR #1 = -32).

In the questions below, it using logical operations on signed numbers is noted as abnormal.

For these questions, assume that the register R0 contains a signed 32-bit integer (e.g., int32_t) with a value of -4 (0xFFFFFFFC)

a. R0 ASR #2: -1

b. R0 ASR #3: -1

c. R0 ASL #2: -16

d. R0 ASL #3: -32

e. R0 ASL #28: -1,073,741,824

f. R0 ASL #29: -2,147,483,648

g. R0 ASL #30: 0

h. R0 LSR #2: 1,073,741,824 (abnormal LSR usage)

Assume that the register R0 contains a signed 32-bit integer (e.g., int32_t) with a value of 8 (0x00000008).

i. R0 ASR #3: 1

j. R0 ASR #4: 0

k. R0 ASL #3: 64

l. R0 ASL #4: 128

m. R0 LSR #3: 1 (abnormal LSR usage)

3. Assuming R0 contains 0x34000000, R1 contains 0xCD1258EF, R2 contains 0x00000002 and R3 contains 0x00000001, write the contents of the memory locations below after the STR instruction writes to memory, assuming that each operation is independent. If a number not known, mark the blank with an "X".

a. STR R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is 0xEF

Value at address 0x34000001 is 0x58

Value at address 0x34000002 is 0x12

Value at address 0x34000003 is 0xCD

b. STRH R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is 0xEF

Value at address 0x34000001 is 0x58

Value at address 0x34000002 is X

Value at address 0x34000003 is X

c. STRB R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is 0xEF

Value at address 0x34000001 is X

Value at address 0x34000002 is X

Value at address 0x34000003 is X

d. STR R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is 0xCD

Value at address 0x34000001 is 0x12

Value at address 0x34000002 is 0x58

Value at address 0x34000003 is 0xEF

e. STRH R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is 0x58

Value at address 0x34000001 is 0xEF

Value at address 0x34000002 is X

Value at address 0x34000003 is X

f. STRB R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is 0xEF

Value at address 0x34000001 is X

Value at address 0x34000002 is X

Value at address 0x34000003 is X

g. STRB R1, [R0, R3]; assuming big-endian convention:

Value at address 0x34000000 is X

Value at address 0x34000001 is 0xEF

Value at address 0x34000002 is X

Value at address 0x34000003 is X

h. STRH R1, [R0, R2]; assuming little-endian convention:

Value at address 0x34000000 is X

Value at address 0x34000001 is X

Value at address 0x34000002 is 0xEF

Value at address 0x34000003 is 0x58

4. Assuming the memory locations contain the data below.

Address	Data
0x53400000	0x23
0x53400001	0x58
0x53400002	0x32
0x53400003	0x8B
0x53400004	0x9A
0x53400005	0xCD
0x53400006	0xDE

What is the value of R0 (all 32-bits in hex) after each of the following instructions executes assuming big-endian convention:

a. LDR R0, [R1] assuming R1 = 0x53400000

0x23 58 32 8B

b. LDRH R0, [R1, R2] assuming R1 = 0x53400000 and R2 = 2

0x00 00 32 8B

c. LDRSH R0, [R1] assuming R1 = 0x53400004

0xFF FF 9A CD

d. LDRB R0, [R1] assuming R1 = 0x53400005

0x00 00 00 CD

e. LDRSB R0, [R1] assuming R1 = 0x53400006

0xFF FF FF DE

f. LDRSB R0, [R1, R2] assuming R1 = 0x53400000 and R2 = 3

0xFF FF FF 8B