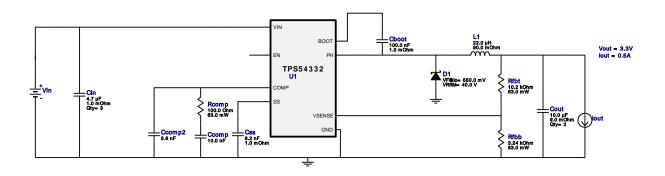
VinMin = 4.5V VinMax = 20.0V Vout = 3.3V Iout = 0.5A Device = TPS54332DDAR Topology = Buck Created = 2022-10-26 13:43:53.844 BOM Cost = \$1.82 BOM Count = 15 Total Pd = 0.43W

WEBENCH® Design Report

Design: 72 TPS54332DDAR TPS54332DDAR 4.5V-20V to 3.30V @ 0.5A

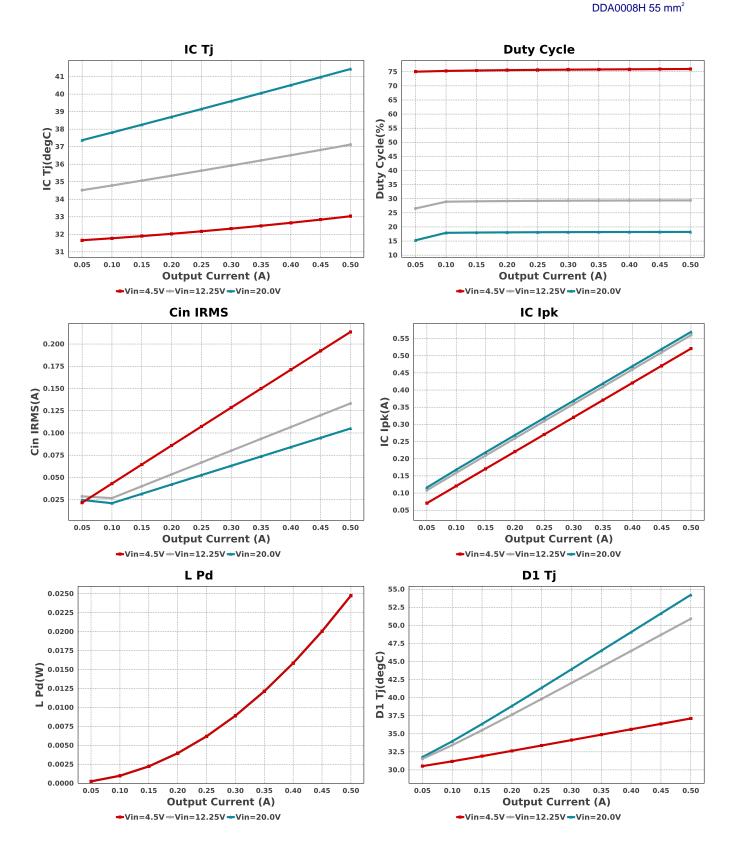


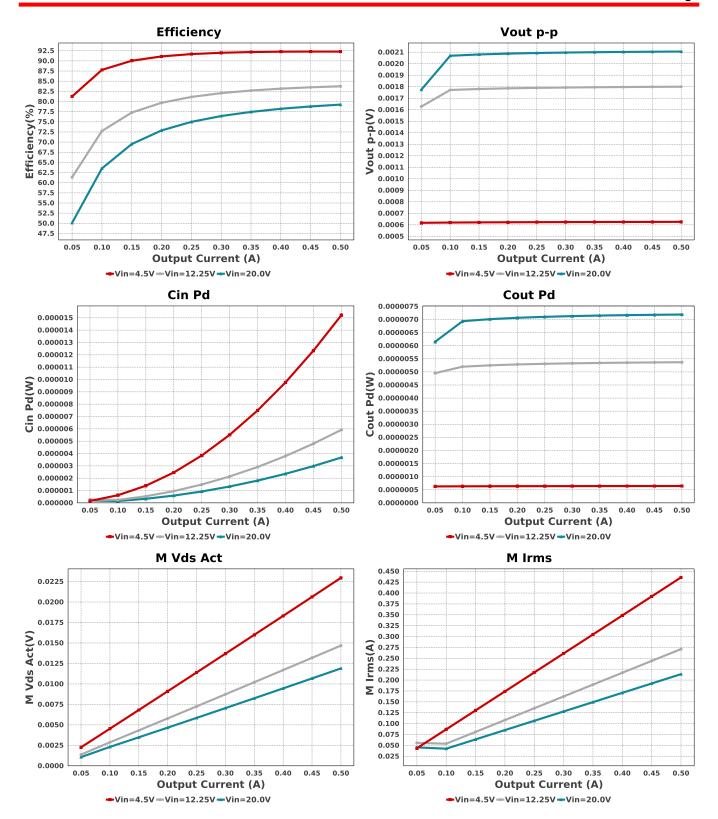
Electrical BOM

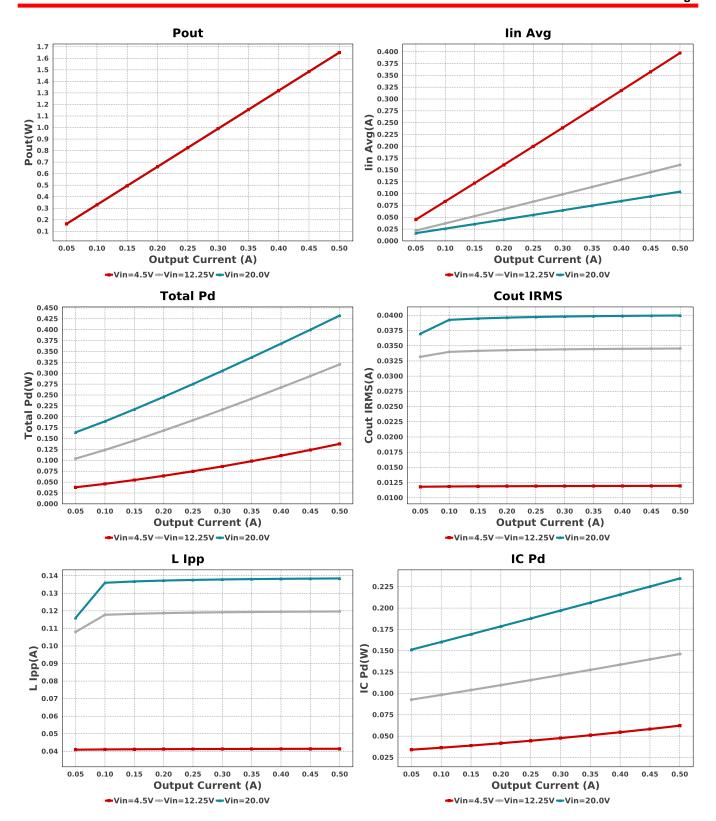
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cboot	MuRata	GRM155R71A104KA01D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	\$0.01	0402 3 mm ²
Ccomp	TDK	CGA4C2C0G1H103J060AA Series= C0G/NP0	Cap= 10.0 nF VDC= 50.0 V IRMS= 0.0 A	1	\$0.06	■ 0805 7 mm ²
Ccomp2	TDK	CGA4C2C0G1H562J060AA Series= C0G/NP0	Cap= 5.6 nF VDC= 50.0 V IRMS= 0.0 A	1	\$0.05	■ 0805 7 mm ²
Cin	MuRata	GRM32ER71H475KA88L Series= X7R	Cap= 4.7 uF ESR= 1.0 mOhm VDC= 50.0 V IRMS= 6.0 A	3	\$0.16	1210 15 mm ²
Cout	MuRata	GRM188R60J106ME47D Series= X5R	Cap= 10.0 uF ESR= 9.0 mOhm VDC= 6.3 V IRMS= 2.74 A	2	\$0.03	0603 5 mm ²
Css	MuRata	GRM033R71A822KA01D Series= X7R	Cap= 8.2 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	\$0.01	0201 2 mm ²
D1	Fairchild Semiconductor	SS14FL	VF@Io= 550.0 mV VRRM= 40.0 V	1	\$0.03	SOD-123F 12 mm ²
L1	TDK	CLF6045T-220M	L= 22.0 μH 90.0 mOhm	1	\$0.39	CLF6045 68 mm ²
Rcomp	Vishay-Dale	CRCW0402100RFKED Series= CRCWe3	Res= 100.0 Ohm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rfbb	Vishay-Dale	CRCW04023K24FKED Series= CRCWe3	Res= 3.24 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rfbt	Vishay-Dale	CRCW040210K2FKED Series= CRCWe3	Res= 10.2 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²

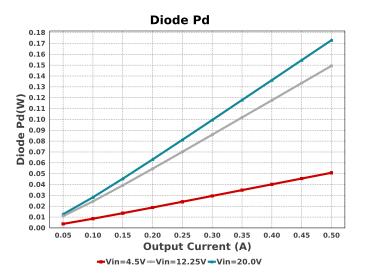
 Name
 Manufacturer
 Part Number
 Properties
 Qty
 Price
 Footprint

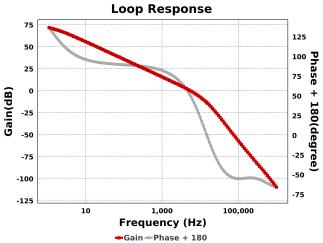
 U1
 Texas Instruments
 TPS54332DDAR
 Switcher
 1
 \$0.70











Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	105.032 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	3.677 µW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	39.972 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	7.19 µW	Capacitor	Output capacitor power dissipation
5.	D1 Tj	54.222 degC	Diode	D1 junction temperature
6.	Diode Pd	173.01 mW	Diode	Diode power dissipation
7.	IC lpk	569.233 mA	IC	Peak switch current in IC
8.	IC Pd	234.74 mW	IC	IC power dissipation
9.	IC Ti	41.432 degC	IC	IC junction temperature
10.	ICThetaJA	48.7 degC/W	IC	IC junction-to-ambient thermal resistance
11.	lin Avg	104.13 mA	IC	Average input current
12.	•	138.465 mA	Inductor	Peak-to-peak inductor ripple current
	L Pd	24.75 mW	Inductor	Inductor power dissipation
	M Irms	213.547 mA	Mosfet	MOSFET RMS ripple current
	M Vds Act	11.893 mV	Mosfet	Voltage drop across the MosFET
16.		3.677 µW	Power	Input capacitor power dissipation
17.		7.19 µW	Power	Output capacitor power dissipation
18.	Diode Pd	173.01 mW	Power	Diode power dissipation
	IC Pd	234.74 mW	Power	IC power dissipation
	L Pd	24.75 mW	Power	Inductor power dissipation
	Total Pd	432.535 mW	Power	Total Power Dissipation
22.	BOM Count	15	System	Total Design BOM count
	20 000		Information	- Otal 2 00.9.1 2 0 111 0 0 0 111
23.	Cross Freq	5.252 kHz	System	Bode plot crossover frequency
_0.	010001104	0.202 N 12	Information	Bodo piot diocester moquency
24.	Duty Cycle	18.241 %	System	Duty cycle
	200, 0,00		Information	
25.	Efficiency	79.231 %	System	Steady state efficiency
_0.		10.201 /0	Information	Cloudy state smoothly
26.	FootPrint	216.0 mm ²	System	Total Foot Print Area of BOM components
_0.		210.011111	Information	rotal rotal rintrinoa of Dom components
27.	Frequency	1000.0 kHz	System	Switching frequency
			Information	Cinicining inequality
28.	Gain Marg	-14.233 dB	System	Bode Plot Gain Margin
_0.	Cam marg	1 1.200 dB	Information	2000 Flot Call Margin
29.	lout	500.0 mA	System	lout operating point
20.	lout	000.0 1111 (Information	Tout operating point
30.	Low Freq Gain	71.165 dB	System	Gain at 1Hz
50.	Low ricq Gain	71.105 GB	Information	Gairr at 1112
31.	Mode	CCM	System	Conduction Mode
51.	Mode	COIVI	Information	Conduction wode
32.	Phase Marg	52.586 deg	System	Bode Plot Phase Margin
32.	Fliase Mary	32.300 deg	Information	Boue Flot Fliase Margill
33.	Pout	1.65 W		Total output power
JJ.	i out	1.00 VV	System Information	ι οιαι ουιρυι ρονισι
34.	Total BOM	\$1.819	System	Total BOM Cost
54.	i otai bolvi	φι.υισ	Information	I otal DOM OUSE
35.	\/in	20.0 V		Vin apprating point
აა.	Vin	∠U.U V	System	Vin operating point
26	Vout	221/	Information	Operational Output Voltage
36.	Vout	3.3 V	System	Operational Output Voltage
			Information	

#	Name	Value	Category	Description
37.	Vout Actual	3.319 V	System Information	Vout Actual calculated based on selected voltage divider resistors
38.	Vout Tolerance	5.087 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
39.	Vout p-p	2.106 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description	
lout	500.0 m	Maximum Output Current	
VinMax	20.0	Maximum input voltage	
VinMin	4.5	Minimum input voltage	
Vout	3.3	Output Voltage	
base_pn	TPS54332	Base Product Number	
source	DC	Input Source Type	
Та	30.0	Ambient temperature	

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

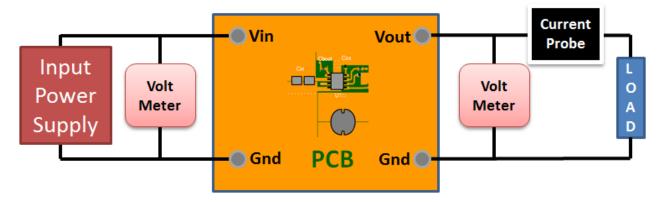
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 4.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum lout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

- 1. Master key: 7E00AF9B0638DEC2[v1]
- 2. TPS54332 Product Folder: http://www.ti.com/product/TPS54332: contains the data sheet and other resources.

Important Notice and Disclaimer

TI provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources AS IS and with all faults, and disclaims all warranties. These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Providing these resources does not expand or otherwise alter TI's applicable Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with TI products.