



FPGA
hackathon
&
conference

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Conference

(online)

Hackathon

(Kraków Technology Park + online)

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Instruction – using AWS

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1. Connection with AWS virtual machine

1.1. Open ssh tunnel for port 5901

To open ssh tunnel type the following command into the command prompt:

```
ssh -N -L 5901:localhost:5901 hackathon_fpga@<SERVER_IP> -i <path_to_ssh_key>
```

Server IP and path to ssh key "SSH_Key_Team" should be provided in email.

Logging in is done with user "hackathon_fpga", to open additional terminal (if needed) use:

```
ssh hackathon_fpga@<SERVER_IP> -i <path_to_ssh_key>
```

*If there is problem with key permissions on Windows - open cmd and use commands:

```
icacls <SSH_KEY_PATH> /inheritance:r  
icacls <SSH_KEY_PATH> /grant:r "%username%": "(R)"
```

*If there is problem with key permissions on Linux - open terminal and use command:

```
chmod 600 <SSH_KEY_PATH>
```

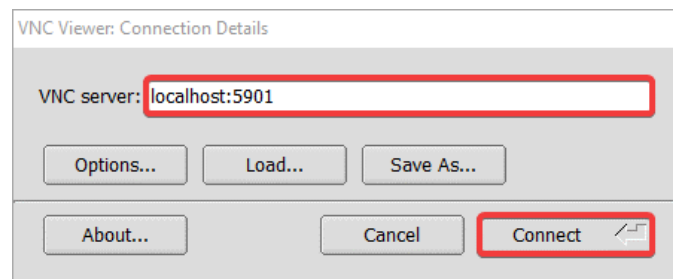
1.2. Connect with AWS virtual machine using TigerVNC (TBD)

TigerVNC Viewer can be downloaded from the official site <https://tigervnc.org/>

Select "Releases", then, after redirection to gitlab, select version which you want, there will be links to binaries. If newest 1.12 version will not work, select version 1.11.0.

After installing the program run it and provide the parameter:

- VNC server: localhost:5901



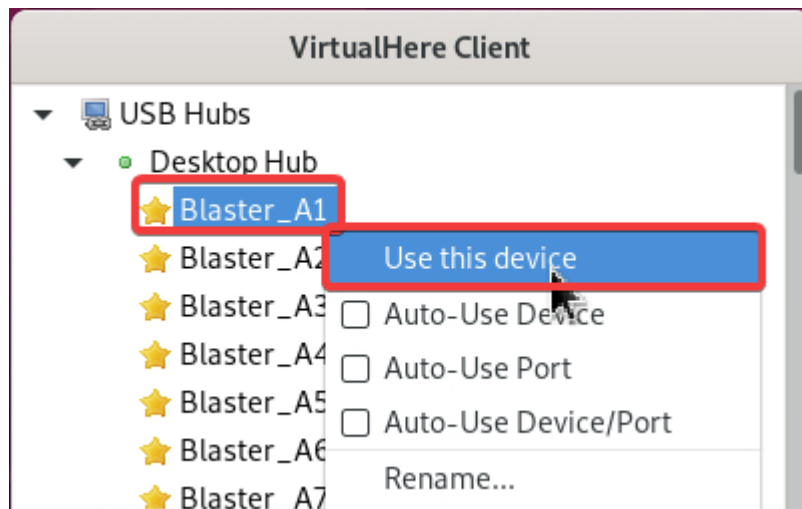
The connection is using the user hackathon_fpga (password: fpga2022). After logging in, the system should be ready to work.

2. Connection with board

The connection to the fpga device is done using the VirtualHere program. To use the VirtualHere client, run the `vhuit64` file from desktop as a superuser:

```
sudo ./vhuit64
```

After the program is loaded, a list of available devices will appear. There is possibility to connect to the selected device by double-clicking with the left mouse button, or by selecting "Use this device" after clicking the right mouse button. A password for device is required to establish a connection. Password which is 12 first characters of the 5th line in the team ssh private key file.

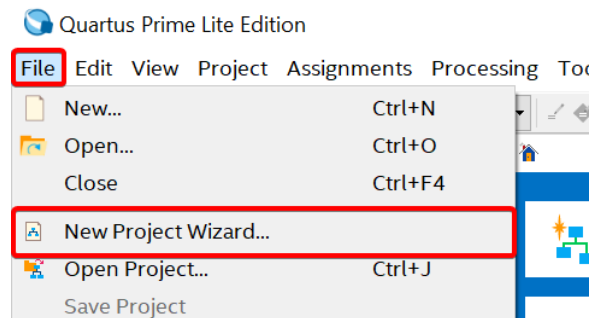


It is possible to use option "Remember". If the remembered password was entered incorrectly, it can be canceled by selecting device and using shortcut Shift+F9.

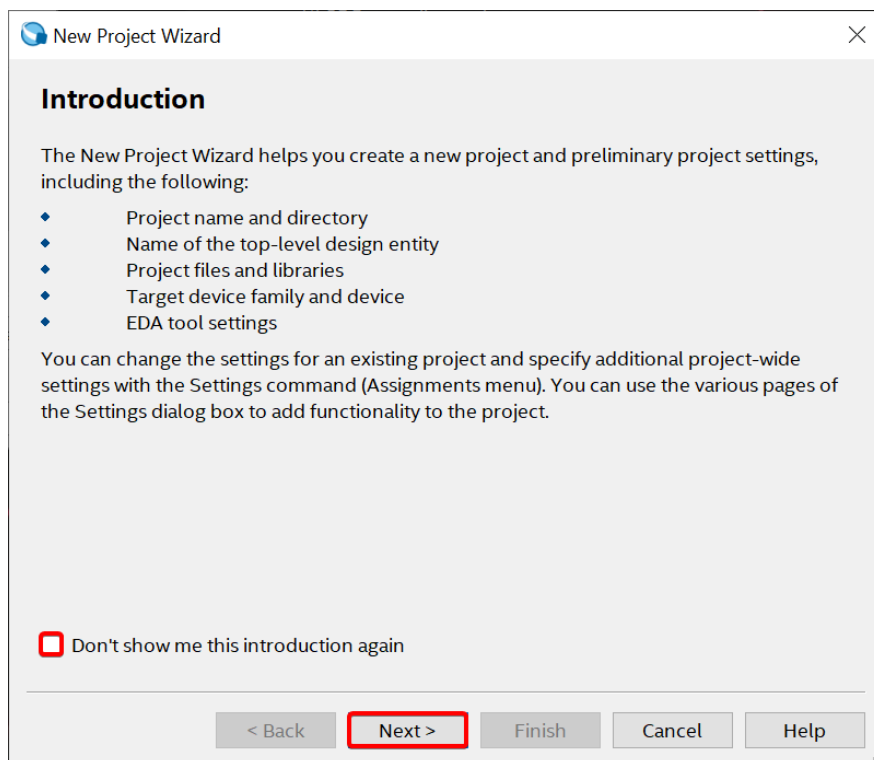
3. Upload bitfile

3.1. Create empty project (*for connection test*)

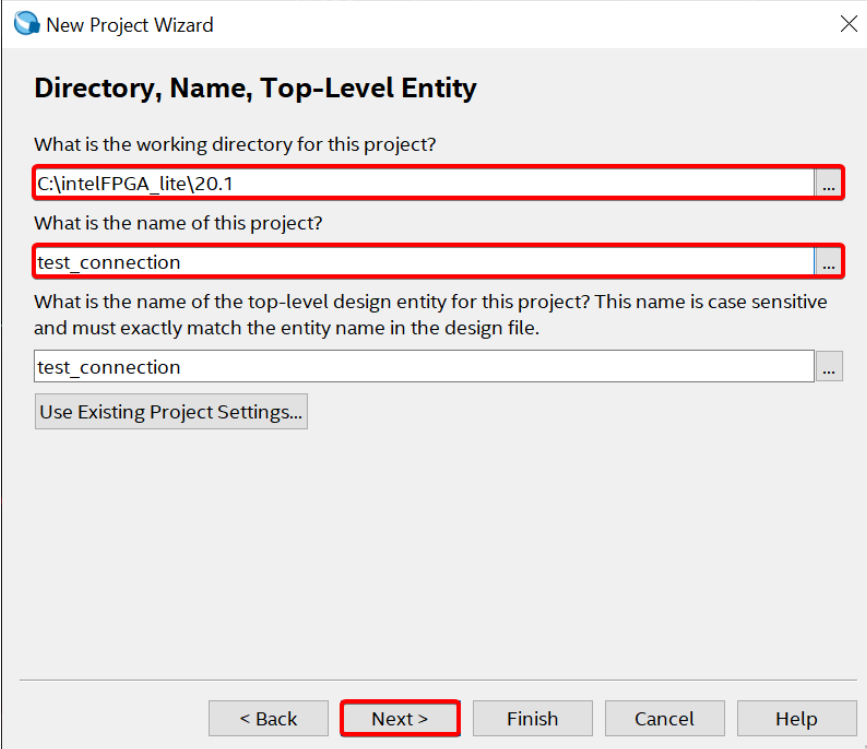
Select “New Project Wizard...” from “File” tab



Select “Next” and check “Don’t show me this introduction again” if you don’t want to see this Introduction again

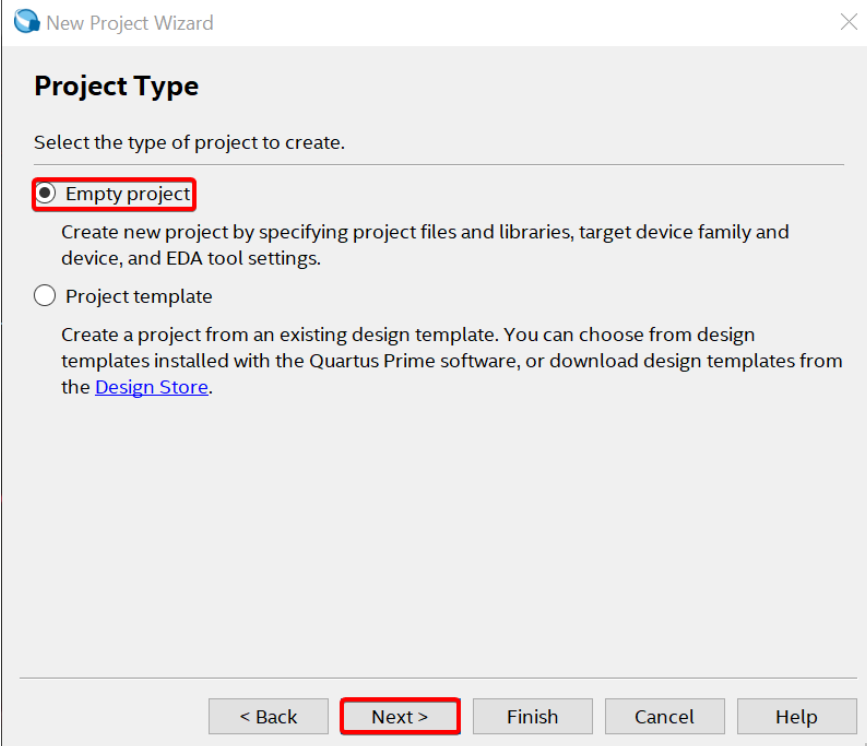


Enter correct project path and name



The screenshot shows the 'New Project Wizard' dialog box, specifically the 'Directory, Name, Top-Level Entity' step. The title bar reads 'New Project Wizard'. The main heading is 'Directory, Name, Top-Level Entity'. There are three text input fields, each with a red rectangular highlight around it. The first field is labeled 'What is the working directory for this project?' and contains the text 'C:\intelFPGA_lite\20.1'. The second field is labeled 'What is the name of this project?' and contains the text 'test_connection'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and also contains the text 'test_connection'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a red rectangular box.

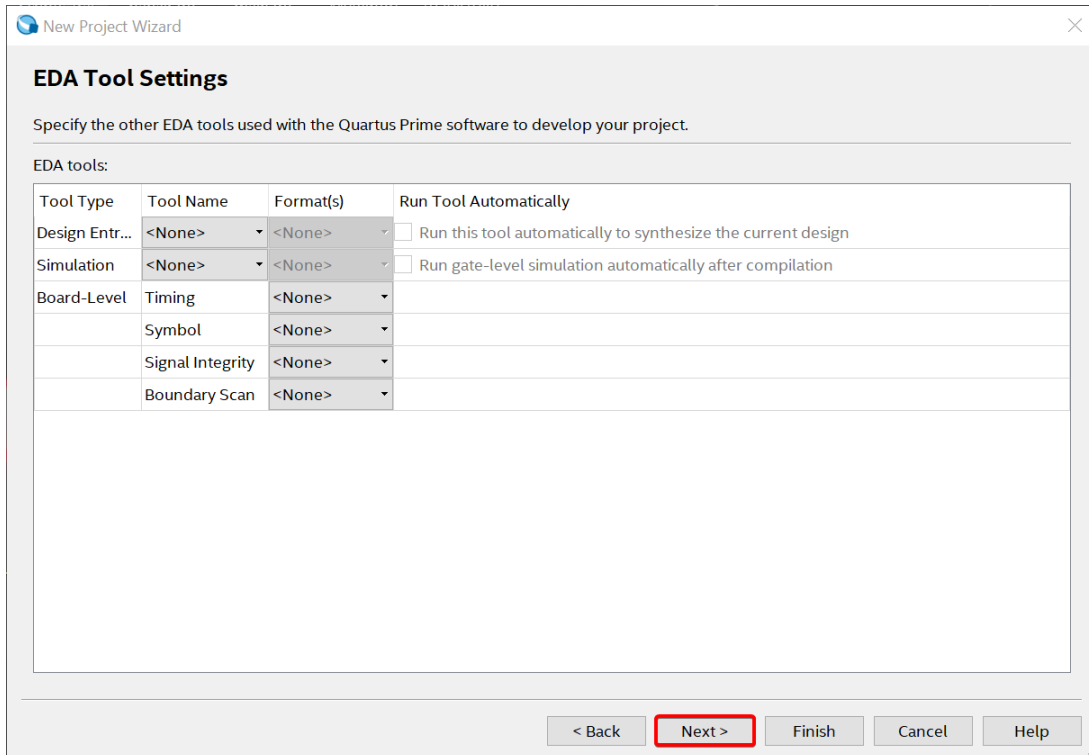
Select "Empty project"



The screenshot shows the 'New Project Wizard' dialog box, specifically the 'Project Type' step. The title bar reads 'New Project Wizard'. The main heading is 'Project Type'. Below the heading is the instruction 'Select the type of project to create.' There are two radio button options. The first option is 'Empty project', which is selected (indicated by a filled circle) and has a red rectangular highlight around it. Below this option is the text 'Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.' The second option is 'Project template', which is not selected (indicated by an empty circle). Below this option is the text 'Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).' At the bottom of the dialog, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a red rectangular box.

Additional files are not needed

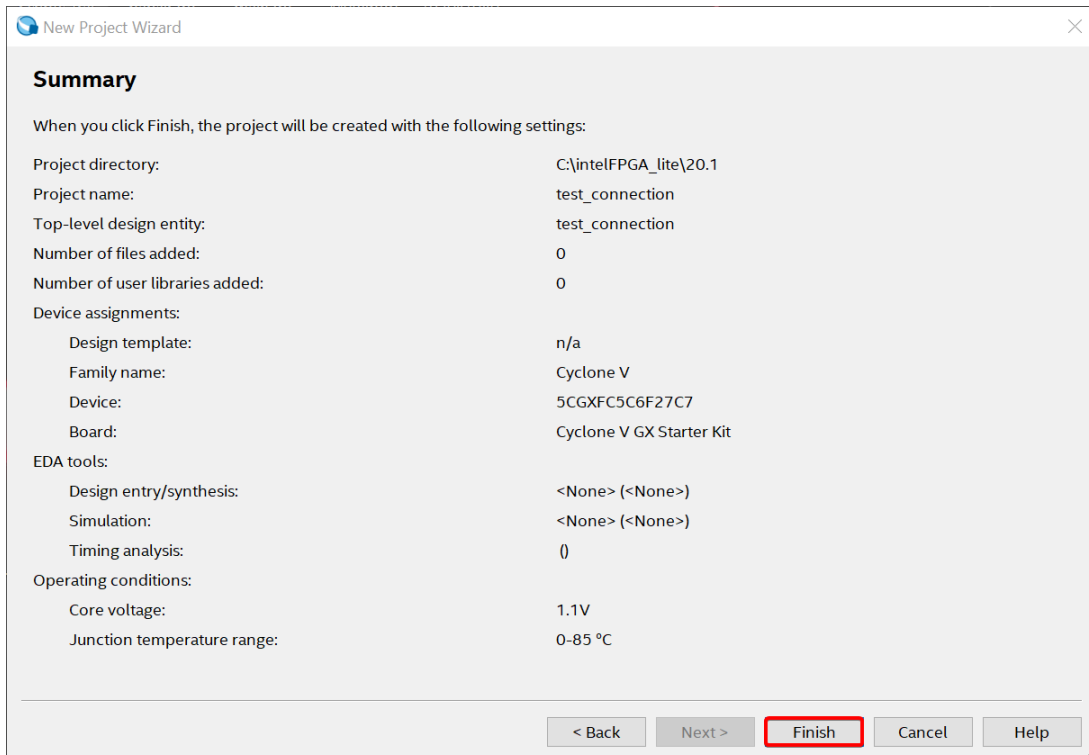
For empty project nothing is needed here



The screenshot shows the 'New Project Wizard' window, specifically the 'EDA Tool Settings' tab. The window title is 'New Project Wizard'. Below the title bar, the text 'EDA Tool Settings' is displayed. A subtitle reads: 'Specify the other EDA tools used with the Quartus Prime software to develop your project.' Below this, a section labeled 'EDA tools:' contains a table with four columns: 'Tool Type', 'Tool Name', 'Format(s)', and 'Run Tool Automatically'. The table has five rows. The first two rows are for 'Design Entr...' and 'Simulation', both with '<None>' for Tool Name and Format(s), and checkboxes for 'Run Tool Automatically'. The next three rows are for 'Board-Level' tools: 'Timing', 'Symbol', and 'Signal Integrity', all with '<None>' for Tool Name and Format(s). The 'Boundary Scan' row is also present with '<None>' for Tool Name and Format(s). At the bottom of the window, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a red rectangle.

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entr...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Select "Finish" to create empty project

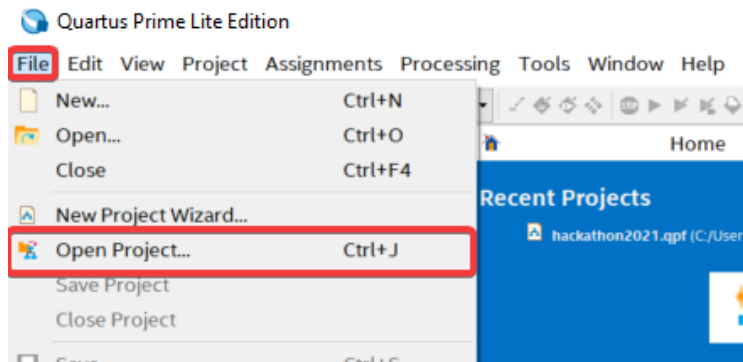


The screenshot shows the 'New Project Wizard' window, specifically the 'Summary' tab. The window title is 'New Project Wizard'. Below the title bar, the text 'Summary' is displayed. A subtitle reads: 'When you click Finish, the project will be created with the following settings:'. Below this, the settings are listed in two columns. The left column lists the settings, and the right column shows the values. The settings are: Project directory: C:\intelFPGA_lite\20.1; Project name: test_connection; Top-level design entity: test_connection; Number of files added: 0; Number of user libraries added: 0; Device assignments: Design template: n/a; Family name: Cyclone V; Device: 5CGXFC5C6F27C7; Board: Cyclone V GX Starter Kit; EDA tools: Design entry/synthesis: <None> (<None>); Simulation: <None> (<None>); Timing analysis: (); Operating conditions: Core voltage: 1.1V; Junction temperature range: 0-85 °C. At the bottom of the window, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Finish' button is highlighted with a red rectangle.

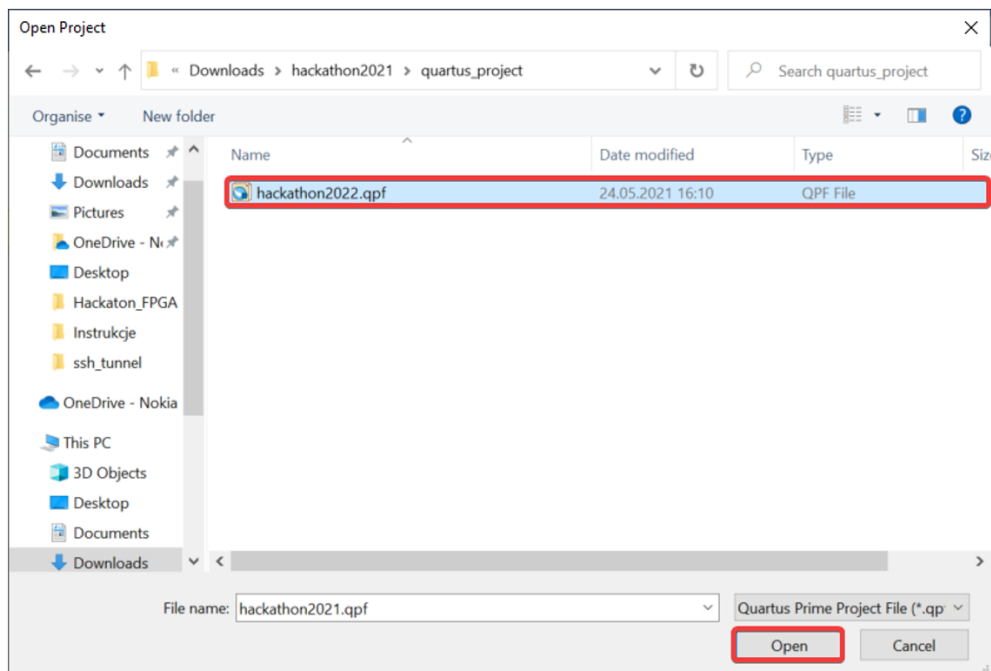
Project directory:	C:\intelFPGA_lite\20.1
Project name:	test_connection
Top-level design entity:	test_connection
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	Cyclone V
Device:	5CGXFC5C6F27C7
Board:	Cyclone V GX Starter Kit
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()
Operating conditions:	
Core voltage:	1.1V
Junction temperature range:	0-85 °C

3.1. Import project

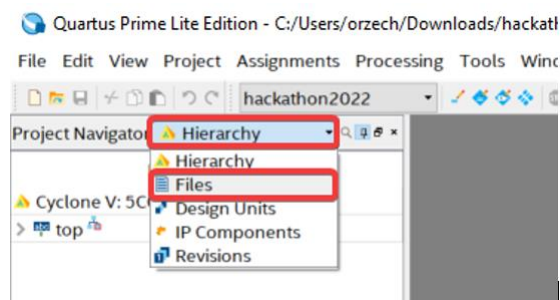
Select “Open Project” from “File” tab.



Enter the path to project (*.qpf file from “quartus_project” directory)

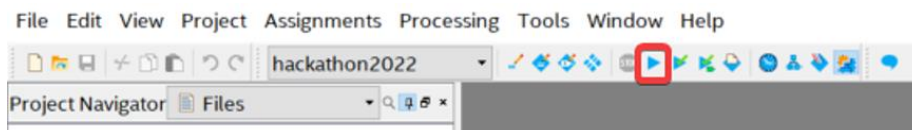


To see all files from project change view from “Hierarchy” to “Files”

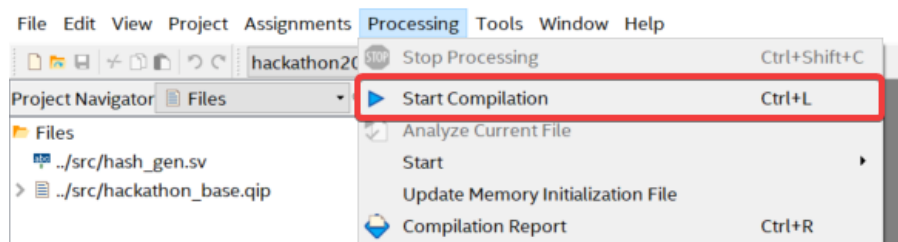


3.3. Compilation

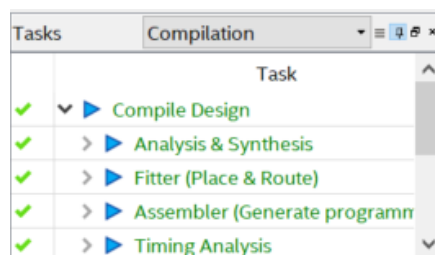
To compile project use button with triangle from tool bar



Or select "Start Compilation" from Processing tab



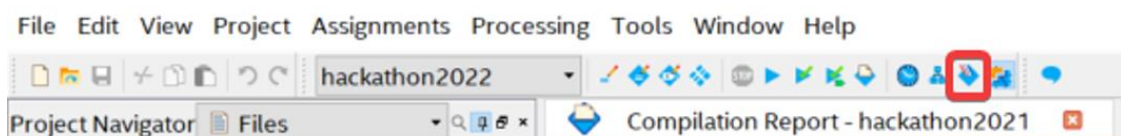
If compilation was successful all compilation phases should have green color



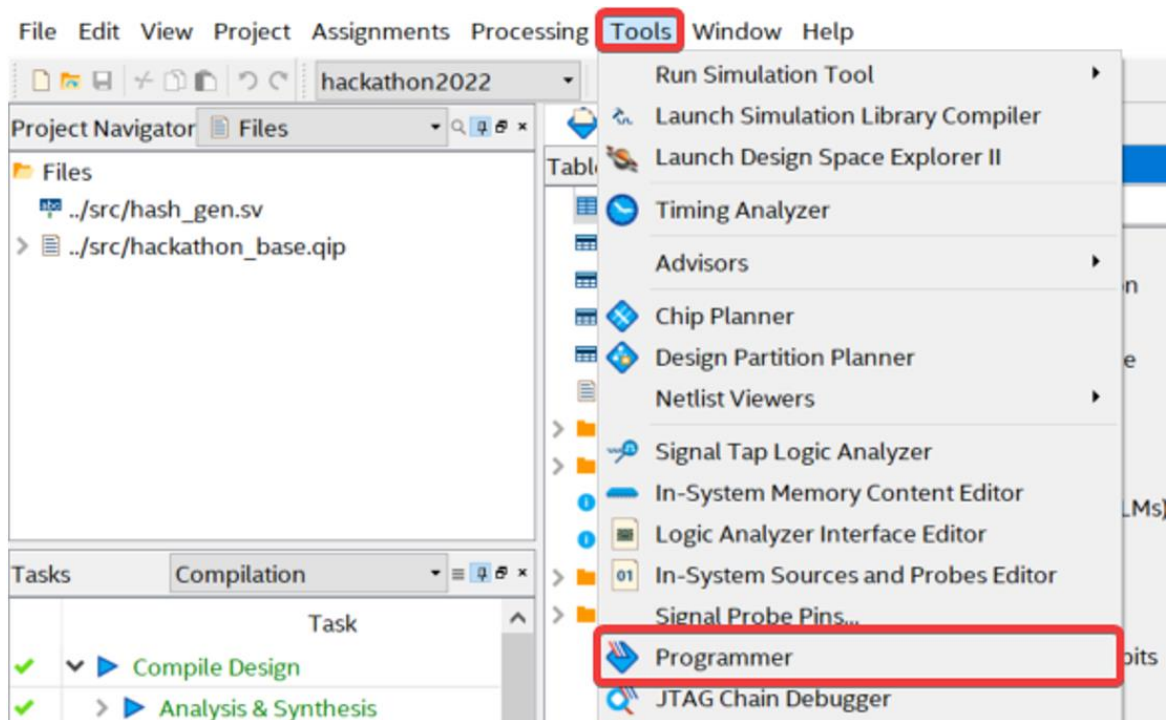
3.3. Uploading bitfile

To upload bitfile right usb device should be connected via virtualhere.

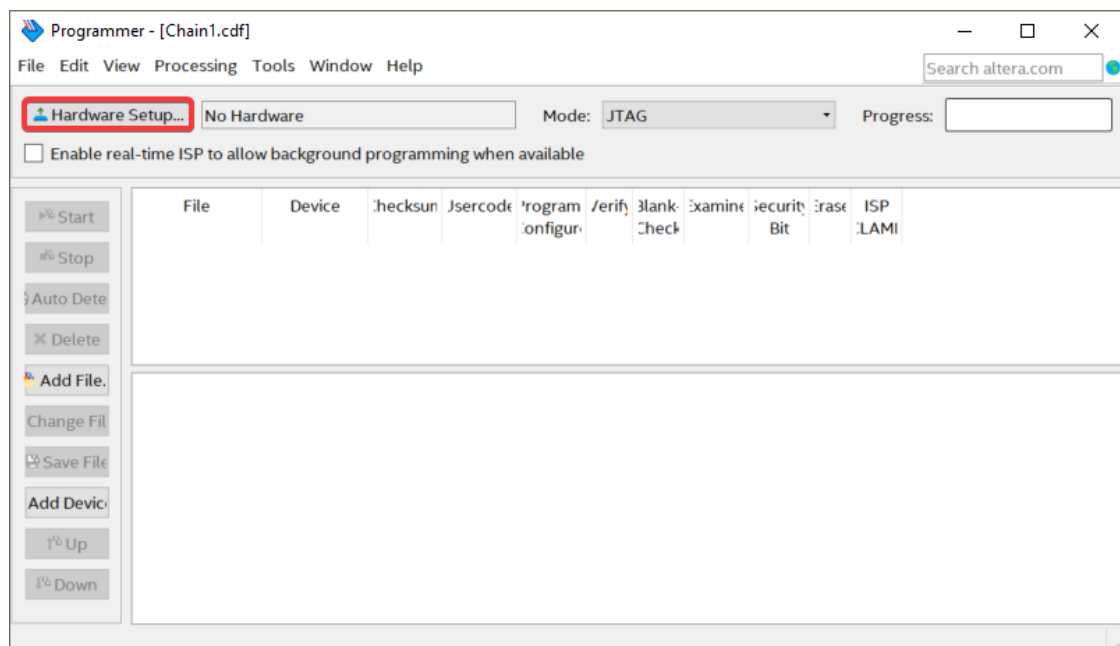
Run Programmer using symbol shown on picture below



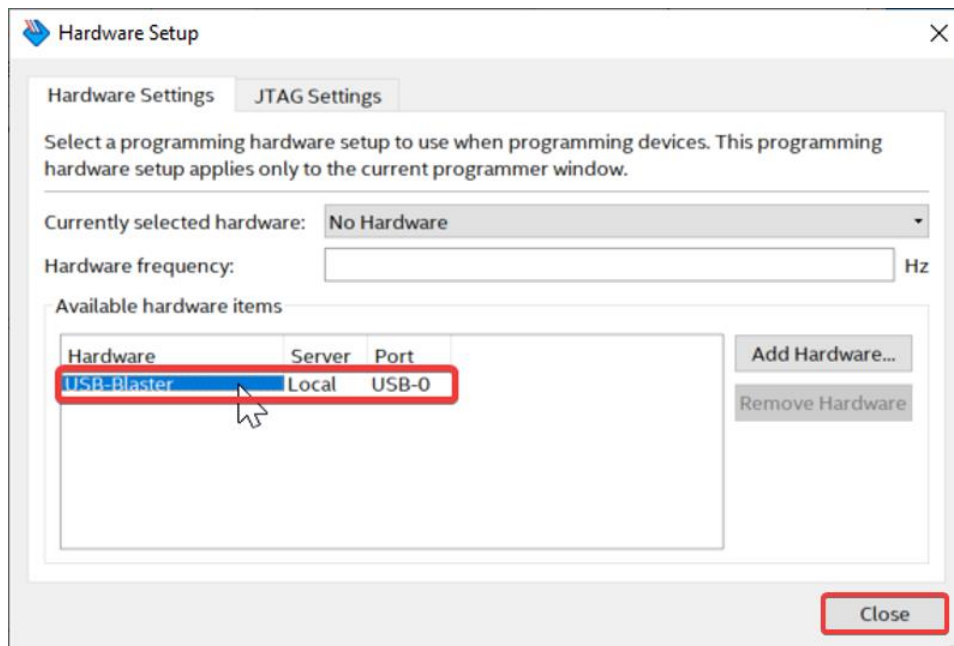
Or select "Programmer" option from "Tools" tab.



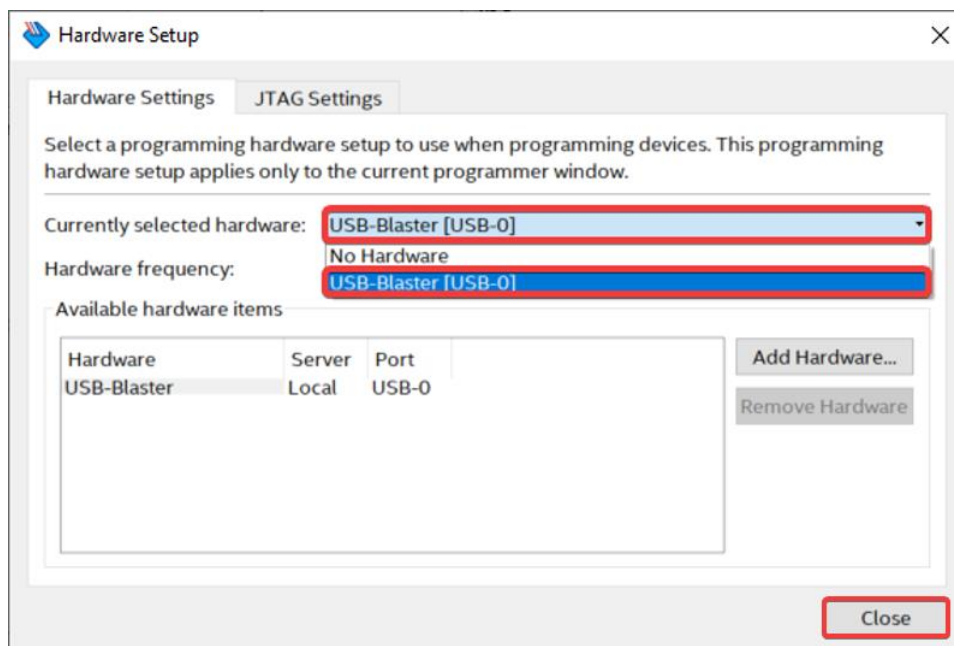
If “USB-Blaster” is not connected select “Hardware Setup”



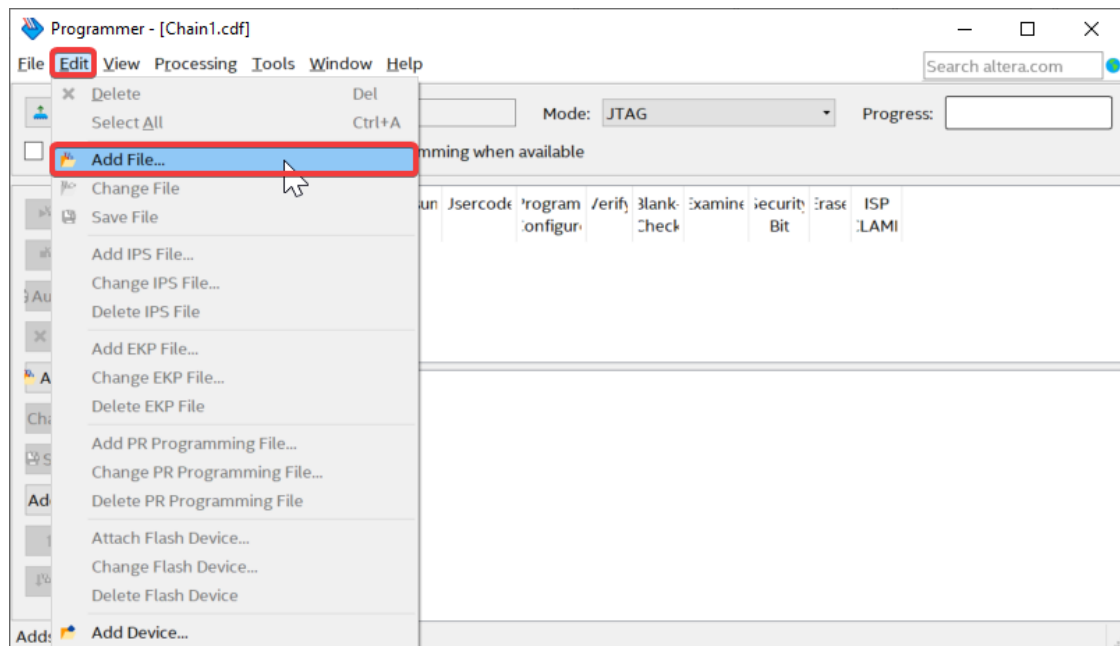
Double click on USB-Blaster connected



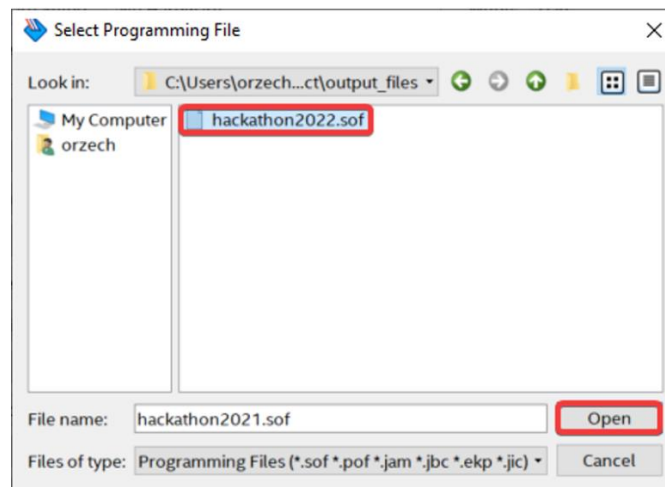
Or select USB-Blaster from drop-down list



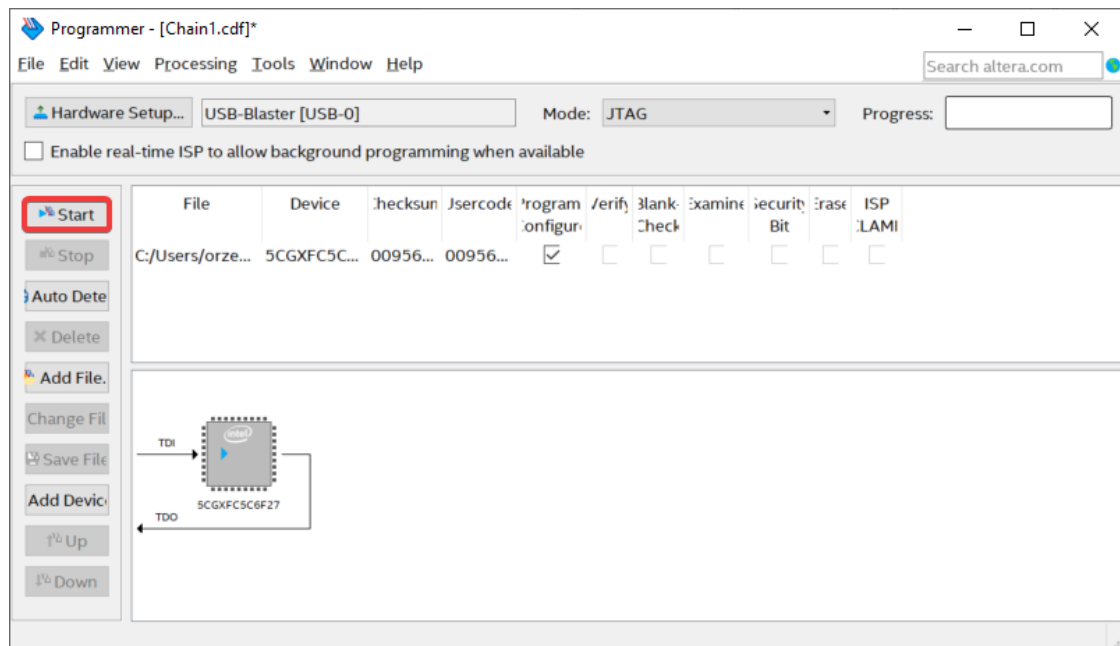
If there is need to choose bitfile expand “Edit” from toolbar and select “Add File”



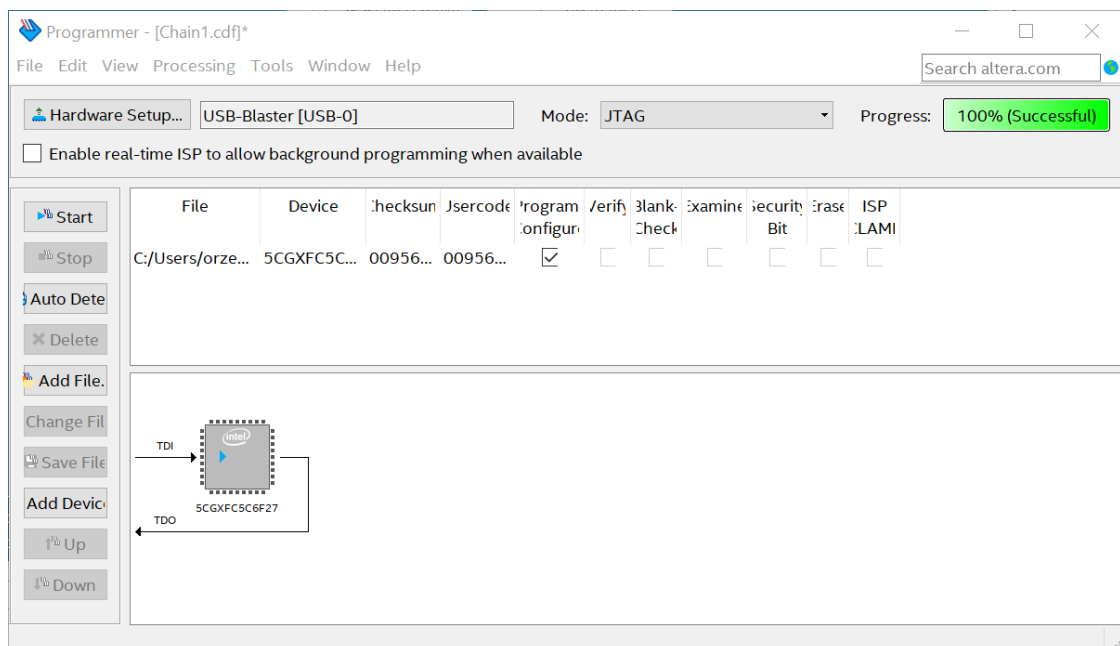
And select bitfile (file *.sof from “output_files” directory)



Use “Start” button to upload bitfile



If everything works bitfile will be uploaded with 100% Success



Sometimes it takes a while, so if “Progress” bar looks stuck - be patient.

If upload bitfile fails close programmer, use command below and try upload bitfile again

```
sudo killall jtagd
```

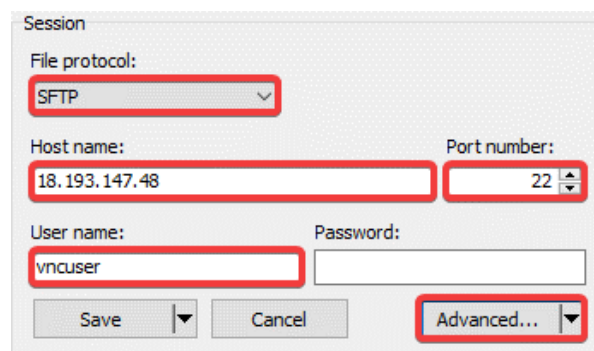

4. Additional actions

4.1. File transfer

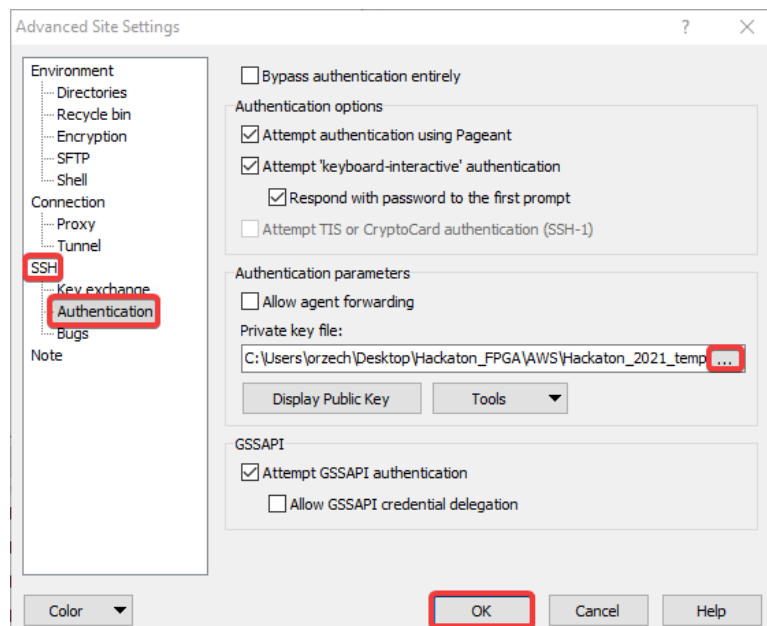
Files can be transferred using WinSCP (or another software). If you using WinSCP required parameters are:

- File protocol: SFTP
- Host name: SERVER_IP (Delivered with mail)
- Port number: 22
- User name: vncuser

Then go to Advanced settings



In the SSH / Authentication tab, enter the path to the ssh key “SSH_Key_Team”



After the configuration save changes and connect to transfer files with the virtual machine.