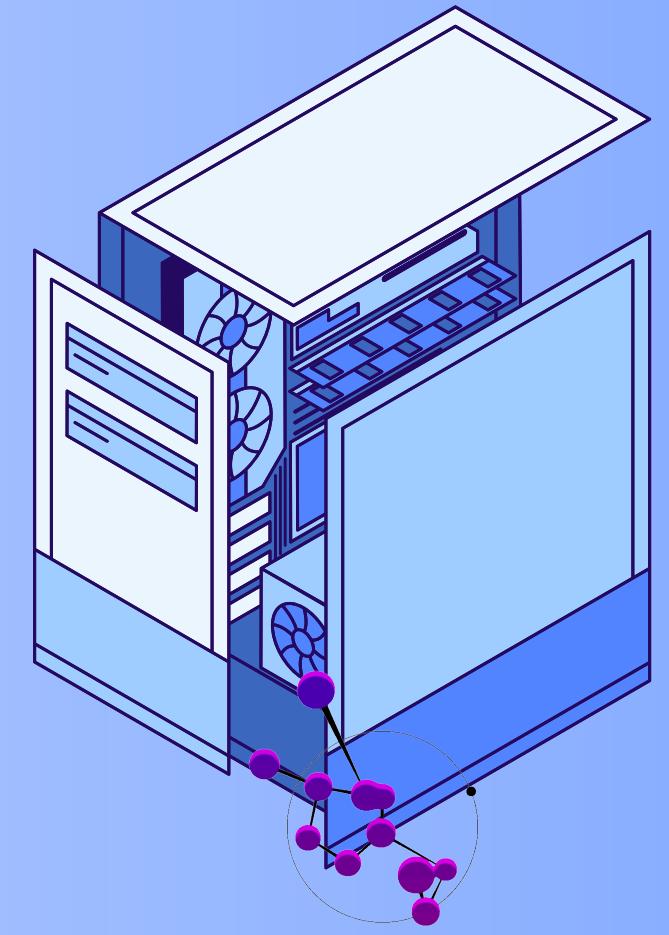
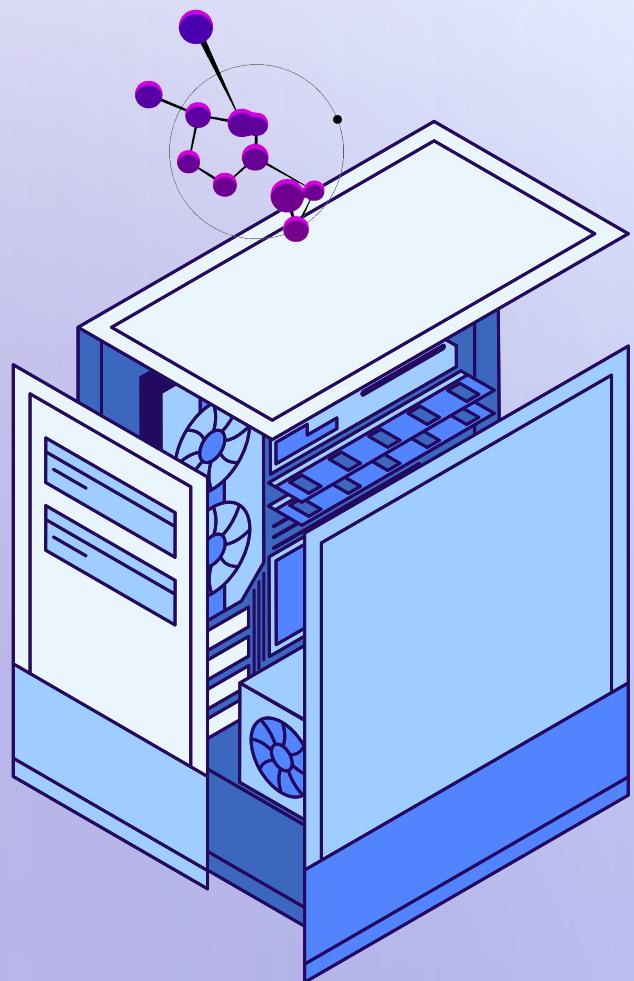


DIGITAL LOGICAL DESIGN



LAB PROJECT

**4 BIT BINARY
SYNCHRONOUS COUNTER**



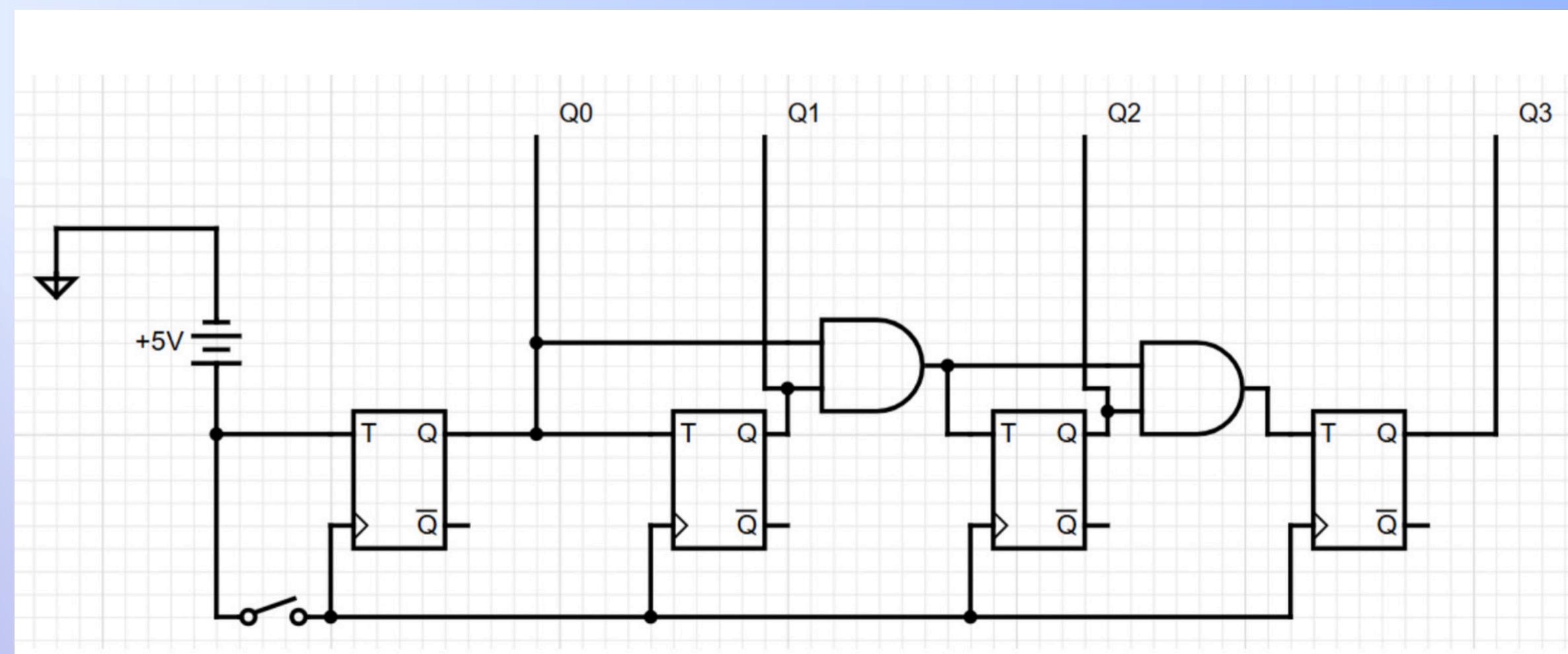
1. Determine from the above description, the equations of T inputs for each T flip flop in the design of the counter.

Clock cycle	Q ₂	Q ₁	Q ₀
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

- 1- $T_0 = 1$: Q₀ changes at every clock cycle, so T₁ must always be 1
- 2- $T_1 = Q_0$: Q₁ changes only when Q₀ is 1, so T₂ depends on Q₀.
- 3- $T_2 = Q_0 \text{ AND } Q_1$: Q₂ changes only when both Q₀ and Q₁ are 1, so T₃ depends on their AND condition



2. Design the circuit for a 4bit up-counter using T flip flop



**3. The equations of T inputs for each T flip flop used in the design of the counter.
The table below shows states every clock cycle.**



Clock Pulse	Q ₃	Q ₂	Q ₁	Q ₀	Flip Notes
0	0	0	0	0	Initial state
1	0	0	0	1	Q ₀ Flip
2	0	0	1	0	Q ₀ , Q ₁ Flip
3	0	0	1	1	Q ₀ Flip
4	0	1	0	0	Q ₀ , Q ₁ , Q ₂ Flip
5	0	1	0	1	Q ₀ Flip
6	0	1	1	0	Q ₀ , Q ₁ Flip
7	0	1	1	1	Q ₀ Flip
8	1	0	0	0	Q ₀ , Q ₁ , Q ₂ , Q ₃ Flip
9	1	0	0	1	Q ₀ Flip
10	1	0	1	0	Q ₀ , Q ₁ Flip
11	1	0	1	1	Q ₀ Flip
12	1	1	0	0	Q ₀ , Q ₁ , Q ₂ Flip
13	1	1	0	1	Q ₀ Flip
14	1	1	1	0	Q ₀ , Q ₁ Flip
15	1	1	1	1	Q ₀ Flip
16	0	0	0	0	Reset (All Flip)



In a T flip-flop. The output flips on the (either falling or rising) edge of the clock, if T is set to 1.

$\therefore Q_0$ Flips on every cycle $\therefore T_0 = 1$

$\therefore Q_1$ Flips only if Q_0 is set to 1 $\therefore T_1 = Q_0$

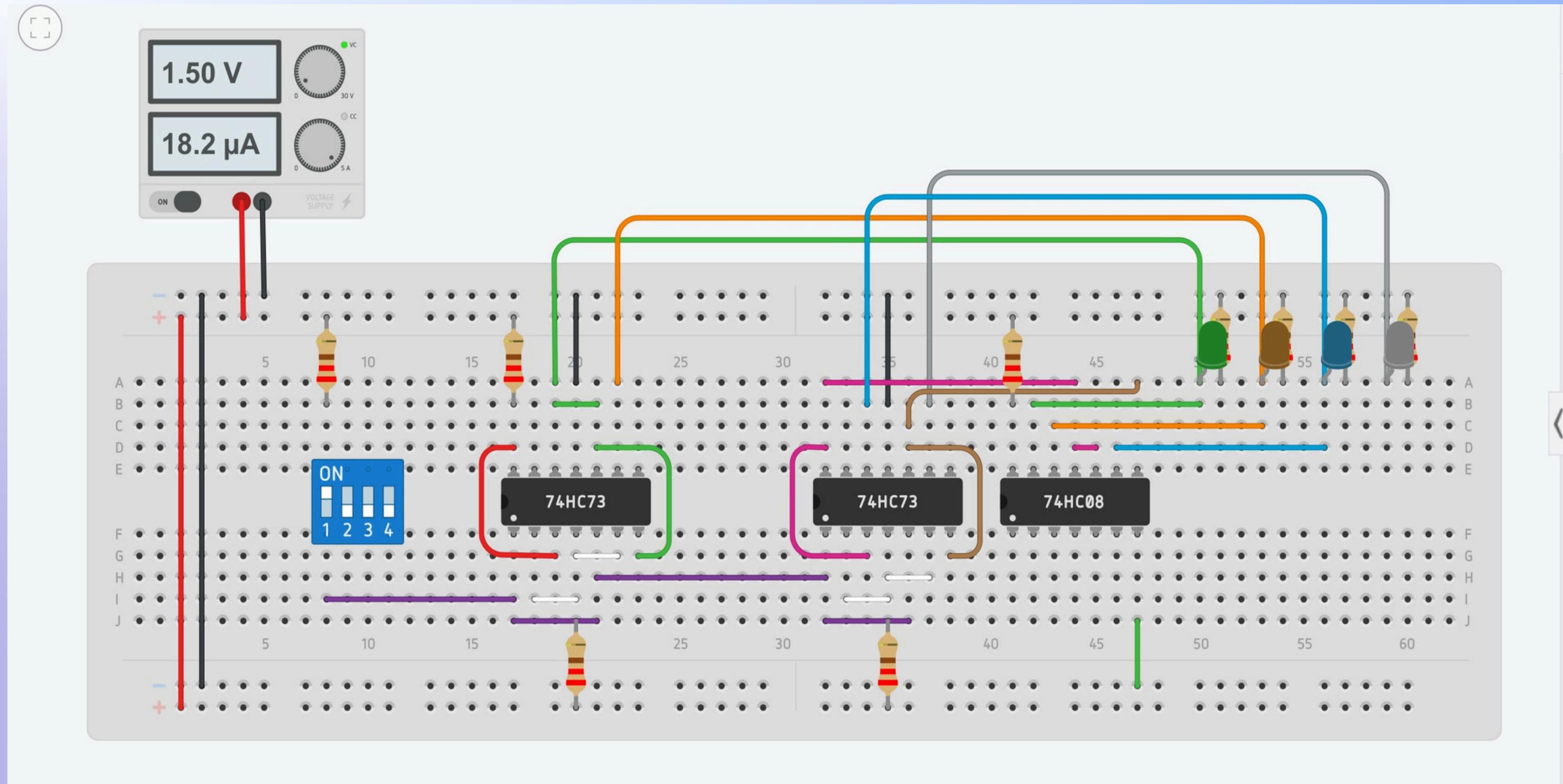
$\therefore Q_2$ Flips only if Q_0 and Q_1 are set to 1 $\therefore T_2 = Q_0.Q_1$

$\therefore Q_3$ Flips only if Q_0 and Q_1 and Q_2 are set to 1 $\therefore T_3 = Q_0.Q_1.Q_2$

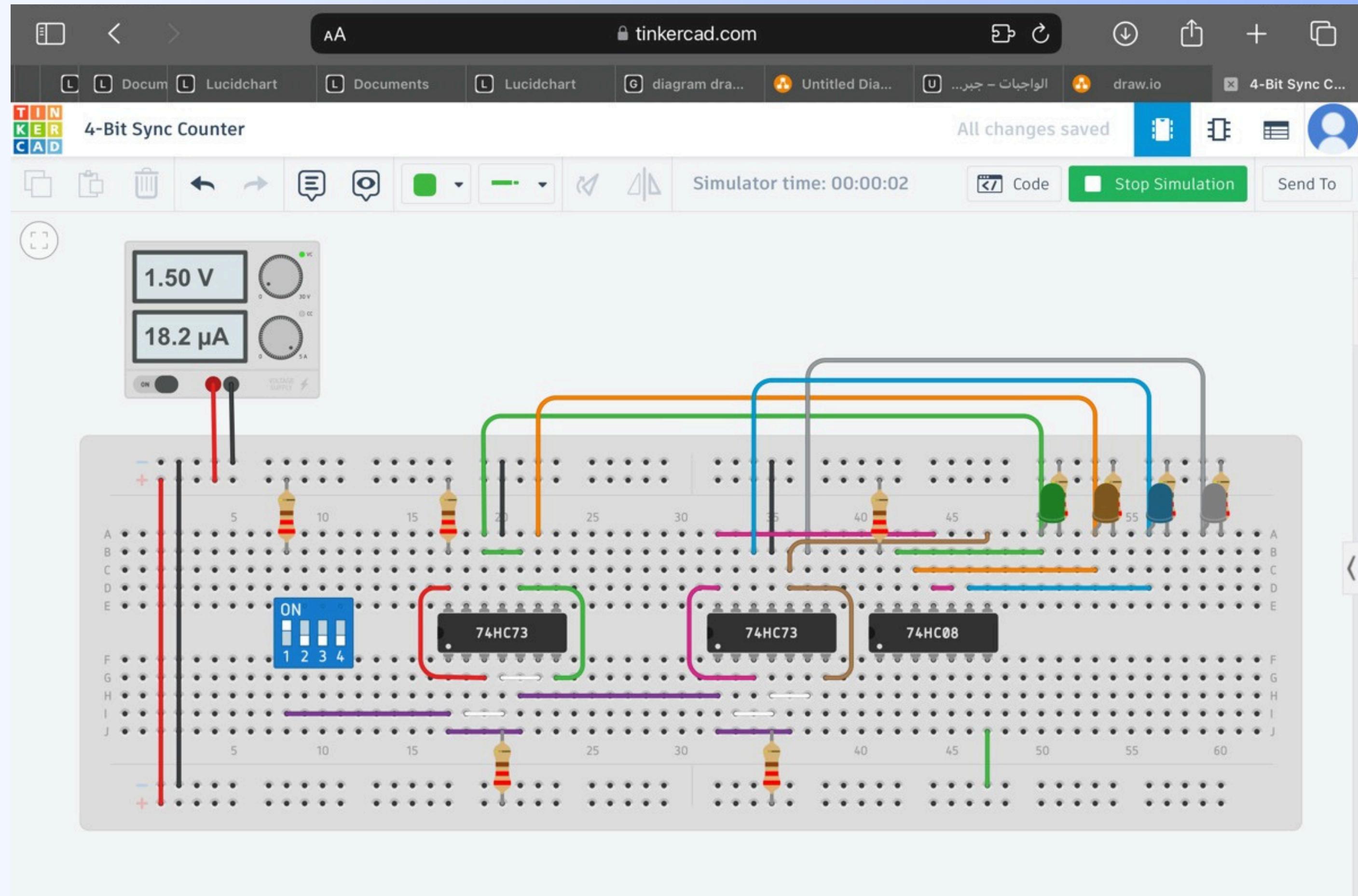


3. Implementation

A T flip-flop was implemented using a dual JK flip-flop IC by setting J, K both to T. Quad and IC 7408 was used to get the calculated T values. Reset was disabled by setting it to high. A DIP switch was used to feed the clock signal.



4. Simulation





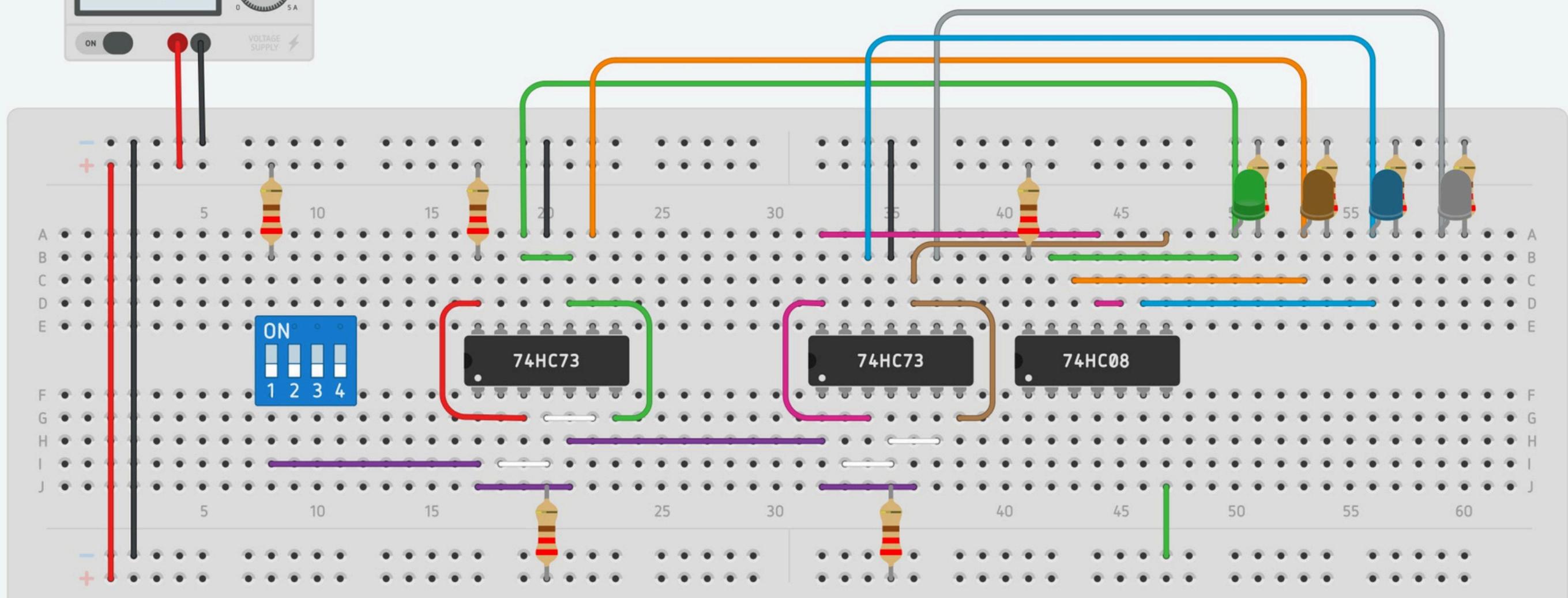
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4-Bit Sync Counter

All changes saved

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4-Bit Sync Counter

All changes saved

Simulator time: 00:00:15

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1.50 V
18.3 μ A

VOLTAGE SUPPLY

ON

1.50 V
18.3 μ A

ON

1 2 3 4

74HC73
74HC73
74HC08

The circuit diagram shows a 4-bit synchronous counter setup. A 1.50V DC voltage source is connected to the breadboard. Address inputs A through J are connected to the inputs of a 74HC14 decoder. The decoder's outputs (pins 1, 2, 3, 4) are connected to the enable pins (CE) of two 74HC73 flip-flops. The 74HC73 flip-flops have their clock inputs (CLK) connected to a 74HC08 chip. The 74HC08 chip also receives address inputs A through J. The 74HC08 chip has four outputs, which are connected to the clock inputs of the 74HC73 flip-flops. The 74HC73 flip-flops have their Q outputs connected to a breadboard output bus. The breadboard has two rows of 30 columns each, with columns numbered 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, and 60. The output bus is labeled with letters A through J above the columns.

4-Bit Sync Counter

All changes saved

VOLTAGE SUPPLY
1.50 V
21.1 μ A

Simulator time: 00:00:19

Code Stop Simulation Send To

The circuit diagram illustrates a 4-bit synchronous counter design using discrete logic components on a breadboard. The power supply is set to 1.50V, providing 21.1 μ A of current. The circuit is color-coded with red, green, orange, blue, and purple wires. Key components include a 74HC73 flip-flop, a 74HC08 AND gate, and an ON Semiconductor 4N27 optoisolator. The circuit is designed to take a 1.50V supply and provide 21.1 μ A of current.

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4-Bit Sync Counter

All changes saved

Simulator time: 00:00:23

Code Stop Simulation Send To

1.50 V
18.3 μ A

VOLTAGE SUPPLY

ON

1.50 V
18.3 μ A

VC 30V CC 5A

ON

74HC73 74HC73 74HC08

1 2 3 4

5 10 15 20 25 30 35 40 45 50 55 60

A B C D E F G H I J

This screenshot shows a digital circuit simulation on Tinkercad. The circuit is a 4-bit synchronous counter. It consists of three 74HC73 flip-flops connected in series, followed by a 74HC08 4-to-1 multiplexer. The circuit is powered by a 1.50 V DC voltage source. The inputs are labeled A through J, and the outputs are labeled 5 through 60. The connections are color-coded: red for power, black for ground, and various colors for signal lines. The circuit is currently active, as indicated by the simulator time of 00:00:23.

4-Bit Sync Counter

All changes saved

VOLTAGE SUPPLY: 1.50 V, 20.2 μ A

Simulator time: 00:00:27

Code Stop Simulation Send To

The circuit diagram illustrates a 4-bit sync counter design using integrated circuits (ICs) and discrete components on a breadboard. The power source provides 1.50 V and 20.2 μ A. The circuit consists of three main sections: an enable section, a clock section, and a data section.

- Enable Section:** An "ON" switch (labeled 1, 2, 3, 4) is connected to pin 1 of a 74HC73 flip-flop. Pin 2 of the 74HC73 is connected to ground through a 10kΩ resistor.
- Clock Section:** A 74HC73 flip-flop is configured as a divide-by-2 counter. Its clock input (pin 13) is connected to its output (pin 12). The clock input is also connected to the output of a 74HC08 logic gate (pin 13).
- Data Section:** The 74HC73 outputs (pins 11, 10, 9, 8) are connected to the data inputs (pins 1, 2, 3, 4) of a second 74HC73 flip-flop via a 74HC08 logic gate. The 74HC08 has four AND gates; its outputs are connected to pins 11, 10, 9, and 8 of the second 74HC73 respectively. The 74HC08's inputs are connected to the outputs of the first 74HC73 (pins 12, 13, 14, 15) and the enable switch (pin 1).

Resistors and capacitors are used throughout the circuit to provide biasing and filtering. The breadboard grid is visible, with component pins numbered from 5 to 60 along the top and bottom edges.



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4-Bit Sync Counter

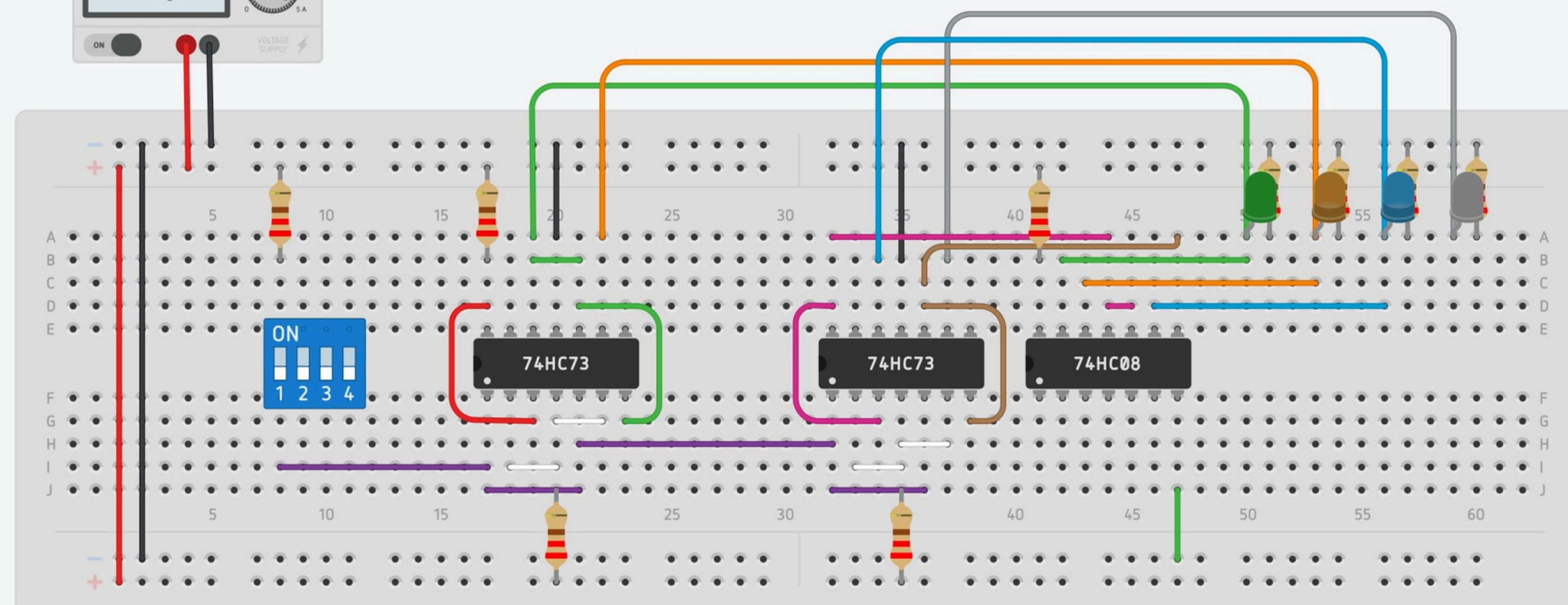
All changes saved



Simulator time: 00:00:41



Send To



4-Bit Sync Counter

All changes saved

Simulator time: 00:00:54

Code Stop Simulation Send To

1.50 V
24.2 μ A

ON VOLTAGE SUPPLY

74HC73
74HC73
74HC08

ON

1 2 3 4



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4-Bit Sync Counter

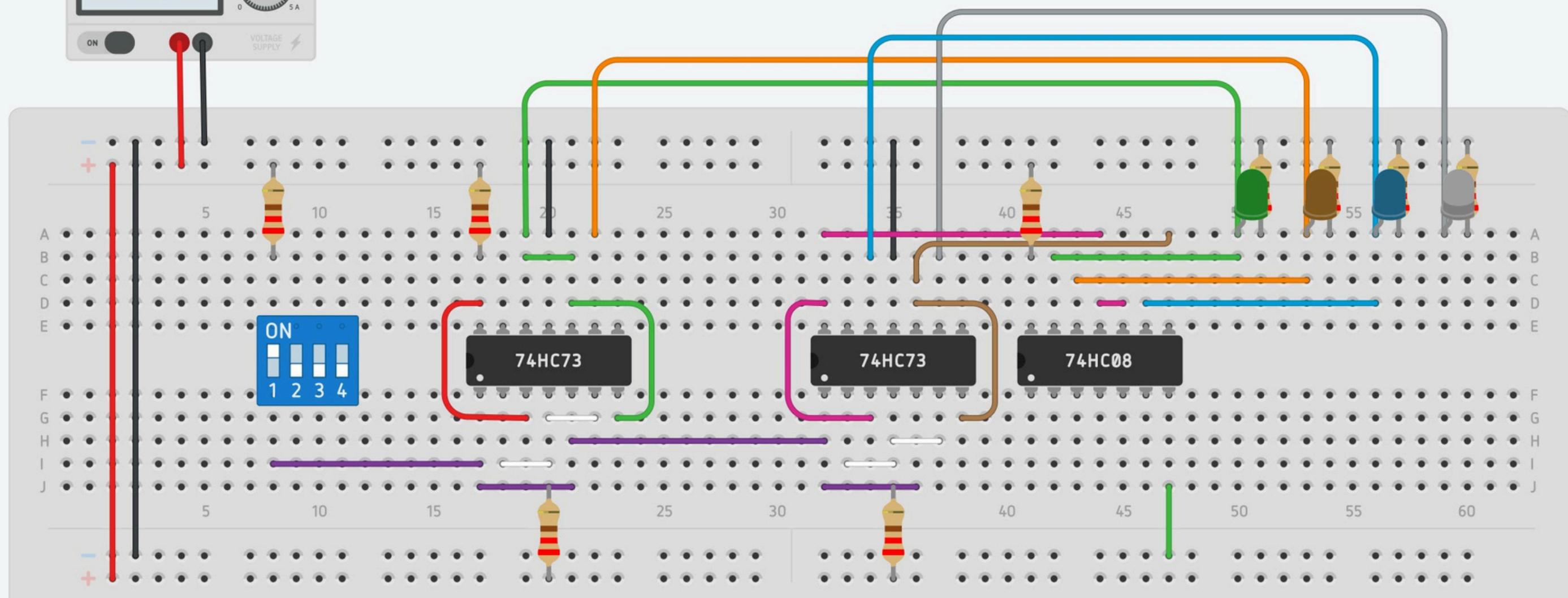
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Simulator time: 00:00:57



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4-Bit Sync Counter All changes saved

VOLTAGE SUPPLY: 1.50 V, 21.1 μ A

Simulator time: 00:01:07

Code Stop Simulation Send To

The circuit diagram illustrates a 4-bit synchronous counter setup. A 1.50V power source is connected to the breadboard. An enable switch (labeled 'ON') is connected to pin 14 of the first 74HC73 IC. The clock input (pin 13) of the first 74HC73 is connected to pin 14 of the second 74HC73 via a green wire. The clock input of the second 74HC73 is connected to pin 13 of the 74HC08 IC. The 74HC08 IC has four outputs, each connected to one of the four data inputs (pins 1, 2, 3, 4) of the first 74HC73 IC. The 74HC73 ICs have three-state outputs (pin 15) connected to pins 1, 2, 3, and 4 of the 74HC08 IC. The 74HC08 IC's outputs are labeled A through E. The circuit also features several resistors and capacitors for biasing and filtering.

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4-Bit Sync Counter

VOLTAGE SUPPLY: 1.50 V, 20.5 μ A

ON: 1 2 3 4

74HC73, 74HC73, 74HC08

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Voltage Supply: 1.50 V, Current: 23.3 μ A

Simulator time: 00:01:23 Code Stop Simulation Send To

4-Bit Sync Counter

The circuit diagram illustrates a 4-bit synchronous counter design using integrated circuits (ICs) and discrete components on a breadboard layout. A voltage source of 1.50 V and a current of 23.3 μ A is connected to the breadboard. An enable switch labeled 'ON' is used to control the clock inputs of the first two flip-flops. The circuit consists of three 74HC73 flip-flops and one 74HC08 logic gate. The connections are color-coded: red, green, orange, and blue. The breadboard has columns labeled 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, and 60 across the top and bottom. Rows are labeled A through J on the left and F through J on the right.



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4-Bit Sync Counter

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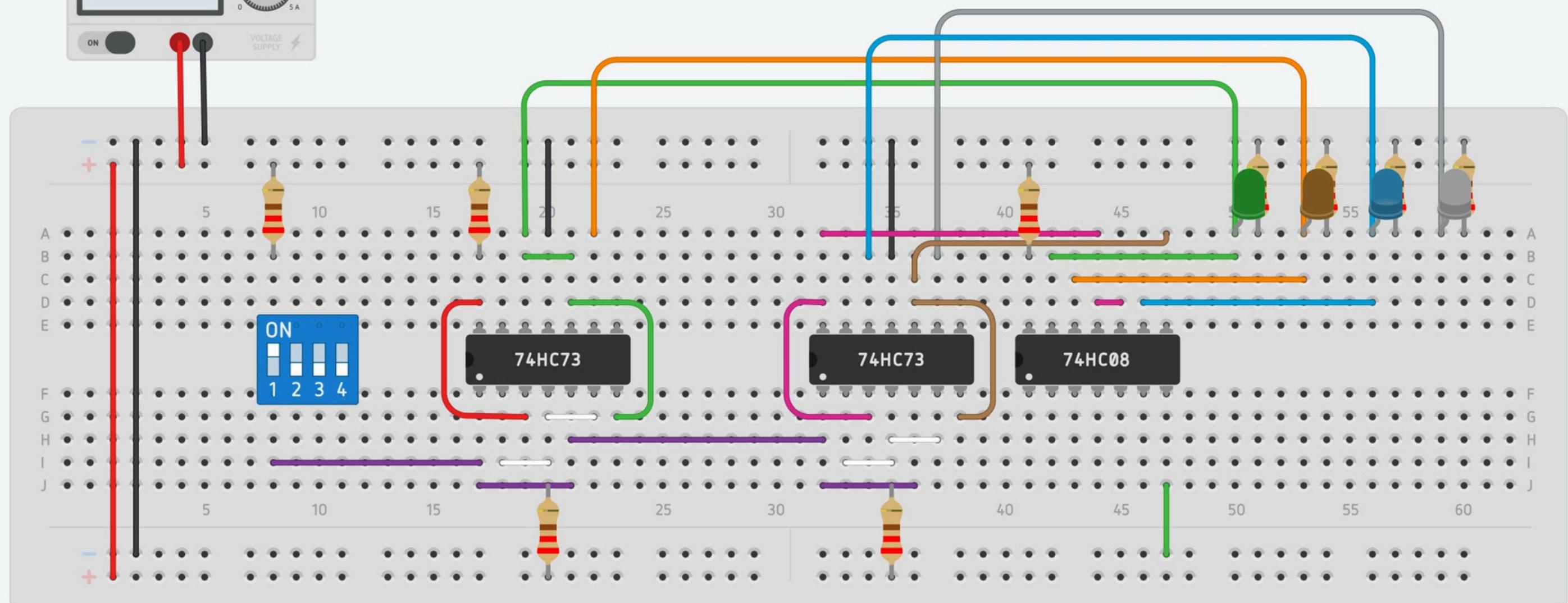


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4-Bit Sync Counter

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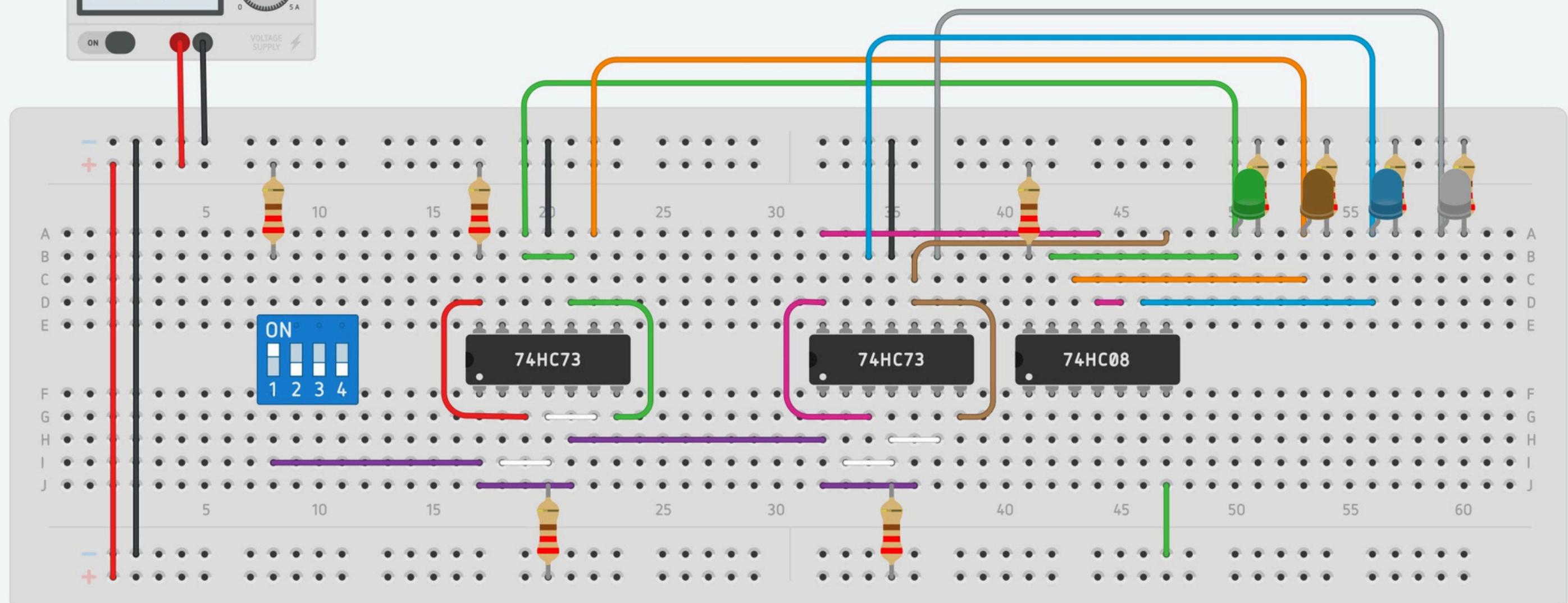


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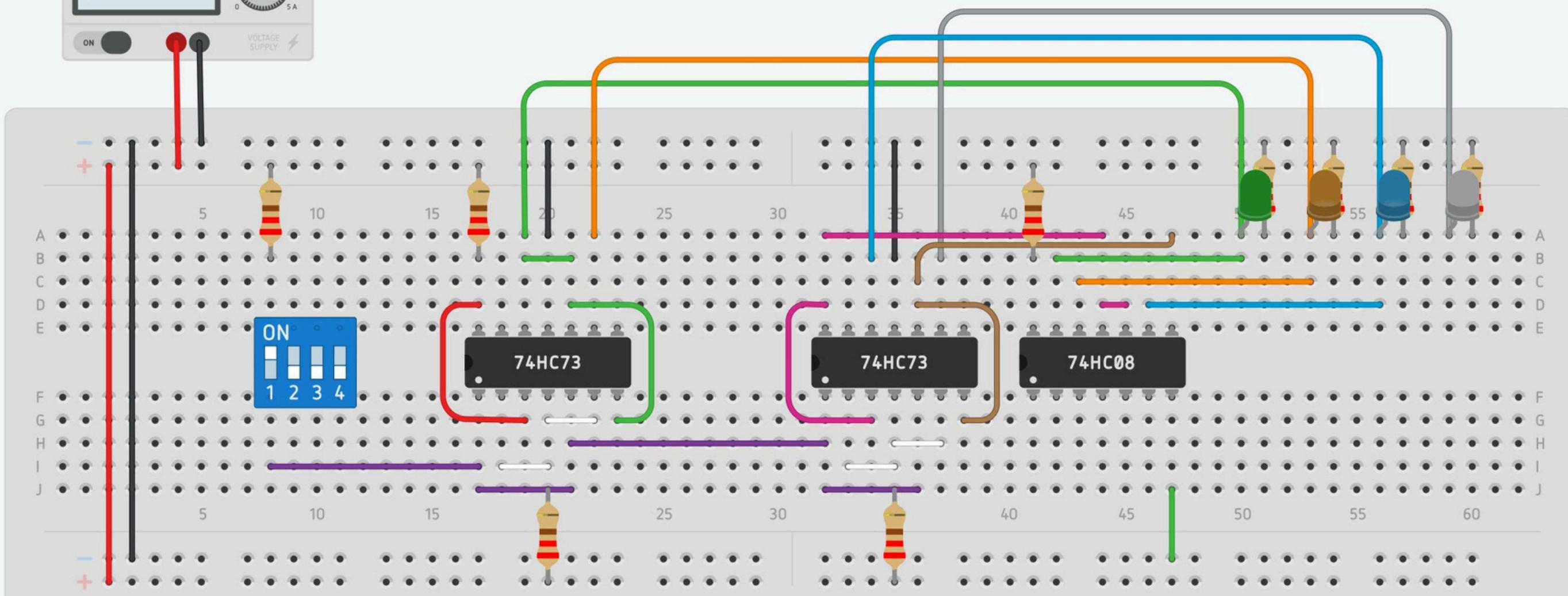


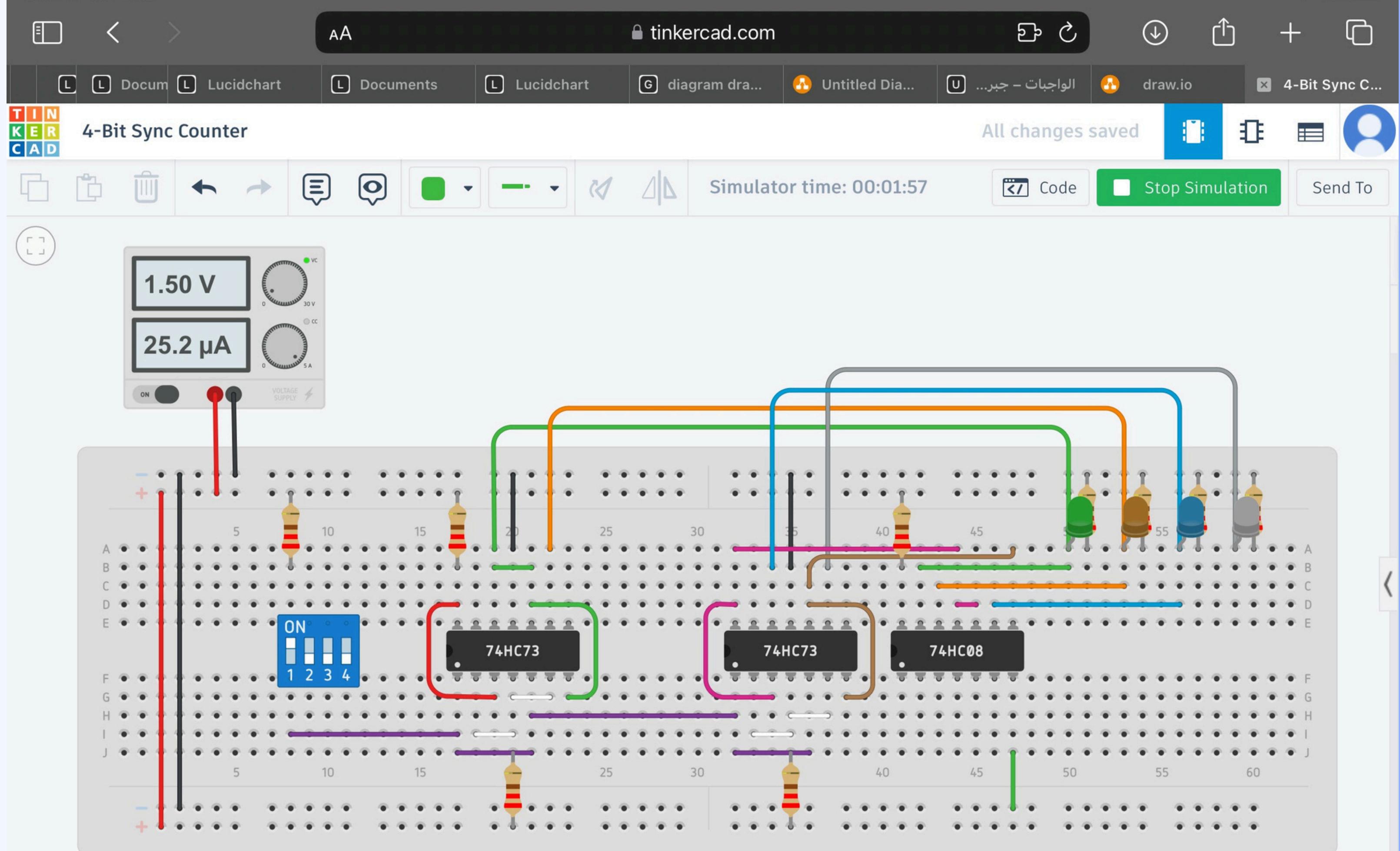
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4-Bit Sync Counter

All changes saved

Simulator time: 00:02:05

Voltage Supply: 1.50 V, 18.2 μ A

Code Stop Simulation Send To

The circuit diagram illustrates a 4-bit synchronous counter design using integrated circuits (ICs) and discrete components on a breadboard. A 1.50 V power source is connected to the breadboard's power rail. A voltage supply component shows 18.2 μ A current. An enable switch (labeled 'ON') is connected to pin 1 of the first 74HC73 flip-flop. The 74HC73 ICs are configured as follows:

- The first 74HC73 (pins 1-14) has its clock input (pin 11) connected to ground through a 10kΩ resistor.
- The second 74HC73 (pins 15-28) has its clock input (pin 21) connected to the output Q of the first flip-flop (pin 12).
- The third 74HC73 (pins 31-44) has its clock input (pin 31) connected to the output Q of the second flip-flop (pin 22).
- The 74HC08 logic gate (pins 45-57) receives its inputs from the outputs of the second and third flip-flops (pins 22 and 32).

Resistors (10kΩ) are placed between the clock inputs of the second and third flip-flops and ground. Various other resistors and capacitors are used throughout the circuit for biasing and timing purposes. The breadboard grid is labeled with letters A-J and numbers 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, and 60.

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Leen Kharraz	2412099	Q1
Wateen Alharthy	2413523	Q2
Sarah Alfowzan	2410916	Q3
All	All	Circuit

