

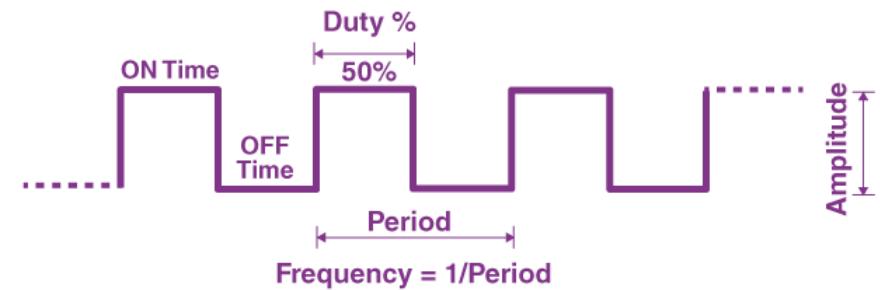
Adjustable PWM Modulator

Yunfan Zhang, Yi Tong



Project Information Review

- **Title:** Adjustable PWM Modulator Chip
- **Team Members:** Yi Tong, Yunfan Zhang
- **Objective:** Build a frequency-adjustable and duty-cycle-adjustable PWM modulator
- **Abstract:** In industrial applications, PWM waveforms are indispensable for tasks such as motor control, audio amplification, power regulator, and signal encoding. Our project integrates various schematics (counters, D Flip-flop, adder, comparison circuit) to achieve this PWM generator with low power consumption.



One of expected PWM waveforms^[1]

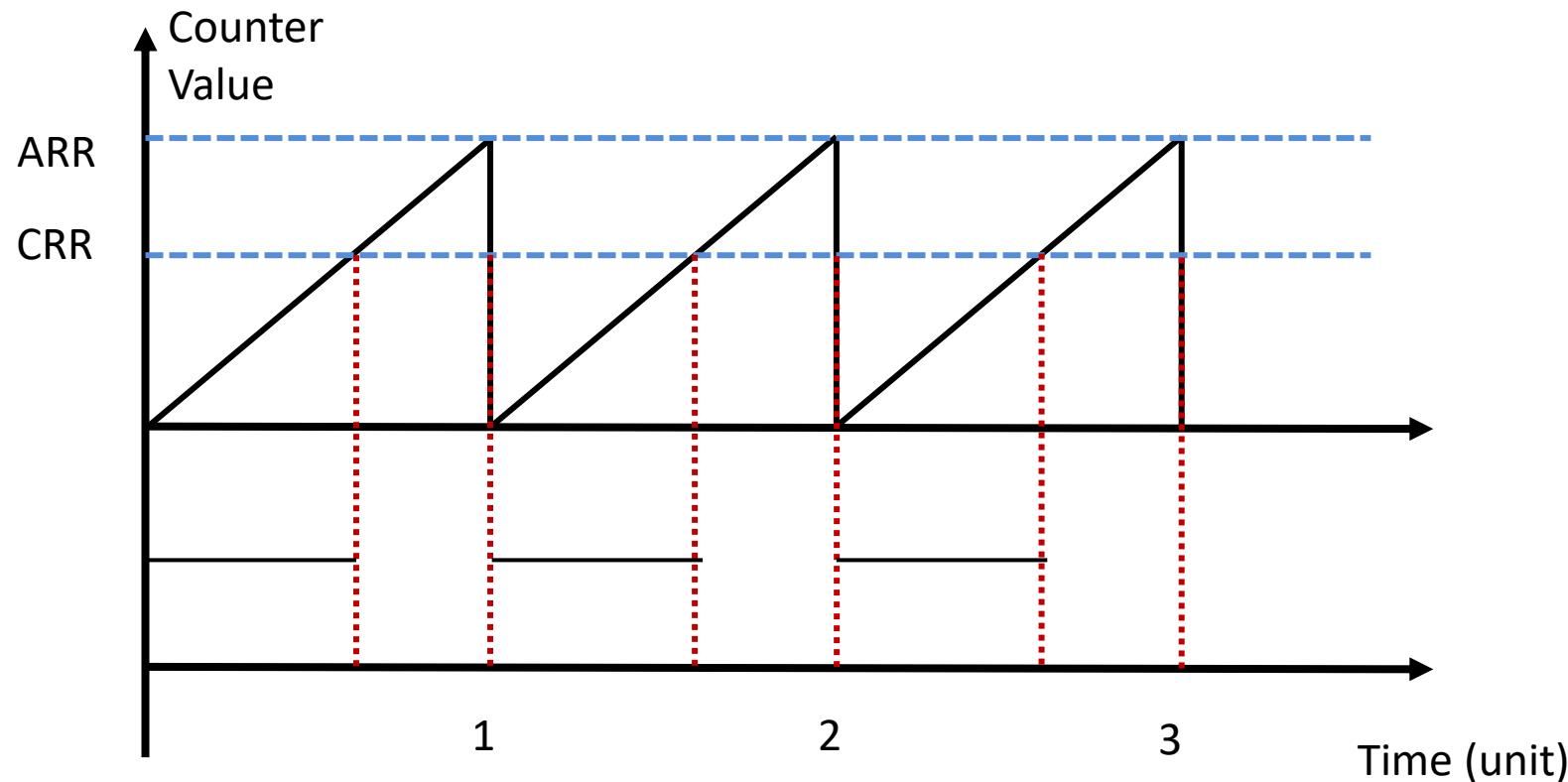
[1] <https://byjus.com/physics/pulse-width-modulation/>



- **Principle of the Circuit**
- **General Structure**
- **Components Design**
- **Testbench and Simulation**
- **Summary**



Principle of the PWM Generator Review



Vary ARR to vary period

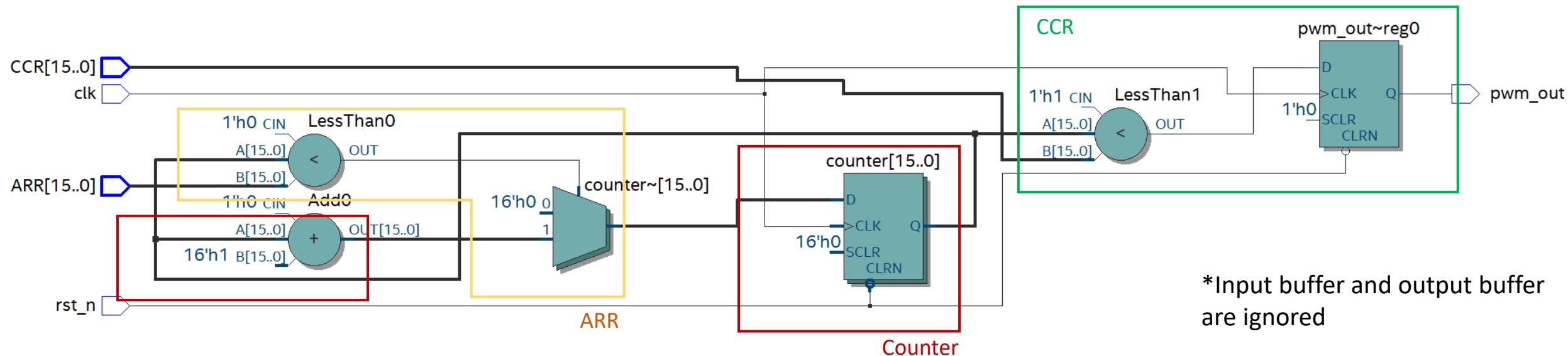
$$f(counter) = \begin{cases} 1 & \text{counter} < CRR \\ 0 & CRR < \text{counter} < ARR \end{cases}$$

ARR(auto-reload register): Threshold to maximum 'voltage' (value)

CRR(capture/compare register): Threshold to triggered voltage



Logic Diagram Review



Input:

- **CCR (16-bit)**: capture/compare register -> Adjust the duty cycle
- **ARR (16-bit)**: auto-reload register -> Adjust the frequency
- **Rst_n**: reset signal
- **Clk**: clock signal

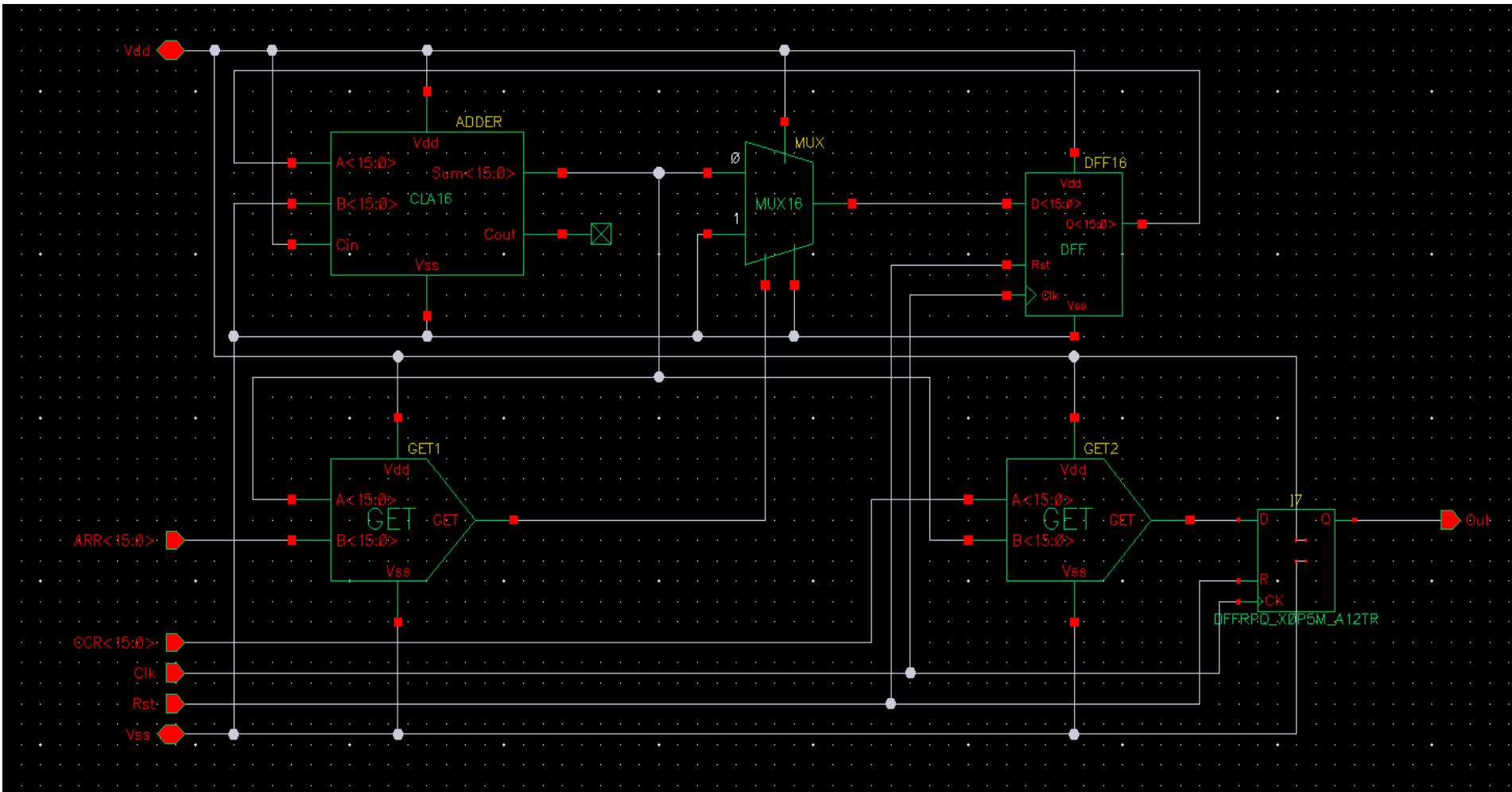
Output:

- **Pwm_out**: output signal

Internal:

- **Counter (16-bit)**

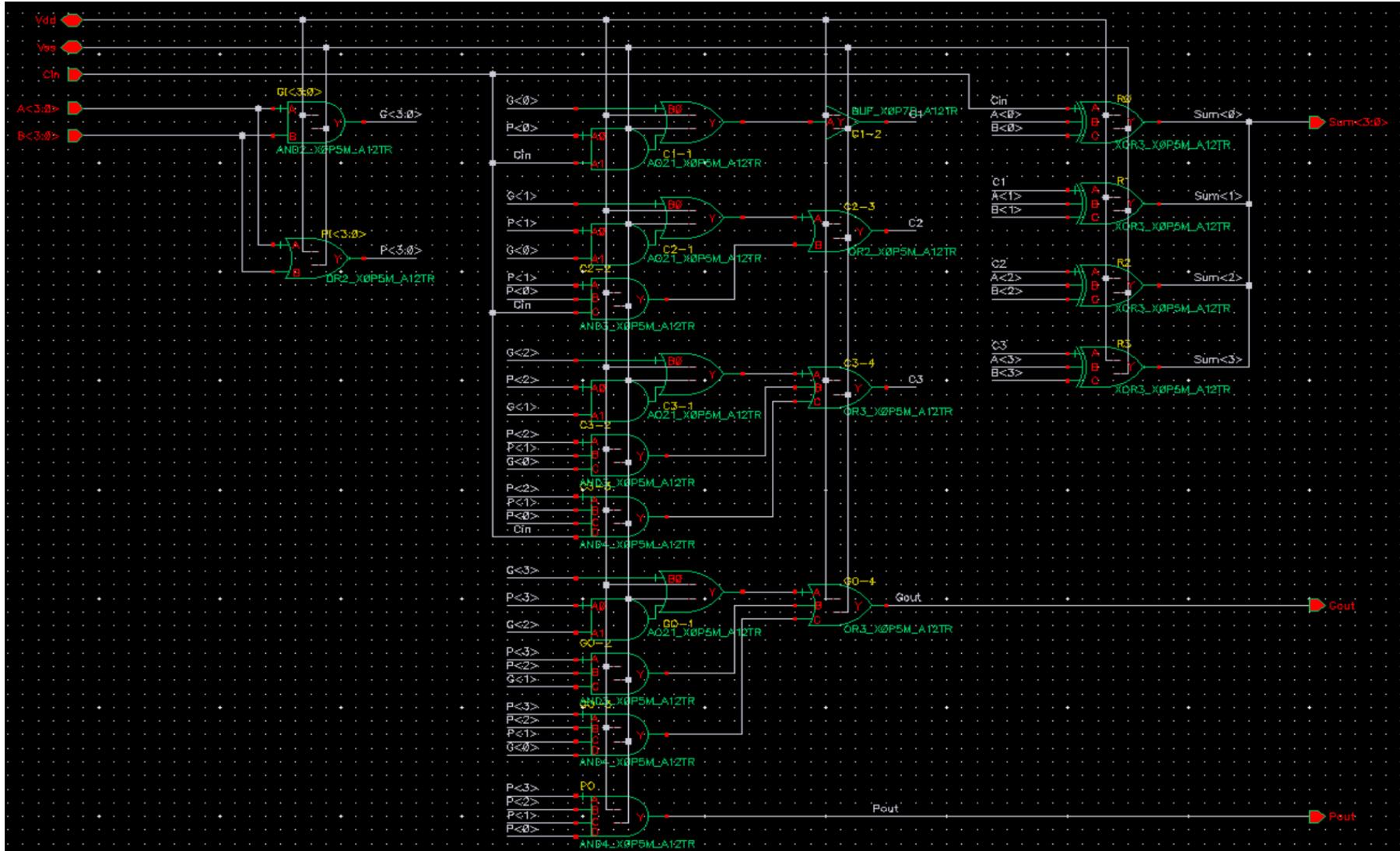
General Structure



Contains:

- One 16-bit Carry-lookahead Adder
- One 16-bit 2-to-1 Mux
- Two compare unit: Greater or equal than (same as less than)
- One 16-bit D-flip flop
- One 1-bit Register

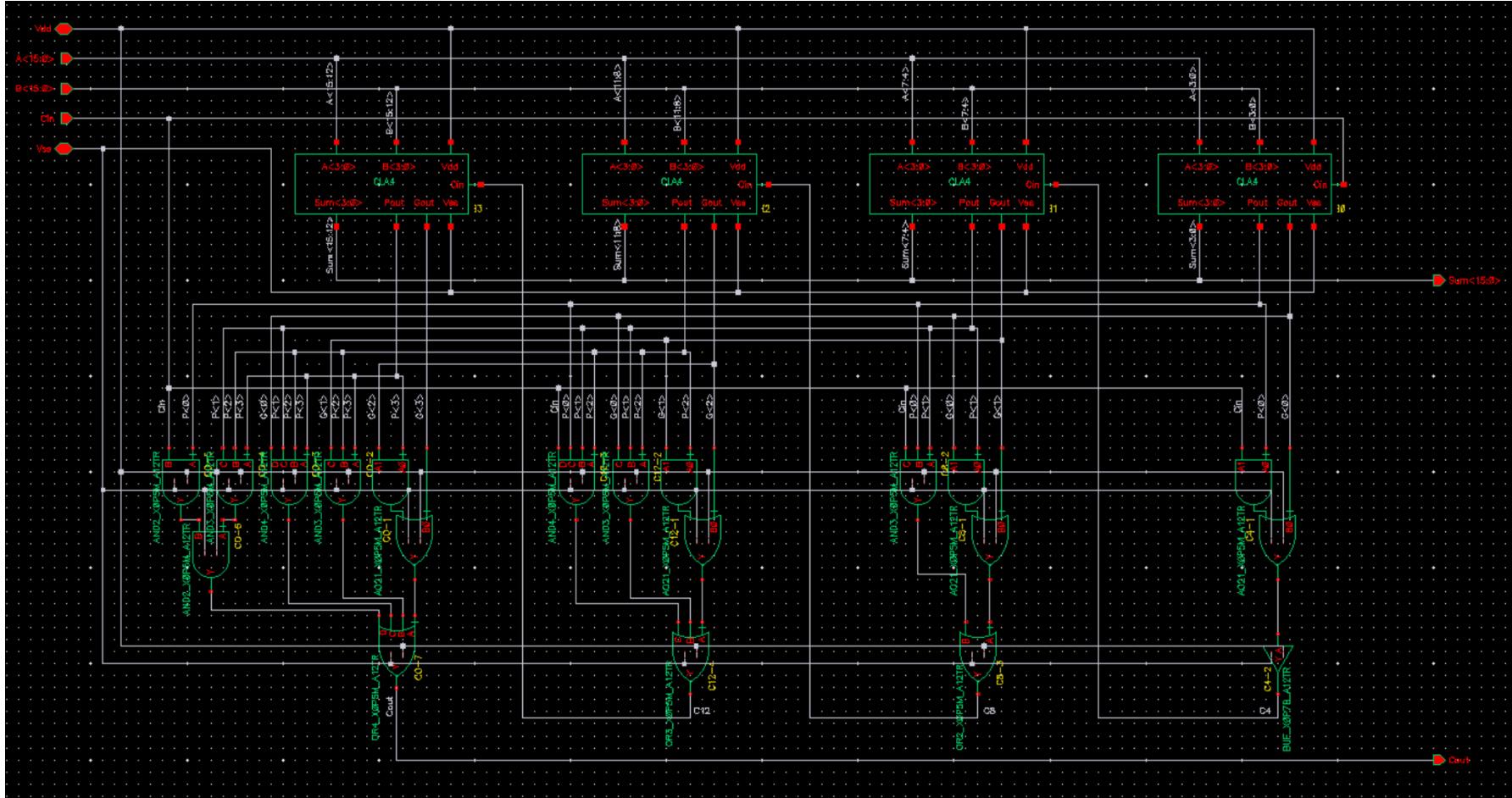
16-bit Carry-Lookahead Adder – First Level (CLA4)



Contains:

- Left-hand side:
Calculating P and G
- Middle Part:
Calculating carry bit
- Right-hand side:
Calculating Sum

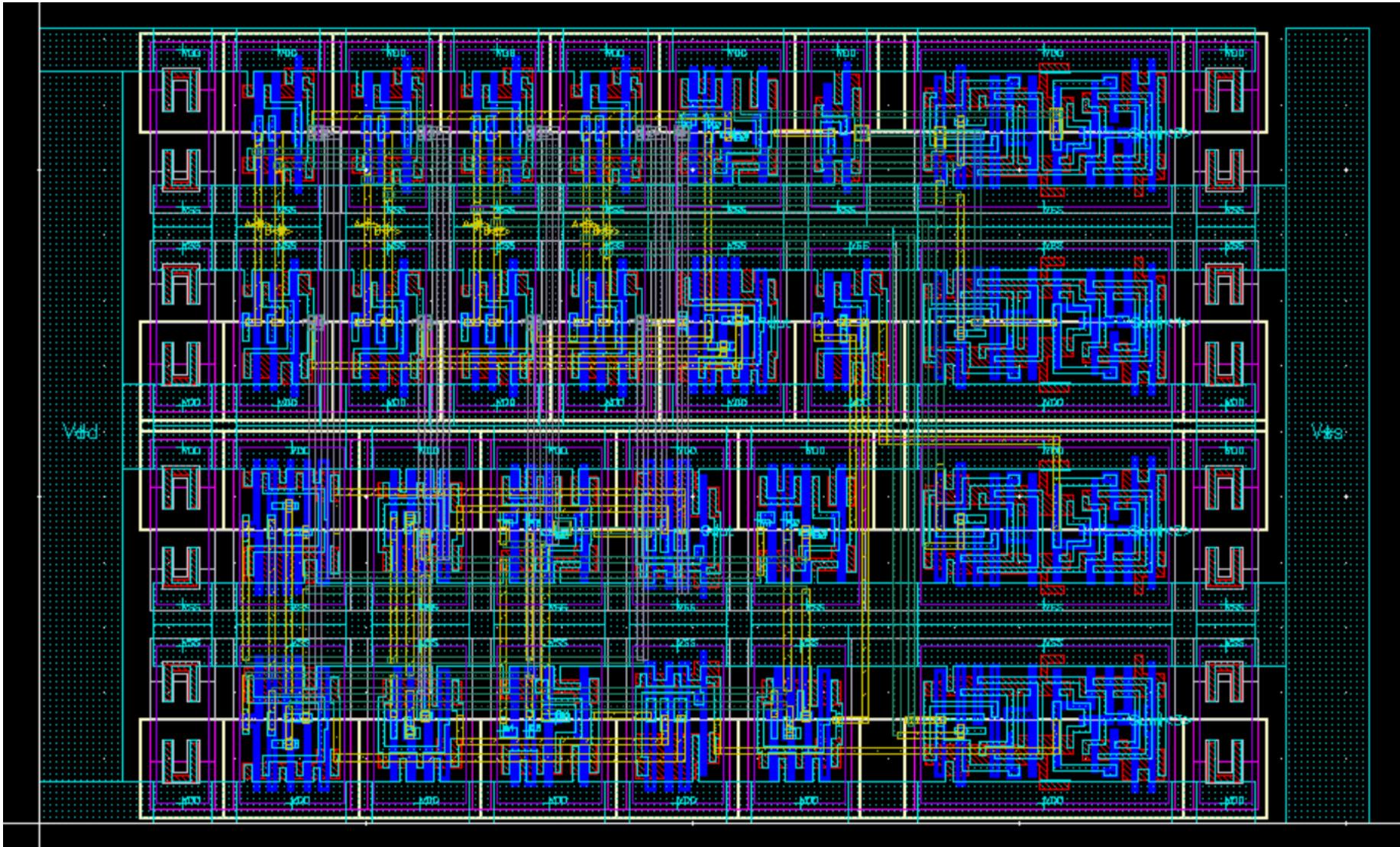
16-bit Carry-Lookahead Adder – Full Level (CLA16)



Contains:

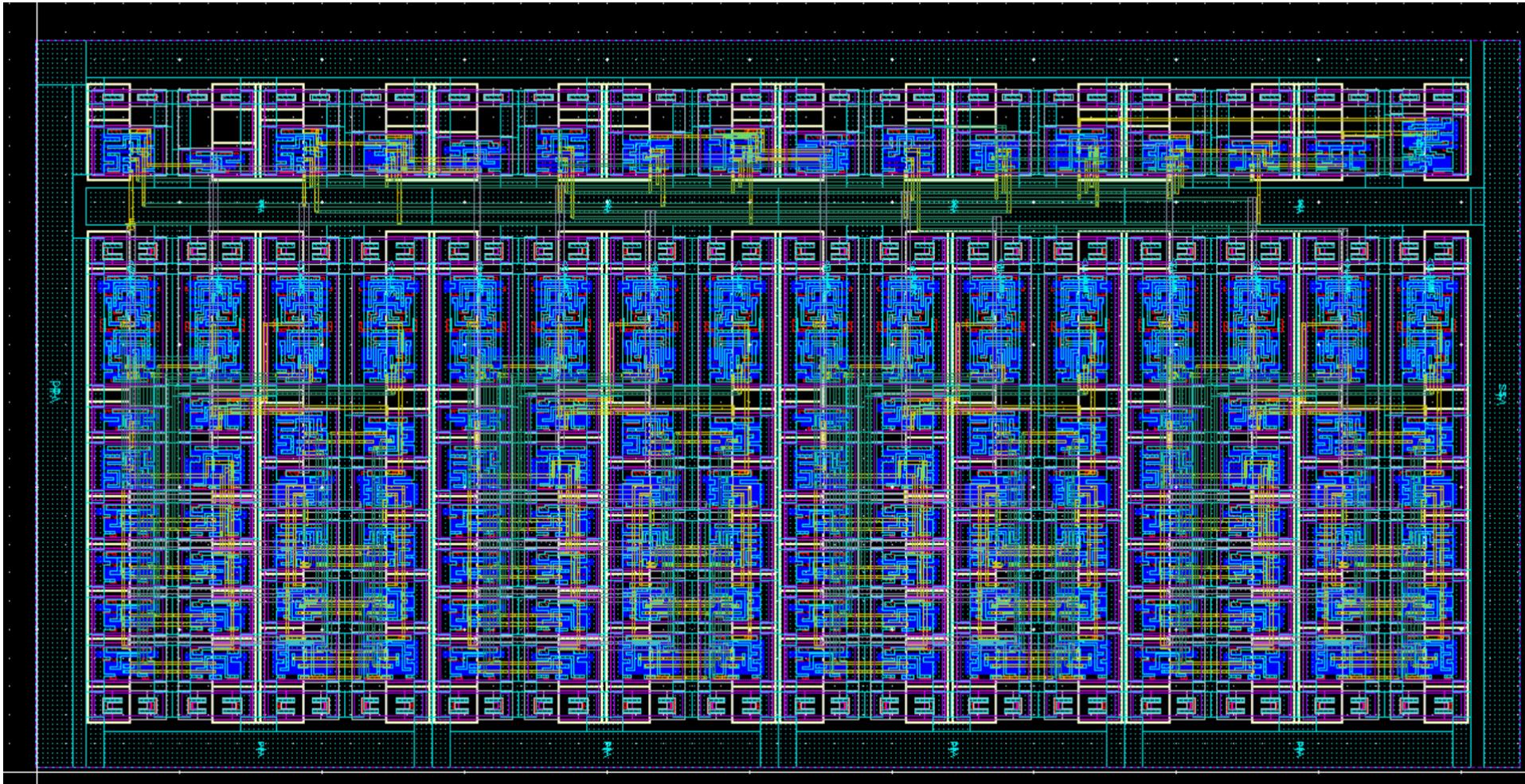
- Second-level
- Four 4-bit Carry-lookahead Adder
- Seven And-Or gates: To earlier propagate carrier to be the C_{in} of following level.
- Three Xor gates and one buffer: To calculate the 4-bit Sum.

16-bit Carry-Lookahead Adder – First Level (CLA4) layout



- Each row is one bit calculation (total 4-bit)
- Mosaic layout
- DRC & LVS clean

16-bit Carry-Lookahead Adder – Full layout



- Show in horizontal
- Each column is one bit (total 16-bit)
- Mosaic layout
- DRC & LVS clean (only density error)

16-bit Carry-Lookahead Adder – Layout DRC, LVS check for CLA4 and CLA16

CLA4:

Calibre - RVE v2020.4_34.17 : CLA4.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All No Results Found

Check / Cell	Result
Check DENSITY_PRINT_FILES	0

```
DD.DN.2L,density
DD.DN.2H_10,density
DD.DN.2H_CORE,density
DD.DN.3L,density
DD.DN.3H,density
DD.DN.3H_CORE,density
P0.DN.2,density
P0.DN.3,density
M1.DN.1L,density
M1.DN.1L,density
M1.DN.2,density
M1.DN.4,density
M2.DN.1L,density
M2.DN.1H,density
M2.DN.2,density
M2.DN.4,density
M3.DN.1L,density
M3.DN.1H,density
```

Check DENSITY_PRINT_FILES

File View Highlight Tools Window Setup Help

Filter: Show All CLA16, 8 Results (in 8 of 11 Checks)

Check / Cell	Result
Check M2.DN.1L	1
Check M3.DN.1L	1
Check M4.DN.1L	1
Check M5.DN.1L	1
Check M6.DN.1L	1
Check M7.DN.1L	1
...	...

```
M2.DN.1L [ @ M2 local density must be >= 0.1 range over 75 um x 75 um step 37.5 um
M2_CHECK < M2.DN.1L M2DN1L_EXC
DTP_CHECK CHIP CHECK < M2.DN.1L WINDOW M2.DN.1L_W STEP M2.DN.1L_S INSIDE OF LAYER CHIPx BACKUP
[ AREA(M2_CHECK) / AREA(CHIP_CHECK) ]
F = WITH WIDTH (ERR_WIN NOT M2DN1L_EXC) >= M2.DN.1L_E
DENSITY F M2_CHECK CHIP CHECK < M2.DN.1L WINDOW M2.DN.1L_W STEP M2.DN.1L_S INSIDE OF LAYER CHIPx BACKUP PRINT M2.DN.1L,density
[ IAREA(F)+AREA(M2_CHECK)/AREA(CHIP_CHECK) ]
```

CLA16:

LVS Report File - CLA4.lvs.rpt

File Edit Options Windows

```
#####
## CALIBRE SYSTEM
##
## LVS REPORT
##
```

REPORT FILE NAME: CLA4.lvs.report
LAYOUT NAME: /home/yz845/workspace/CL4.sp ('CL4')
SOURCE NAME: /home/yz845/workspace/CL4.src.net ('CL4')
RULE FILE: /home/yz845/workspace/_calibre.lvs_
CREATION TIME: Fri Dec 15 02:04:55 2023
CURRENT DIRECTORY: /home/yz845/workspace
USER NAME: yz845
CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS



CELL SUMMARY

Result	Layout	Source
CORRECT	CLA4	CLA4

Edit Row 8 Col E

File Edit Options Windows

```
#####
## CALIBRE SYSTEM
##
## LVS REPORT
##
```

REPORT FILE NAME: CLA16_lvs.rpt
LAYOUT NAME: /home/yz845/workspace/CL4.sp ('CL4')
SOURCE NAME: /home/yz845/workspace/CL4.src.net ('CL4')
RULE FILE: /home/yz845/workspace/_calibre.lvs_
CREATION TIME: Fri Dec 15 02:11:05 2023
CURRENT DIRECTORY: /home/yz845/workspace
USER NAME: yz845
CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

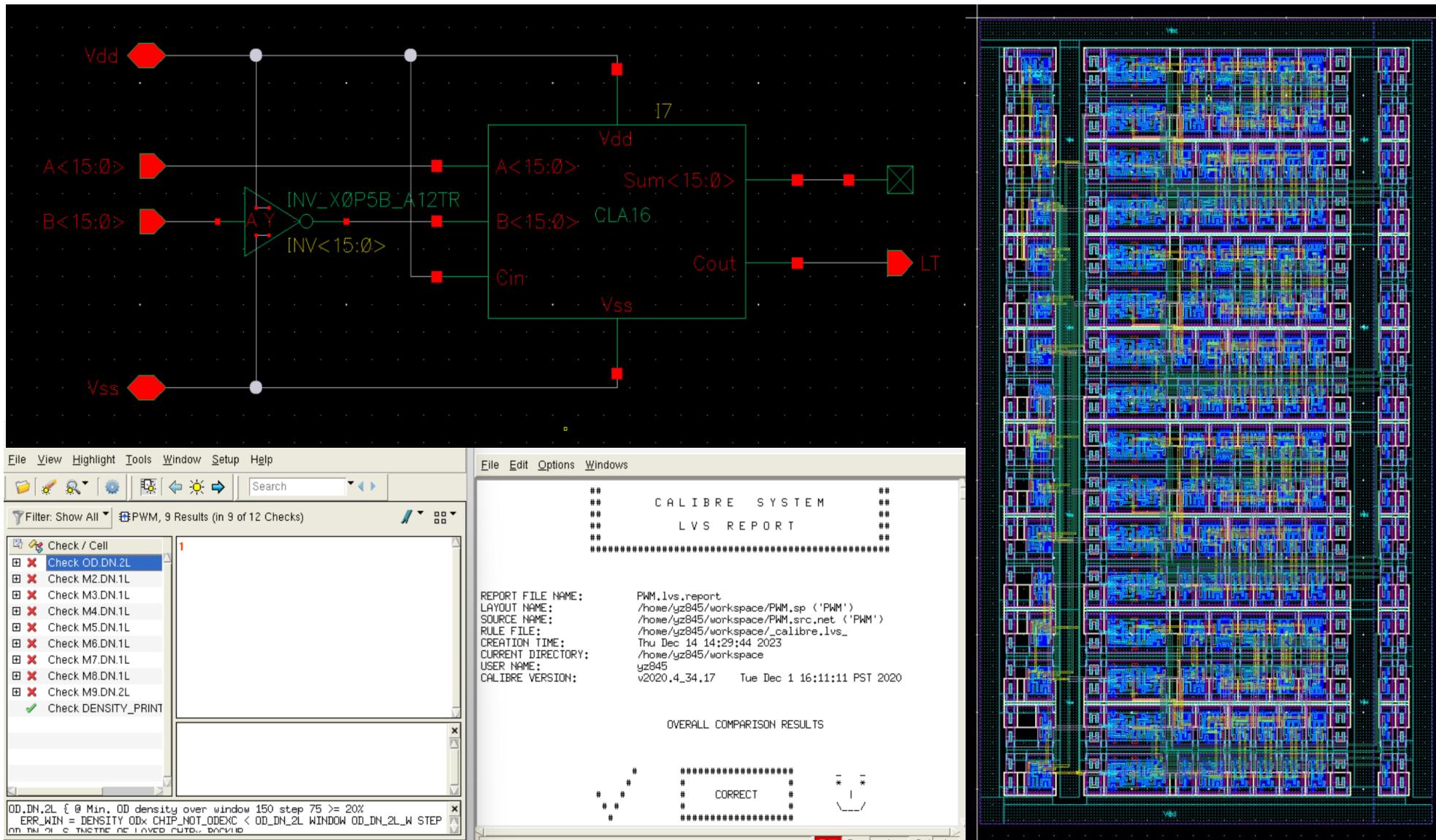
OVERALL COMPARISON RESULTS



CELL SUMMARY

Result	Layout	Source
CORRECT	CLA16	CLA16

Greater or Equal Than

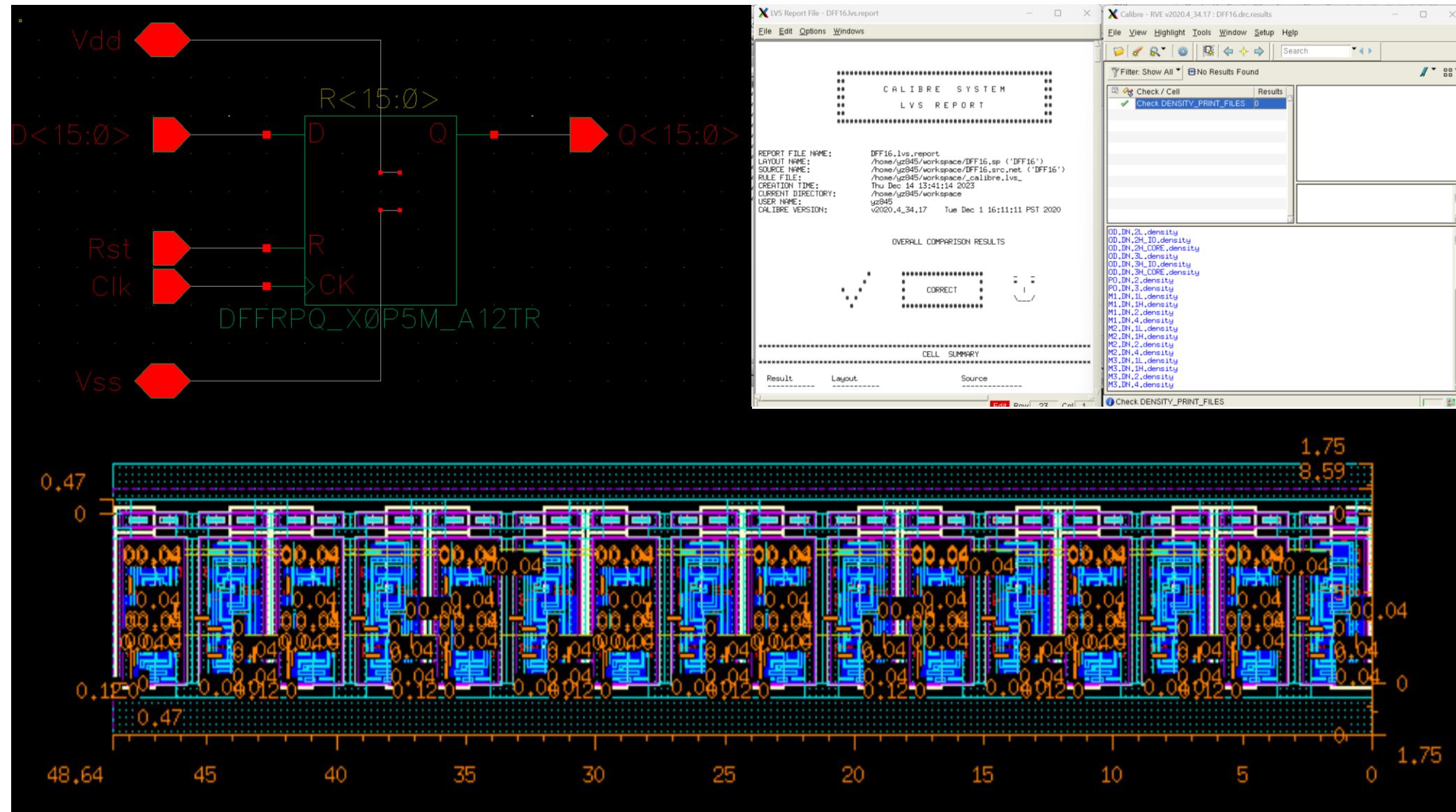


Principle:

For unsigned number:

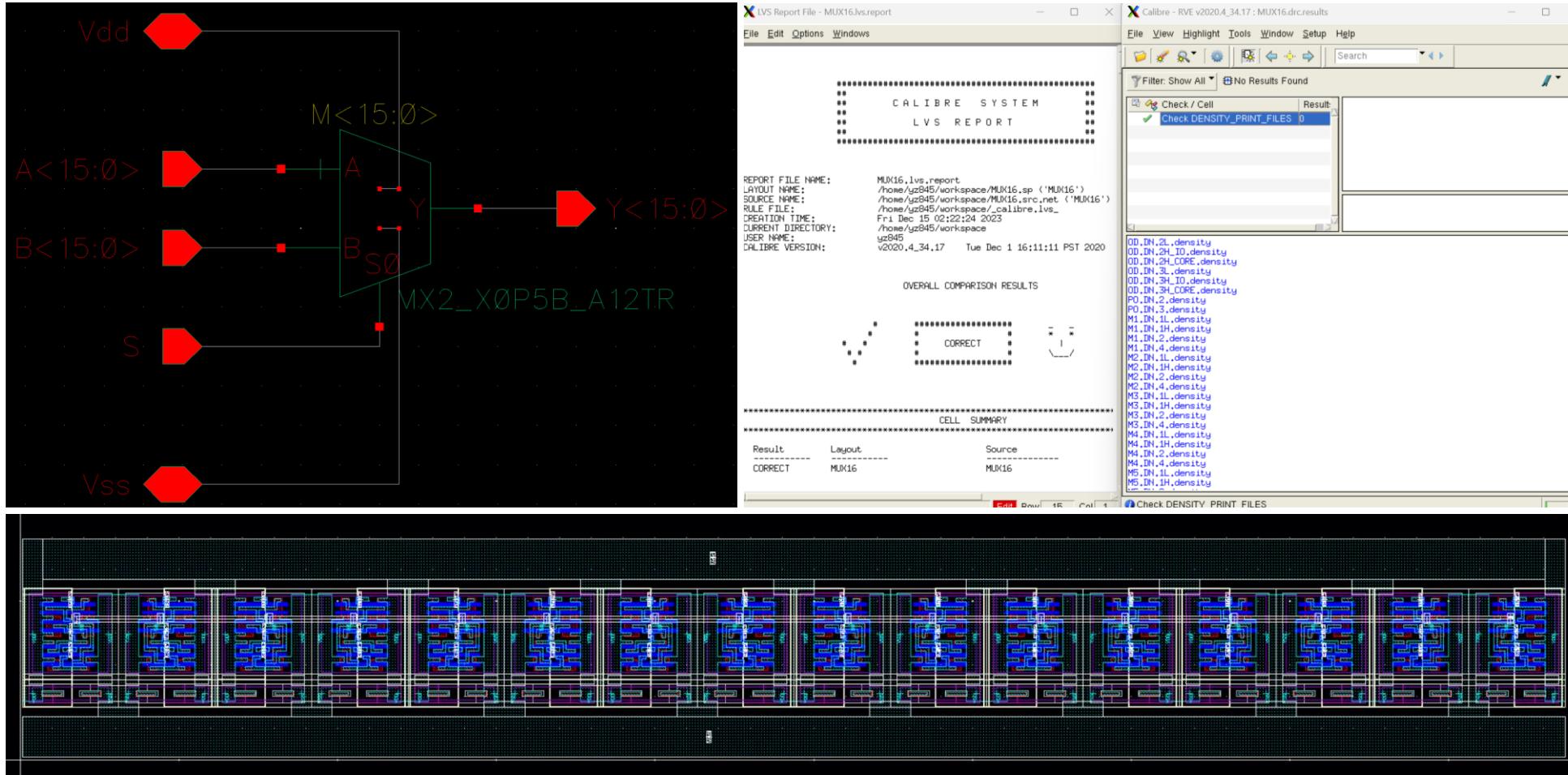
- If $A - B$ have $Cout = 1$, indicating $A \geq B$
- Mosaic layout
- DRC & LVS clean (only density error)

16-bit D-Flipflop (Register)



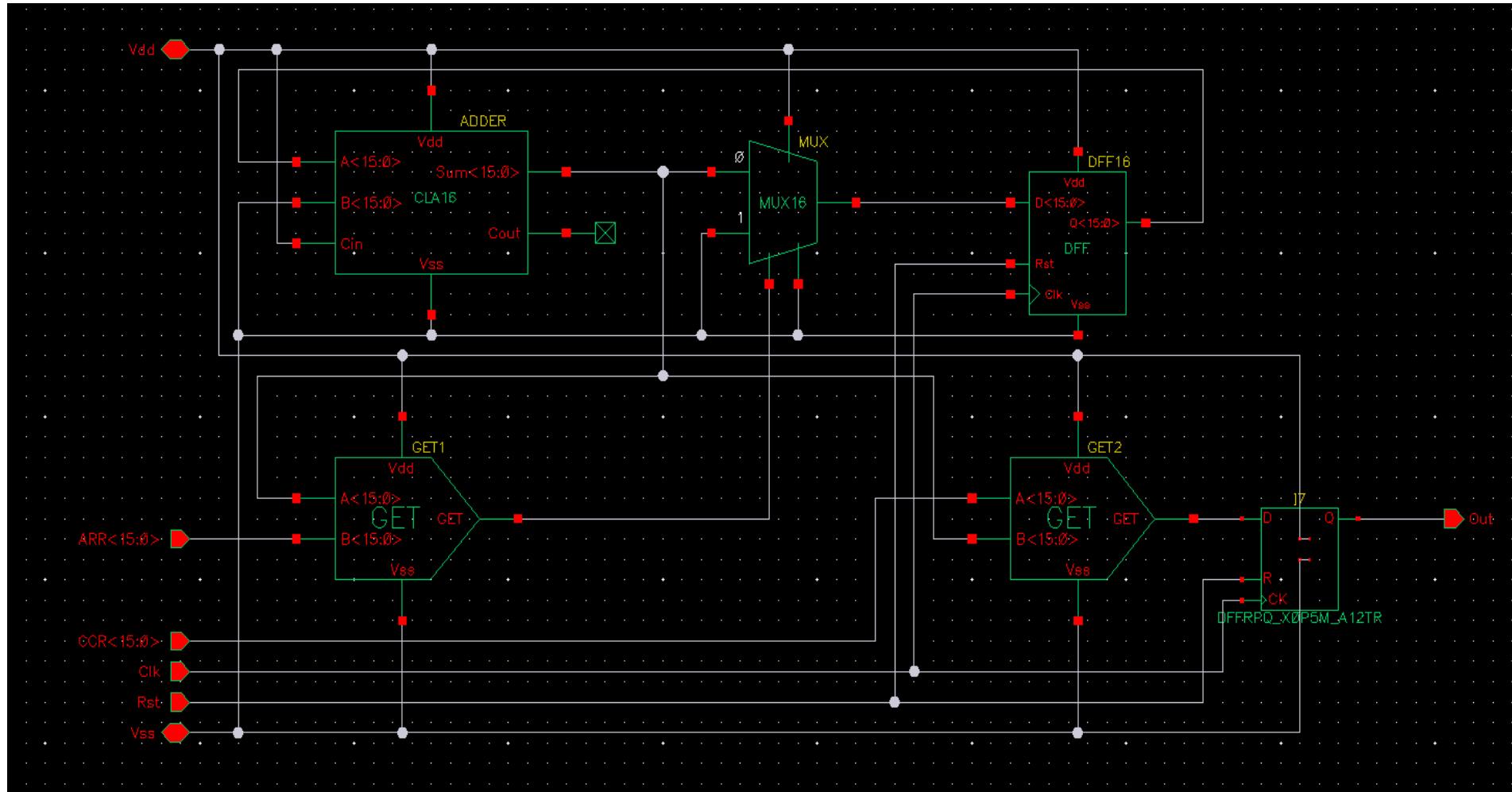
- Show in horizontal
- Each column is one bit (total 16-bit)
- Mosaic layout
- DRC & LVS clean

16-bit 2-to-1 Mux



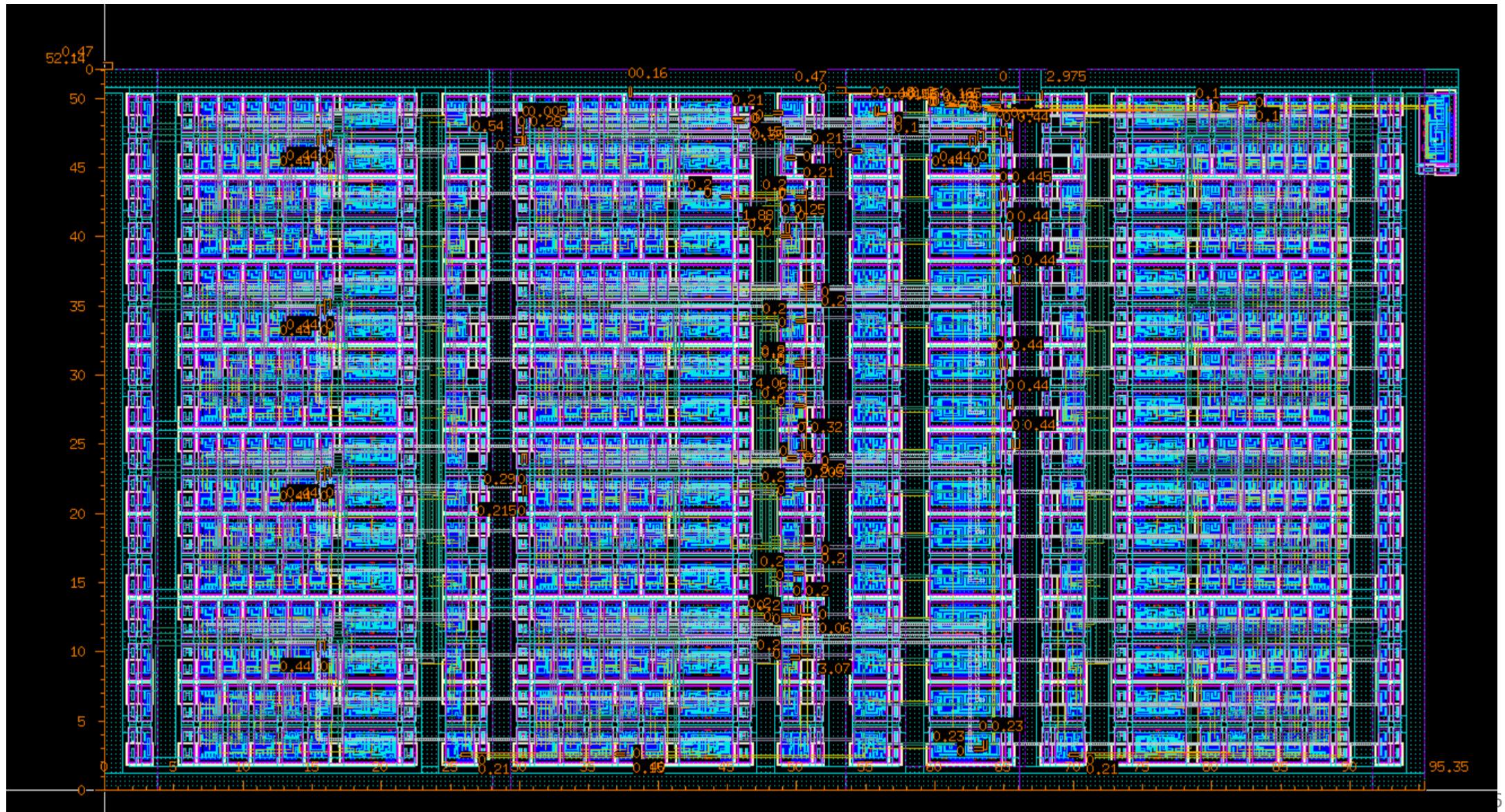
- Show in horizontal
- Each column is one bit (total 16-bit)
- Mosaic layout
- DRC & LVS clean

PWM Generator (Schematic)





PWM Generator (Layout)



PWM Generator (DRC, LVS clean)

The image shows two windows side-by-side. On the left is the 'Calibre - RVE v2020.4_34.17 : PWM.drc.results' window, which displays a list of DRC check results. The 'Check OD.DN.2L' item is selected and highlighted with a red border. On the right is the 'LVS Report File - PWM.lvs.report' window, which displays the LVS report details.

Calibre - RVE v2020.4_34.17 : PWM.drc.results

- File View Highlight Tools Window Setup Help
- Search
- Filter: Show All ▾ PWM, 9 Results (in 9 of 12 Checks)
- Check / Cell
- Check OD.DN.2L
- Check M2.DN.1L
- Check M3.DN.1L
- Check M4.DN.1L
- Check M5.DN.1L
- Check M6.DN.1L
- Check M7.DN.1L
- Check M8.DN.1L
- Check M9.DN.2L
- Check DENSITY_PRINT

OD.DN.2L { @ Min. OD density over window 150 step 75 >= 20%
ERR_WIN = DENSITY ODx CHIP_NOT_ODEXC < OD_DN_2L WINDOW OD_DN_2L_W STEP
on DN 2L c TNCTRC AC | NCED rule.. parv10

LVS Report File - PWM.lvs.report

- File Edit Options Windows

```
## CALIBRE SYSTEM ##
## LVS REPORT ##
#####
REPORT FILE NAME: PWM.lvs.report
LAYOUT NAME: /home/yz845/workspace/PWM.sp ('PWM')
SOURCE NAME: /home/yz845/workspace/PWM/src.net ('PWM')
RULE FILE: /home/yz845/workspace/_calibre.lvs_
CREATION TIME: Thu Dec 14 14:29:44 2023
CURRENT DIRECTORY: /home/yz845/workspace
USER NAME: yz845
CALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020
```

OVERALL COMPARISON RESULTS

```
# ##### * *
# # CORRECT # * /
# # #####
```



Testbench and Simulation

Method: Vector file in ADE L

- Solution for bulk simulation for our circuit is from Candence Staff (thanks for Andrew) using random number
- 80 cases for 4-bit CLA, 16-bit CLA and Greater or equal than (a C file could generate more testcases)
- 40 cases for testing function of D-flipflop and Mux
- 19 cases for modifying PWM duty cycle (with F constant) and 19 cases for changing PWM frequency (with D constant)

```
output_wf 1
radix 4444 4444 1
io iiii iiii o
vname ARR<[15:0]> CCR<[15:0]> Out
tunit ns

trise 0.005
tfall 0.005
vih 1.2
vil 0.0
voe 1.15
vol 0.05

2.5 00C8 0040 1
202.5 00FA 0050 1
452.5 012C 0060 1
752.5 015E 0070 1
1102.5 0190 0080 1
1502.5 01C2 0090 1
1952.5 01F4 00A0 1
2452.5 0226 00B0 1
3002.5 0258 00C0 1
3602.5 028A 00D0 1
4252.5 02BC 00E0 1
4952.5 02EE 00F0 1
5702.5 0320 0100 1
6502.5 0352 0110 1
7352.5 0384 0120 1
8252.5 03B6 0130 1
9202.5 03E8 0140 1
10202.5 041A 0150 1
11252.5 044C 0160 1
12352.5 047E 0170 1
13402.5 0000 0000 0
```

```
output_wf 1
radix 4444 4444 1
io iiii iiii o
vname ARR<[15:0]> CCR<[15:0]> Out
tunit ns

trise 0.005
tfall 0.005
vih 1.2
vil 0.0
voe 1.15
vol 0.05

2.5 0064 0000 1
102.5 0064 0005 1
202.5 0064 000A 1
302.5 0064 000F 1
402.5 0064 0014 1
502.5 0064 0019 1
602.5 0064 001E 1
702.5 0064 0023 1
802.5 0064 0028 1
902.5 0064 002D 1
1002.5 0064 0032 1
1102.5 0064 0037 1
1202.5 0064 003C 1
1302.5 0064 0041 1
1402.5 0064 0046 1
1502.5 0064 004B 1
1602.5 0064 0050 1
1702.5 0064 0055 1
1802.5 0064 005A 1
1902.5 0064 005F 1
2002.5 0064 0064 1
```

```
output_wf 1
radix 4444 4444 1
io iiii iiii o
vname A<[15:0]> B<[15:0]> Cin Sum<[15:0]> Cout
tunit ns
period 3
chk_window 0 1 1 period=3 first=1

trise 0.005
tfall 0.005
vih 1.2
vil 0.0
voe 1.15
vol 0.05

0000 0000 0000 0
3333 3333 0
1F75 8E63 0
6A25 EEE0 0
DE74 39F7 1
5230 72DA 0
9260 C2FC 0
D14B 030A 1
67DB 2EF8 1
0547 C2FC 0
F7D1 AE2C 1
BDA1 3F41 1
BA6A D504 0
58C5 AA81 0
2D90 FB80 0
A6DE B2F6 0
12BB 924E 0
C6FE CFD1 0
E799 F3D5 0
8FC0 F179 0
C614 3A72 1
3829 A795 0
C7B4 9E67 1
24A5 CBE1 0
C750 987C 1
```

```
radix 4444 4444 1
io iiii iiii o
vname A<[15:0]> B<[15:0]> GET
tunit ns
period 3
chk_window 0 1 1 period=3 first=1
```

- File 1: test for duty cycle
- File 2: test for frequency
- File 3: test for CLA16
- File 4: test for mux and DFF
- More testbench are shown in Dropbox folder ‘testbench’

1

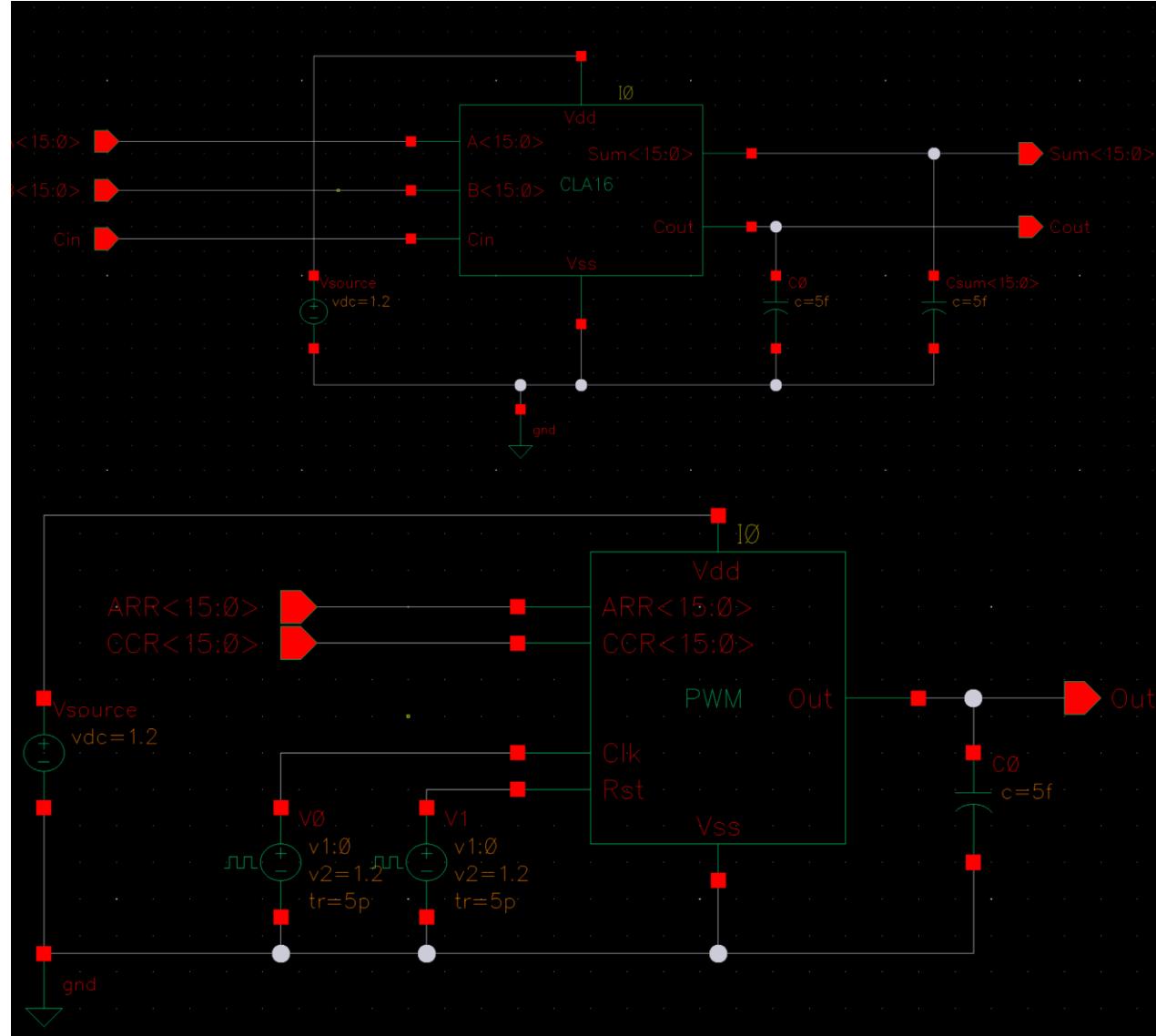
2

3

4



Testbench and Simulation



Testbench for simulation

- Leaving port for vector file input
- Each of the component have been tested
- Reason: It is very inefficient to have 16 power source and changing the voltage to test the circuit.

Testbench and Simulation – CLA16

```
****VectorCheck of logic state for Cout: All good!
  Number of total vector checks          = 53
  Number of X's matched correctly       = 0
  Number of Zero's matched correctly    = 27
  Number of One's matched correctly     = 26
  Number of Z's matched correctly      = 0
  Number of total states matched correctly = 53
  Number of total errors               = 0

****VectorCheck of logic state for Sum<0>: All good!
  Number of total vector checks          = 53
  Number of X's matched correctly       = 0
  Number of Zero's matched correctly    = 26
  Number of One's matched correctly     = 27
  Number of Z's matched correctly      = 0
  Number of total states matched correctly = 53
  Number of total errors               = 0

****VectorCheck of logic state for Sum<1>: All good!
  Number of total vector checks          = 53
  Number of X's matched correctly       = 0
  Number of Zero's matched correctly    = 29
  Number of One's matched correctly     = 24
  Number of Z's matched correctly      = 0
  Number of total states matched correctly = 53
  Number of total errors               = 0

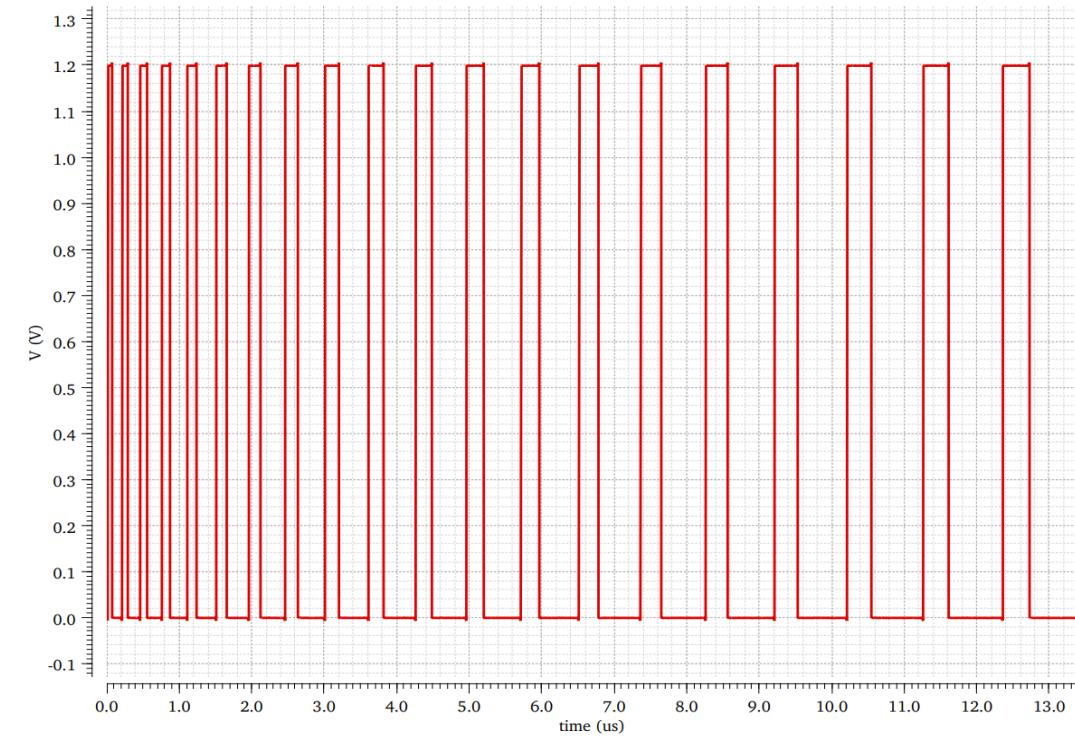
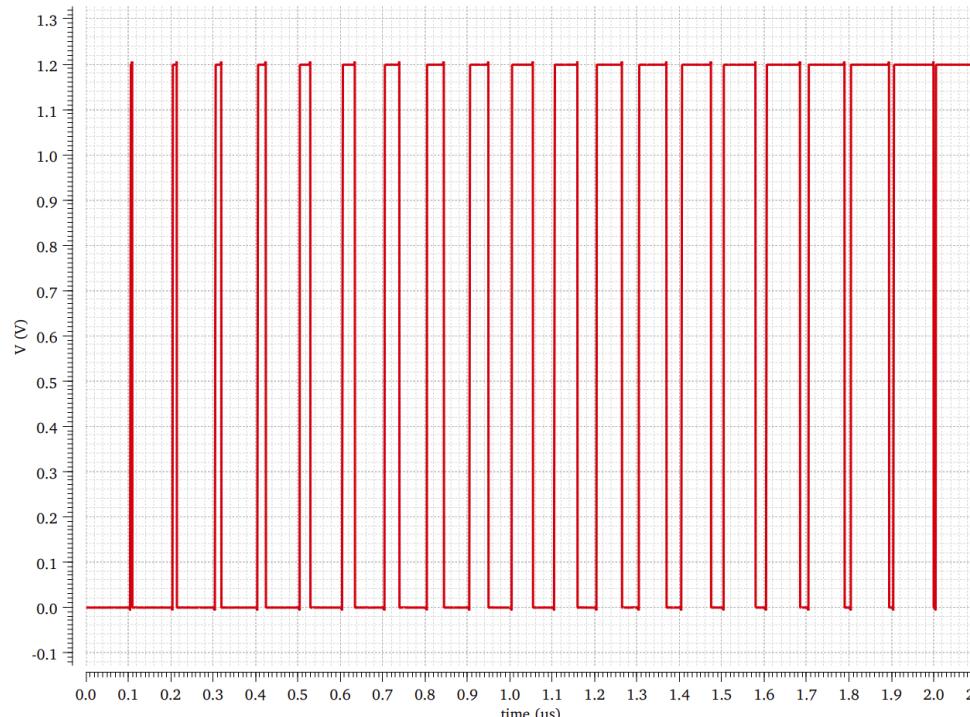
****VectorCheck of logic state for Sum<2>: All good!
  Number of total vector checks          = 53
  Number of X's matched correctly       = 0
  Number of Zero's matched correctly    = 26
  Number of One's matched correctly     = 27
  Number of Z's matched correctly      = 0
  Number of total states matched correctly = 53
  Number of total errors               = 0

****VectorCheck of logic state for Sum<3>: All good!
  Number of total vector checks          = 53
  Number of X's matched correctly       = 0
  Number of Zero's matched correctly    = 28
  Number of One's matched correctly     = 25
  Number of Z's matched correctly      = 0
  Number of total states matched correctly = 53
```

****VectorCheck of logic state for GET: Number of total vector checks = 53
Number of X's matched correctly = 0
Number of Zero's matched correctly = 29
Number of One's matched correctly = 23
Number of Z's matched correctly = 0
Number of total states matched correctly = 52
Number of total errors = 1
From 4.00000e-09 to 5.00000e-09, Expected state = zero, Actual state = one



Testbench and Simulation – PWM



cycle	time (s)	DutyCycle (%)	Freq (Hz)	cycle	time (s)	DutyCycle (%)	Freq (Hz)
0	1.00E-07	4.998	1.00E+07	9	1.00E-06	49.99	1.00E+07
1	2.00E-07	9.998	1.00E+07	10	1.10E-06	54.99	1.00E+07
2	3.00E-07	14.99	1.00E+07	11	1.20E-06	59.99	1.00E+07
3	4.00E-07	19.99	1.00E+07	12	1.30E-06	64.99	1.00E+07
4	5.00E-07	24.99	1.00E+07	13	1.40E-06	69.99	1.00E+07
5	6.00E-07	29.99	1.00E+07	14	1.50E-06	74.99	1.00E+07
6	7.00E-07	34.99	1.00E+07	15	1.60E-06	79.99	1.00E+07
7	8.00E-07	39.99	1.00E+07	16	1.70E-06	84.99	1.00E+07
8	9.00E-07	44.99	1.00E+07	17	1.80E-06	89.99	1.00E+07

cycle	time (s)	DutyCycle (%)	Freq(Hz)	cycle	time (s)	DutyCycle (%)	Freq(Hz)
0	5.08E-11	31.99	5.00E+06	9	3.60E-06	31.99	1.54E+06
1	2.00E-07	31.99	4.00E+06	10	4.25E-06	31.99	1.43E+06
2	4.50E-07	31.99	3.33E+06	11	4.95E-06	31.99	1.33E+06
3	7.50E-07	31.99	2.86E+06	12	5.70E-06	31.99	1.25E+06
4	1.10E-06	31.99	2.50E+06	13	6.50E-06	31.99	1.18E+06
5	1.50E-06	31.99	2.22E+06	14	7.35E-06	31.99	1.11E+06
6	1.95E-06	31.99	2.00E+06	15	8.25E-06	31.99	1.05E+06
7	2.45E-06	31.99	1.82E+06	16	9.20E-06	31.99	1.00E+06
8	3.00E-06	31.99	1.67E+06	17	1.02E-05	31.99	9.52E+05

The result meet the requirement (changing duty cycle and frequency).

Summary

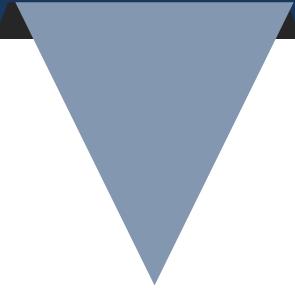
Specifications:

Chip Area: $52.14 \mu m \times 95.35 \mu m = 4971.55 \mu m^2$

Number of instances: This chip has 4022 instances totally.

Estimated Power Consumption (normal): The circuit draws a DC current about 12.6 uA. Since VDD = 1.2V, power consumption is estimated at 15.12 uW (10MHz).

Maximum Clk: 1GHz (the maximum frequency we have tested).



Thank you

Yunfan Zhang, Yi Tong