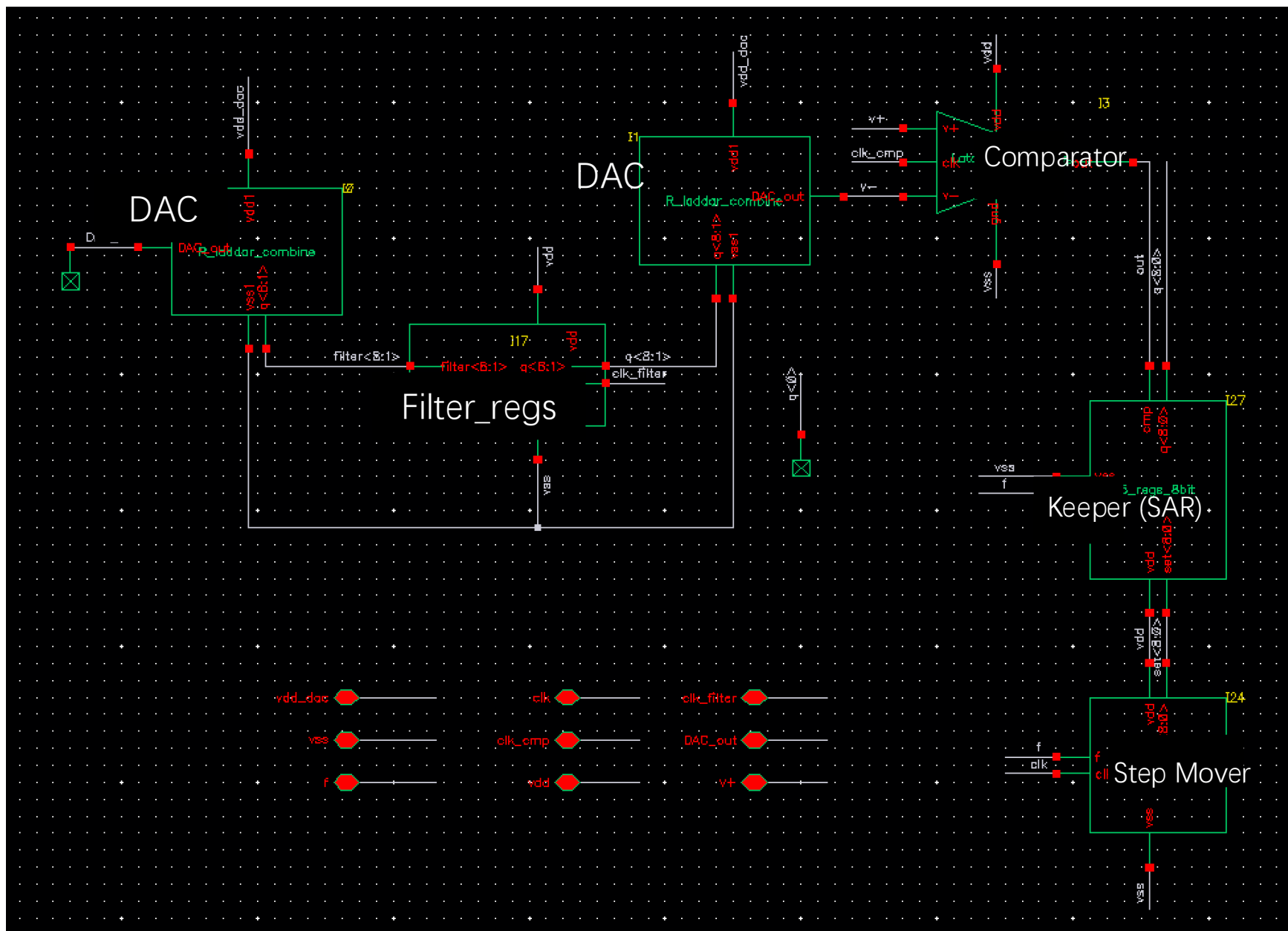


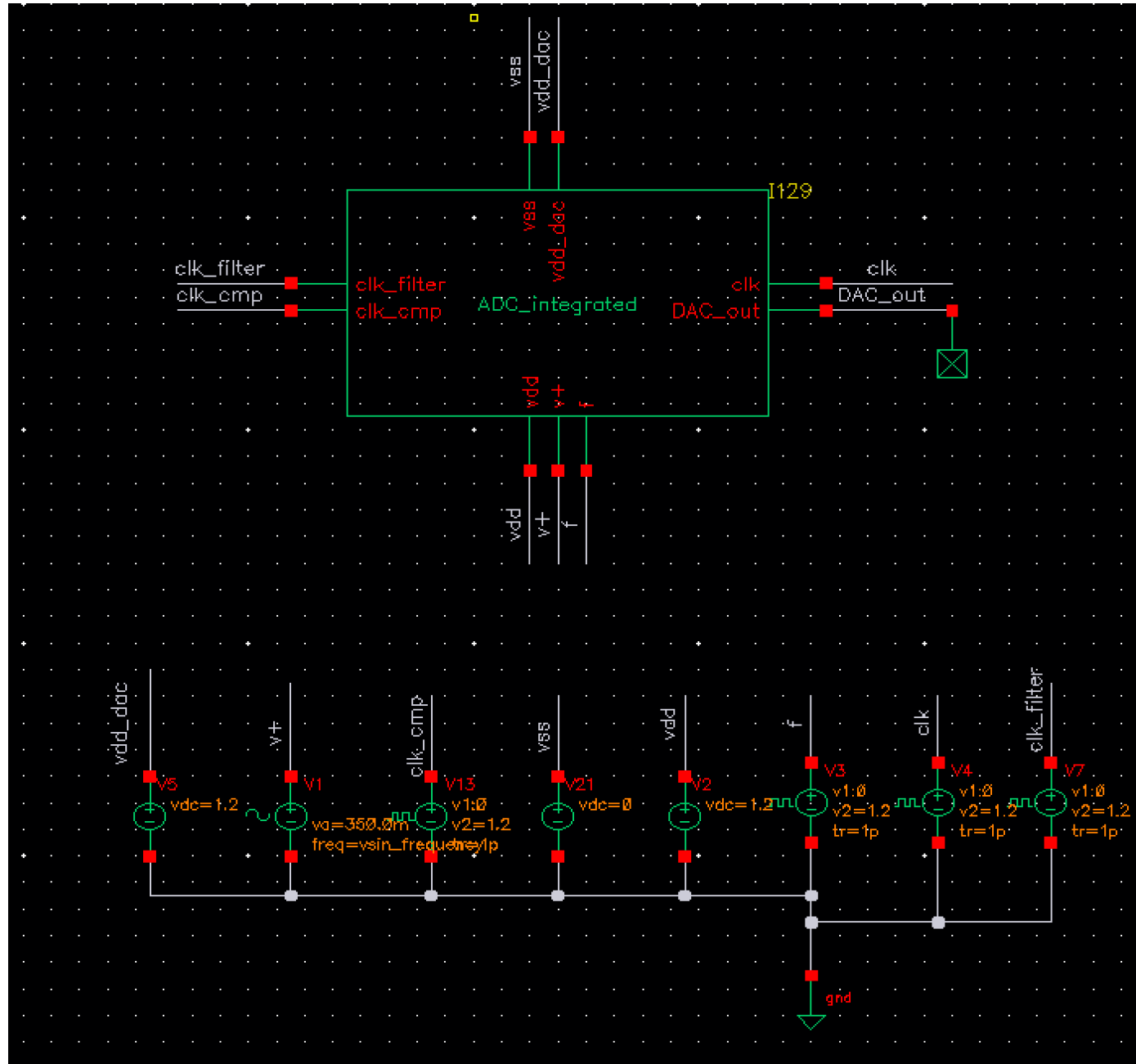
SAR - ADC

Yi Tong

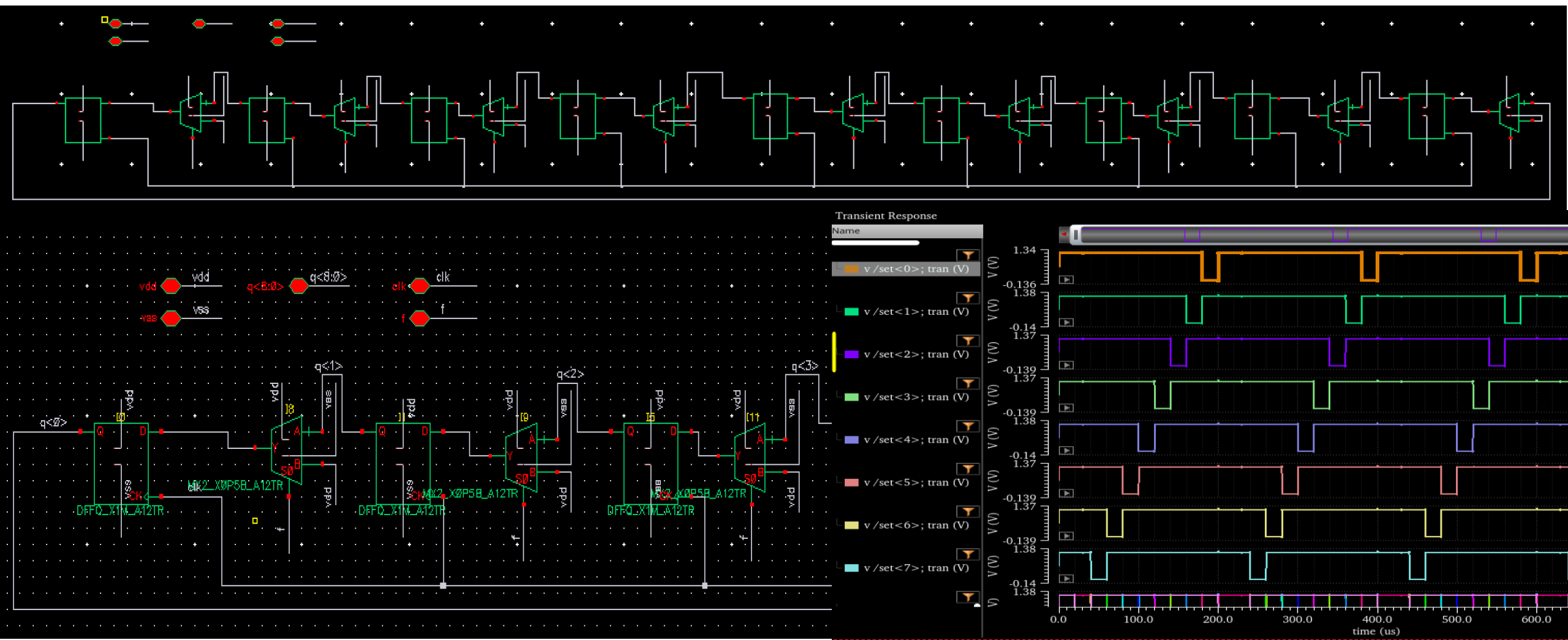
Schematic



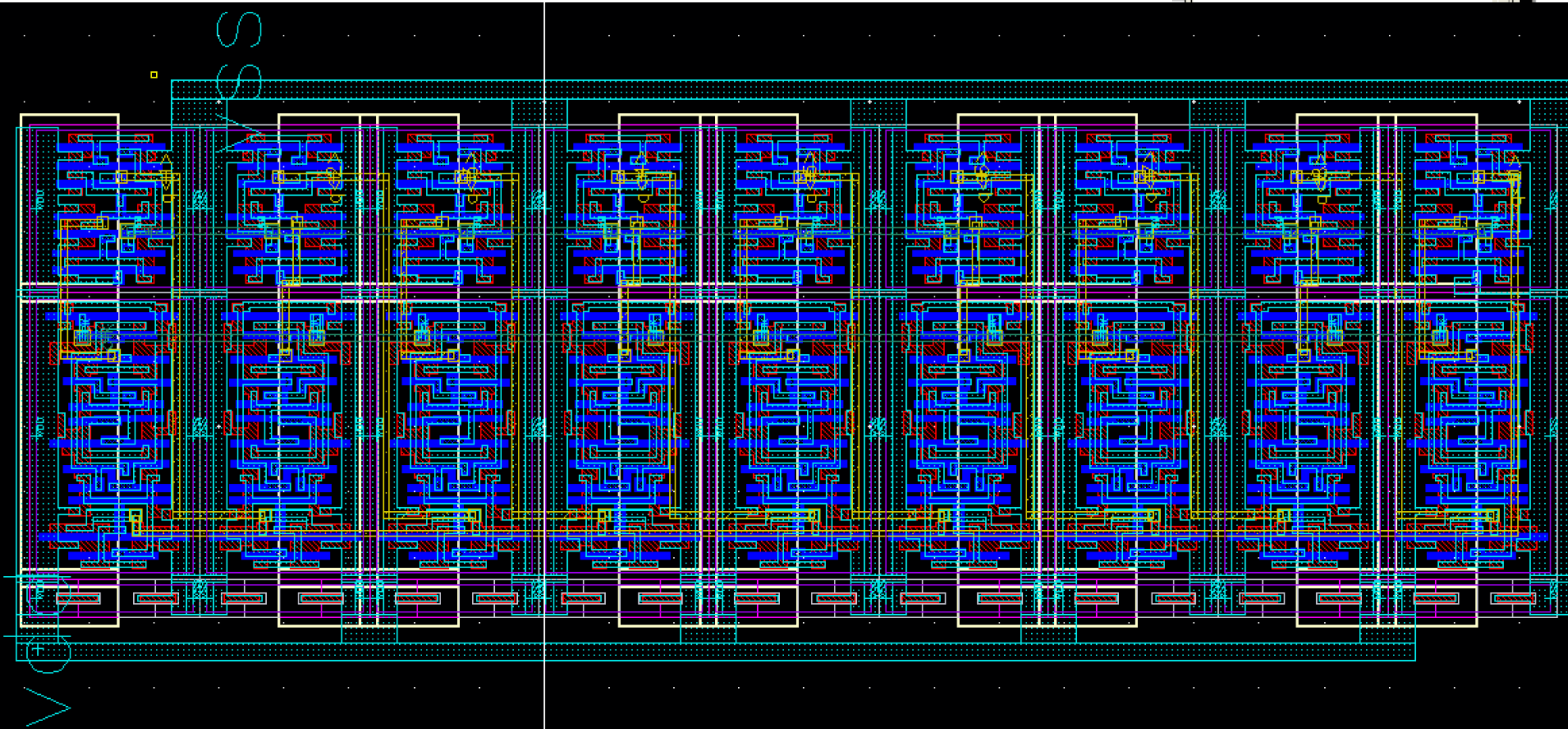
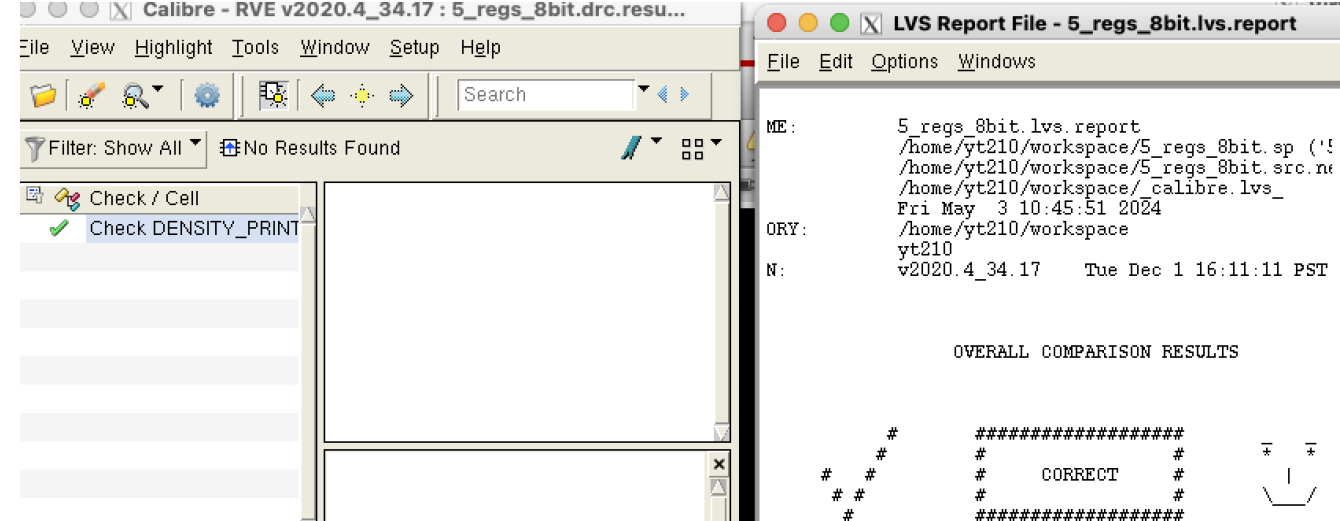
Top view



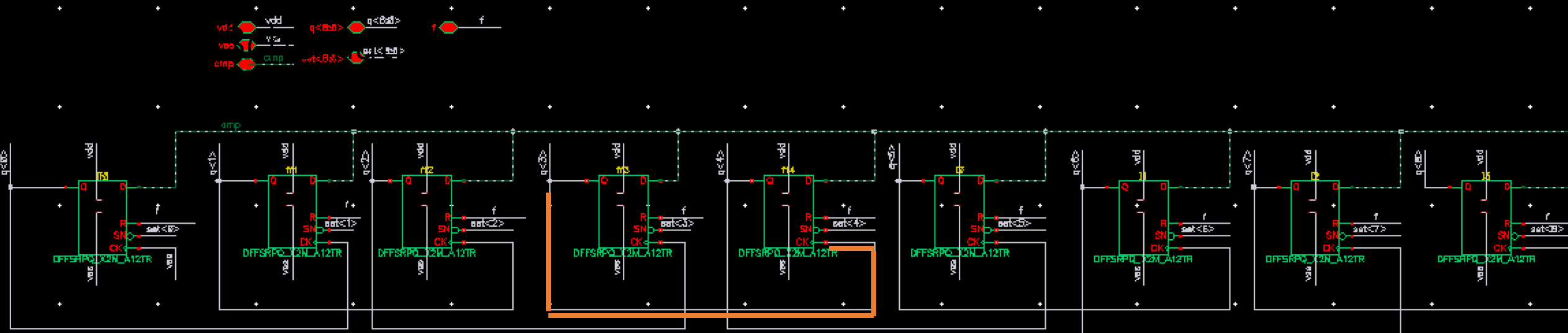
Set Mover- schematic



Set Mover - Layout



Keeper (SAR Logic)



Comparator - schematic

Calibre - RVE v2020.4_34.17 : Latch_comp...

File View Highlight Tools Window Setup Help

Search

Filter: Show All No Results Found

Check / Cell

Check DENSITY_PRINT

OD.DN.2L.density

OD.DN.2H.I0.density

OD.DN.2H.CORE.density

OD.DN.3L.density

OD.DN.3H.I0.density

OD.DN.3H.CORE.density

P0.DN.2.density

P0.DN.3.density

M1.DN.1L.density

M1.DN.1H.density

M1.DN.0.density

Check DENSITY_PRINT_FILES

LVS Report File - Latch_comparator.lvs.report

File Edit Options Windows

OVERALL COMPARISON RESULTS

#

#

#

#

#

#####

CORRECT

#####

#

#

#

#

#

CELL SUMMARY

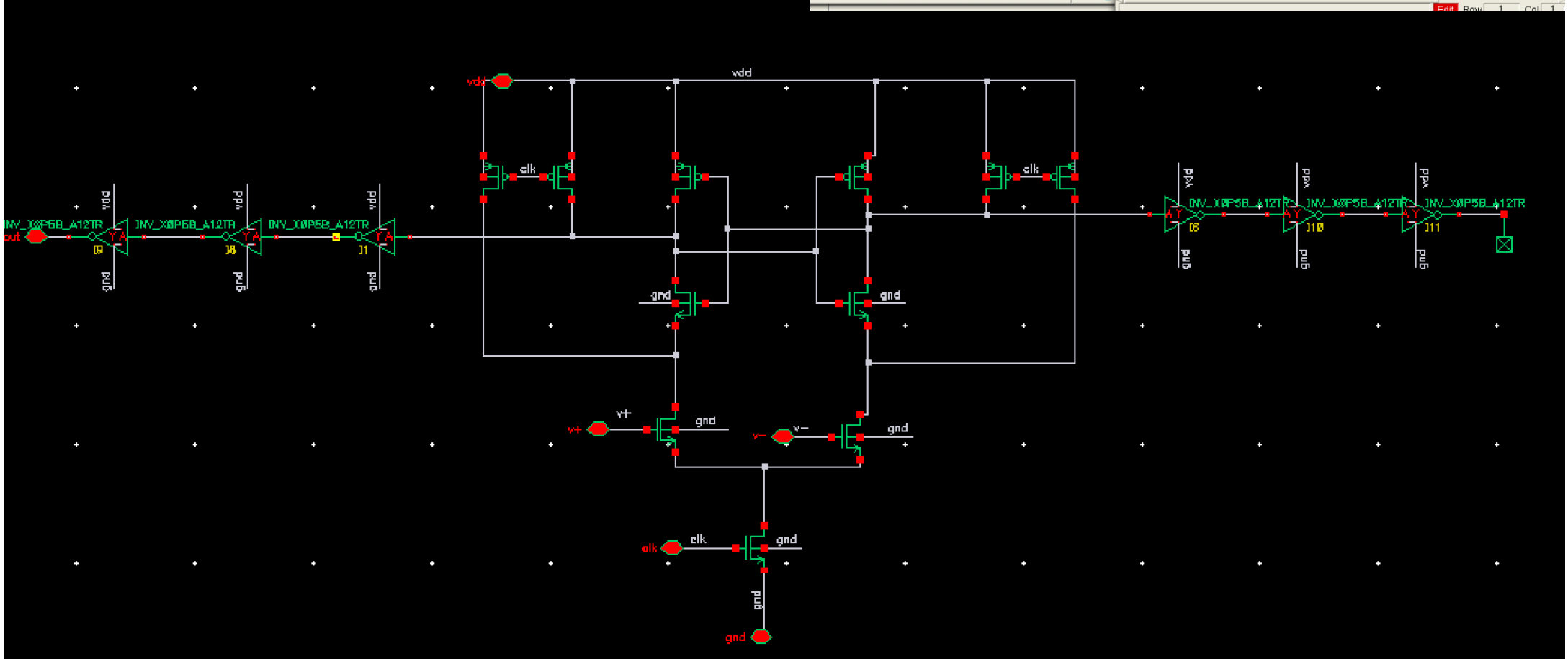
Result	Layout	Source
CORRECT	Latch_comparator	Latch_comparator

LVS PARAMETERS

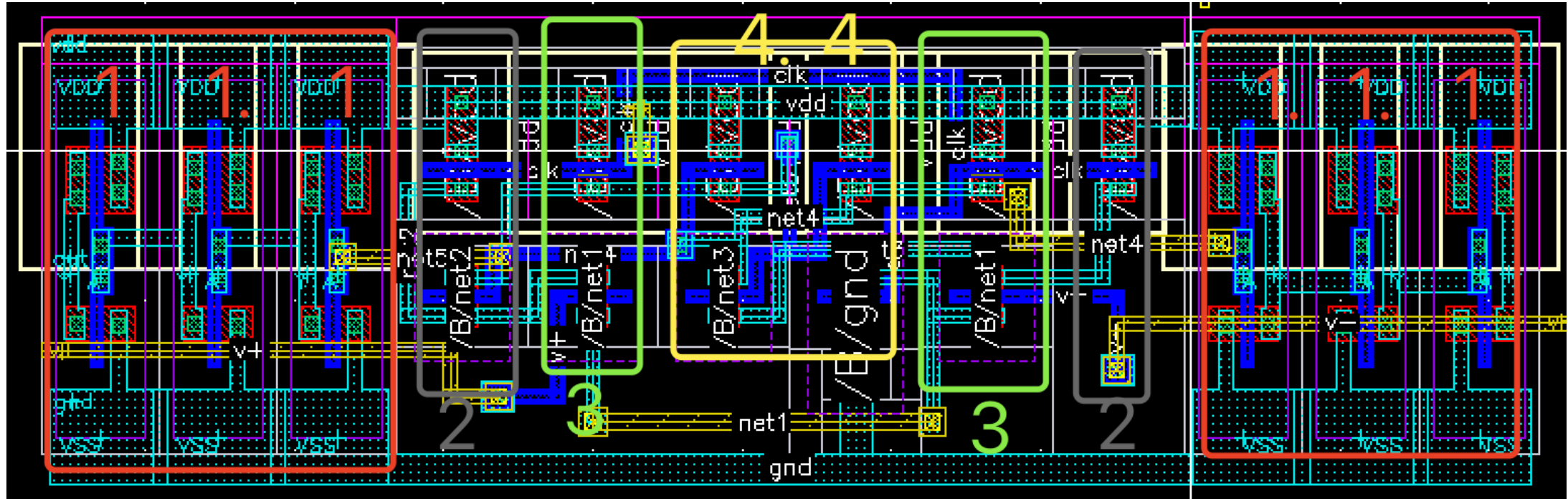
o LVS Setup:

// LVS COMPONENT TYPE PROPERTY

// LVS COMPONENT SUBTYPE PROPERTY



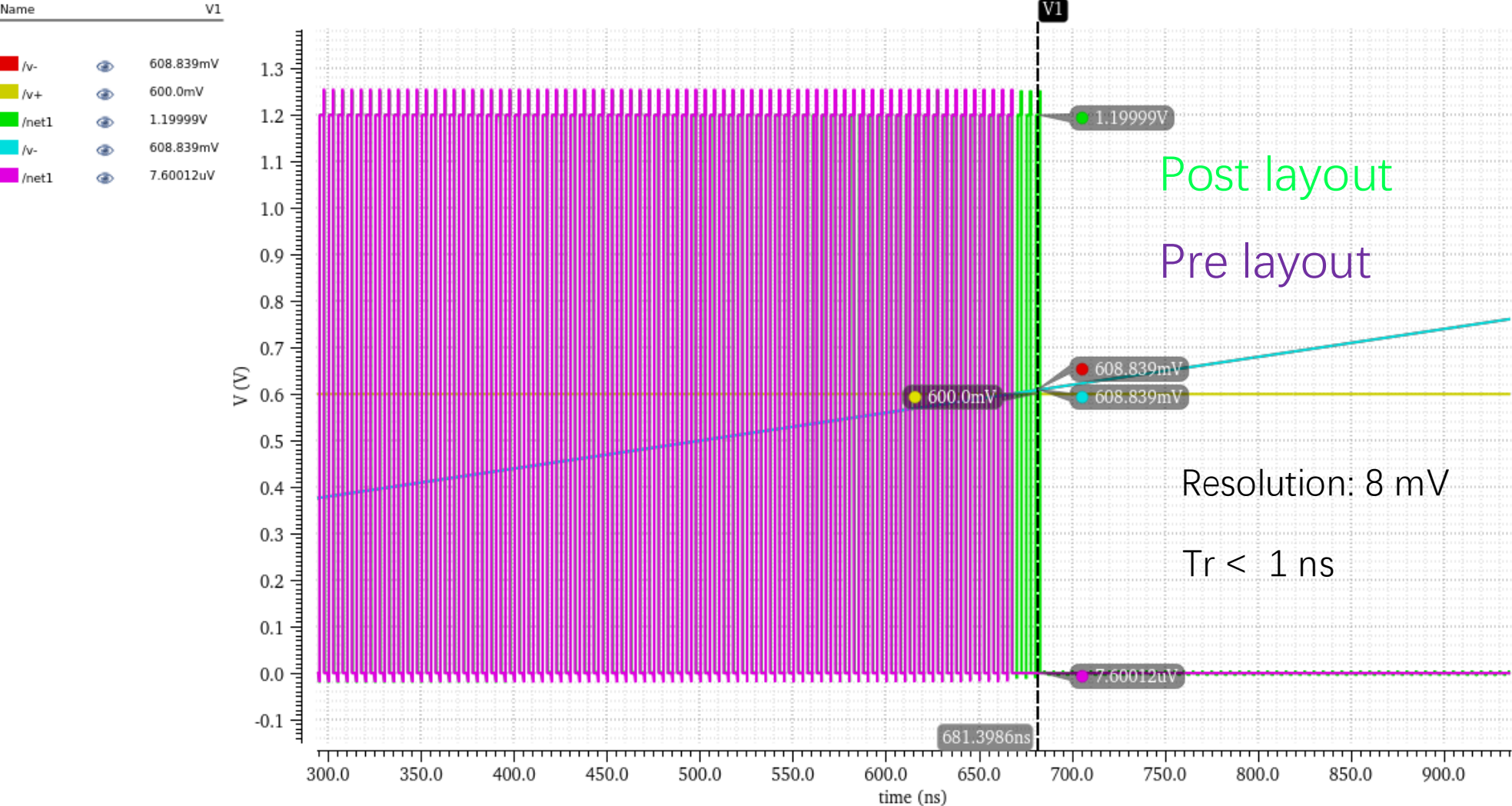
Comparator – layout



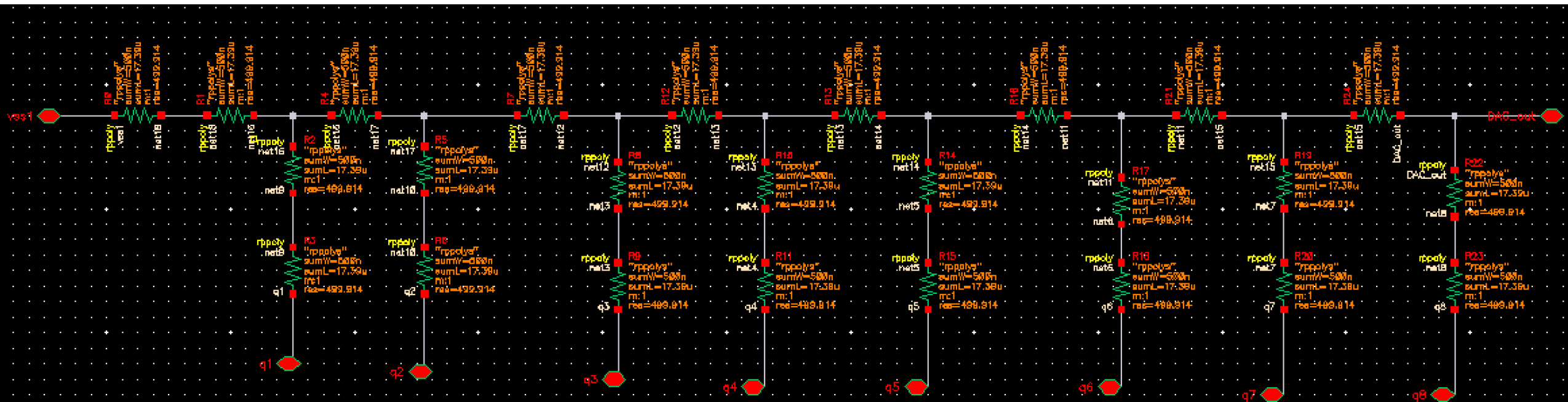
Comparator – simulation (pre&post)

Transient Response

Thu May 2 14:56:48 2024 1



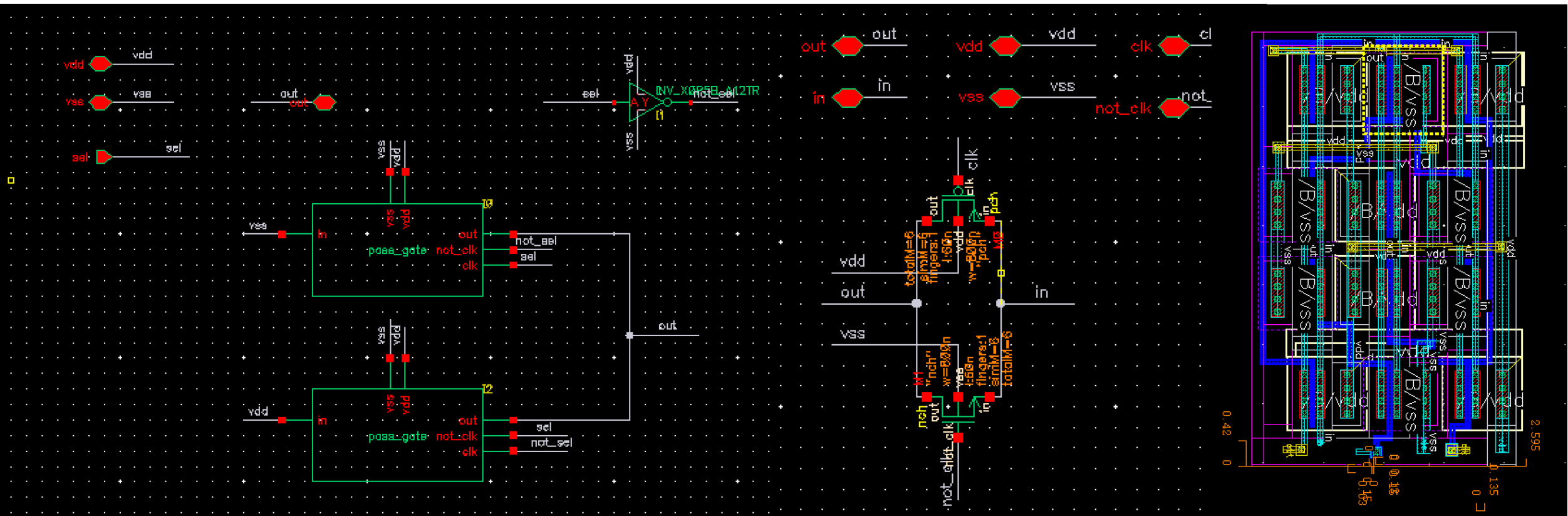
DAC-R 2R Ladder (Resistor tree)



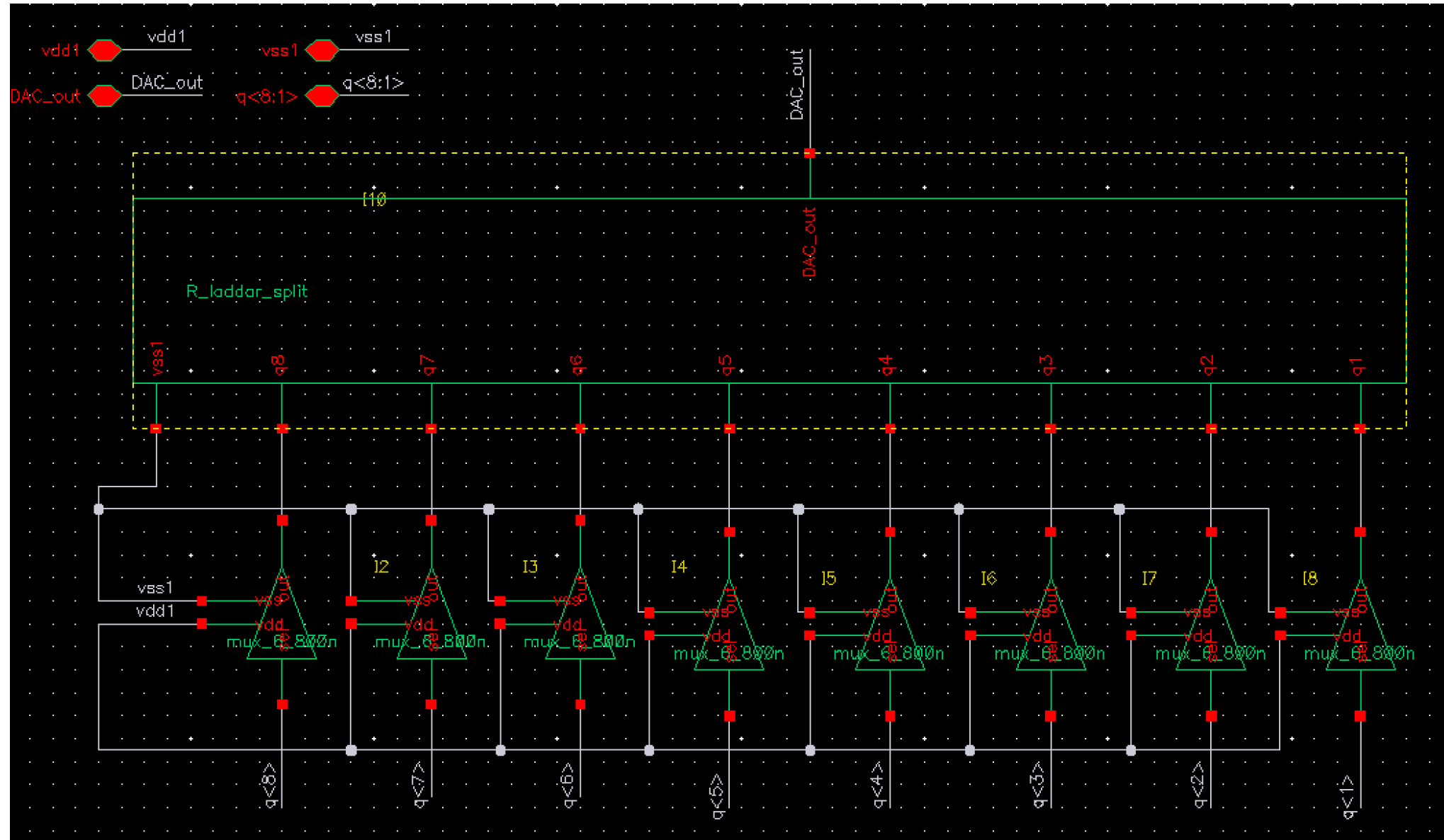
DAC-R 2R Laddar (Switches)

T_gate size: $w = 5u$, $l = 60n$

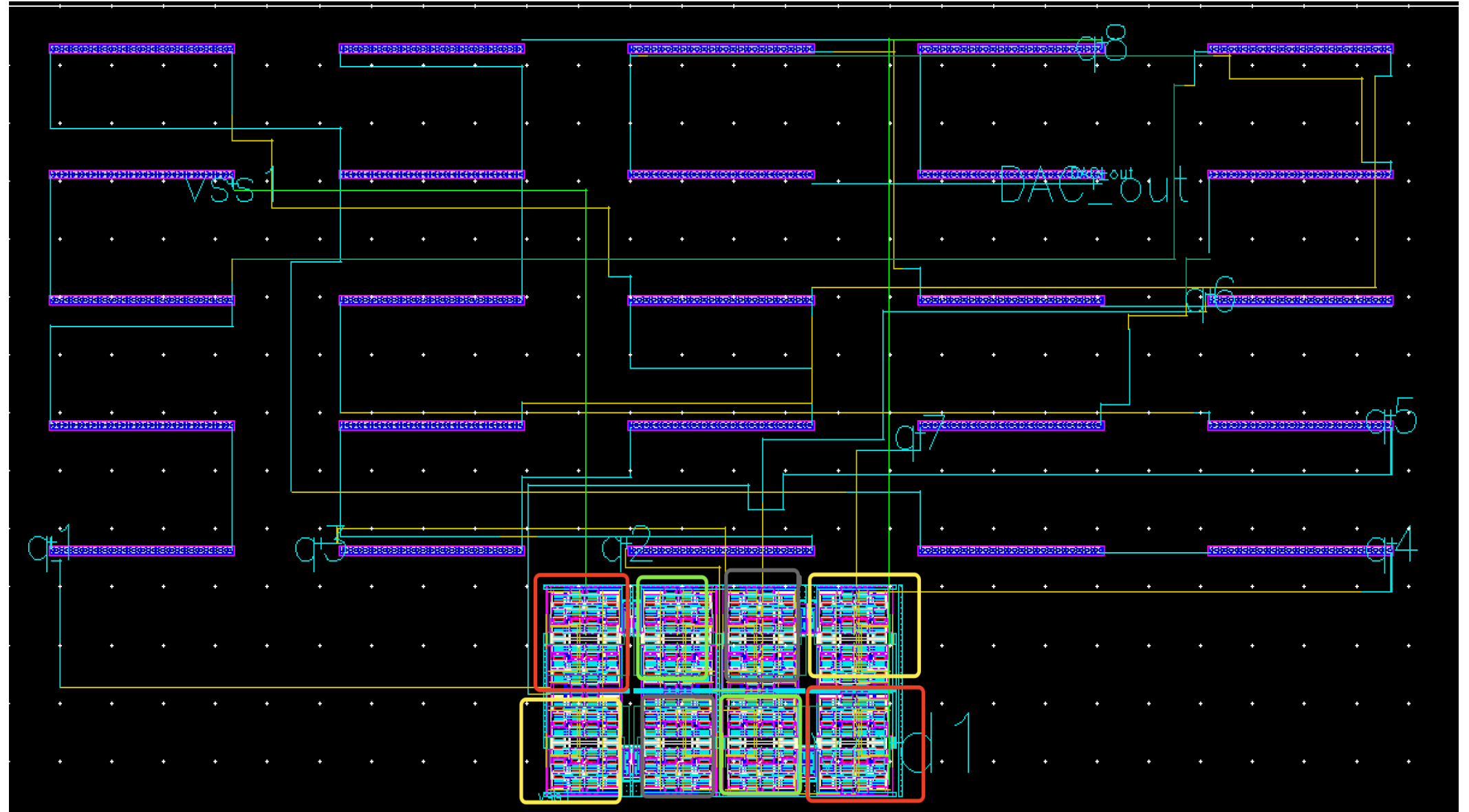
Inverter: library



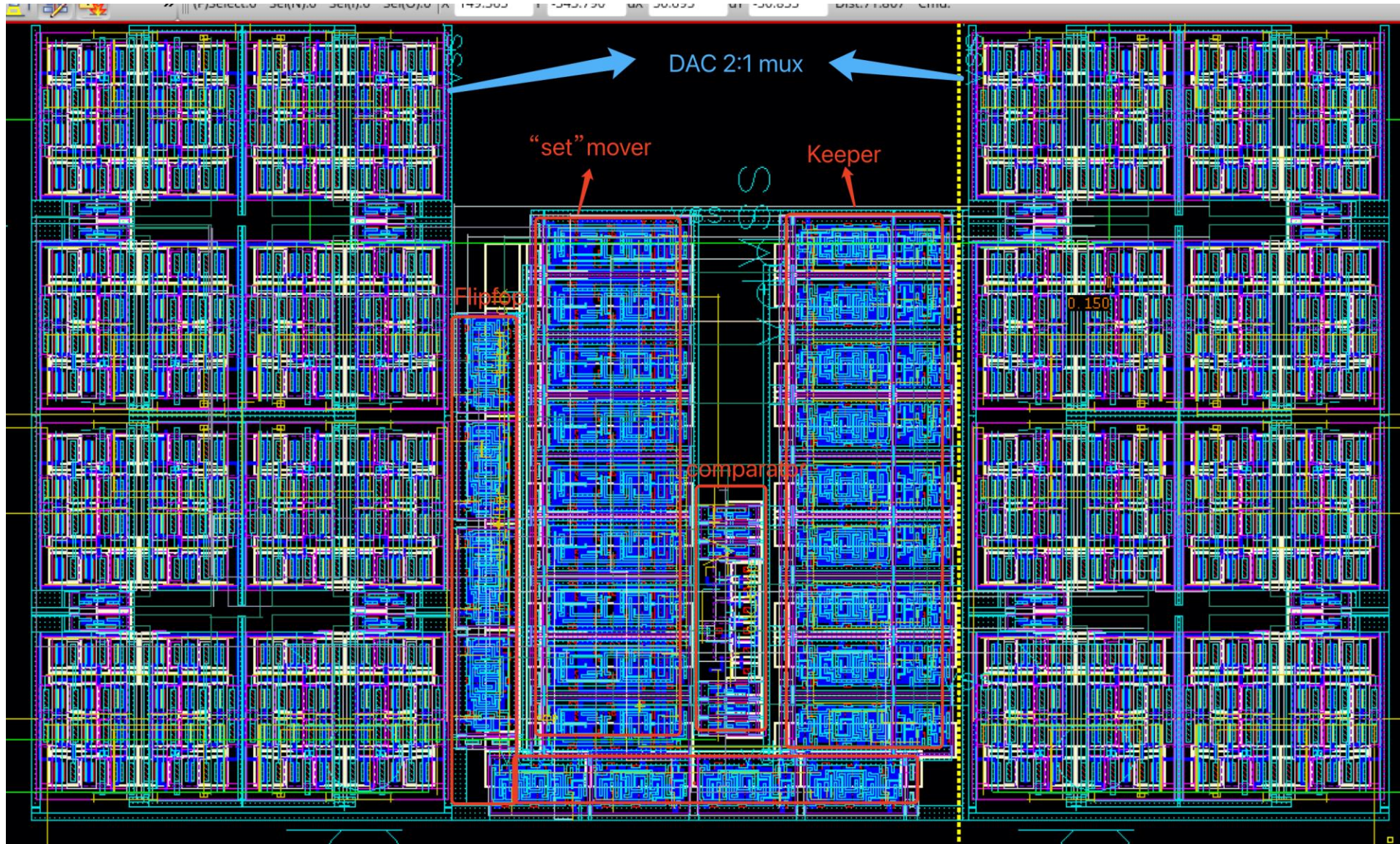
DAC-R2R Laddar (whole)



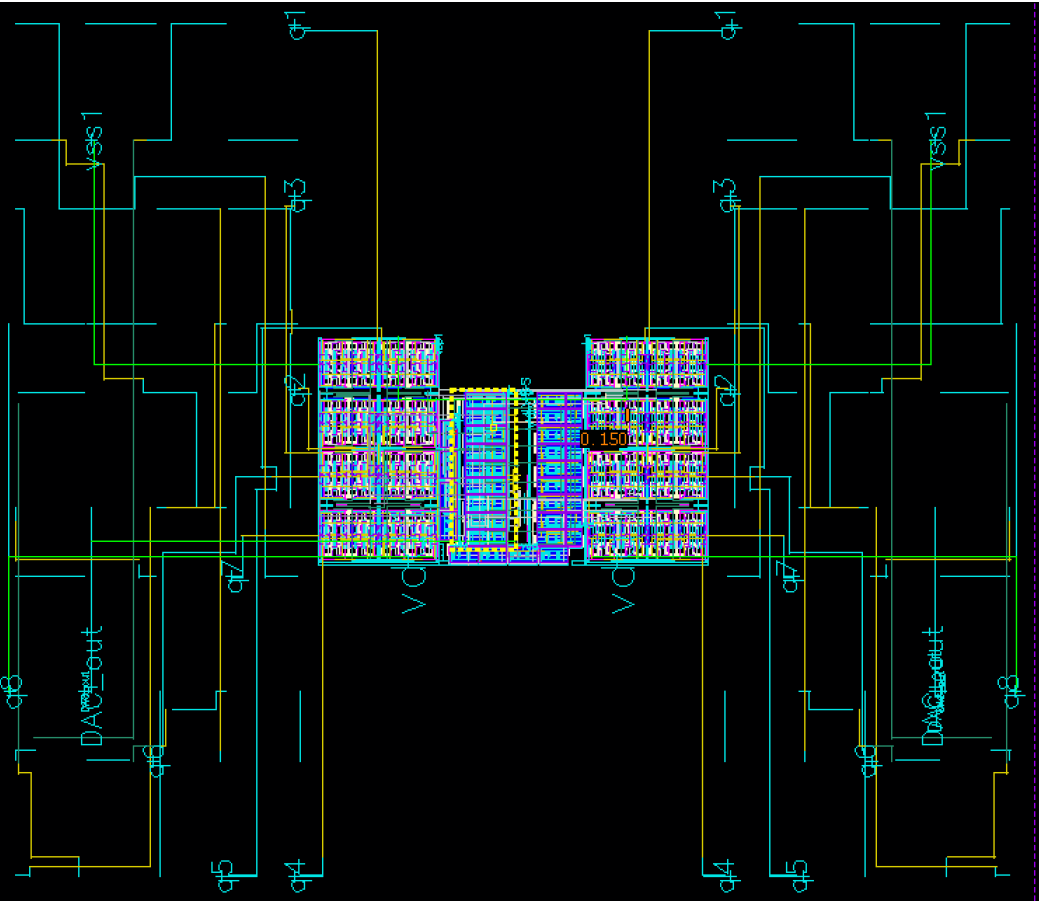
DAC-R2R Laddar



Layout (except rpoly)



Full Layout



Calibre - RVE v2020.4_34.17 : ADC_integrated.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All ADC_integrated, 12 Results (in 11 of 14 Checks)

- Check OD.DN.2L
- Check PO.DN.2
- Check M1.DN.1L
- Check M2.DN.1L
- Check M3.DN.1L
- Check M4.DN.1L
- Check M5.DN.1L
- Check M6.DN.1L
- Check M7.DN.1L
- Check M8.DN.1L
- Check M9.DN.2L
- Check DENSITY_PRINT

OD.DN.2L { @ Min. OD density over window 150 step 75 >= 20%
ERR_WIN = DENSITY ODx CHIP NOT ODEX < OD_DN_2L WINDOW OD_DN_2L_W
STEP OD_DN_2L_S INSIDE OF LAYER CHIPx BACKUP
[AREA(ODx)/AREA(CHIP_NOT_ODEX)]
F = WITH WIDTH (ERR_WIN NOT OD_EXC) >= OD_DN_2L_E
DENSITY F ODx CHIP NOT ODEX < OD_DN_2L WINDOW OD_DN_2L_W STEP
OD_DN_2L_S INSIDE OF LAYER CHIPx BACKUP PRINT OD.DN.2L.density
[!AREA(F)+AREA(ODx)/AREA(CHIP_NOT_ODEX)]

Check OD.DN.2L

LVS Report File - ADC_integrated.lvs.report

File Edit Options Windows

JLE FILE: /home/yt210/workspace/_calibre.lvs_
REATION TIME: Wed May 1 22:17:43 2024
URRENT DIRECTORY: /home/yt210/workspace
SER NAME: yt210
ALIBRE VERSION: v2020.4_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS

CORRECT #
#####

CELL SUMMARY

Layout	Source
ADC_integrated	ADC_integrated

Edit Row 1 Col 1

- All clean

SAR Extracted result – 100K Hz

db20(dft(v("/DAC_out" ?result "tran") 0.0 10.00u 1024 "Rectangular" 0 0 1))

Name

spectrum_DAC_out

Thu May 2 23:51:24 2024 1

30 dB

Transient Response

Name

/DAC_out

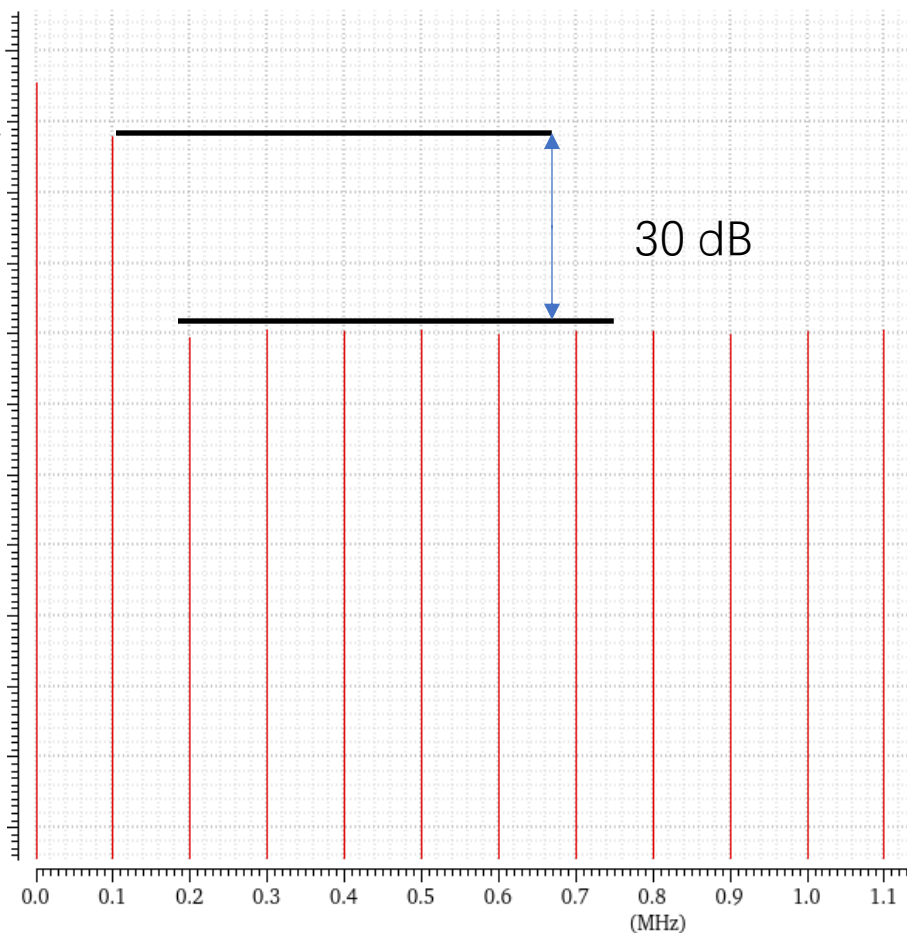
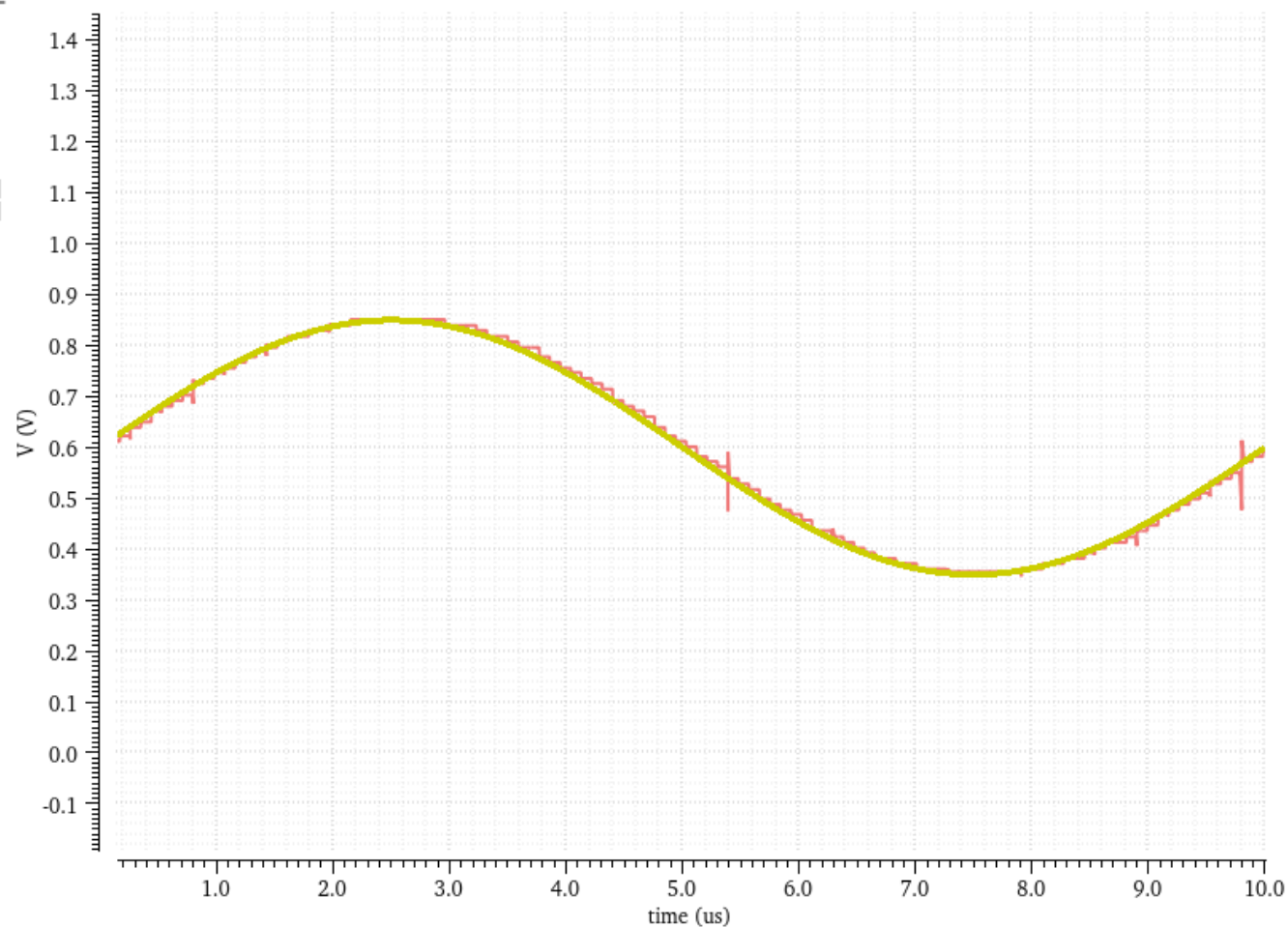
/v+

/I129/v-

/vdd

/I129/q<8:0>

/I129/set<8:0>



SAR result

Transient Response

Thu May 2 23:51:24 2024 1

Name	...	bit
------	-----	-----

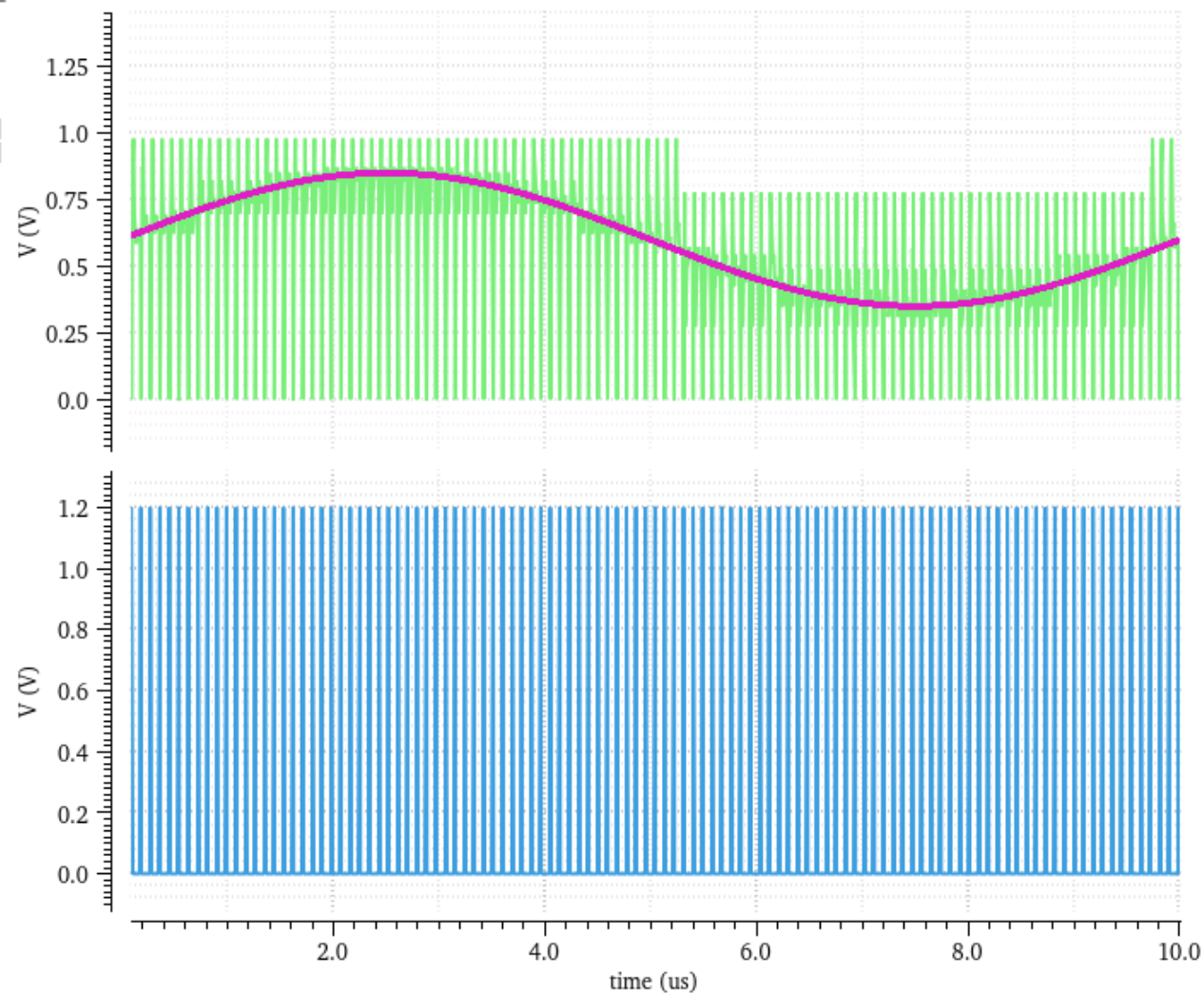
<input checked="" type="checkbox"/> /v+	<input checked="" type="checkbox"/>	
---	-------------------------------------	--

<input checked="" type="checkbox"/> /i129/v-	<input checked="" type="checkbox"/>	
--	-------------------------------------	--

/i129/set<8:0>		
----------------	--	--

/i129/q<8:0>		
--------------	--	--

<input checked="" type="checkbox"/> v /f; tran (V)	<input checked="" type="checkbox"/>	
--	-------------------------------------	--



SAR result

Transient Response

Name: ... bit

/v+



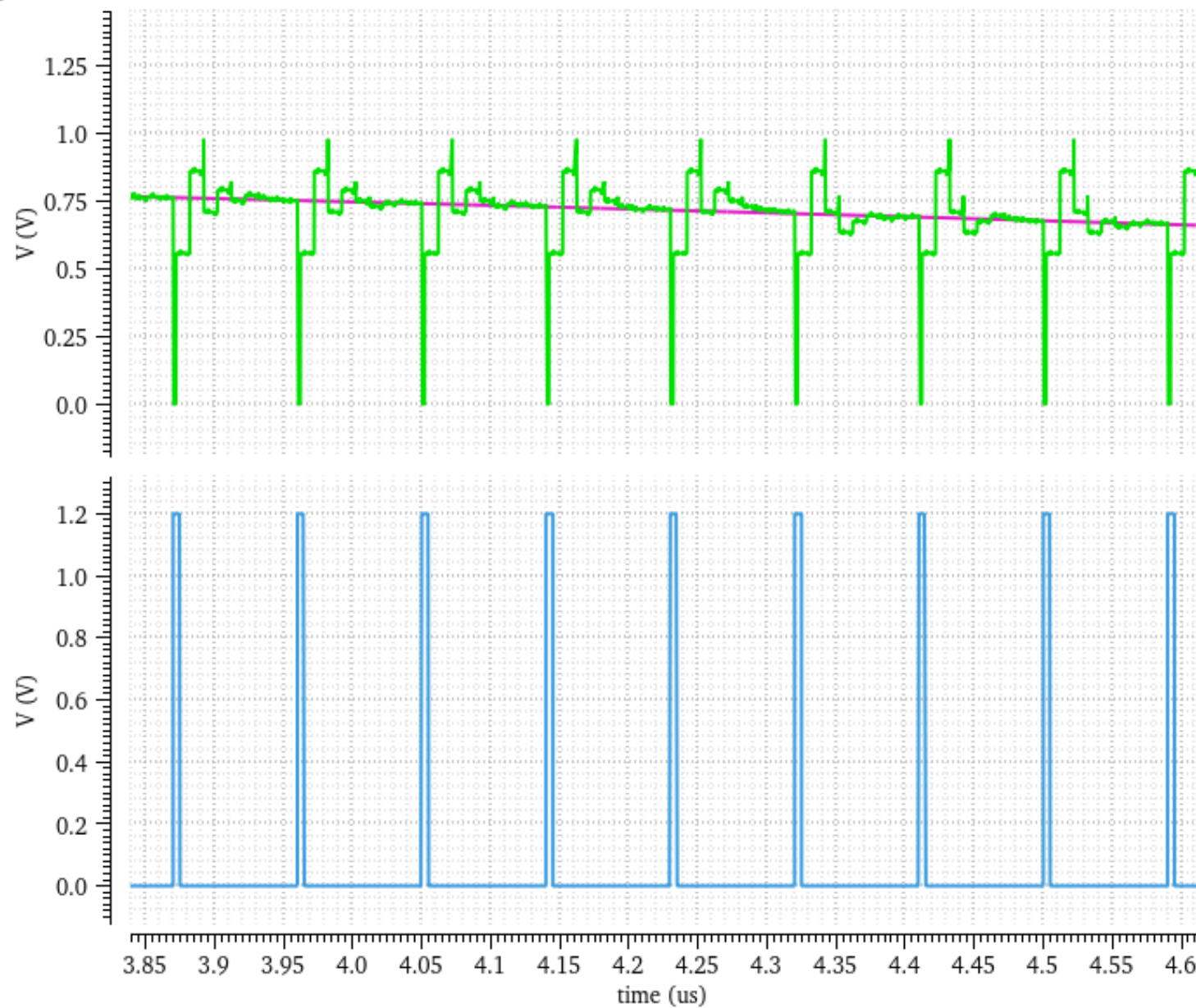
/I129/v-



/I129/set<8:0>

/I129/q<8:0>

v /f; tran (V)

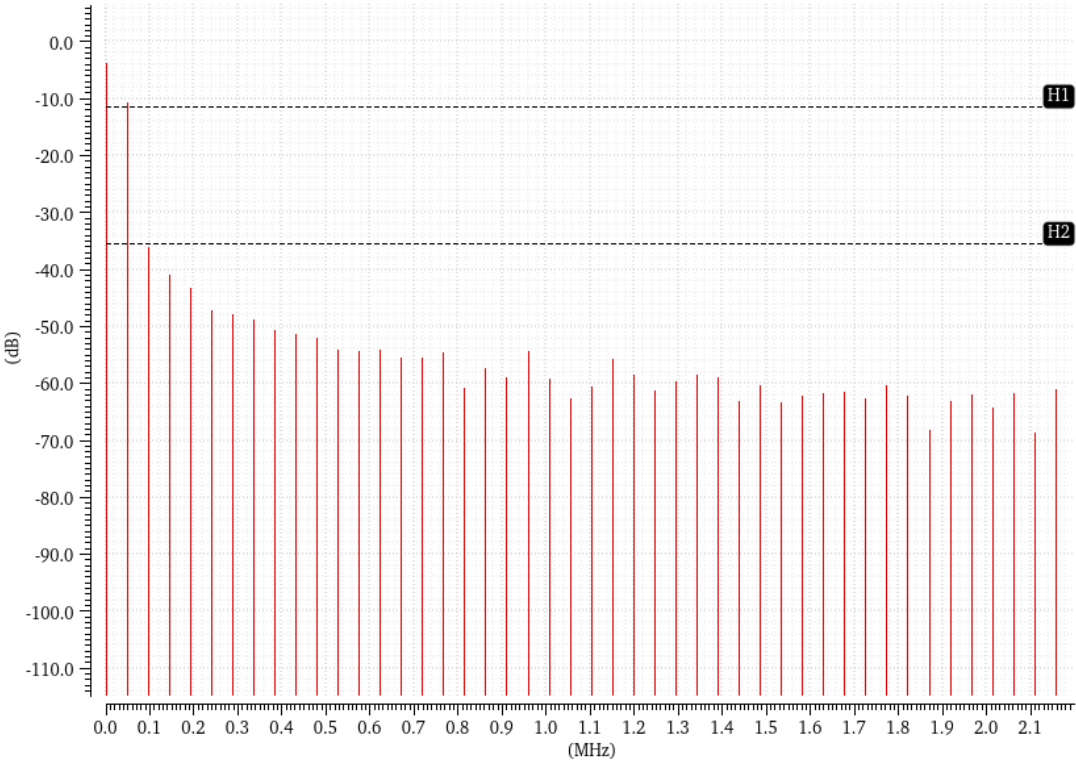


Simulation – 50K Hz

db20(dft(v("/DAC_out" ?result "tran") 1u 21.86u 1024 "Rectangular" 0 0 1))

Name

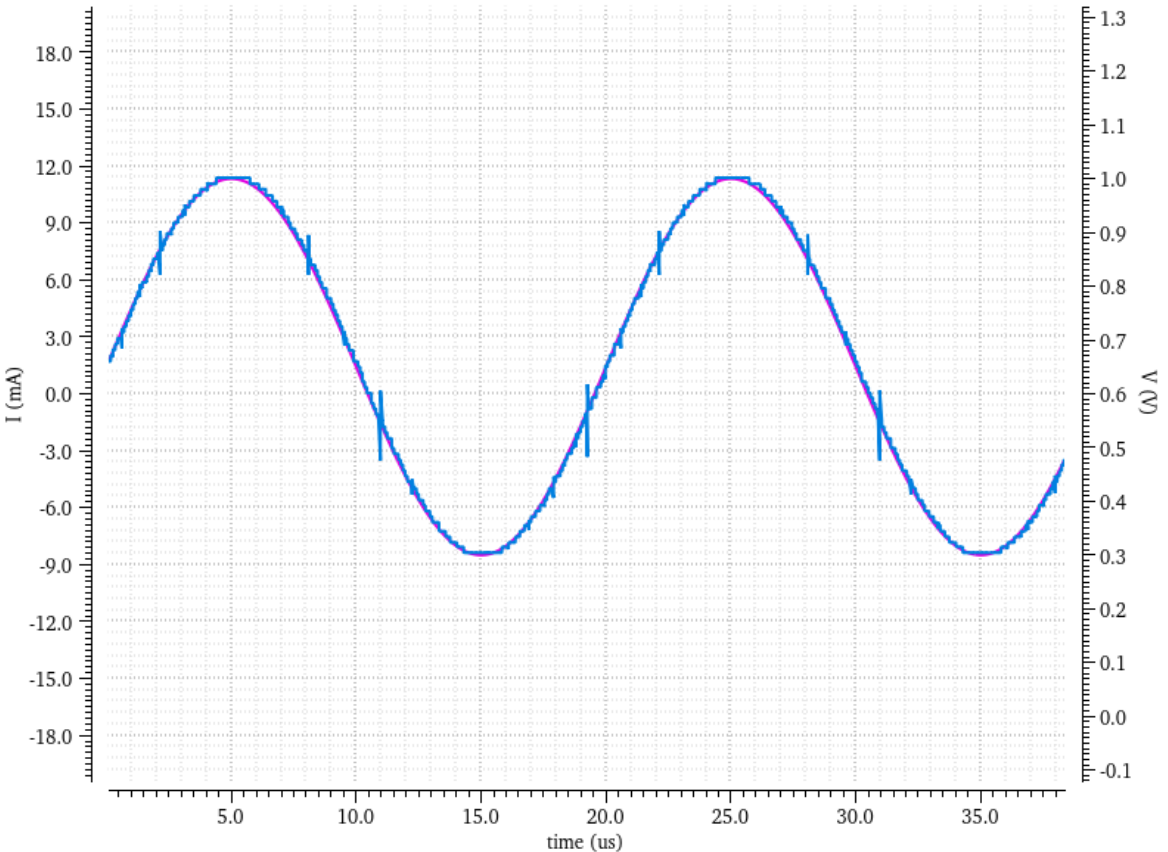
spectrum_DAC_out



Transient Response

Name

- /V3/MINUS
- /V3/PLUS
- /I129/v-
- /f
- /v+
- v /DAC_out; tran (V)
- v /DAC_out; tran (V)




Thu May 2 18:42:51 2024 1

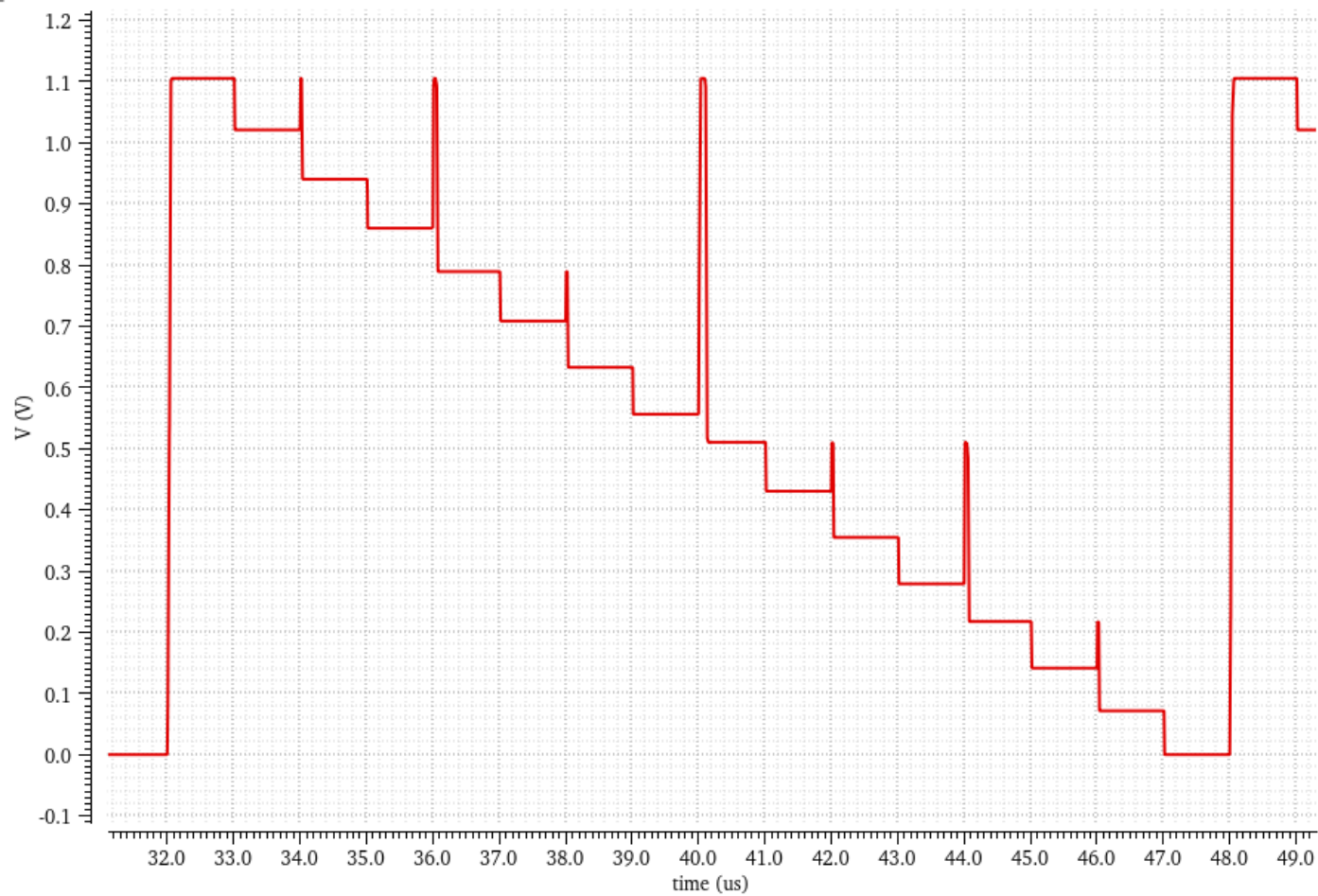
Defects:

Transient Response

Fri May 3 09:46:28 2024 1

Name Vis

■ /net11 



SAR Extracted result – 100K Hz

db20(dft(v("/DAC_out" ?result "tran") 0.0 10.00u 1024 "Rectangular" 0 0 1))

Name

spectrum_DAC_out

Thu May 2 23:51:24 2024 1

30 dB

Transient Response

Name

/DAC_out

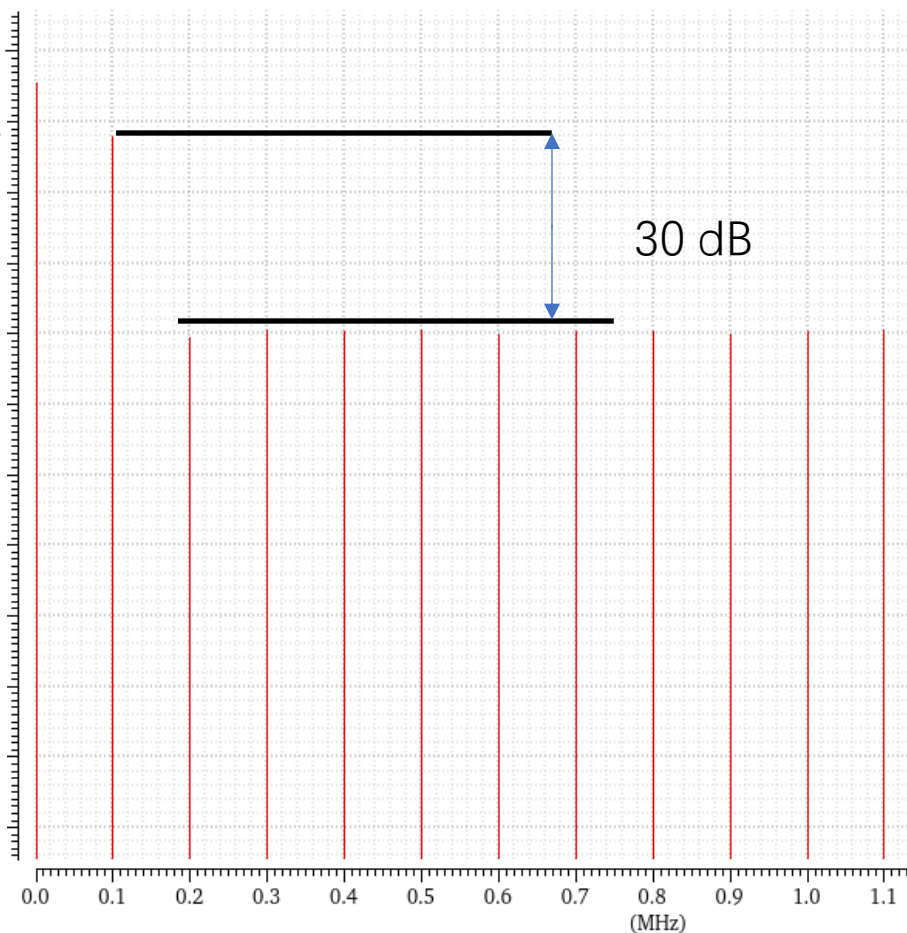
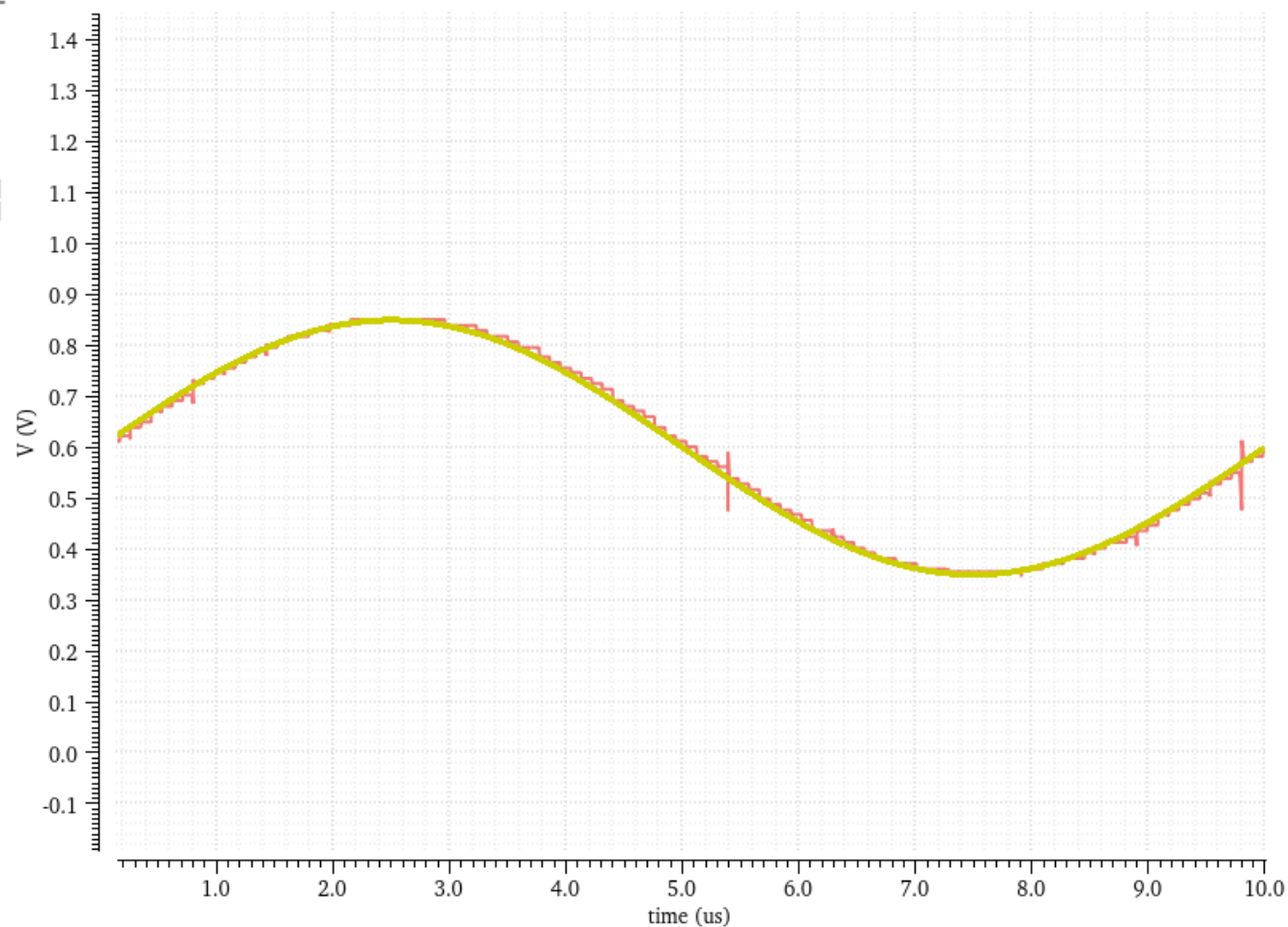
/v+

/I129/v-

/vdd

/I129/q<8:0>

/I129/set<8:0>



Simulation – 500K Hz

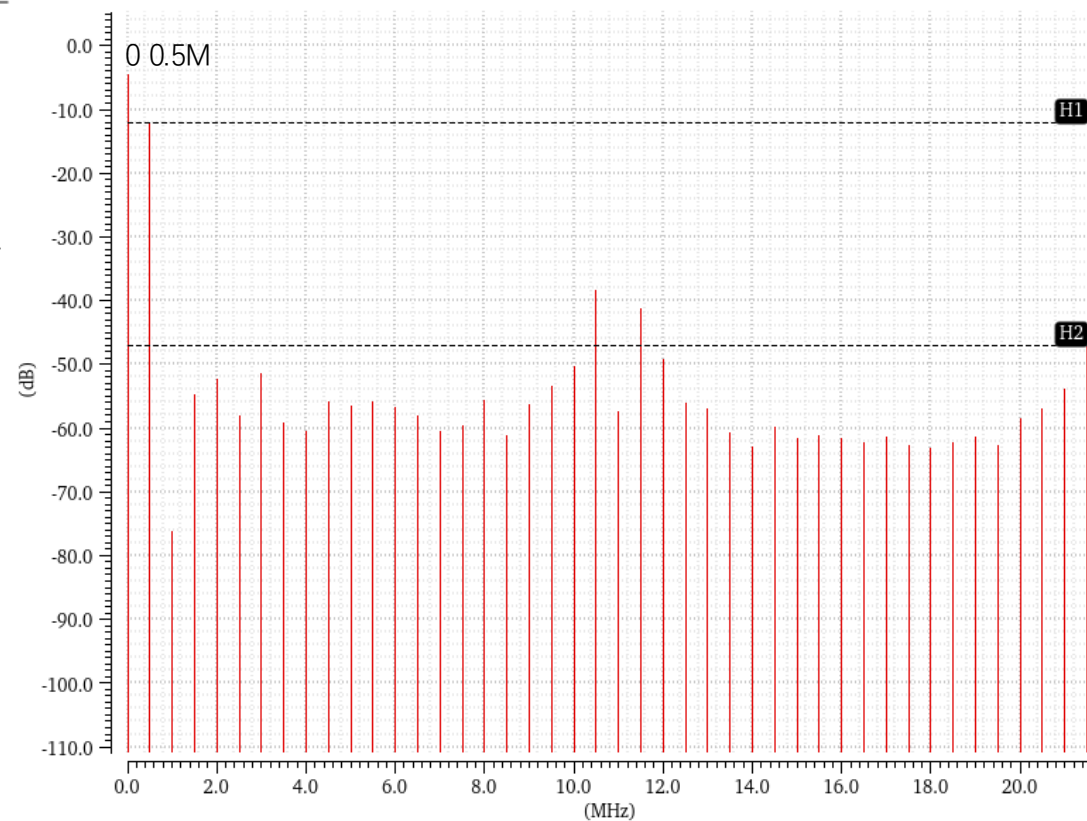
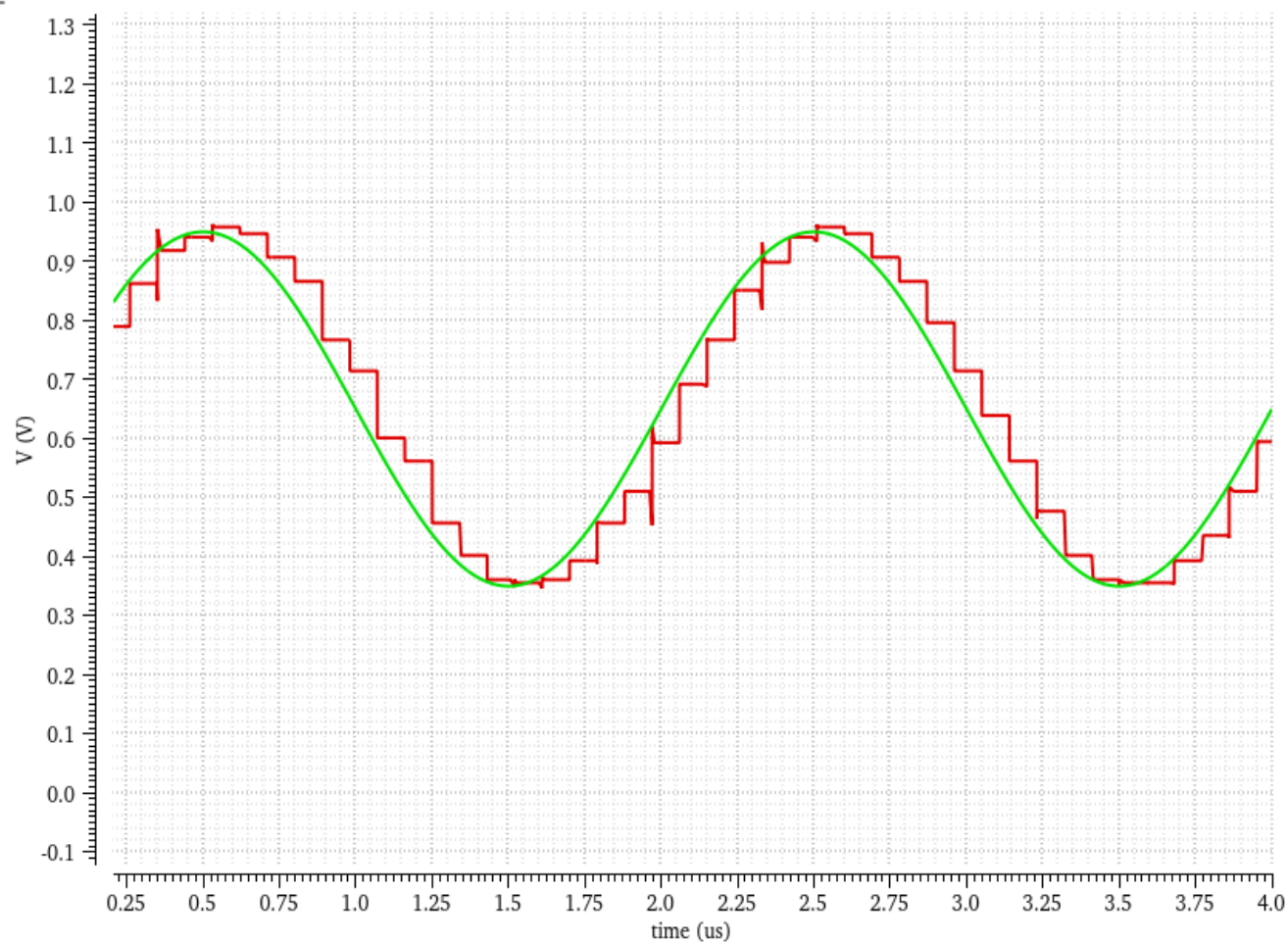
db20(dft(v("/DAC_out" ?result "tran") 1u 3.000u 1024 "Rectangular" 0 0 1))

Name

spectrum_DAC_out



Thu May 2 19:19:04 2024 1



Simulation – 1M Hz




db20(dft(v("/DAC_out" ?result "tran") 0.0 3.000u 1024 "Rectangular" 0 0 1))

Name	Vis
------	-----

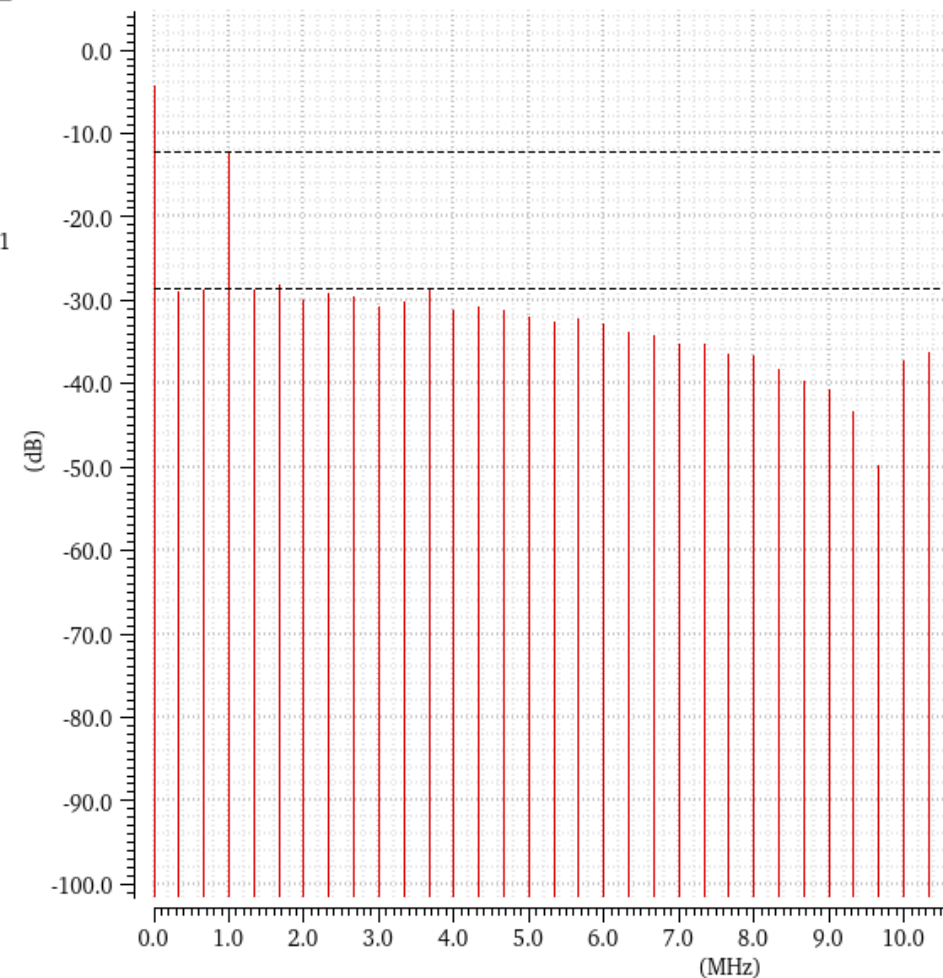
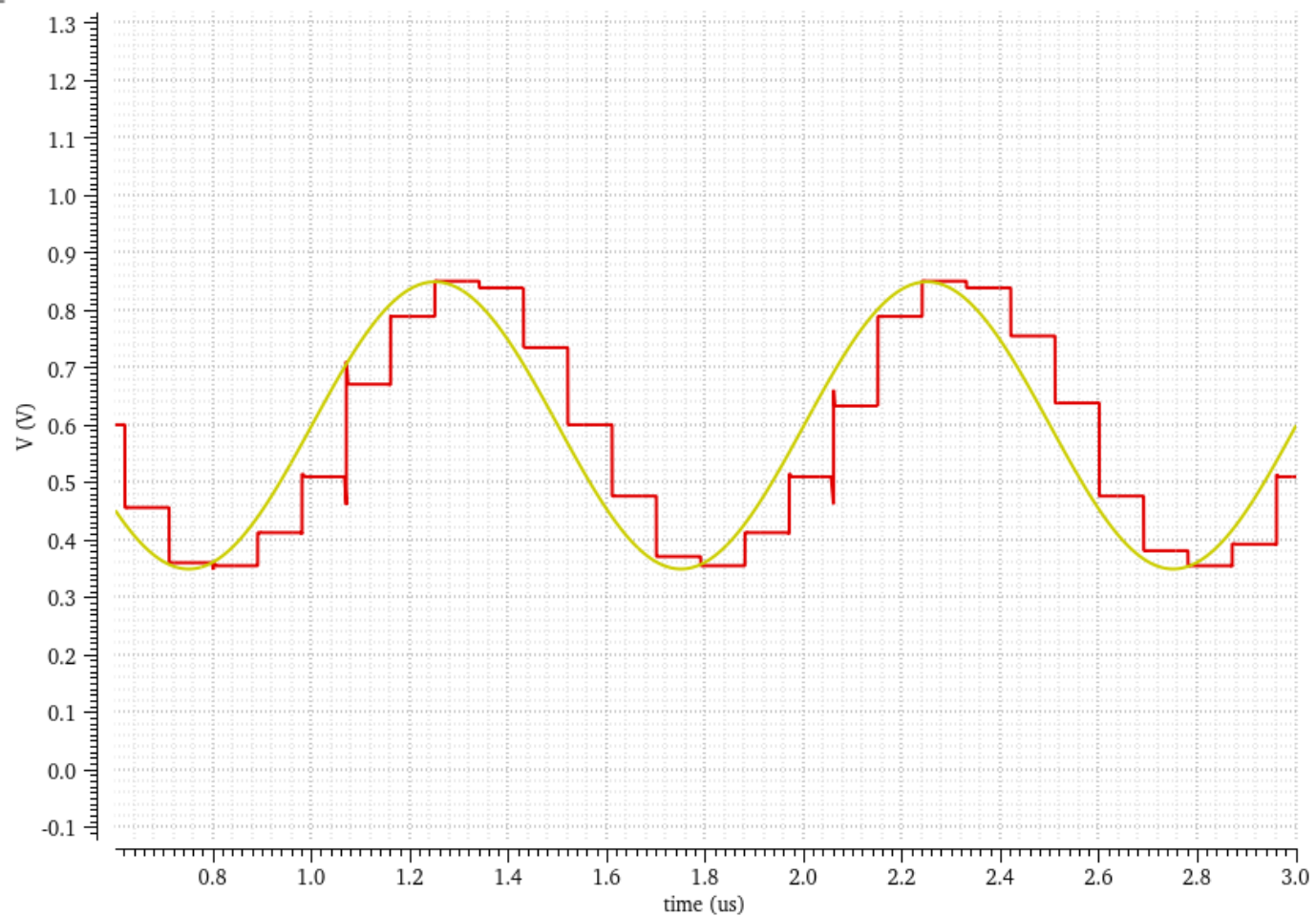
■ spectrum_DAC_out	
---	---

Transient Response

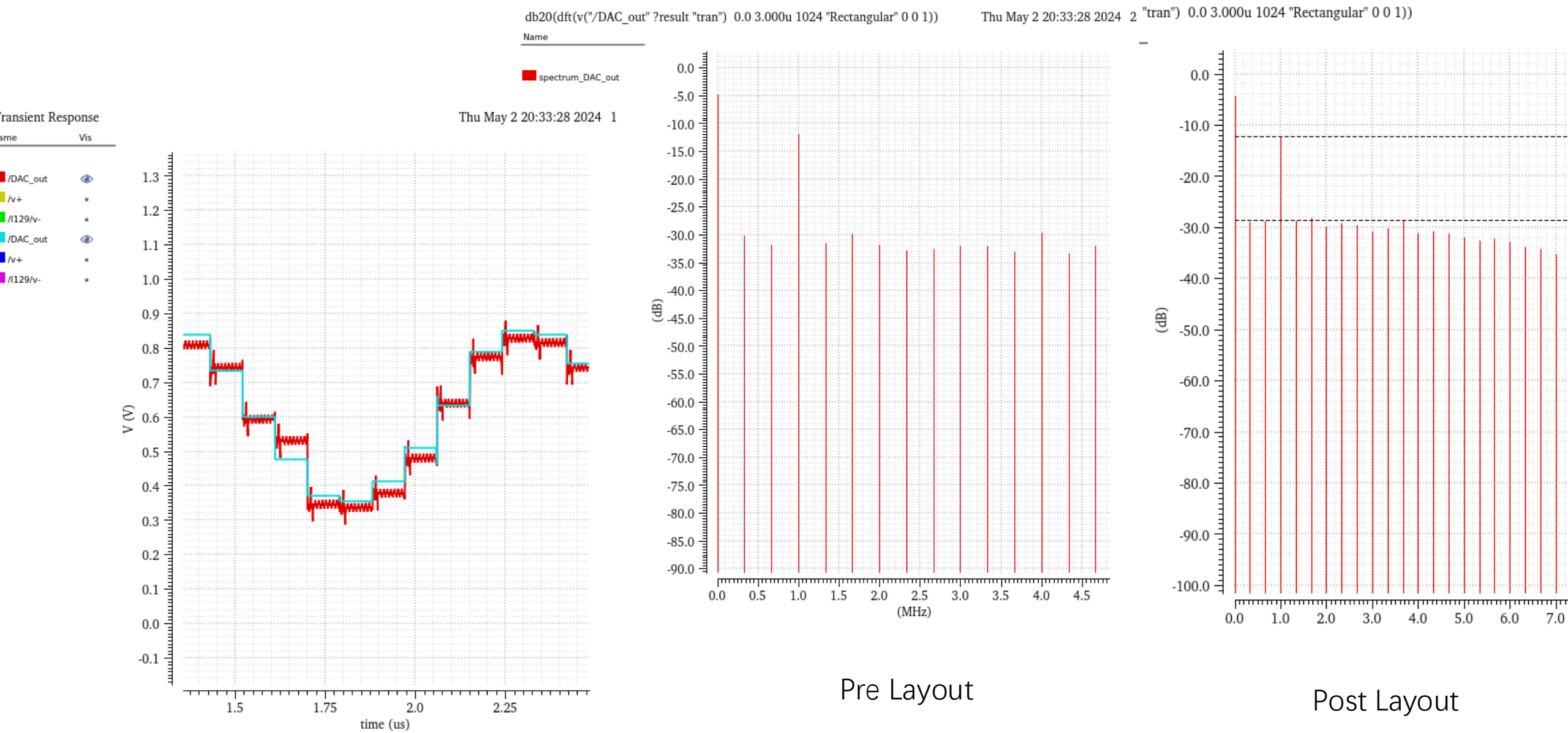
Name	Vis
------	-----

■ /DAC_out	
■ /v+	
■ /I129/v-	

Thu May 2 19:33:34 2024 1



Simulation – 1M Hz, Pre&post layout

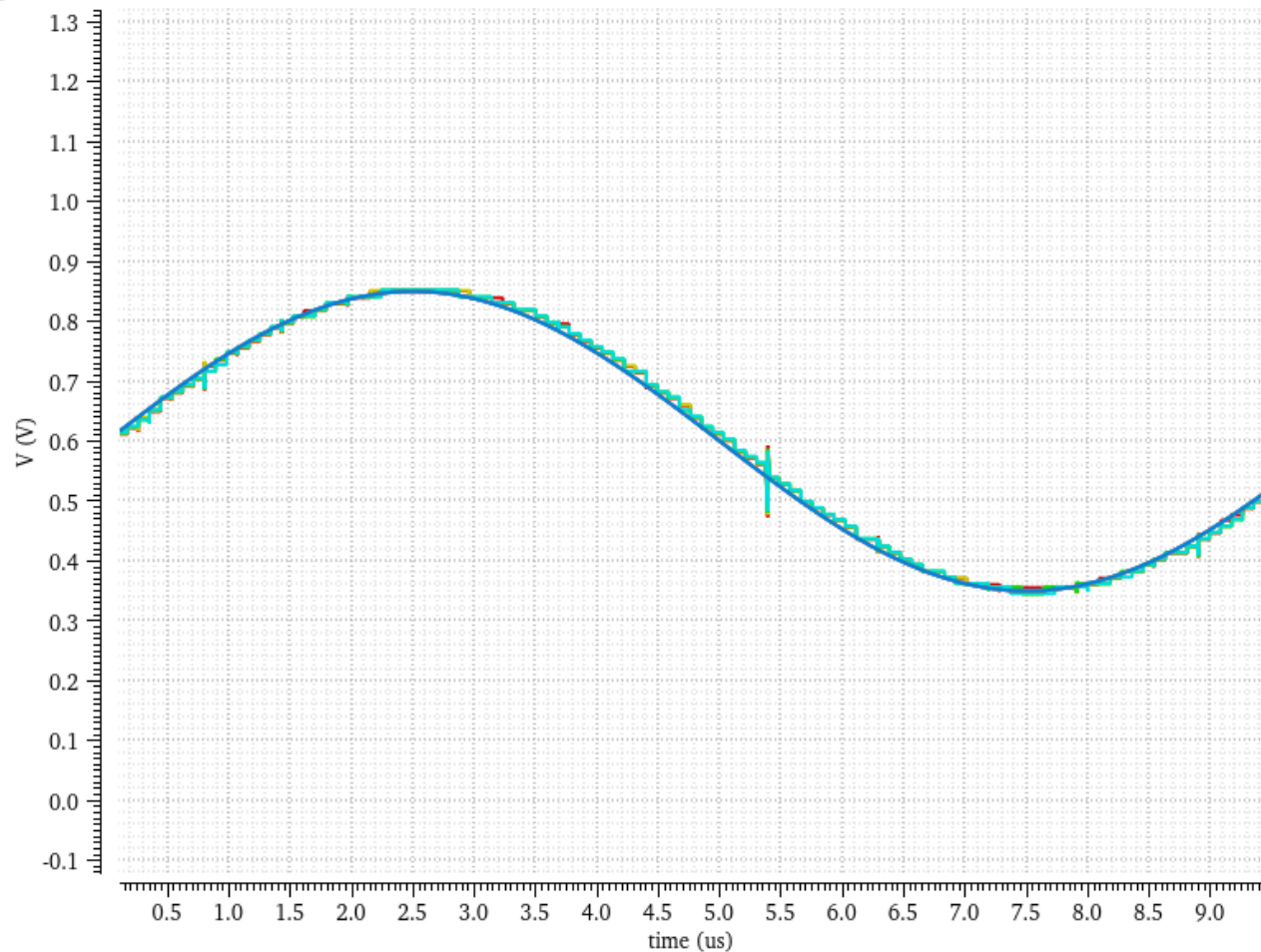


Temp drifting

Transient Response

Thu May 2 23:35:40 2024 1

Name		temp
/DAC_out		
■ /DAC_out		20.0
■ /DAC_out		46.67
■ /DAC_out		73.33
■ /DAC_out		100.0
/v+		
/I129/v-		
/vdd		



Specs

Area: $55 \times 34 - 22.45 \times 8.38 = 1681 \text{ um}^2$

Total inst: 1338

Resolution: 8 Bits

Range: 0.25V ~ 1.2 V

Sampling frequency: 10 MHz