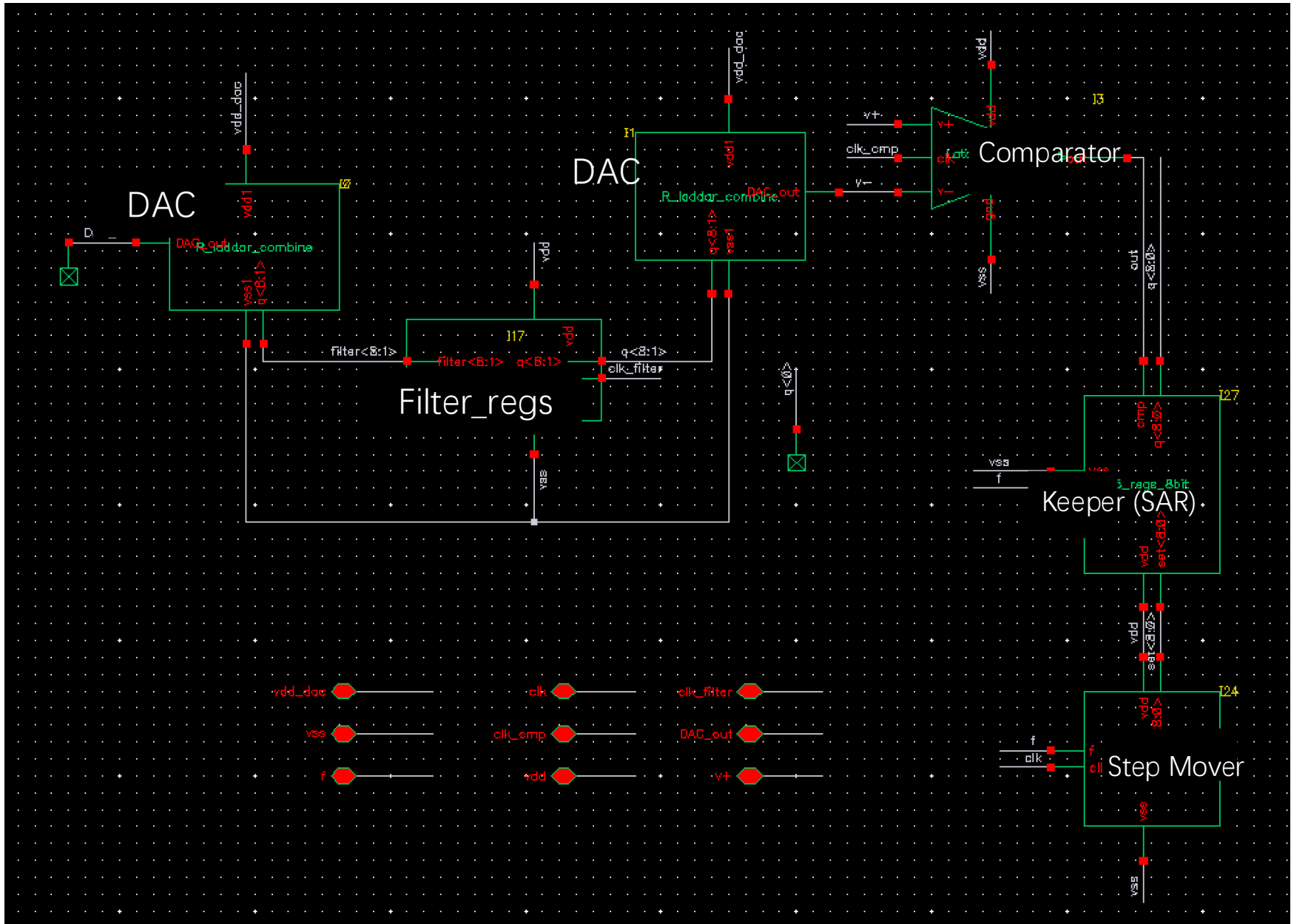
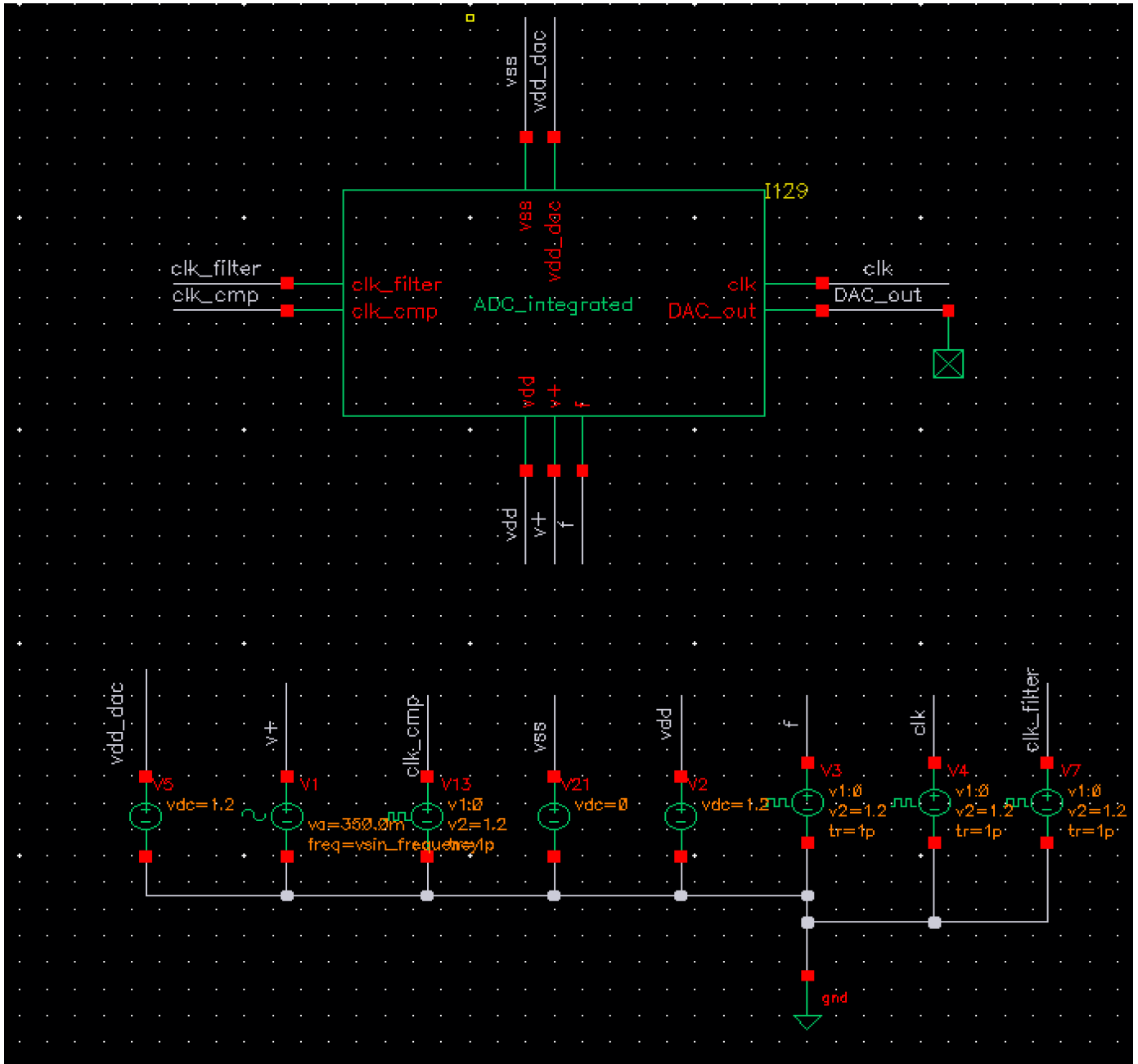
# *SAR - ADC*

Yi Tong

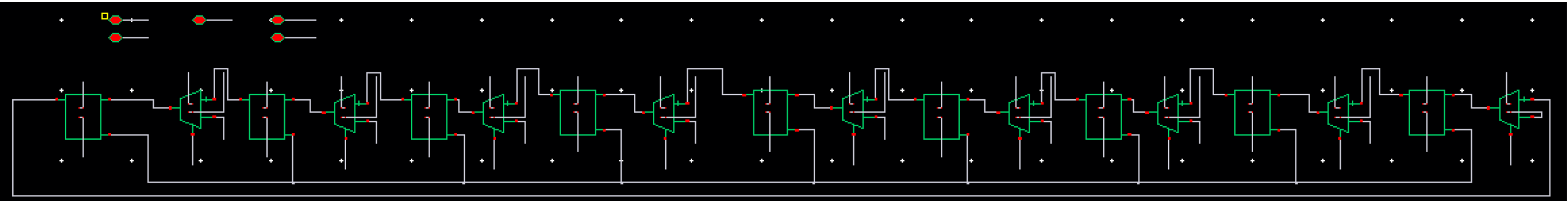
# Schematic

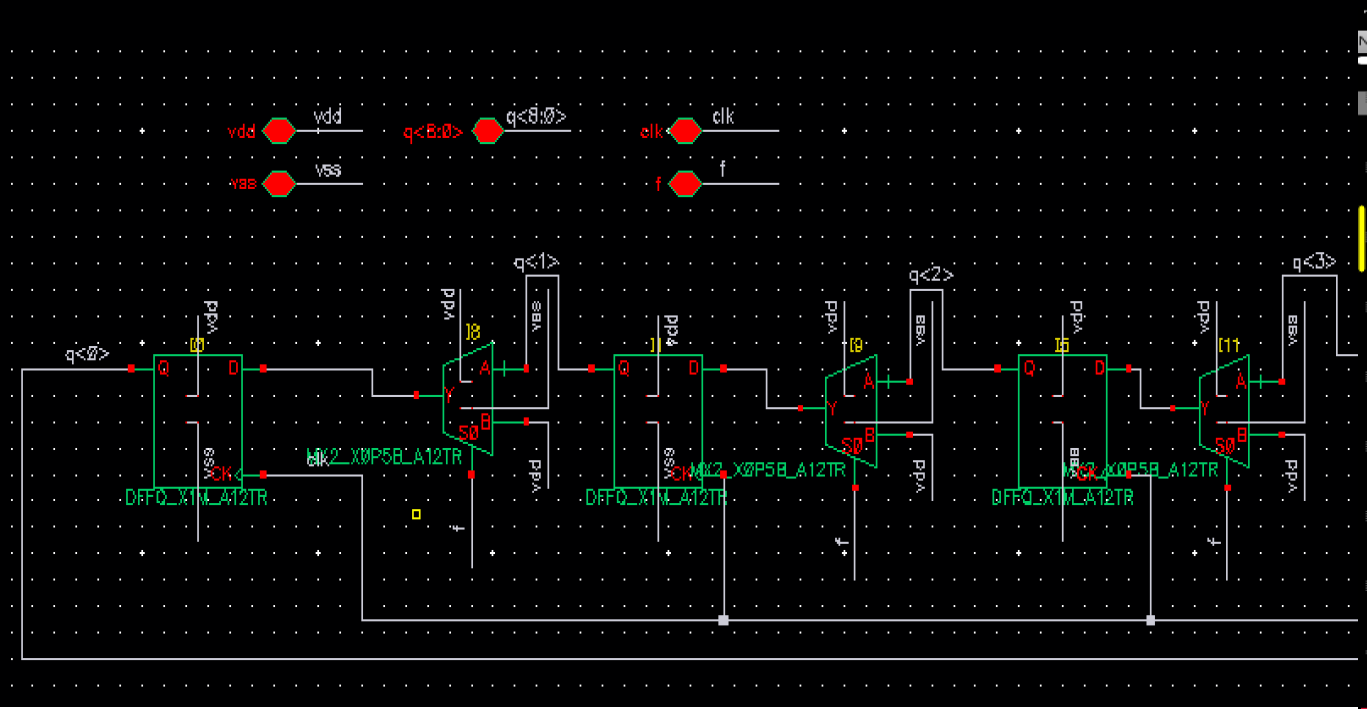

DAC
DAC
Comparator
Filter_regs
Keeper (SAR)
Step Mover
vdd_dac
clk
clk_filter
vss
clk_cmp
DAC_out
f
vdd
v+

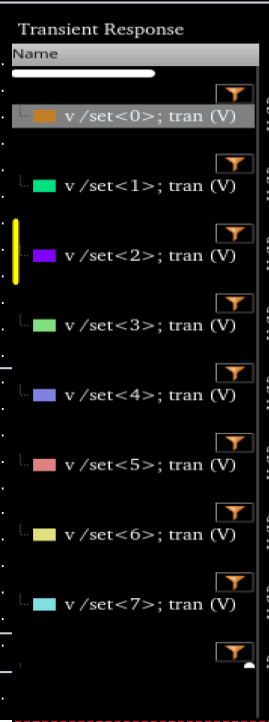
# Top view


vss
vdd_dac
I129
clk_filter
clk_cmp
clk_filter
clk_cmp
ADC_integrated
clk
DAC_out
clk
DAC_out
vdd
v+
f
vdd_dac
v+
clk_cmp
vss
vdd
f
clk
clk_filter
V5
vdc=1.2
V1
va=350.0m
freq=vsin_frequency
V13
v1:0
v2=1.2
V21
vdc=0
V2
vdc=1.2
V3
v1:0
v2=1.2
tr=1p
V4
v1:0
v2=1.2
tr=1p
V7
v1:0
v2=1.2
tr=1p
gnd

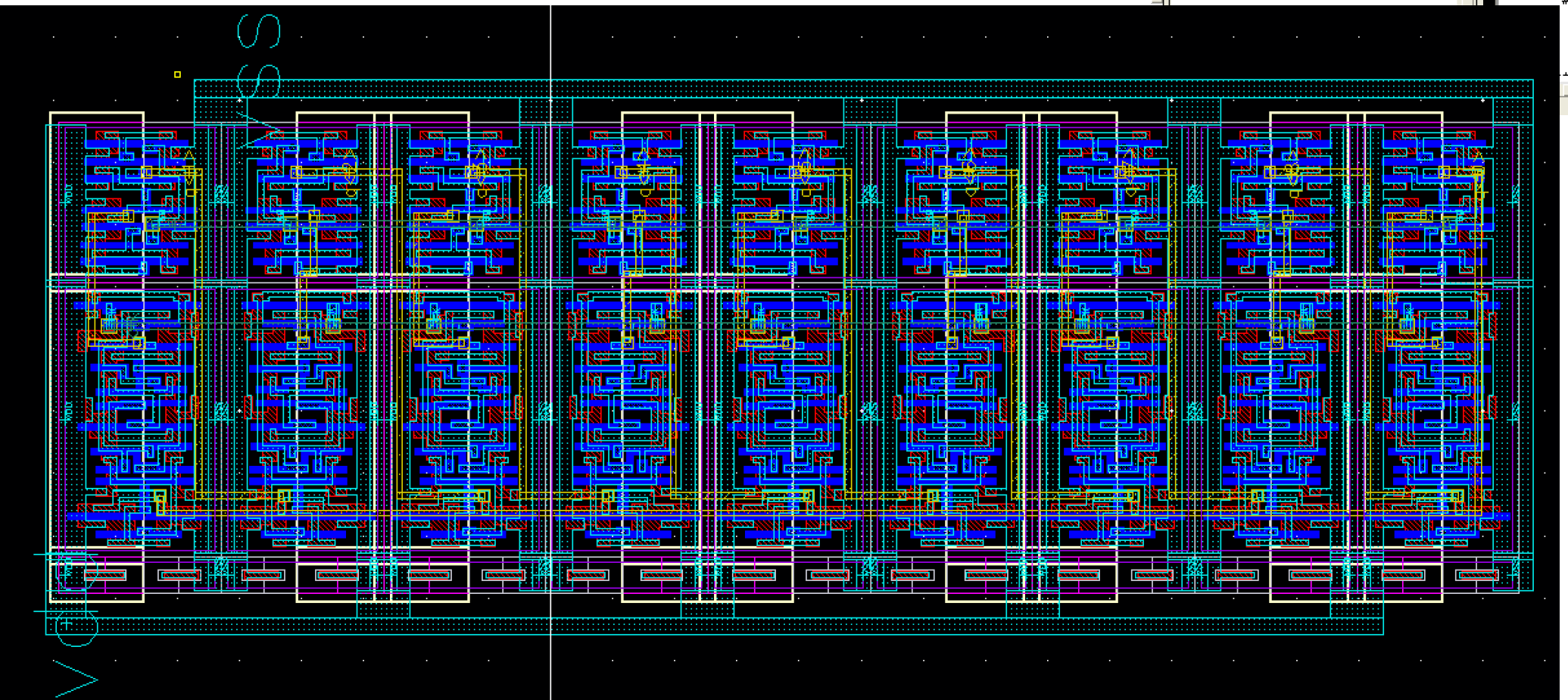
# Set Mover- schematic

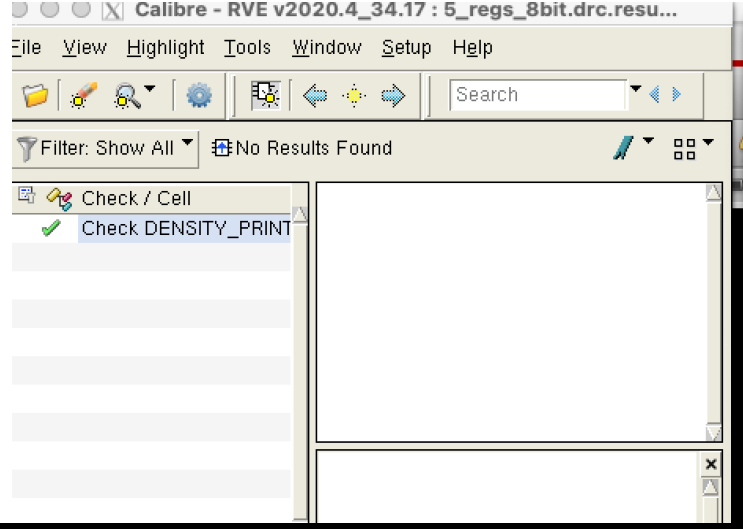


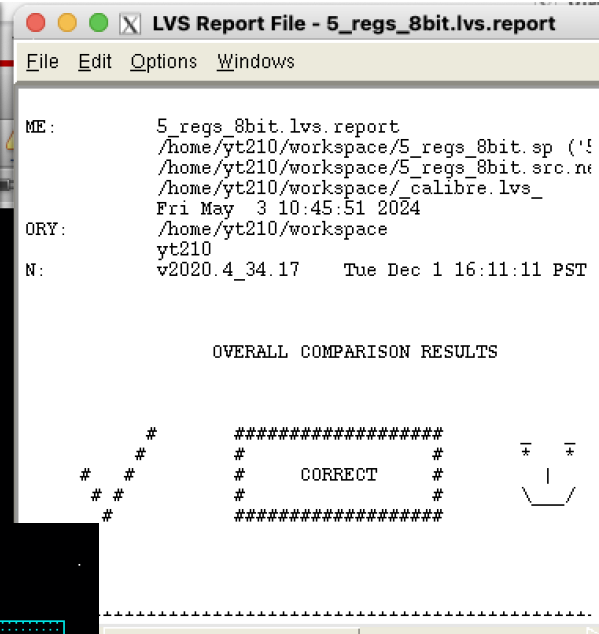


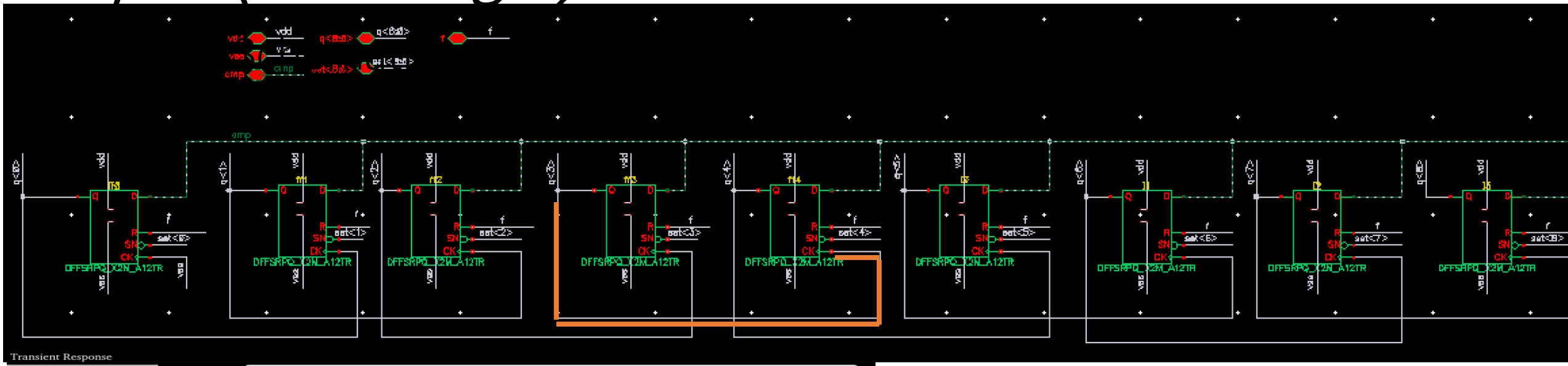

# Set Mover - Layout



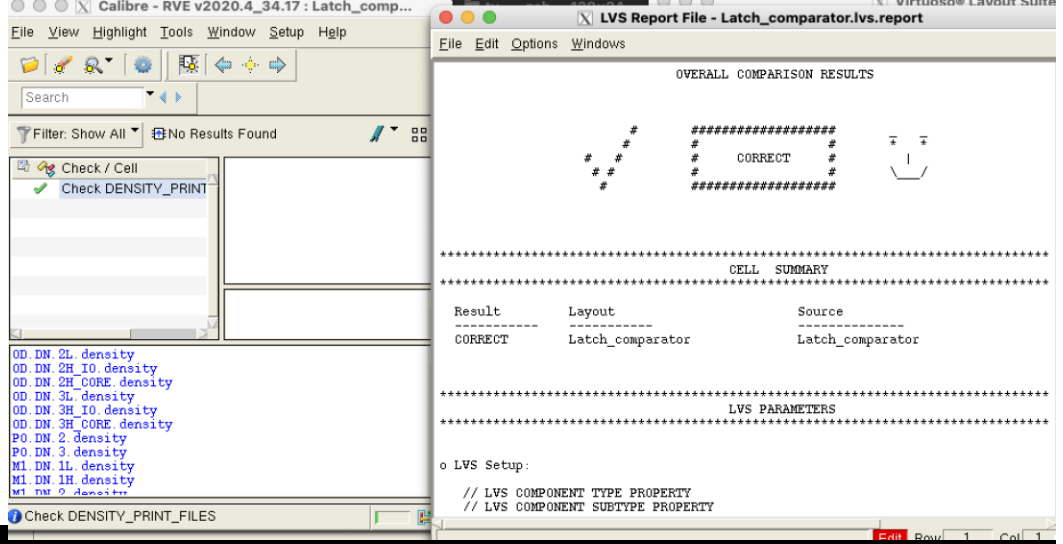


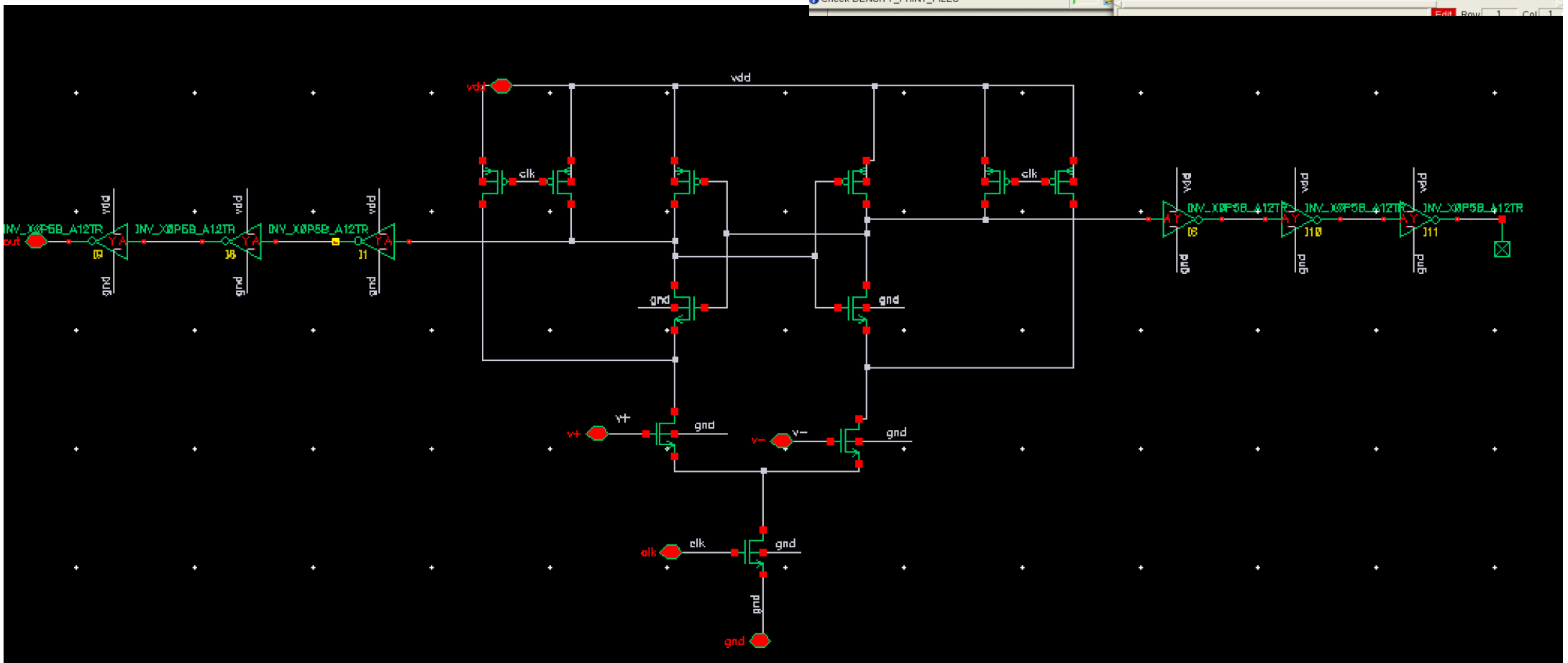



# Keeper (SAR Logic)

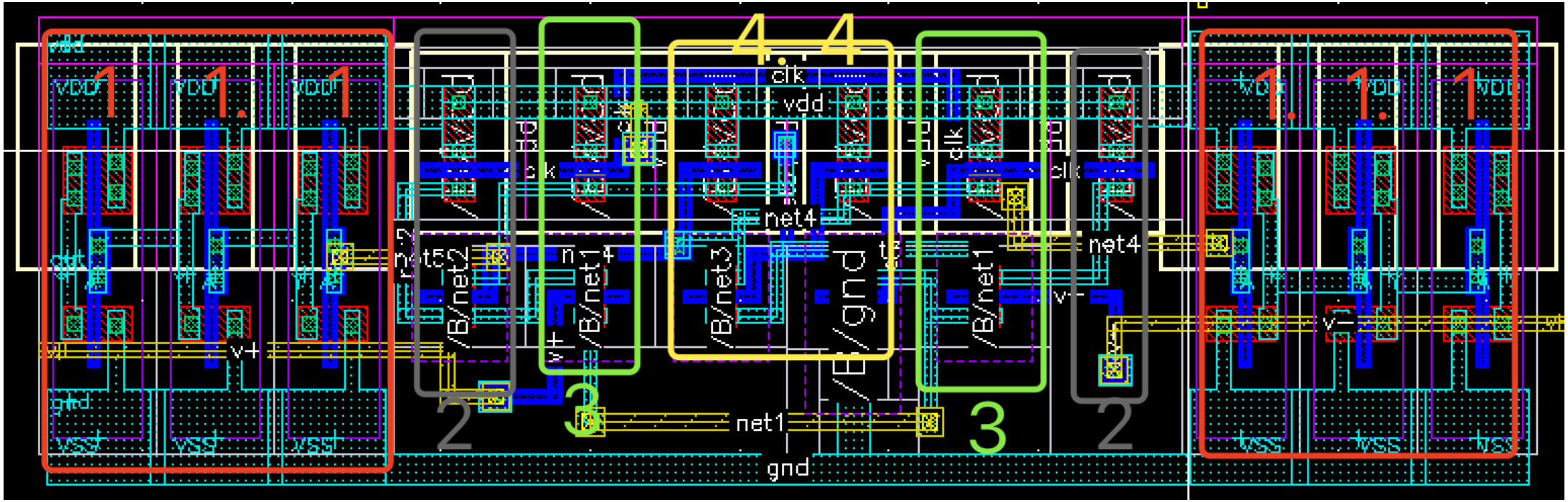



# Comparator - schematic

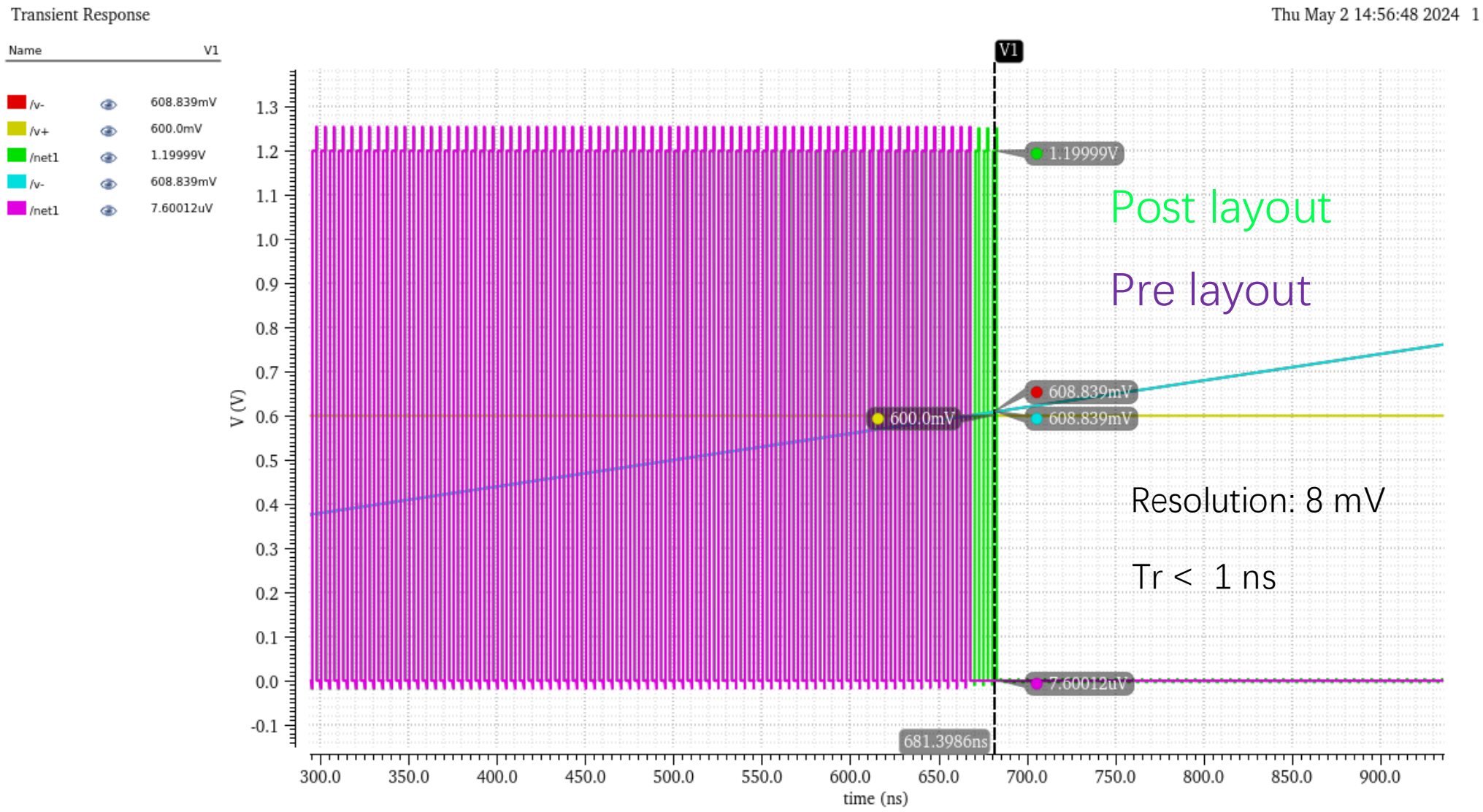


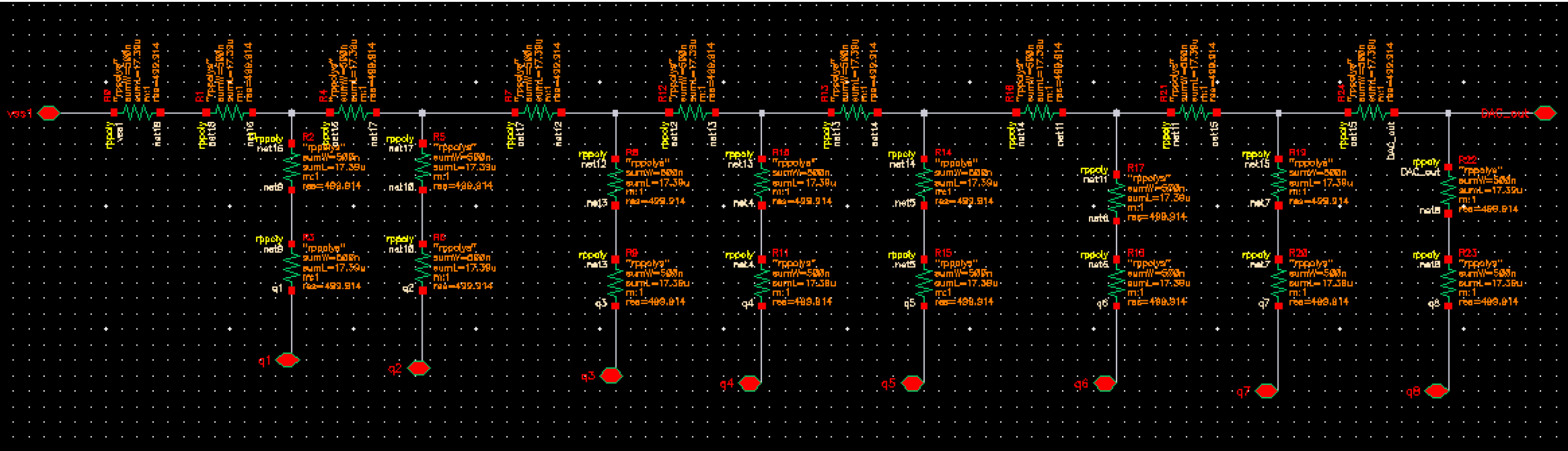
# *Comparator – layout*



# Comparator – simulation (pre&post)

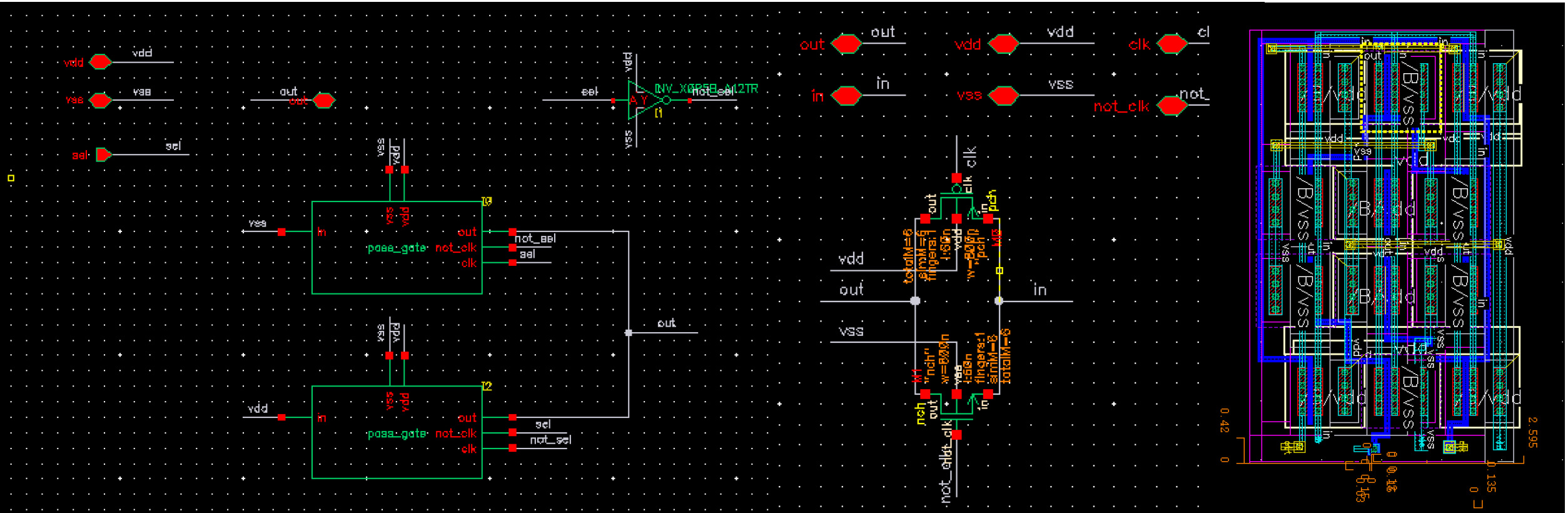


# DAC-R 2R Laddar (Resistor tree)

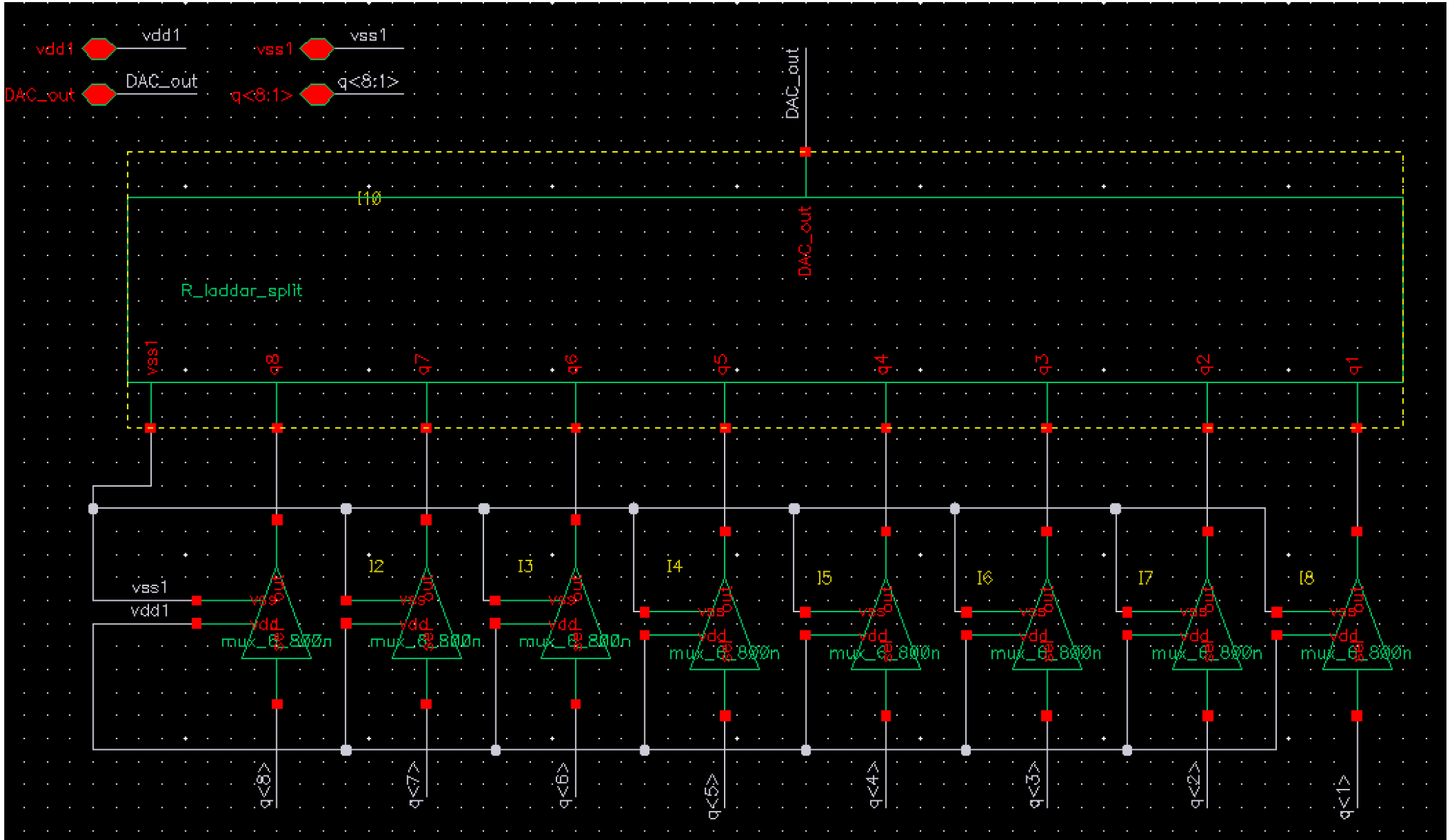


# *DAC-R 2R Laddar (Switches)*

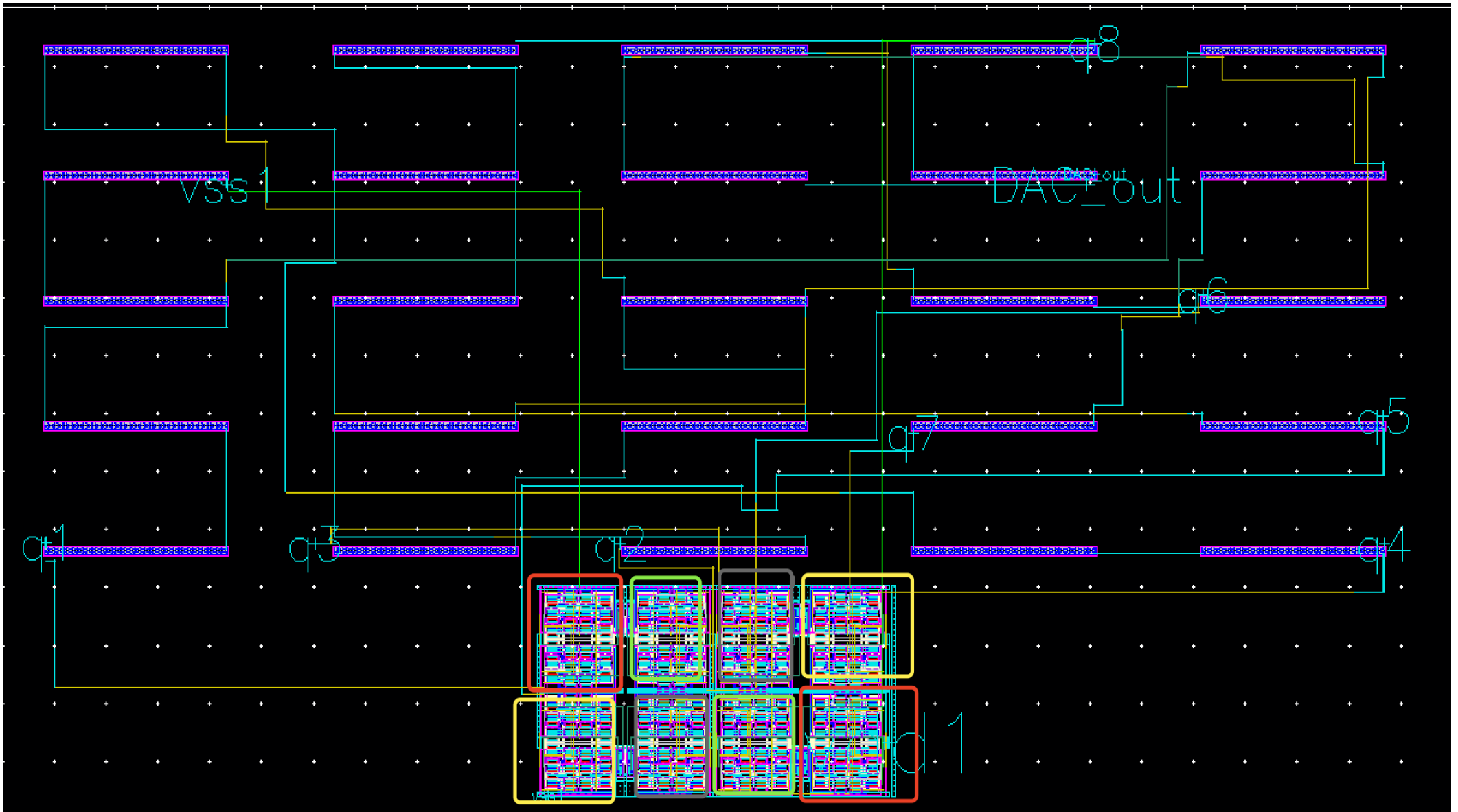
T_gate size: w = 5u, l = 60n
Inverter: library



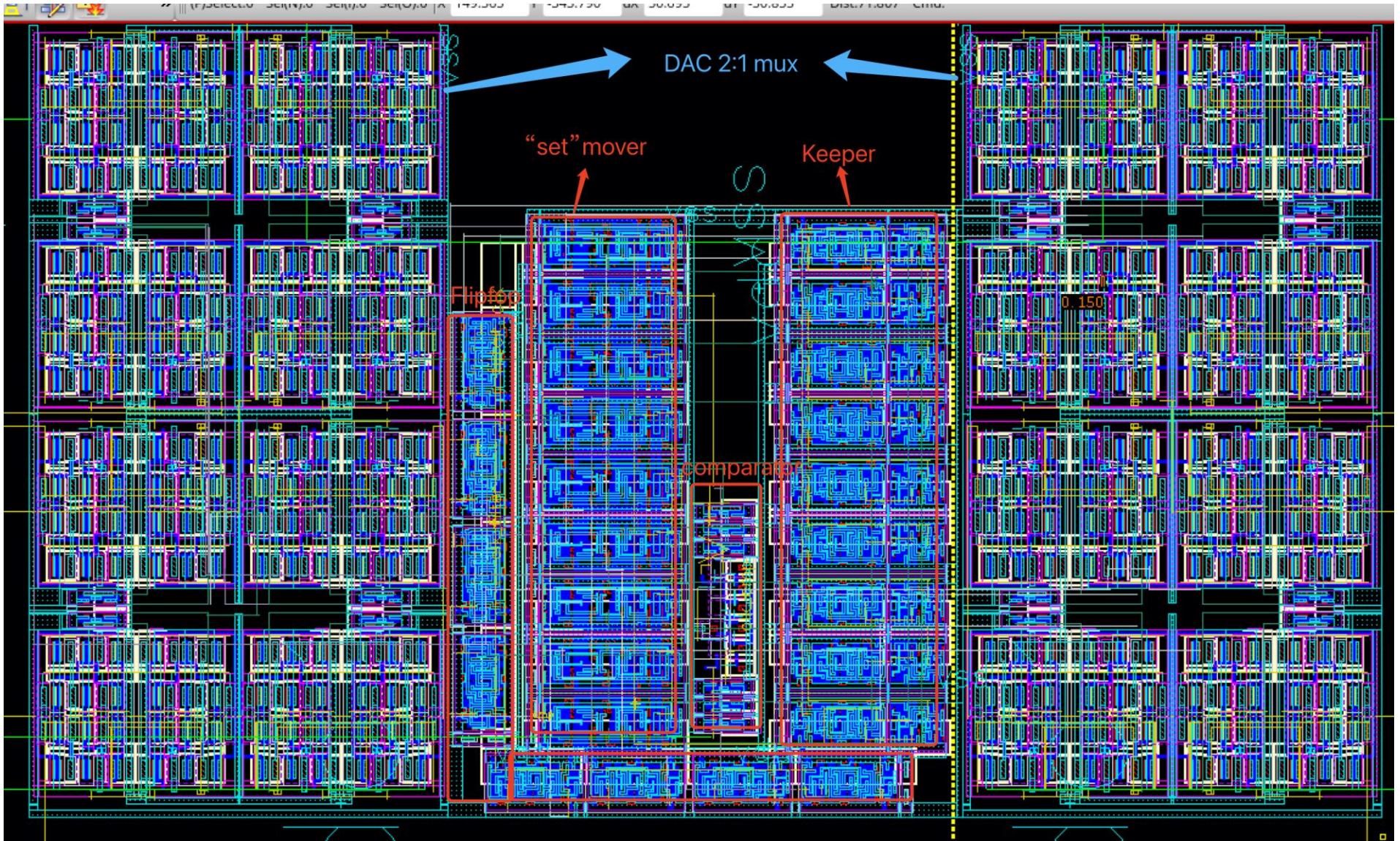
# DAC-R2R Laddar (whole)



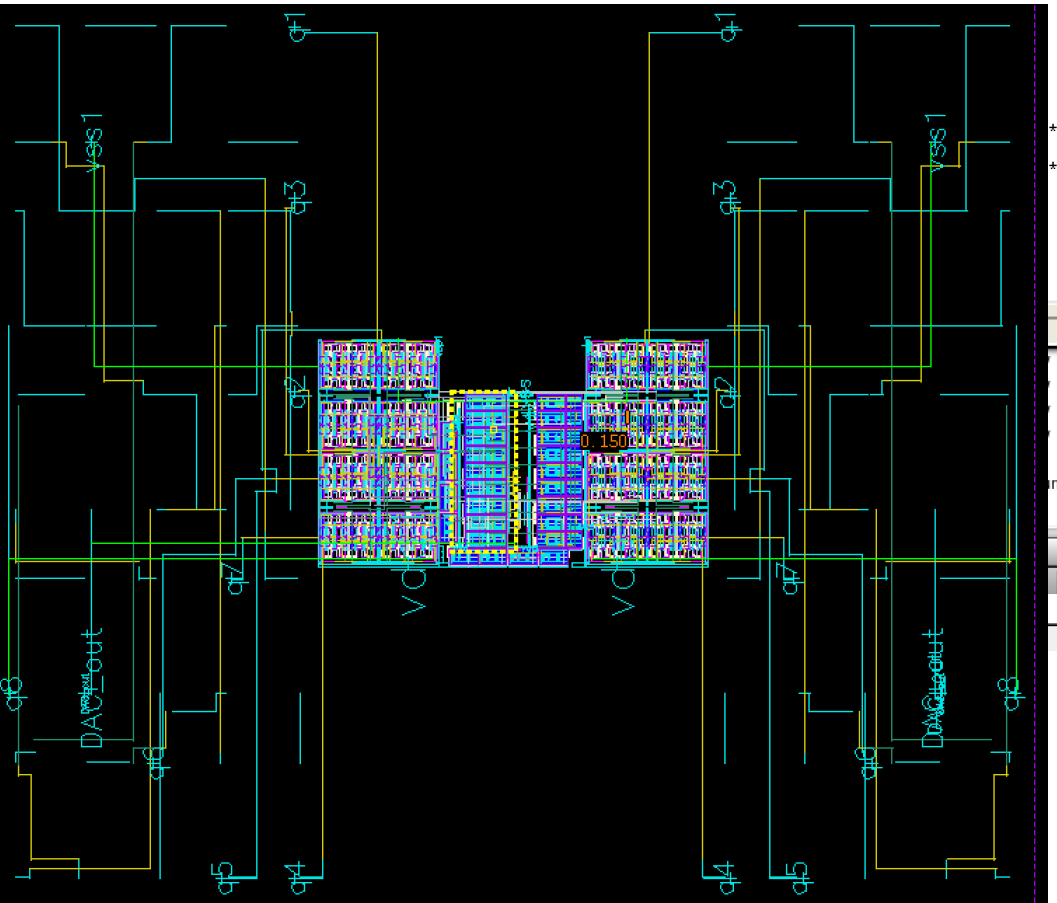
# DAC-R2R Laddar

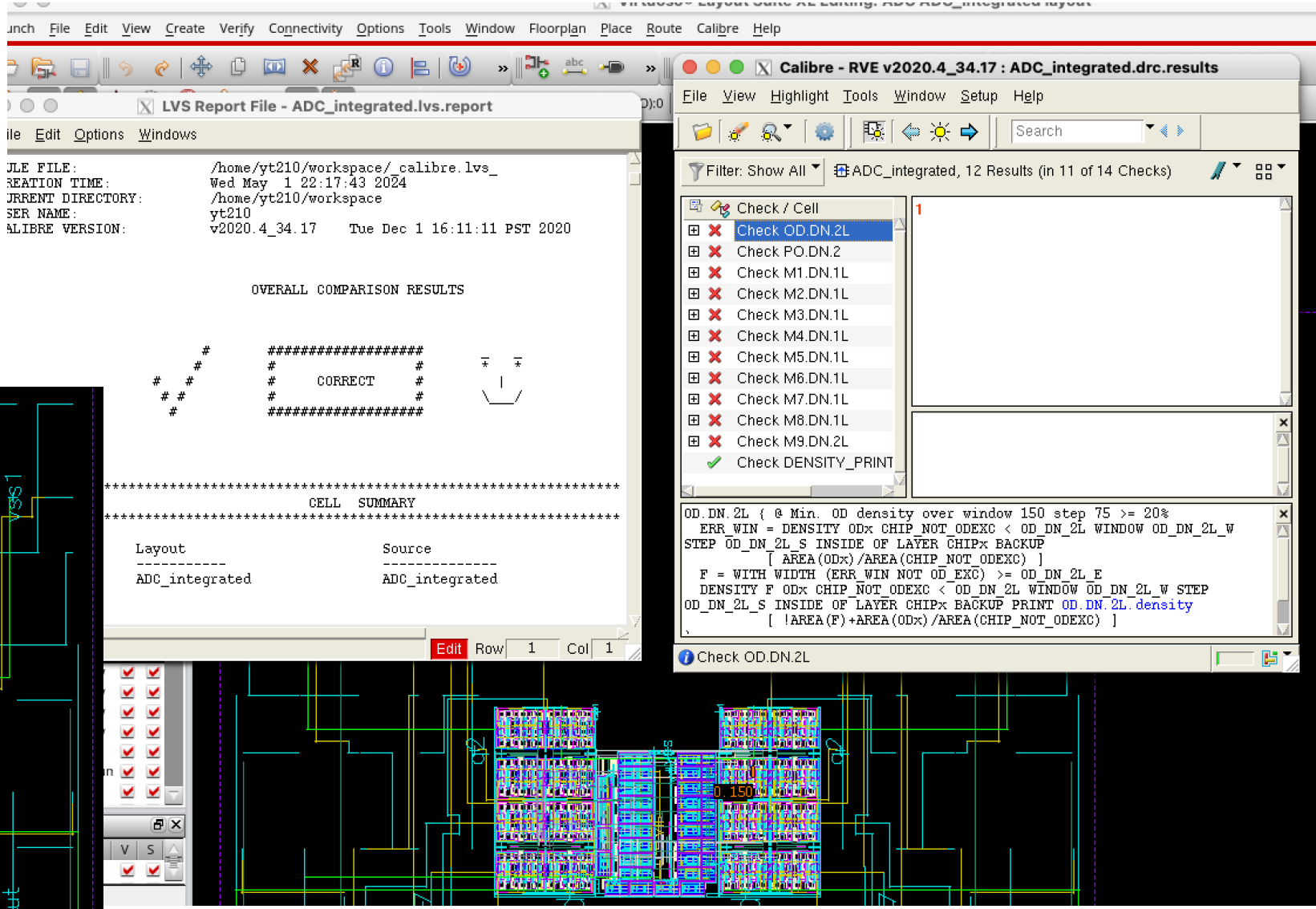


# *Layout (except rpoly)*



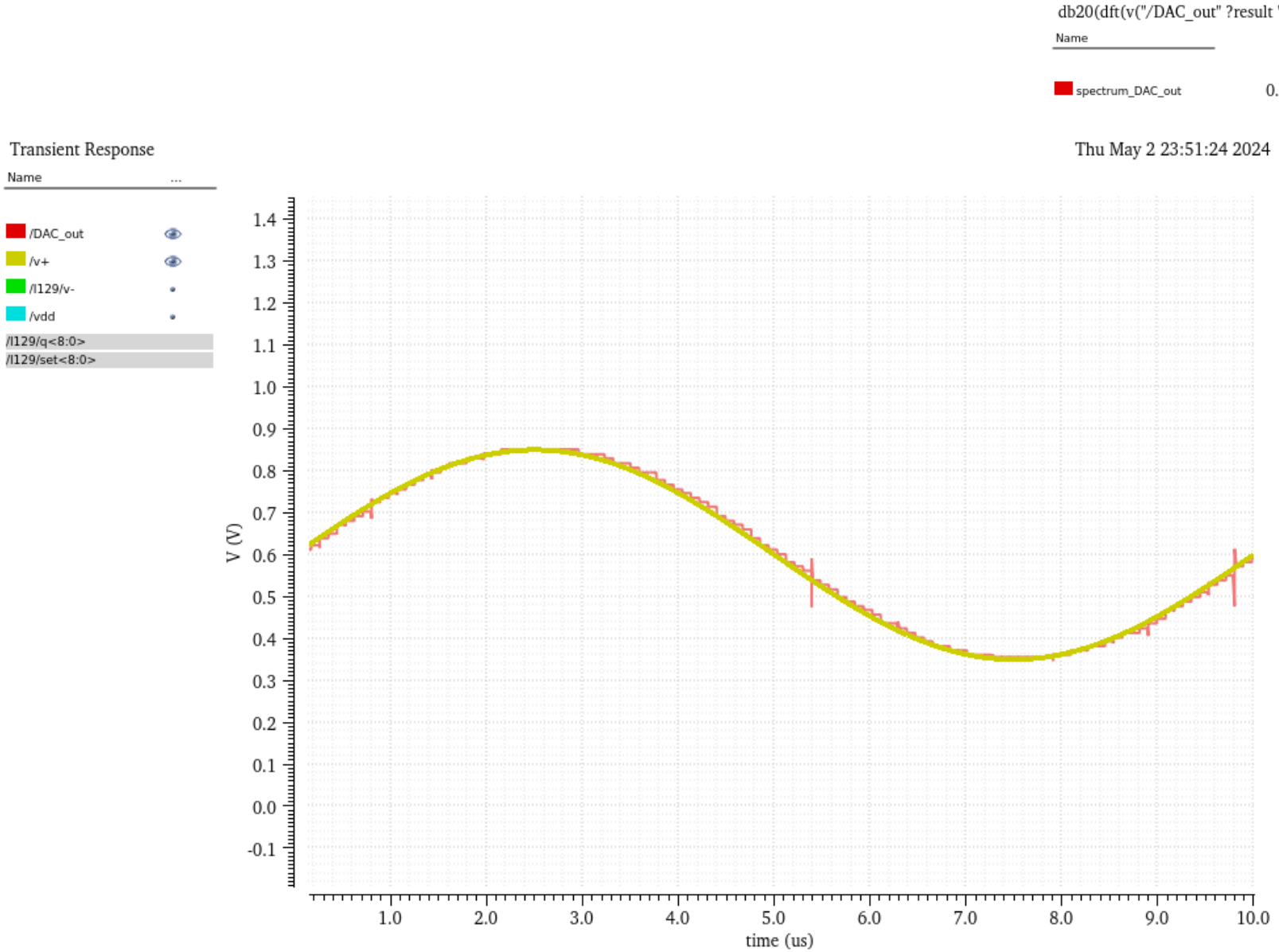
# *Full Layout*

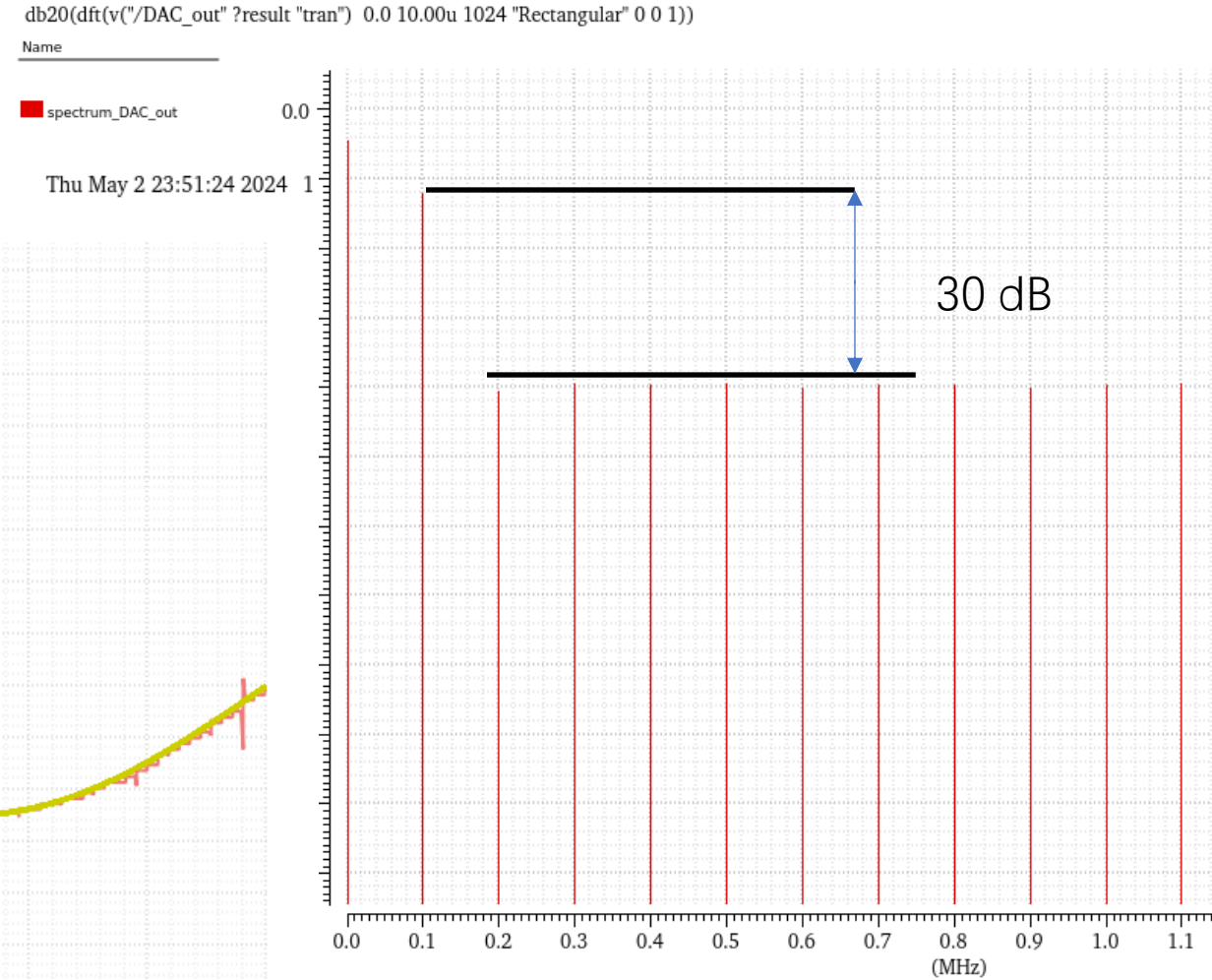




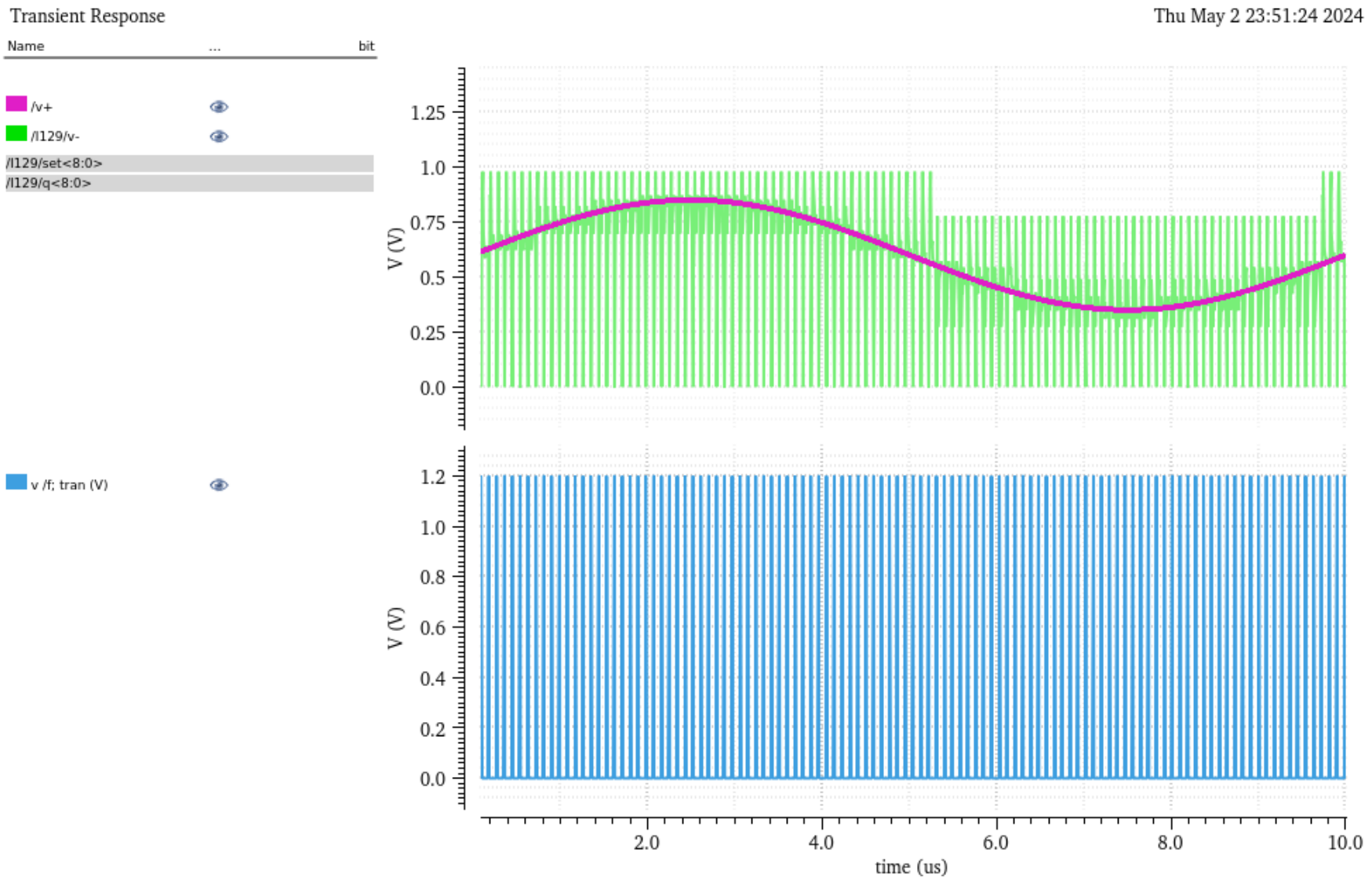

- All clean

# SAR Extracted result – 100K Hz

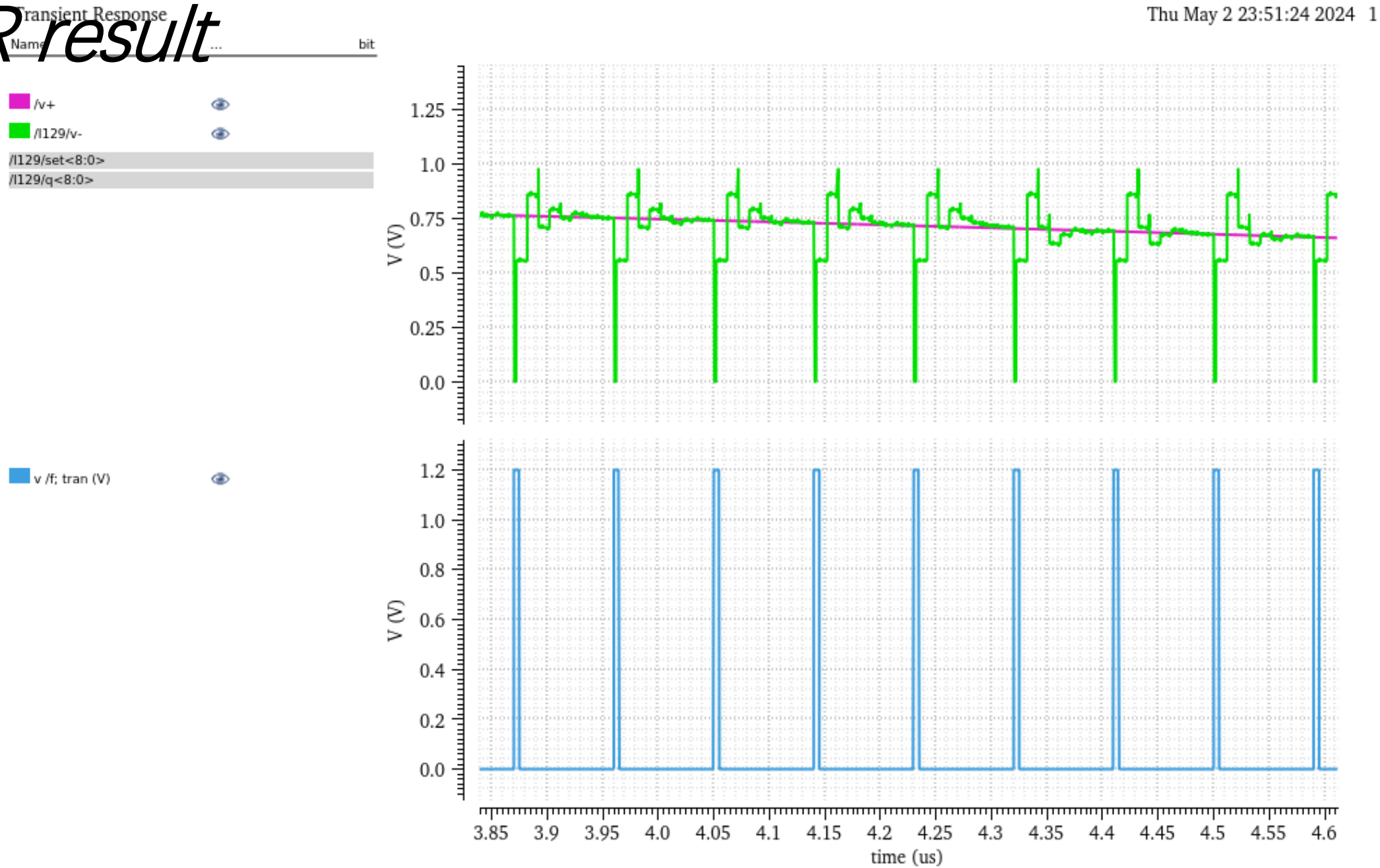


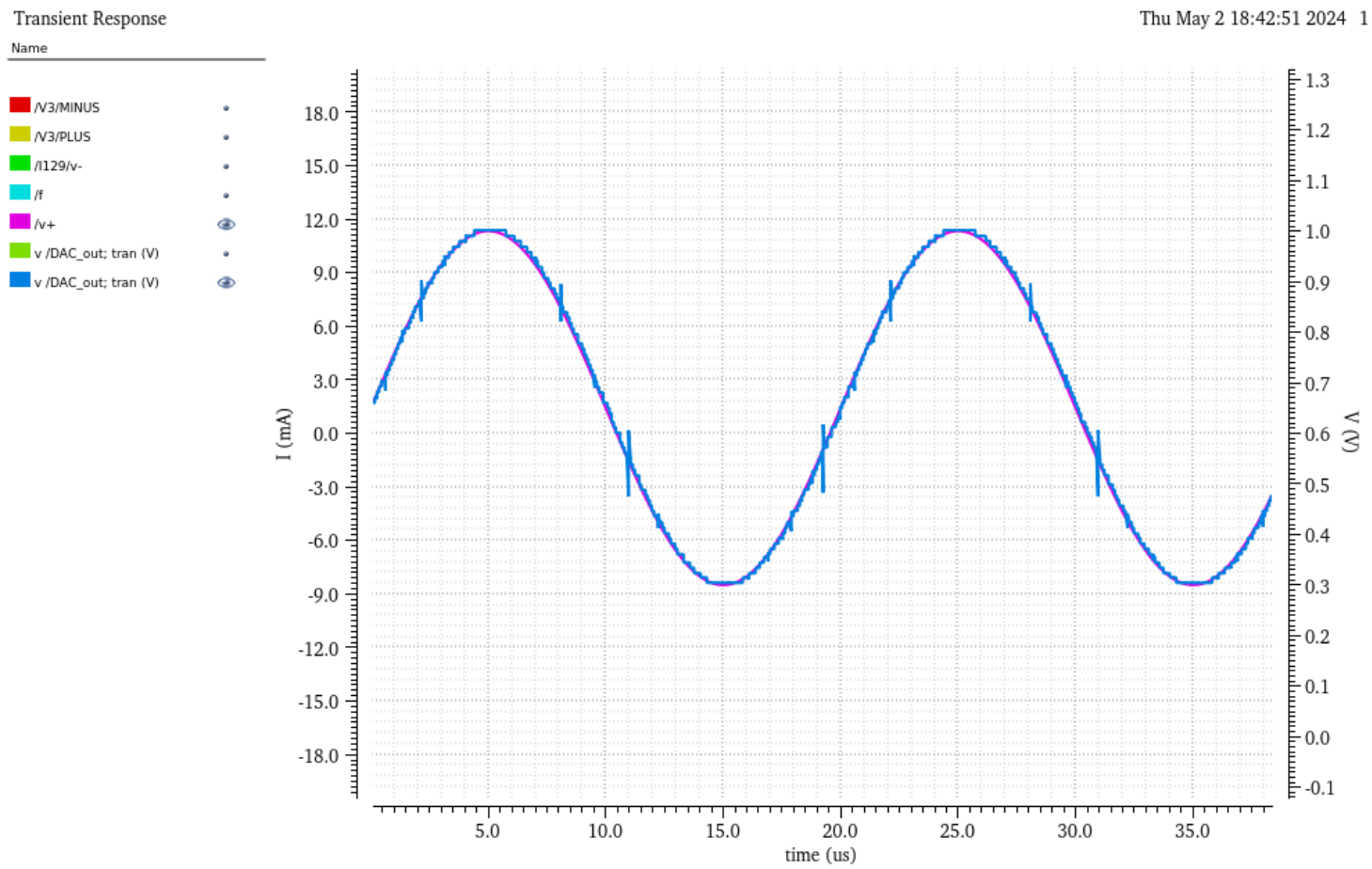
# SAR result

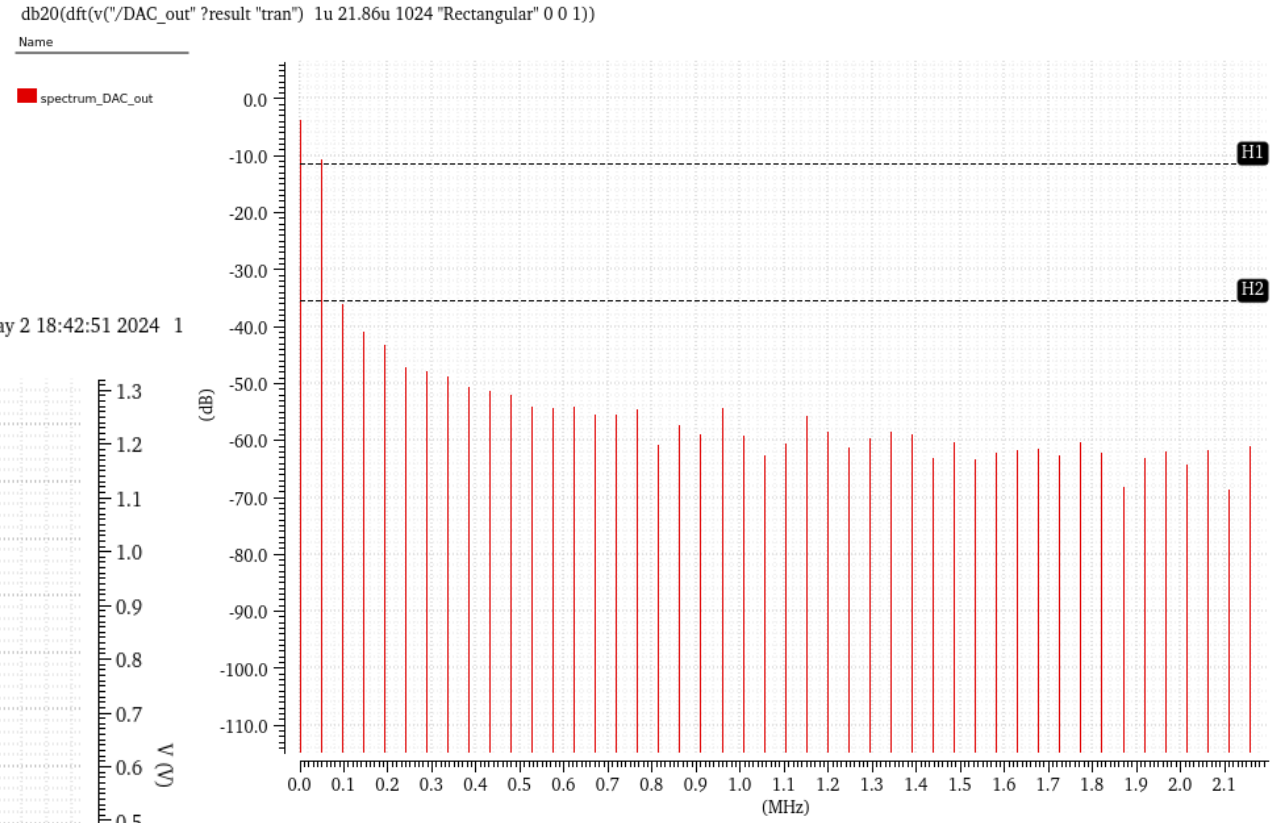

Transient Response
Thu May 2 23:51:24 2024 1
Name
...
bit
/v+
/I129/v-
/I129/set<8:0>
/I129/q<8:0>
v /f; tran (V)
V (V)
1.25
1.0
0.75
0.5
0.25
0.0
V (V)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
2.0
4.0
6.0
8.0
10.0
time (us)

# SAR result

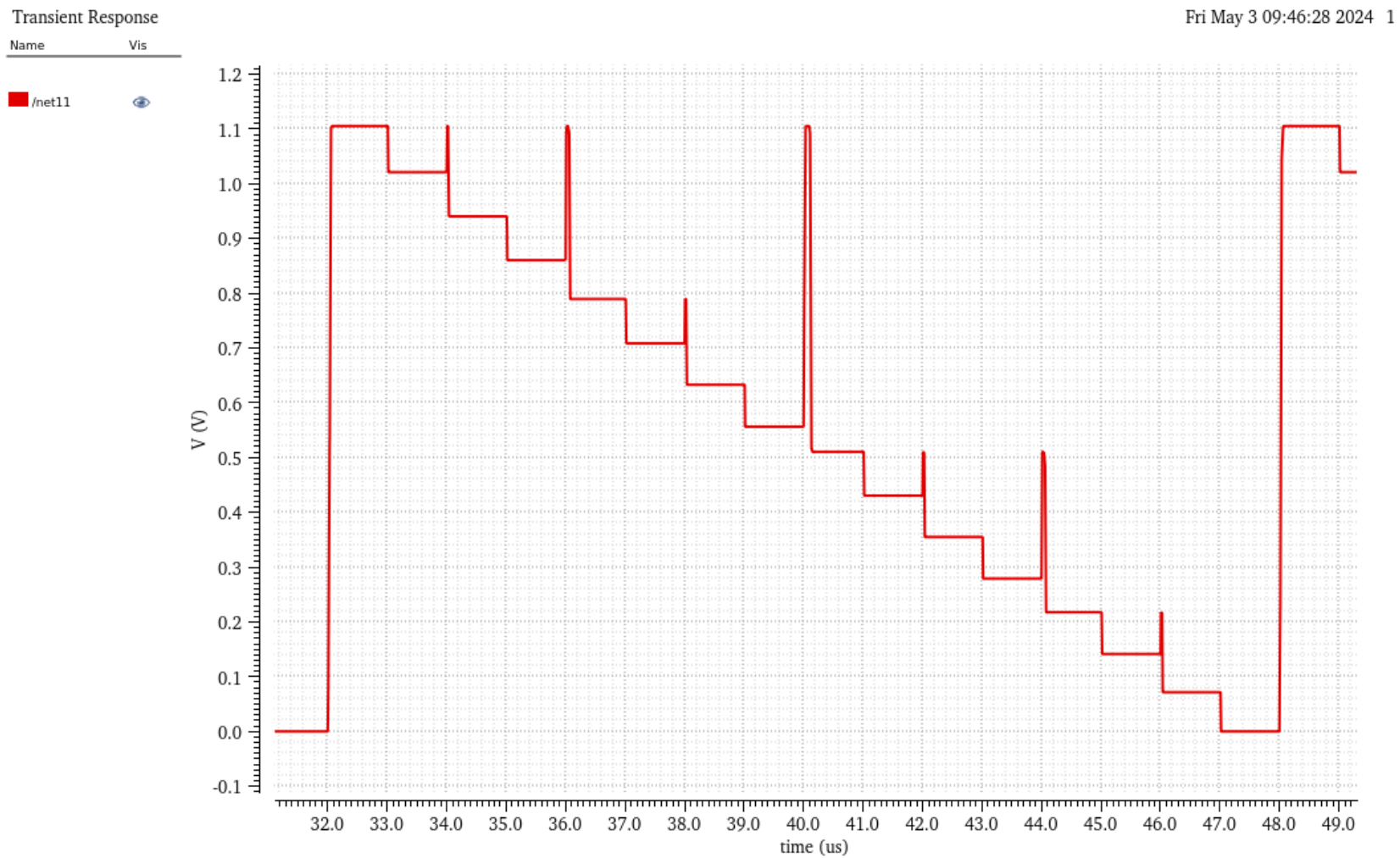

Transient Response
Thu May 2 23:51:24 2024 1
Nam
bit
/v+
/I129/v-
/I129/set<8:0>
/I129/q<8:0>
v /f; tran (V)
V (V)
1.25
1.0
0.75
0.5
0.25
0.0
V (V)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
3.85
3.9
3.95
4.0
4.05
4.1
4.15
4.2
4.25
4.3
4.35
4.4
4.45
4.5
4.55
4.6
time (us)

# Simulation – 50K Hz

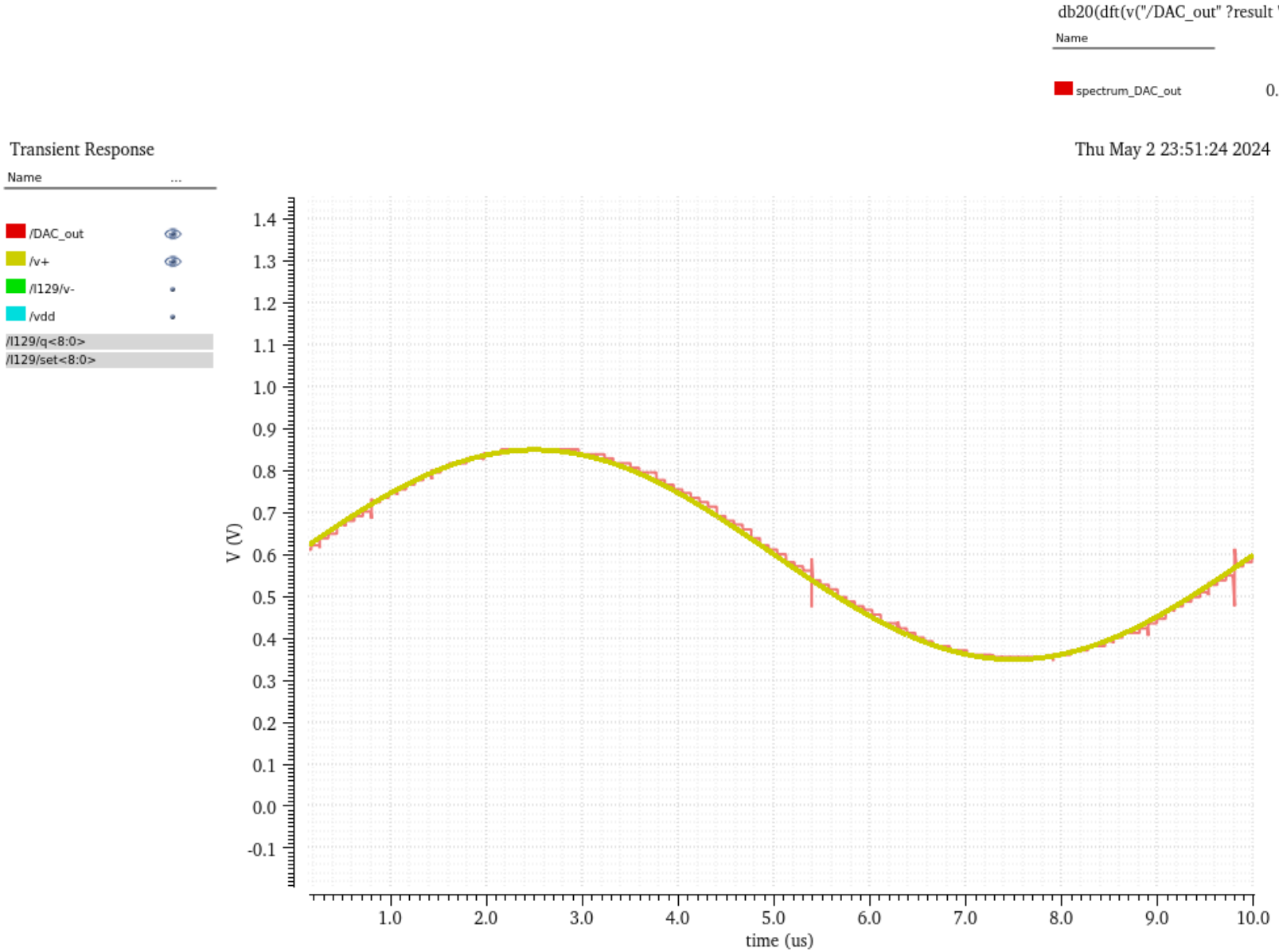


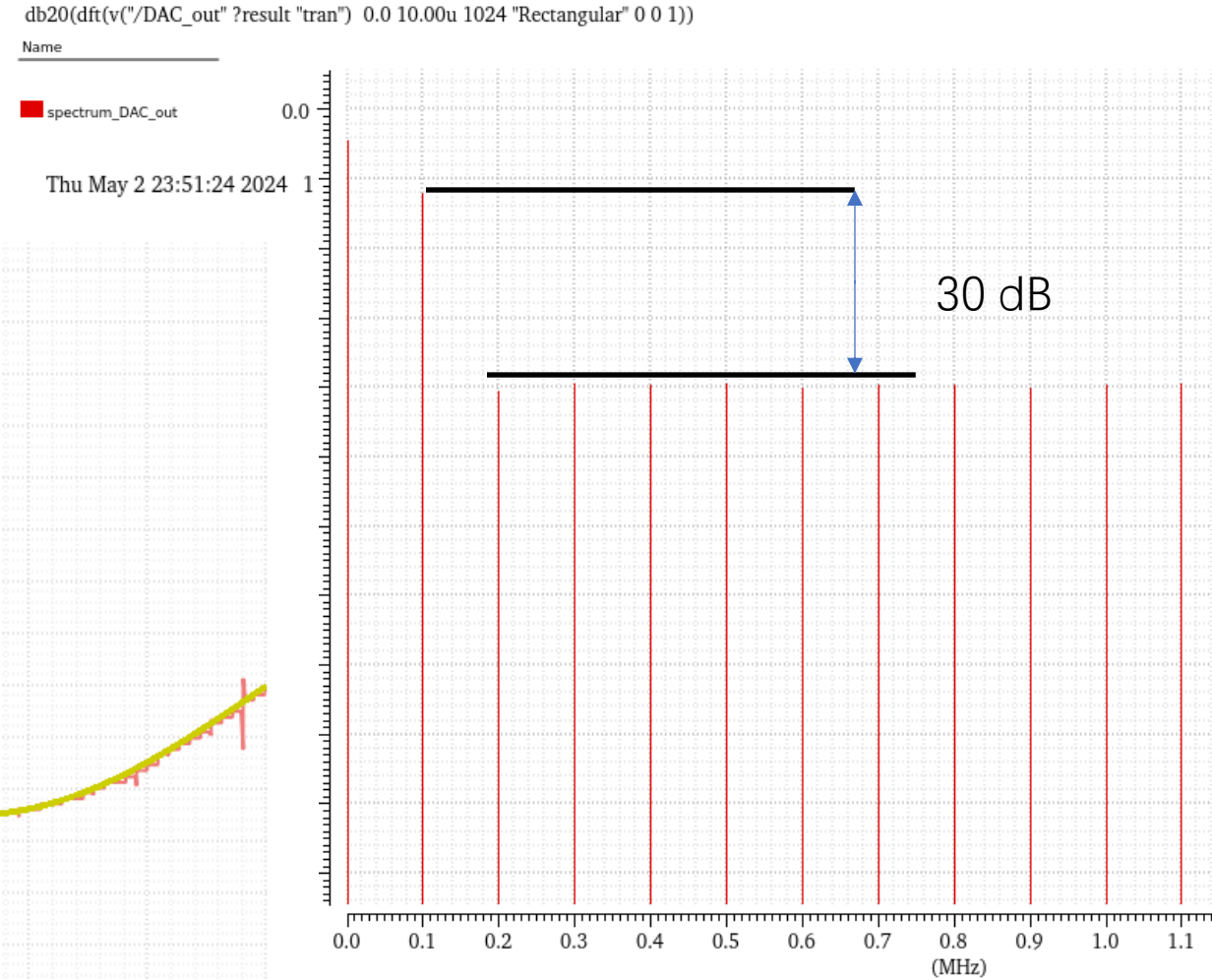



# Defects:

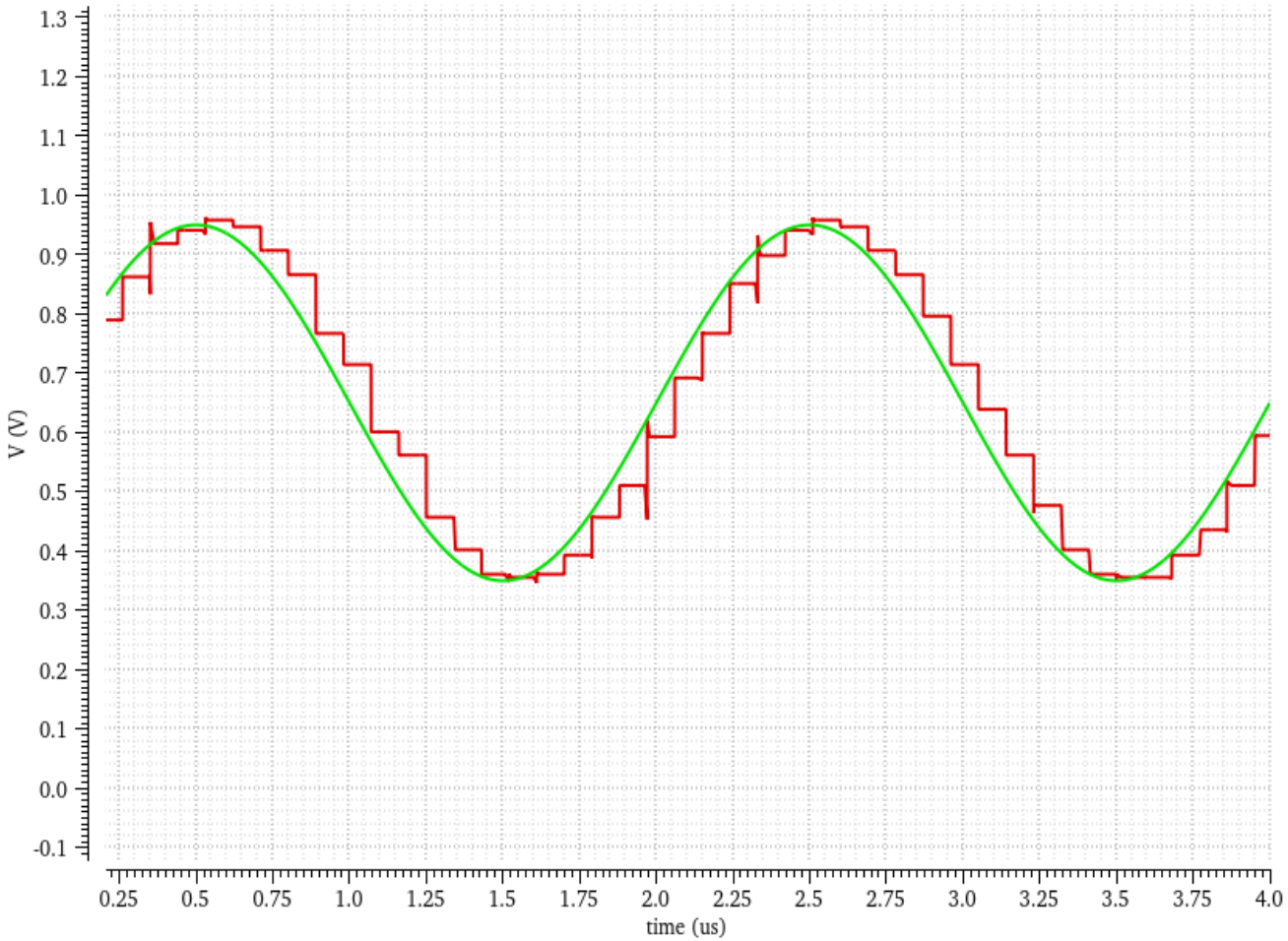

Transient Response
Fri May 3 09:46:28 2024 1
Name
Vis
/net11
V (V)
time (us)
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
32.0
33.0
34.0
35.0
36.0
37.0
38.0
39.0
40.0
41.0
42.0
43.0
44.0
45.0
46.0
47.0
48.0
49.0

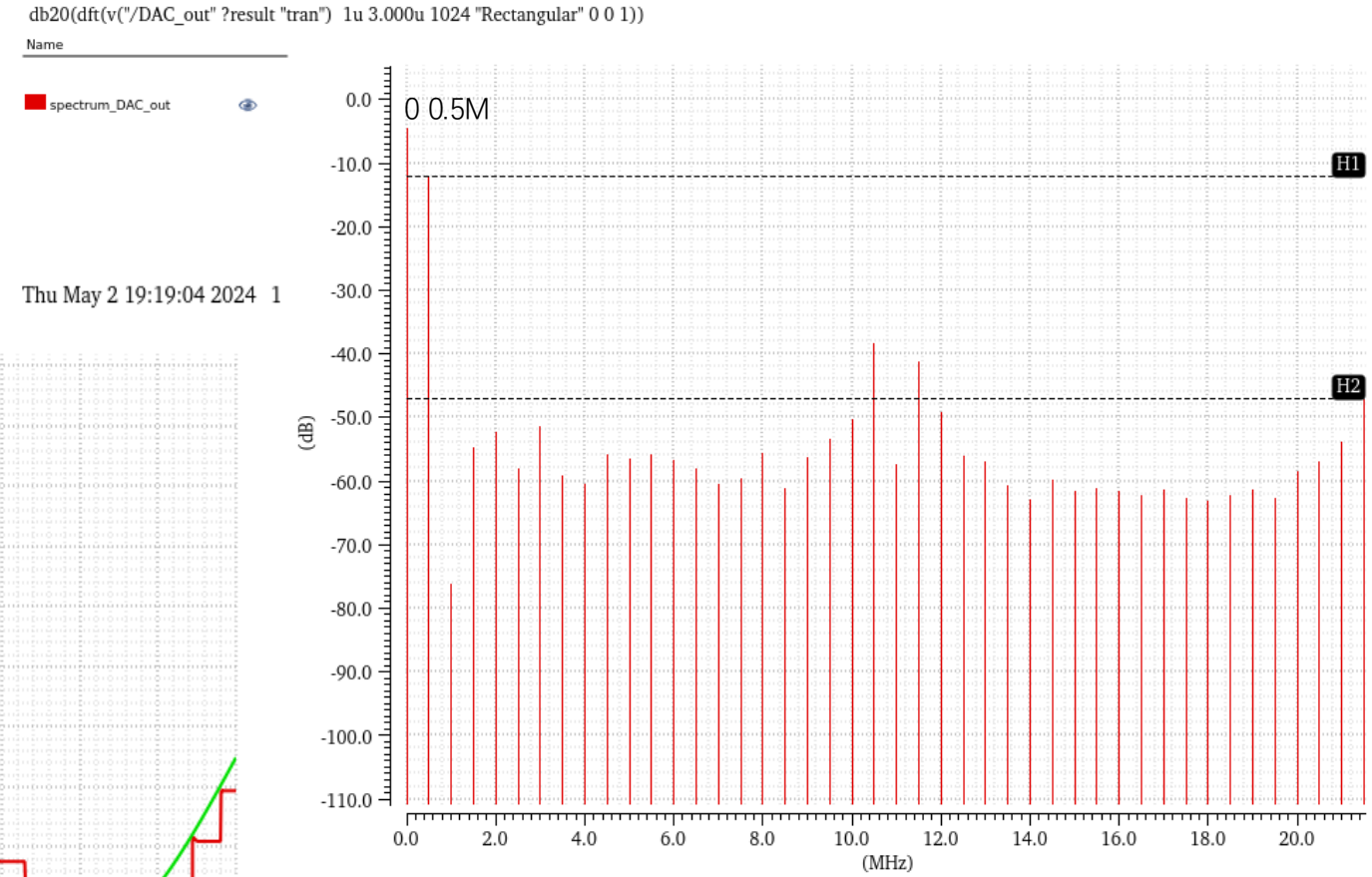
# SAR Extracted result – 100K Hz



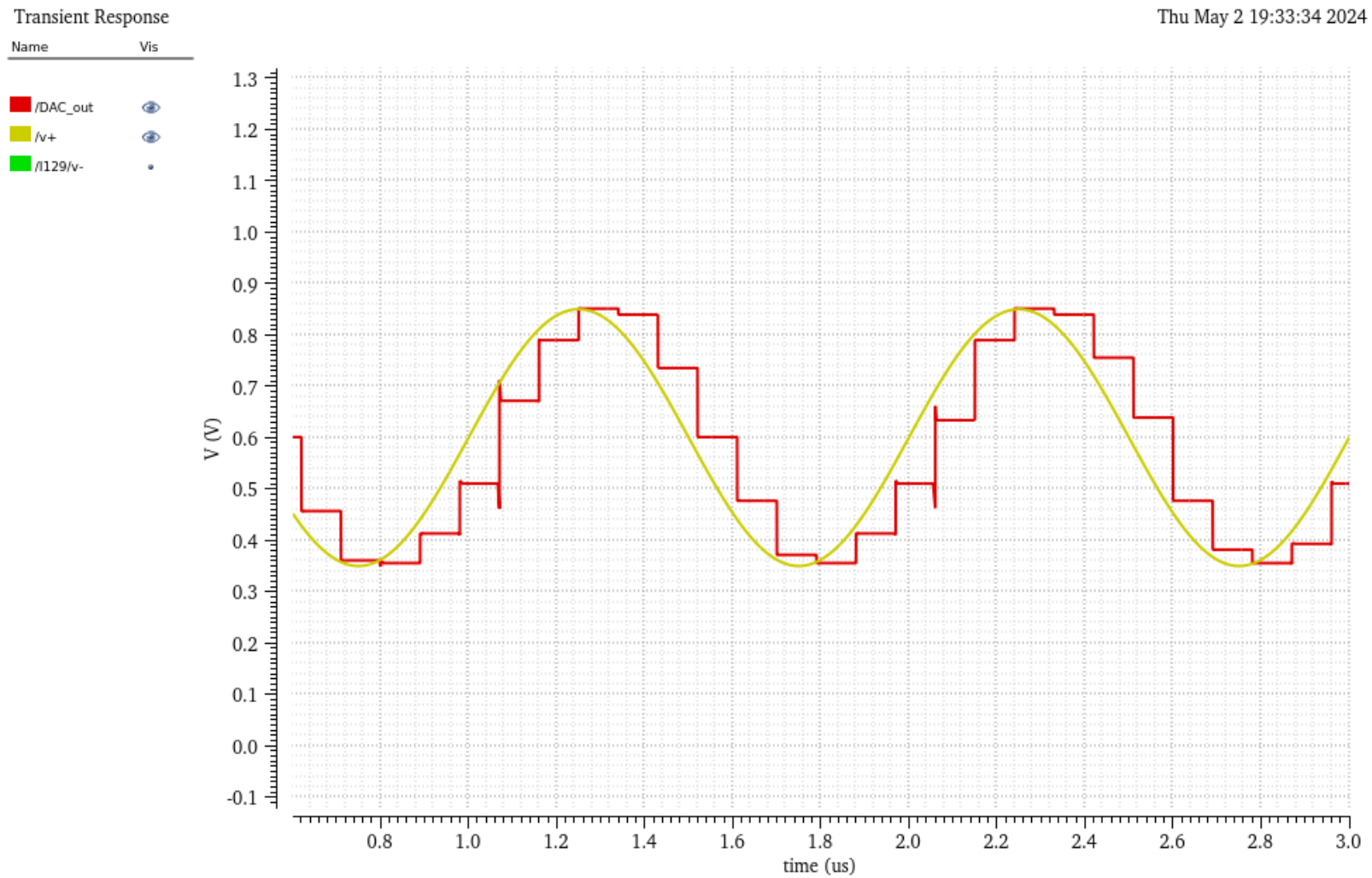



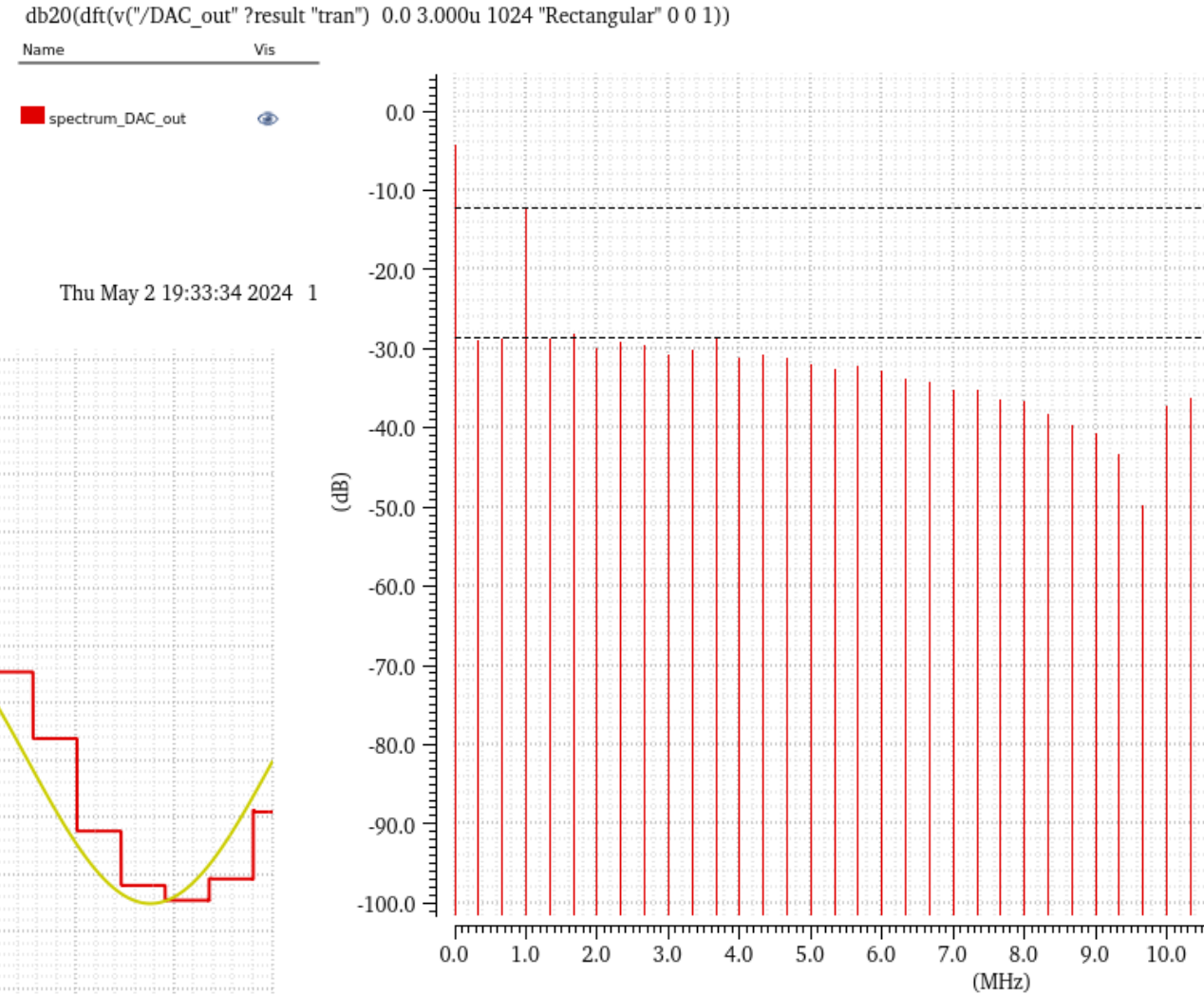
# Simulation – 500K Hz



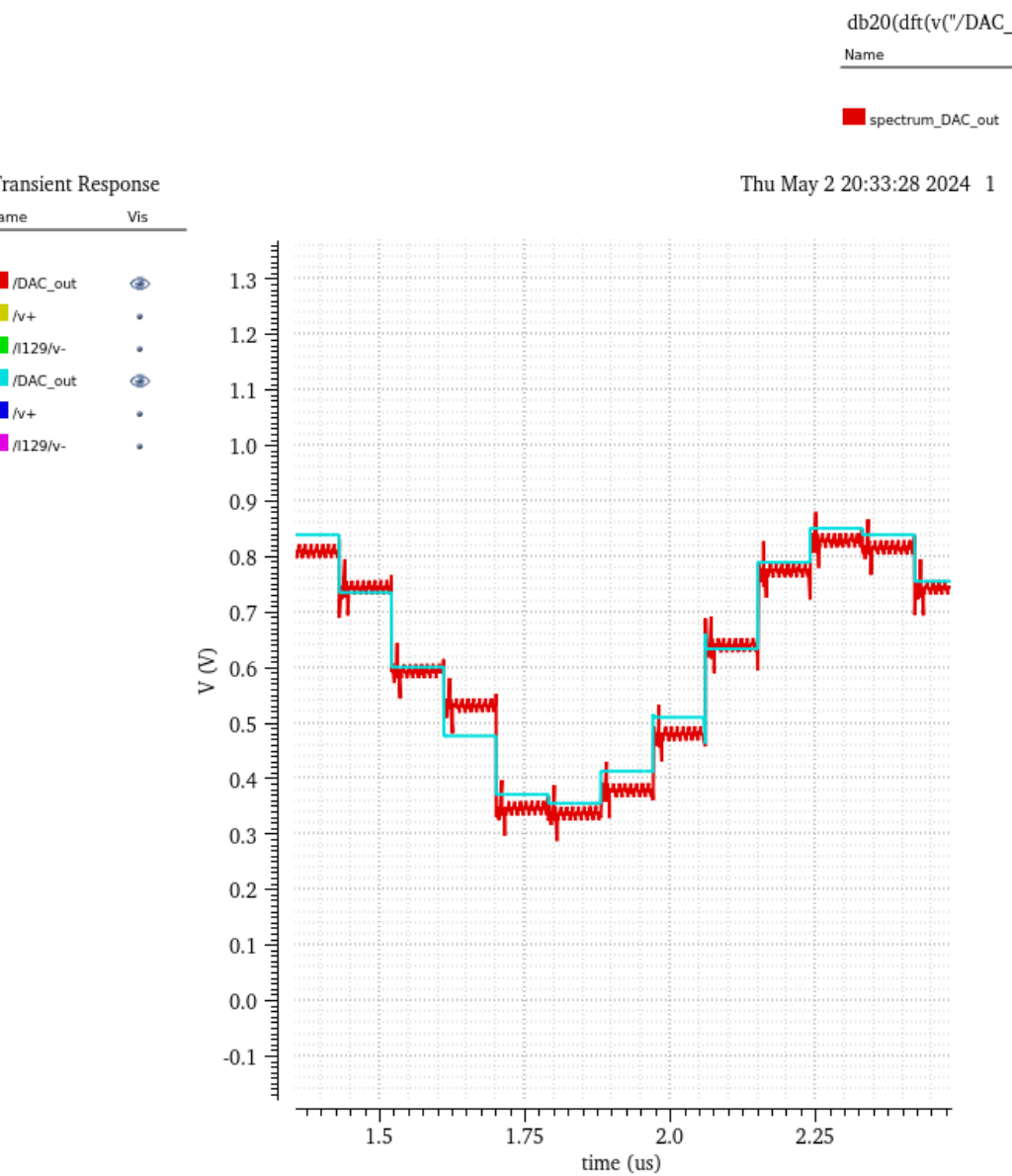



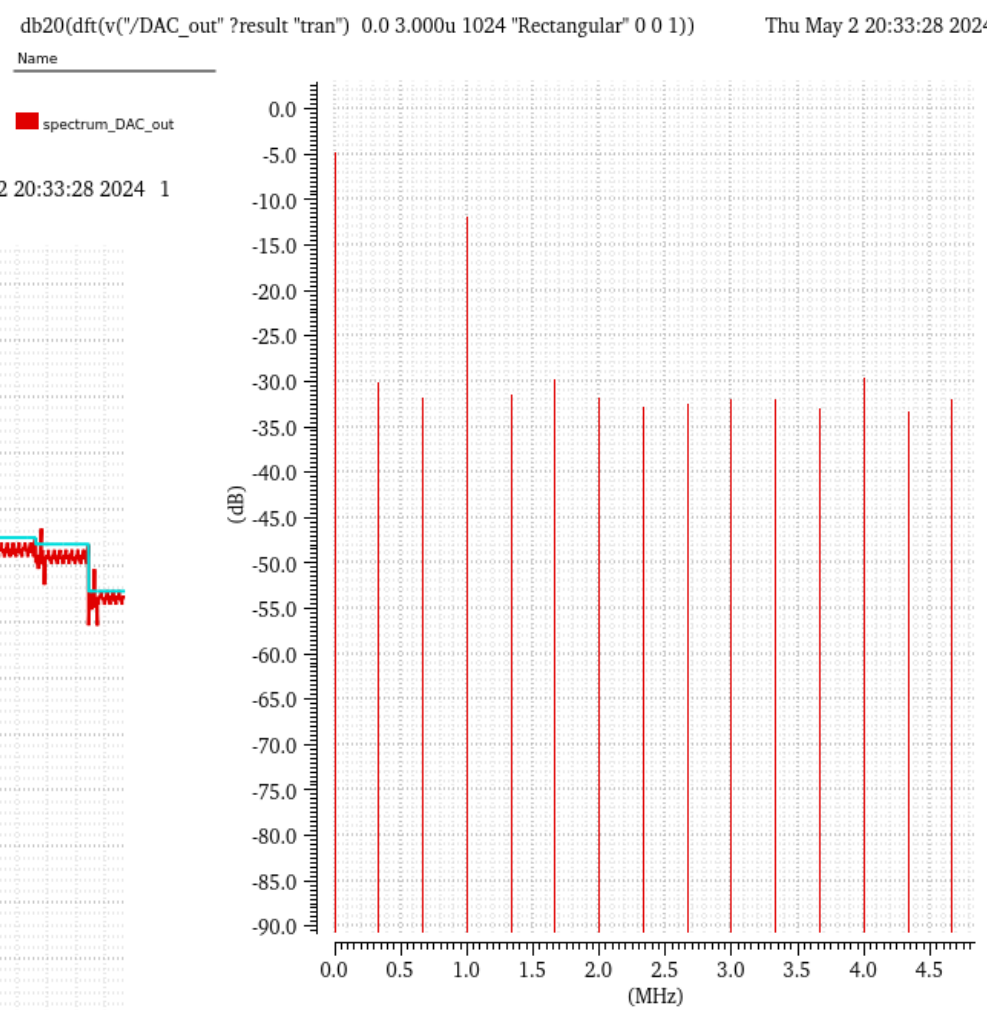
# Simulation – 1M Hz



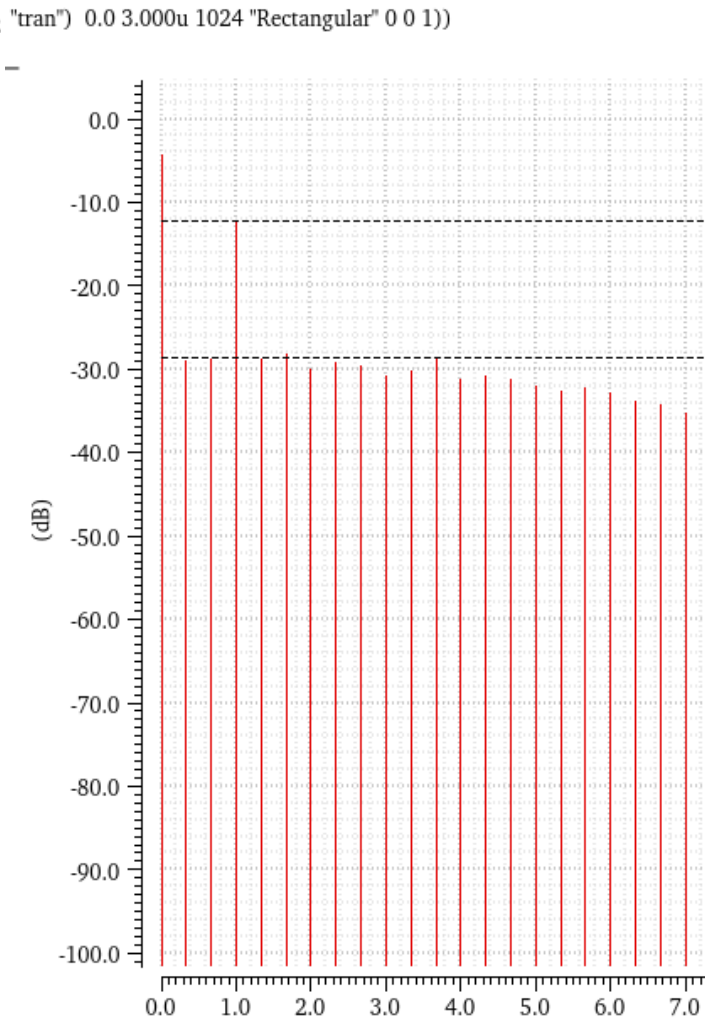



# Simulation – 1M Hz, Pre&post layout



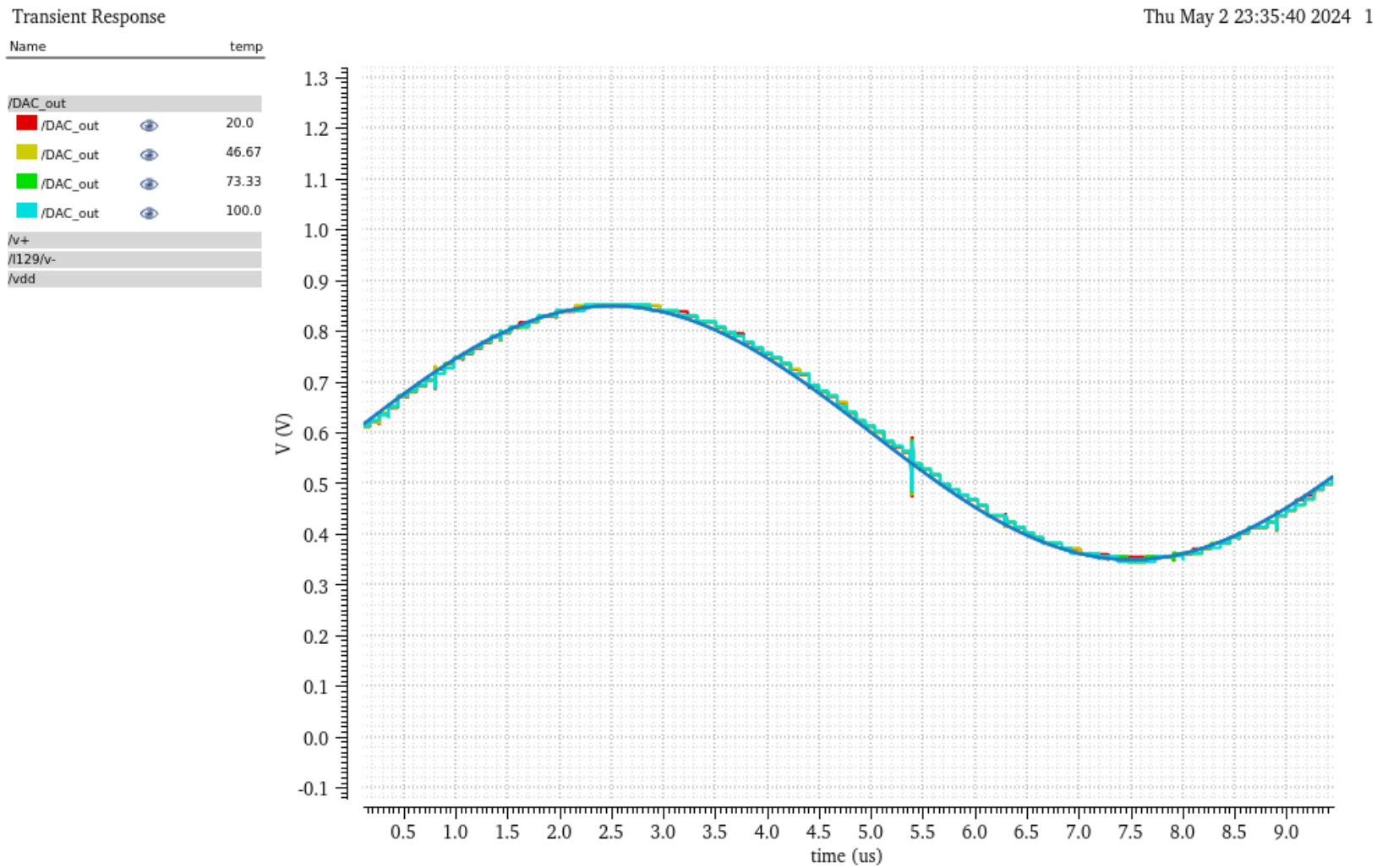




Pre Layout




Post Layout

# Temp drifting



# *Specs*

Area: 55x34 – 22.45x8.38 = 1681 $um^2$

Total inst: 1338

Resolution: 8 Bits

Range: 0.25V ~ 1.2 V

Sampling frequency: 10 MHz