~	Replacement algorithms used in associative and set-associative mapping of cache memory are: *	
0	LFU	
0	LRU	
0	FIFO	
	All of the above	/
×	Cache Memory is implemented using the DRAM chips. *	0/1
•	TRUE	×
0	FALSE	
Corr	ect answer	
•	FALSE	
~	LRU stands for*	1/1
0	Low Rate Usage	
0	Least Rate Usage	
•	Least Recently Used	✓
0	Low Required Usage	
×	When the data at a location in cache is different from the data located in the main memory, the cache is called *	0/1
	cache is different from the data located in the main memory, the cache is called*	0/1
0	cache is different from the data located in the main memory, the cache is called* Unique	0/1
0	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent	0/1
0 0	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable	0/1
0 0 0	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault	0/1
0 0 0	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other:	0/1
Corr	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other:	0/1
Corr	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other:	0/1
Corr	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other:	0/1
Corr	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other:	×
○○○○Corrr●	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache	×
CorrO	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? *	×
 ○ ○ ○ Corrr ● 	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: eect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? *	×
○○○○Corr●○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○<td>cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? * Write through Write within </td><td>×</td>	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? * Write through Write within	×
○○○○Corr●○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○<td>cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? * Write through Write within Write back </td><td>×</td>	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? * Write through Write within Write back	×
○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○	cache is different from the data located in the main memory, the cache is called* Unique Inconsistent Variable Fault Other: ect answer Inconsistent Which of the following is not a write policy to avoid Cache Coherence? * Write through Write within Write back	X 1/1

The instruction, "INC" increases 1/1 the contents of the specified register or memory location by *
O 0
● 1
O 2
O 3
✓ The instruction that enables 1/1 subtraction with borrow is *
O DEC
O SUB
● SBB
O ADC
✓ In general, the source operand of 1/1 an instruction can be *
O memory location
O register
O immediate data
All of these
All of these
 ♠ All of these ✓ In general, the destination operand of an instruction can be *
✓ In general, the destination 1/1 operand of an instruction can
✓ In general, the destination 1/1 operand of an instruction can be *
✓ In general, the destination 1/1 operand of an instruction can be * O memory location
✓ In general, the destination operand of an instruction can be * Omemory location oregister
✓ In general, the destination operand of an instruction can be * Omemory location Oregister Oimmediate data
✓ In general, the destination operand of an instruction can be * Omemory location Oregister Oimmediate data
✓ In general, the destination operand of an instruction can be* Omemory location Oregister Oimmediate data Omemory location and register ✓ ✓ The instruction, CMP to compare 1/1 source and destination operands,
✓ In general, the destination operand of an instruction can be* Omemory location Oregister Oimmediate data omemory location and register ✓ ✓ The instruction, CMP to compare 1/1 source and destination operands, it performs*
✓ In general, the destination operand of an instruction can be* Omemory location register immediate data memory location and register ✓ The instruction, CMP to compare 1/1 source and destination operands, it performs*
✓ In general, the destination operand of an instruction can be* Omemory location register immediate data memory location and register ✓ The instruction, CMP to compare 1/1 source and destination operands, it performs*

located in the main memory, the

cache is called. *

- Unique
- Inconsistent
- Variable
- Fault

- ✓ Which of the following is not a 1/1 write policy to avoid Cache Coherence? *
 - Write through
 - Write within
 - Write back
 - Buffered write
- In Direct Mapping of a cache the 1/1 relation holds good is: *
 - i = j modulo k
 - i = j modulo m



X	The processor used in a	0/1
	smartphone is an example of: *	

- O Dedicated Processor
- Application Processor
- Tiny Processor
- Multiprocessor

Correct answer

Application Processor



- O High speed processors and require more power
- High speed processors and require
 less power
- O Low speed processors and require less power
- O Low speed processors and require more power



★ Intel's first 32-bit machine was: * 0/1

- Pentium

Correct answer

- X The processor used in a 0/1 smartphone is an example of: *

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- ✓ The main structural components 1/1 of a computer are: *
 - O CPU, VDU, Main Memory, Secondary Memory
- CPU, I/O, Main Memory, System
 Interconnections
 - CPU, Keyboard, Mouse, Printer
 - CPU, CU, ALU, I/O
- ✓ The Von Neumann architecture 1/1 consists of: *
 - Main Memory, System interconnections, Speakers, Monitor
 - O Main Memory, Display Unit, Circuit Board, Power Supply
- Main Memory, ALU, CU, I/O, System
 Interconnections

Main Memory, CPU, Secondary Memory, Speakers



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- If the offset of the operand is 1/1 stored in one of the index registers, then it is known as *
 - base index addressing mode
 - indexed addressing mode
 - relative base indexed addressing mode
 - none of these

The microprocessor can 1/1 read/write 16-bit data from or to

Memory



- I/O devices
- Processor
- None of these















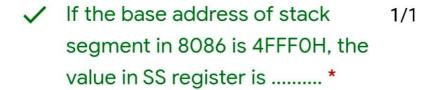






✓	During read operation, CPU		1/1
	fetches	*	

- Data
- Instruction
- another address
- all of the above



- 8FFFH
- **4FFEH**
- 5FFEH
- 4FFFH





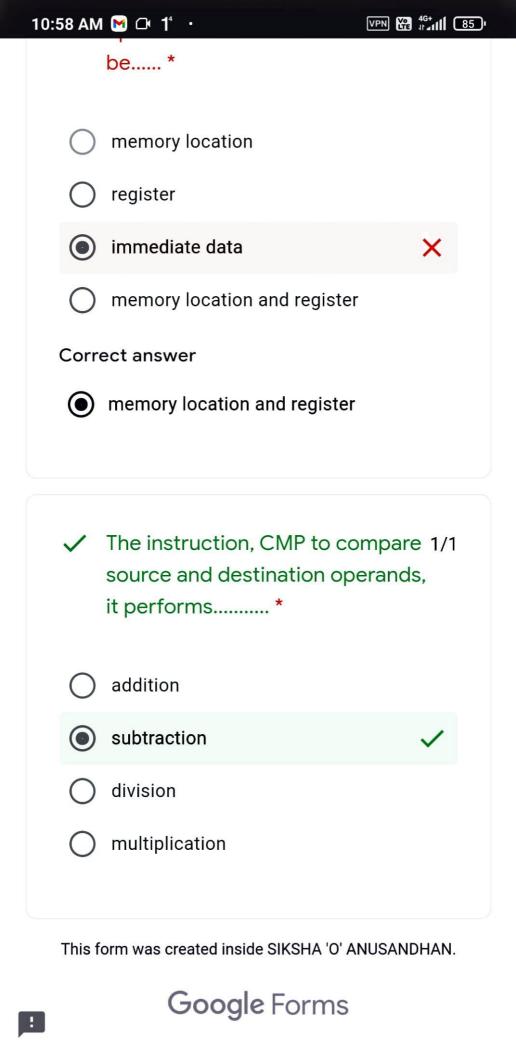












/	In general, the source operand of 1/1
	an instruction can be *

- memory location
- register
- immediate data
- All of these

X In general, the destination 0/1 operand of an instruction can be..... *

- memory location
- register
- immediate data

memory location and register

Correct answer

memory location and register

✓ The instruction, "INC" increases 1/1 the contents of the specified register or memory location by...... *

0

1

O 2

 \bigcirc 3

✓ The instruction that enables 1/1 subtraction with borrow is..... *

O DEC

SUB

SBB

ADC

✓ In general, the source operand of 1/1 an instruction can be....... *

✓ An example of non-erasable memory is: *
 ○ RAM
 ○ ROM
 ✓ CACHE
 ○ MAIN MEMORY
 ✓ Storage which stores or retains data after power off is called_ *

Volatile storage

Non-volatile storage

/

Sequential Storage

Direct storage

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~	Which of the following is independent of the address be	1/1 us?
•	Secondary memory	✓
0	Main memory	
0	Cache memory	
0	None of these	
✓	An example of non-erasable memory is: *	1/1
		1/1
0	memory is: *	1/1
0	memory is: * RAM	1/1

✓ Storage which stores or retains 1/1 data after power off is called_ *

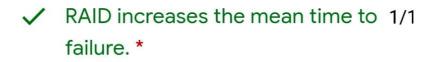


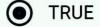






✓	RAID stands for* 1/1	
•	Redundant Array of Independent Disks	
0	Reduced Array of Independent Disks	
0	Redundant Array of Independent Devices	
0	IR Redundant Array of Interleaved Disks	







FALSE

Which of the following is 1/1 independent of the address bus?













- ✓ Which of the following is not a 1/1 write policy to avoid Cache Coherence? *
 - Write through
 - Write within
 - Write back
 - Buffered write

- ✓ In Direct Mapping of a cache the 1/1 relation holds good is: *
 - i = j modulo k
 - i = j modulo m
 - i = j modulo v
 - i = j modulo w

This form was created inside SIKSHA 'O' ANUSANDHAN.

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✓ When the data at a location in cache is different from the data located in the main memory, the cache is called. *	/1
Unique	
Inconsistent	Ċ
Variable	
Fault	
✓ Which of the following is not a 1.	/1
write policy to avoid Cache Coherence? *	
Write through	
Write within	
Write back	
O Buffered write	







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Replacement algorithms used in 1/1 associative and set-associative mapping of cache memory are: *

LFU

LRU

FIFO

All the above

For a hamming code of parity bit 1/1 m=8, what is the total bits and data bits? *

(255, 247)

(127, 119)

(31, 26)

(0, 8)

















- LFU
- LRU
- FIFO
- All the above

- For a hamming code of parity bit1/1 m=8, what is the total bits and data bits? *
 - (255, 247)
 - (127, 119)
 - (31, 26)
- $\bigcirc (0,8)$
- ✓ When the data at a location in 1/2 cache is different from the data located in the main memory, the cache is called. *