COA MCQ CHAPTER 7

Q1. The main importance of ARM micro-processors is providing operation with _____

A. Low cost and low power consumption
B. Higher degree of multi-tasking
C. Lower error or glitches
D. Efficient memory management

ANS 1. A

Q2. ARM processors are basically designed for _____.

A. Mainframe systems
B. Distributed systems
C. Mobile systems
D. Super computers

ANS2. C

Q3. The address system supported by ARM system(s) is / are_____.

A. Little Endian
B. Big Endian
C. X-liitle Endian
D. Both Little and Big Endian

ANS 3. D

Q4. In the ARM, PC is implemented using _____.

A. Caches
B. Heaps
C. General Purpose registers
D. Stack

ANS 4. C

Q5. How many registers are there in ARM7?

A. 35 registers (28 GPR & 7 SPR)
B. 37 registers (28 GPR & 9 SPR)
C. 37 registers (31 GPR & 6 SPR)
D. 35 registers (30 GPR & 5 SPR)

ANS 5. C

Q6. Which processor requires more number of registers?

A. CISC
B. ISA

C. RISC
D. ANNA

ANS 6. C

Q7. The method which offers higher speeds of I/O transfers is _____.

A. Interrupts
B. Memory mapping
C. Program-controlled I/O
D. DMA

ANS 7. D

Q8. In memory-mapped I/O _____.

A. The I/O devices have a separate address space
B. The I/O devices and the memory share the same address space
C. A part of the memory is specifically set aside for the I/O operation
D. The memory and I/O devices have an associated address space

ANS 8. B

Q9. The _____ circuit is basically used to extend the processor BUS to connect devices.

A. Router
B. Repeater
C. Bridge
D. All of the above

ANS 9. C

Q10. Keyboard and Mouse comes under _____.

A. Input peripherals
B. Output peripherals
C. I/O devices
D. None of the above.

ANS 10. A

Q11. RAM is a _____ memory.

A. External
B. Internal
C. Main
D. Auxiliary

ANS 11. C

Q12. _____ is the permanent memory unit built into the computer systems.

A. ROM
B. CPU
C. DVD-ROM
D. RAM

ANS 12. A

Q13. Hard-disk drives are considered as _____ storage medium.

A. Flash
B. Non-volatile
C. Temporary
D. Permanent

ANS 13. B

Q14. The storage element of a SRAM is _____.

A. Diode
B. Resistor
C. Capacitor
D. Flip-flop

ANS 14. D

Q15. Capacity of hard-disk is measured in _____.

A. Gigabytes
B. Megabytes
C. Kilobytes
D. Bytes

ANS 15. A

8086 MICROPROCESSOR

Q1. 8086 microprocessor supports _____ modes of operation.

A. 2
B. 3
C. 4
D. 5

ANS1. A

Q2. 8086 can access up to _____ memory.

A. 512 KB
B. 1 MB
C. 2 MB
D. 256 KB

ANS1. B

Q3. 8086 has _____ address bus.

A. 16-bit
B. 18-bit
C. 20-bit
D. 24-bit

ANS1. C

Q4. Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to zero?

A. Trap flag
B. Zero flag
C. Carry flag
D. Overflow flag

ANS1. B

Q5. Which flag represents the result when the system capacity is exceeded?

A. Trap flag
B. Auxiliary flag
C. Carry flag
D. Overflow flag

ANS1. B

Q6. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

A. IR

B. HLDA
C. HR
D. WR

ANS1. D

Q7. Which instruction is used to load the address of operand into the provided register?

A. LEA
B. LDS
C. LES
D. LAHF

ANS1. A

Q8. The different ways in which a source operand is denoted in an instruction is known as:

A. Instruction Set
B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS1. B

Q11. The register used to store the flags is called as _____.

A. Flag register
B. Status register
C. Test register
D. Log register

ANS 11. B

Q12. The 16 bit flag of 8086 microprocessor is responsible to indicate _____.

A. The condition of result of ALU operation
B. The condition of memory
C. The result of addition
D. The result of subtraction

ANS 12. A

Q13. The CF is known as _____.

A. Carry flag
B. Condition flag
C. Common flag
D. Single flag

ANS 13. A

Q14. The SF is known as _____.

A. Service flag
B. Sign flag
C. Single flag
D. Condition flag

ANS 14. B

Q15. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 15. C

Q16. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 16. C

Q17. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 17. C

Q18. The instruction that is used to transfer the data from source operand to destination operand is :

A. Data copy / transfer instruction
B. Branch instruction
C. Arithmetic / logical instruction
D. String instructions

ANS 17. C

CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION

Q1. _____ bus structure is usually used to connect I/O devices..

A. Single bus
B. Multiple bus
C. Star bus
D. RAM bus

ANS 1. A

Q2. The main advantage of using single bus structure is _____.

A. Fast data transfers
B. Cost effective connectivity and speed
C. Cost effective connectivity and ease of attaching peripheral devices
D. None of the above

ANS 2. C

Q3. The ISA standard buses are used to connect _____.

A. RAM and Processor
B. GPU and Processor
C. Hard-disk and Processor
D. CD / DVD drives and Processor

ANS 3. C

Q4. Which registers can interact with the secondary storage?

A. MAR
B. PC
C. IR

D. AC

ANS 4. A

Q5. To extend the connectivity of the processor bus we use _____.

A. PCI Bus
B. SCSI Bus
C. Controllers
D. Multiple Bus

ANS 5. A

Q6. A source program is usually written in _____.

A. Assembly language
B. Machine-level language
C. High-level language
D. Natural language

ANS 6. C

Q7. _____ are numbers and encoded characters which are generally used as operands.

A. Input
B. Data
C. Information
D. Stored values

ANS 7. B

Q8. The ALU stores the immediate result in _____.

A. Accumulator
B. Queue
C. Stack
D. Memory locations

ANS 8. A

Q9. The control unit controls other units by generating _____.

A. Control signals
B. Timing signals
C. Transfer signals
D. Command signals

ANS 9. B

Q10. The extremely small and fast RAM is known as _____.

A. Cache

B. Heaps
C. Accumulators
D. Stacks

ANS 10. A

Q11. The smallest entity of memory is called _____.

A. Cell
B. Block
C. Instance
D. Unit

ANS 11. A

Q12. The branch of study that deals with the computer system's conceptual design and basic overview is known as:

A. Computer Anatomy
B. Computer Architecture
C. Computer OS
D. Computer Interface

ANS12. B

Q13. Which of the following technologies was used in second generation computer?

A. Vacuum Tubes
B. Transistors
C. Integrated Circuits
D. VLSI Circuits

ANS13. B

CHAPTER 2: PERFORMANCE ISSUES

Q1. _____ are used to overcome the difference in data transfer speeds of various devices.

A. Speed enhancing circuitry
B. Bridge circuits
C. Multiple buses
D. Buffer registers

ANS 1. D

Q2. Two processors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

A. A
B. B
C. Both takes equal amount of time
D. None of the above

ANS 2. A

Q3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____.

A. Super-scaling
B. Pipelining
C. Parallel computation
D. Architecture

ANS 3. B

Q4. The clock rate of the processor can be improved by _____.

A. Improving the IC technology of the logic circuits
B. Reducing the amount of processing done in one step
C. By using the over-clocking method
D. All of the above

ANS 4. D

Q5. SPEC stands for _____.

A. Standard Performance Evaluation Code
B. System Processing Enhancing Code
C. System Performance Evaluation Corporation
D. Standard Processing Enhancement Corporation

ANS 5. C

Q6. CISC stands for _____.

A. Complete Instruction Sequential Compilation
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation

ANS 6. C

Q7. Which instruction is used to load the address of operand into the provided register?

A. LEA

B. LDS
C. LES
D. LAHF

ANS1. A

Q8. The different ways in which a source operand is denoted in an instruction is known as:

A. Instruction Set
B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS10. B

Q11. Which of the following is the important characteristics of computers?

E. speed
F. accuracy
G. storage
H. all of the above

ANS11. D

Q12. Which of the following is not a hardware component of computer?

A. memory
B. scanner
C. operating system
D. CPU

ANS12. C

CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

Q1. During the execution of a program which gets initialized first?

A. MDR
B. IR
C. PC
D. MAR

ANS1. C

Q2. The decoded instruction is stored in _____.

A. IR
B. PC
C. Registers
D. AC

ANS1. A

Q3. Which of the register(s) of the processor is / are connected to Memory Bus?

A. PC
B. MAR
C. IR
D. Both PC AND MAR

ANS1. B

Q4. ISP stands for _____.

A. Instruction Set Processor
B. Information Standard Processing
C. Interchange Standard Protocol
D. Interrupt Service Procedure

ANS1. A

Q5. The interrupt request line is a part of the _____.

A. Data line
B. Control line

C. Address line
D. None of the above

ANS1. B

Q6. The signal set to the device from the processor to the device after receiving an interrupt is _____.

A. Interrupt acknowledge
B. Return signal
C. Service signal
D. Permission signal

ANS1. A

CHAPTER 4: CACHE MEMORY

Q1. To reduce the memory access time we generally make use of _____.

A. Heaps
B. SSD
C. SDRAMs
D. Cache memory

ANS 1. D

Q2. _____ is usually used to increase the size of physical memory.

A. Secondary memory
B. Virtual memory
C. Hard-disk
D. Disks

ANS 2. B

Q3. The internal components of the processor are connected by _____.

A. Processor intra-connectivity circuitry
B. Processor bus
C. Memory bus
D. Single bus

ANS 3. B

Q4. During the execution of instructions, a copy of the instructions is placed in the _____.

A. Register
B. RAM
C. Main memory
D. Cache

ANS 4. D

Q5. To get the physical address from the logical address generated by CPU we use _____

A. MAR
B. MMU
C. Overlays
D. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use _____.

A. Cache
B. TLB
C. Buffers
D. Registers

ANS 6. D

Q7. _____ method is used to map logical address of variable length onto physical memory.

A. Paging
B. Overlays
C. Segmentation
D. Paging with segmentation

ANS1. C

Q8. Physical memory is divided into sets of finite size called as _____.

A. Frames
B. Pages
C. Blocks
D. Vectors

ANS1. A

Q9. What is the high speed memory between the main memory and the CPU called?

A. Registers
B. Cache memory
C. Secondary storage memory
D. Virtual memory

ANS 9. B

Q10. Whenever the data is found in the cache memory it is called a _____.

A. HIT
B. MISS
C. FOUND
D. ERROR

ANS 10. A

Q11. The transfer between CPU and Cache is called _____.

A. Block transfer
B. Word transfer
C. Set transfer
D. Associative transfer

ANS 11. B

Q12. LRU stands for _____.

A. Low Rate Usage
B. Least Rate Usage
C. Least Recently Used
D. Low Required Usage

ANS 12. C

Q13. When the data at a location in cache is different from the data in the main memory, the cache is called _____.

A. Unique
B. Inconsistent
C. Variable
D. Fault

ANS 13. B

Q14. Which of the following is not a write policy to avoid Cache Coherence?

A. Write through
B. Write within
C. Write back
D. Write buffer

ANS 14. B

Q15. In _____ mapping, the data can be mapped anywhere in the Cache Memory.

A. Associative
B. Direct
C. Set-associative

D. Indirect

ANS 15. A

Q16. Cache Memory is implemented using the DRAM chips.

A. True
B. False

ANS 16. B

COA MCQ CHAPTER 5 & 6

Q1. What is the permanent memory built into your computer called?

A. RAM
B. ROM
C. CPU
D. CD-ROM

ANS 1. B

Q2. Storage which stores or retains data after power off is called _____.

A. Volatile storage
B. Non-volatile storage
C. Sequential storage
D. Direct storage

ANS2. B

Q3. The contents of memory into blocks of the same size is called as _____.

A. ROM
B. EPROM
C. EEPROM
D. All of the above

ANS 3. D

Q4. Main memory of computer is _____.

A. Internal
B. External
C. Both
D. Auxilliary

ANS 4. A

Q5. Which of the following memories must be refreshed many times per second?

A. EPROM
B. ROM
C. Static RAM
D. Dynamic RAM

ANS 5. D

Q6. A half-byte is known as _____.

A. data
B. bit
C. half-byte
D. nibble

ANS 6. D

Q7. USB type storage device is _____.

A. Secondary
B. Auxiliary
C. Tertiary
D. Primary

ANS 7. A

Q8. Which device is used to back-up the data?

A. Floppy disk
B. Tape
C. Network drive
D. All of the above

ANS 8. D

Q9. With a CD you can perform _____.

A. read
B. write
C. read and write
D. none of these

ANS 9. A

Q10. Flash memory is also known as _____.

A. Flash RAM
B. Flash ROM
C. Flash DRAM
D. Flash DROM

ANS 10. A

Q11. RAM is a _____ memory.

A. External
B. Internal
C. Main
D. Auxiliary

ANS 11. C

Q12. _____ is the permanent memory unit built into the computer systems.

A. ROM
B. CPU
C. DVD-ROM
D. RAM

ANS 12. A

Q13. Hard-disk drives are considered as _____ storage medium.

A. Flash
B. Non-volatile
C. Temporary
D. Permanent

ANS 13. B

Q14. The storage element of a SRAM is _____.

A. Diode
B. Resistor
C. Capacitor
D. Flip-flop

ANS 14. D

Q15. Capacity of hard-disk is measured in _____.

A. Gigabytes
B. Megabytes
C. Kilobytes
D. Bytes

ANS 15. A

COA MCQ CHAPTER 8

Q1. Which of the following is not a type of Operating System?

A. Batch Processing

B. Multi-programming
C. Latch Programming
D. Real time programming

ANS 1. C

Q2. BIOS programs are embedded on a chip called

A. Firmware
B. IC
C. Hardware
D. Application programs

ANS 1. A

COA MCQ CHAPTER 5 & 6

Q1. What is the permanent memory built into your computer called?

A. RAM
B. ROM
C. CPU
D. CD-ROM

ANS 1. B

Q2. Storage which stores or retains data after power off is called _____.

A. Volatile storage
B. Non-volatile storage
C. Sequential storage
D. Direct storage

ANS2. B

Q3. The contents of memory into blocks of the same size is called as _____.

A. ROM
B. EPROM
C. EEPROM
D. All of the above

ANS 3. D

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ANS 11. C

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ANS 12. A

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ANS 13. B

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C. Capacitor
D. Flip-flop

ANS 14. D

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A. Gigabytes
B. Megabytes
C. Kilobytes
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ANS 15. A

COA MCQ CHAPTER 4

Q1. LRU stands for _____.

A. Low Rate Usage
B. Least Rate Usage
C. Least Recently Used
D. Low Required Usage

ANS 1. C

Q2. When the data at a location in cache is different from the data in the main memory, the cache is called _____.

A. Unique
B. Inconsistent
C. Variable
D. Fault

ANS 2. B

Q3. Which of the following is not a write policy to avoid Cache Coherence?

A. Write through
B. Write within
C. Write back
D. Write buffer

ANS 3. B

Q4. In _____ mapping, the data can be mapped anywhere in the Cache Memory.

A. Associative
B. Direct
C. Set-associative
D. Indirect

ANS 4. A

Q5. To get the physical address from the logical address generated by CPU we use _____

A. MAR
B. MMU
C. Overlays
D. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use _____.

A. Cache

B. TLB
C. Buffers
D. Registers

ANS 6. D

Q7. _____ method is used to map logical address of variable length onto physical memory.

A. Paging
B. Overlays
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D. Paging with segmentation

ANS1. C

Q8. Physical memory is divided into sets of finite size called as _____.

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8086 MICROPROCESSOR

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A. 512 KB
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Q3. 8086 has _____ address bus.

A. 16-bit
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C. 20-bit
D. 24-bit

ANS1. C

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C. HR
D. WR

ANS1. D

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A. LEA
B. LDS
C. LES
D. LAHF

ANS1. A

Q8. The different ways in which a source operand is denoted in an instruction is known as:

A. Instruction Set
B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS1. B

Q11. The register used to store the flags is called as _____.

A. Flag register
B. Status register
C. Test register
D. Log register

ANS 11. B

CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION

Q1. _____ bus structure is usually used to connect I/O devices..

A. Single bus
B. Multiple bus
C. Star bus
D. RAM bus

ANS 1. A

Q2. The main advantage of using single bus structure is _____.

A. Fast data transfers
B. Cost effective connectivity and speed
C. Cost effective connectivity and ease of attaching peripheral devices
D. None of the above

ANS 2. C

Q3. The ISA standard buses are used to connect _____.

A. RAM and Processor
B. GPU and Processor
C. Hard-disk and Processor
D. CD / DVD drives and Processor

ANS 3. C

Q4. Which registers can interact with the secondary storage?

A. MAR
B. PC
C. IR
D. AC

ANS 4. A

Q5. To extend the connectivity of the processor bus we use _____.

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B. SCSI Bus
C. Controllers
D. Multiple Bus

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Q6. A source program is usually written in _____.

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B. Machine-level language
C. High-level language
D. Natural language

ANS 6. C

Q7. _____ are numbers and encoded characters which are generally used as operands.

A. Input
B. Data
C. Information
D. Stored values

ANS 7. B

Q8. The ALU stores the immediate result in _____.

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B. Queue
C. Stack
D. Memory locations

ANS 8. A

Q9. The control unit controls other units by generating _____.

A. Control signals
B. Timing signals
C. Transfer signals
D. Command signals

ANS 9. B

Q10. The extremely small and fast RAM is known as _____.

A. Cache
B. Heaps
C. Accumulators
D. Stacks

ANS 10. A

Q11. The smallest entity of memory is called _____.

A. Cell
B. Block
C. Instance
D. Unit

ANS 11. A

CHAPTER 2: PERFORMANCE ISSUES

Q1. _____ are used to overcome the difference in data transfer speeds of various devices.

A. Speed enhancing circuitry
B. Bridge circuits
C. Multiple buses
D. Buffer registers

ANS 1. D

Q2. Two processors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

A. A
B. B
C. Both takes equal amount of time
D. None of the above

ANS 2. A

Q3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____.

A. Super-scaling
B. Pipelining
C. Parallel computation
D. Architecture

ANS 3. B

Q4. The clock rate of the processor can be improved by _____.

A. Improving the IC technology of the logic circuits
B. Reducing the amount of processing done in one step
C. By using the over-clocking method
D. All of the above

ANS 4. D

Q5. SPEC stands for _____.

A. Standard Performance Evaluation Code
B. System Processing Enhancing Code
C. System Performance Evaluation Corporation
D. Standard Processing Enhancement Corporation

ANS 5. C

Q6. CISC stands for _____.

A. Complete Instruction Sequential Compilation
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation

ANS 6. C

Q7. Which instruction is used to load the address of operand into the provided register?

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Q8. The different ways in which a source operand is denoted in an instruction is known as:

A. Instruction Set
B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS1. B

CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

Q1. During the execution of a program which gets initialized first?

A. MDR
B. IR
C. PC
D. MAR

ANS1. C

Q2. The decoded instruction is stored in _____.

A. IR
B. PC
C. Registers
D. AC

ANS1. A

Q3. Which of the register(s) of the processor is / are connected to Memory Bus?

A. PC
B. MAR
C. IR
D. Both PC AND MAR

ANS1. B

Q4. ISP stands for _____.

A. Instruction Set Processor
B. Information Standard Processing
C. Interchange Standard Protocol
D. Interrupt Service Procedure

ANS1. A

Q5. The interrupt request line is a part of the _____.

A. Data line
B. Control line
C. Address line
D. None of the above

ANS1. B

Q6. The signal set to the device from the processor to the device after receiving an interrupt is _____.

A. Interrupt acknowledge
B. Return signal
C. Service signal
D. Permission signal

ANS1. A

CHAPTER 4: CACHE MEMORY

Q1. To reduce the memory access time we generally make use of _____.

A. Heaps
B. SSD
C. SDRAMs
D. Cache memory

ANS 1. D

Q2. _____ is usually used to increase the size of physical memory.

A. Secondary memory
B. Virtual memory
C. Hard-disk
D. Disks

ANS 2. B

Q3. The internal components of the processor are connected by _____.

A. Processor intra-connectivity circuitry
B. Processor bus
C. Memory bus
D. Single bus

ANS 3. B

Q4. During the execution of instructions, a copy of the instructions is placed in the _____.

A. Register
B. RAM
C. Main memory
D. Cache

ANS 4. D

Q5. To get the physical address from the logical address generated by CPU we use _____

A. MAR
B. MMU
C. Overlays
D. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use _____.

A. Cache
B. TLB
C. Buffers
D. Registers

ANS 6. D

Q7. _____ method is used to map logical address of variable length onto physical memory.

A. Paging
B. Overlays
C. Segmentation
D. Paging with segmentation

ANS1. C

Q8. Physical memory is divided into sets of finite size called as _____.

A. Frames
B. Pages
C. Blocks
D. Vectors

ANS1. A

1. What is DEN in 8086 microprocessor?
   A. direct enable
   B. data entered
   C. data enable
   D. data encountered
   ANS- C
2. Status register is also called as _____
   A. Accumulator
   B. Stack
   C. Counter
   D. Flags
   ANS- D
3. Which method bypasses CPU for certain type of data transfer?
   A. software interrupts
   B. interrupt-driven I/O
   C. Direct memory Access
   D. Polled I/O
   ANS- C
4. A 20 bit address bus allows access to a memory of capacity____
   A. 1 MB
   B. 2 MB
   C. 4 MB
   D. 8 MB
   ANS- A
5. Which group of instructions do not affect the flags?
   A. Arithmetic
   B. Logical
   C. Data transfer
   D. Branch
   ANS- C
6. If the offset of the operand is stored in one of the index registers, then it is known as __
   A. base index addressing mode
   B. indexed addressing mode
   C. relative base indexed addressing mode
   D. none of these
   ANS- B
7. Which of the following is not a data copy/transfer instruction?
   A. MOV
   B. PUSH
   C. POP
   D. DAS
   ANS- D
8. Which is not a valid one?

A. MOV AX, BX
B. MOV DS, 5000H
C. MOV AX, 5000H
D. PUSH AX

ANS- B

9. Which register is used to get input data and send output data when I/O instructions are executed in 8086?
   A. AX
   B. BX
   C. DX
   D. SI

   ANS- A
10. QPI in point to point stands as _____
    A. quick process interconnect
    B. quick path interconnect
    C. quick peripheral interconnect
    D. none of these

    ANS- B
11. Computer bus line consists of _____
    A. Registers
    B. Accumulators
    C. set of parallel lines
    D. computer clock

    ANS- C
12. Way in which computer components are connected with each other is called __
    A. computer layout
    B. computer architecture
    C. computer parts
    D. computer hardware

    ANS- B
13. Computer system mainly consists of _____
    A. CPU
    B. Memory
    C. I/O Unit
    D. All of the above

    ANS- D
14. Computer instructions are divided into ___
    A. function code
    B. instruction code
    C. operand
    D. both a and c

    ANS- D
15. Which is not part of the execution unit?
    A. Clock

B. ALU
C. General registers
D. Flags
ANS- A

16. Which Bus is bidirectional?
A. Address bus
B. control bus
C. Data bus
D. All of the above
ANS- C

17. The primary function of _____ is to accept data from I/O devices.
A. Multiprocessor
B. Microprocessor
C. Peripherals
D. Interfaces
ANS- B

18. The microprocessor can read/write 16 bit data from or to ___
A. Memory
B. I/O devices
C. Processor
D. none of the above
ANS- A

19. A 20 bit address bus can locate_____
A. 1048576 locations
B. 2097152 locations
C. 419304 locations
D. none of these
ANS- A

20. _____ generate interrupt signal to microprocessor and receive acknowledgement.
A. Decoder
B. control logic
C. interrupt register
D. all of the above
ANS- B

21. During read operation, CPU fetches _____
A. Data
B. Instruction
C. another address
D. all of the above
ANS- D

22. PCI stands for _____
A. Peripheral Component Interconnect
B. Peripheral Computer Internet

C. Processor Computer Interconnect
D. Processor Cable Interconnect
ANS- A

23. What will be the contents of AL register after the following instructions have been executed? MOV BL, 8C
MOV AL, 7E
ADD AL, BL
A. 0A and carry flag is set
B. 0A and carry flag is reset
C. 6A and carry flag is set
D. 6A and carry flag is reset
ANS- A

24. A scheme in which the register given in the instruction specifies the memory address of the operand is called_____.
A. immediate addressing
B. base addressing
C. direct addressing
D. indirect addressing
ANS-D

25. The flag which is to be set for enabling single step or trap interrupt in the 8086 is_____.
A. CF
B. DF
C. TF
D. IF
ANS- C

26. If the base address of stack segment in 8086 is 4FFF0H, the value in SS register is _____.
A. 8FFFH
B. 4FFEH
C. 5FFEH
D. 4FFFH
ANS- D

27. Clock frequencies of two processors A and B are 700 MHz and 900 MHz respectively. A executes an instruction with an average of 3 steps. B executes the same instruction with an average of 5 steps. Which processor is faster?
A. A
B. B
C. Botha are same
D. Cannot be predicted
ANS- A

28. A processor is performing fetch or decoding of different instructions during the execution of another instruction is called as ____.
A. super scaling

B. pipe-lining
C. parallel processing
D. none of these
ANS- B

29. If a processor clock rate is 1250 million cycles per second, then its clock period is_____.
A. 1.9×10^{-10} sec
B. 1.6×10^{-6} sec
C. 1.2×10^{-10} sec
D. 8×10^{-10} sec
ANS- D

30. CISC stands for_____.
A. complete instruction sequential compilation
B. computer integrated sequential compiler
C. complex instruction set computer
D. complex instruction sequential compilation
ANS- C

31. SPEC stands for_____.
A. standard performance evaluation criteria
B. standard performance evaluation corporation
C. Anyone from above
D. None of the above
ANS- B

32. Which is not a characteristics of benchmark program?
A. wide distribution
B. easy measurement
C. representative of a particular kind of programming domain
D. low level language
ANS- D

33. Find speed up if N =10 and f=0.9.
A. 5.123
B. 5.2632
C. 5.0
D. 4.9
ANS- B

34. The owner of a shop observes that on average 18 customers per hour arrive and there are typically 8 customers in the shop. What is the average length of time each customer spends in the shop?
A. 0.44 hour
B. 1.2 hour
C. 0.64 hour
D. none of these
ANS- A

35. Techniques used in contemporary processors to increase speed are _____.

A. Pipelining
B. branch prediction
C. super scalar execution
D. all of the above
ANS- D

36. Which one is a performance metrics?
A. Mean
B. Clock Speed
C. CPU Cycles
D. All of the above
ANS- D

37. The Arithmetic mean rate of computer A, B and C are 0.12, 0.38 and 0.625 respectively. Which one is faster?
A. A
B. B
C. C
D. All are equally faster
ANS- C

38. Classification of computers based on computing applications and their characteristics are _____.
A. Desktop
B. Server
C. Super computer
D. All of the above
ANS- D

39. 8086 microprocessor is a _____type of processor.
A. 8 bit
B. 16 bit
C. 32 bit
D. None of the above
ANS- B

40. What is the basic functions of a computer?
A. Processing
B. Storage
C. Output
D. All of the above
ANS- D

41. The instructions that are used for reading an input port and writing an output port respectively are
a) MOV, XCHG
b) MOV, IN
c) IN, MOV
d) IN, OUT
ANS- D

42. The instruction that loads effective address formed by destination operand into the specified source register is
    a) LEA
    b) LDS
    c) LES
    d) LAHF
    ANS- A
43. The instruction that supports addition when carry exists is
    a) ADD
    b) ADC
    c) ADD & ADC
    d) None of the mentioned
    ANS- B
44. A machine language instruction format consists of
    a) Operand field
    b) Operation code field
    c) Operation code field & operand field
    d) none of the mentioned
    ANS- C
45. The instruction, “INC” increases the contents of the specified register or memory location by
    a) 2
    b) 0
    c) 1
    d) 3
    ANS- C
46. 3. The instruction that enables subtraction with borrow is
    a) DEC
    b) SUB
    c) SBB
    d) None of the mentioned
    ANS- C
47. In general, the source operand of an instruction can be
    a) memory location
    b) register
    c) immediate data
    d) all of the mentioned
    ANS- D
48. The number of address bits in a 32K×12 memory is _____.
    A. 10
    B. 12
    C. 15
    D. 16
    ANS- C

49. The number of index bits in a direct mapping of 32K×12 main memory and 512 ×12cache memory is __.
    A. 6
    B. 7
    C. 8
    D. 9

    ANS- D

8086: Microprocessor

Multiple Choice Questions and Answers:-

1. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple

B. single

C. double

D. triple

Answer: B

2. Microprocessor is a/an _____ circuit that functions as the CPU of the compute

A. electronic

B. mechanic

C. integrating

D. processing

Answer: A

3. Microprocessor is the _____ of the computer and it perform all the computational tasks

A. main

B. heart

C. important

D. simple

Answer: B

4. The purpose of the microprocessor is to control _____

A. memory

B. switches

C. processing

D. tasks

Answer: A

5. The first digital electronic computer was built in the year_____

A. 1950

B. 1960

C. 1940

D. 1930

Answer: C

6. In 1960's texas institute invented _____

A. integrated circuits

B. microprocessor

C. vacuum tubes

D. transistors

Answer: A

7. The intel 8086 microprocessor is a _____ processor

A. 8 bit

B. 16 bit

C. 32 bit

D. 4 bit

Answer: B

8. The microprocessor can read/write 16 bit data from or to _____

A. memory

B. I /O device

C. processor

D. register

Answer: A

9. In 8086 microprocessor , the address bus is _____ bit wide

A.1

2 bit

B. 10 bit

C. 16 bit

D. 20 bit

Answer: D

10. The work of EU is _____

A. encoding

B. decoding

C. processing

D. calculations

Answer: B

11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____

A. the condition of result of ALU operation

B. the condition of memory

C. the result of addition

D. the result of subtraction

Answer: A

12. The CF is known as _____

A. carry flag

B. condition flag

C. common flag

D. single flag

Answer: A

13. The SF is called as _____

A. service flag

B. sign flag

C. single flag

D. condition flag

Answer: B

14. The OF is called as _____

A. overflow flag

B. overdue flag

C. one flag

D. over flag

Answer: A

15. The IF is called as _____

A. initial flag

B. indicate flag

C. interrupt flag

D. inter flag

Answer: C

16. The register AX is formed by grouping _____

A. AH & AL

B. BH & BL

C. CH & CL

D. DH & DL

Answer: A

17. The SP is indicated by _____

A. single pointer

B. stack pointer

C. source pointer

D. destination pointer

Answer: B

18. The BP is indicated by _____

A. base pointer

B. binary pointer

C. bit pointer

D. digital pointer

Answer: A

19. The SS is called as _____

A. single stack

B. stack segment

C. sequence stack

D. random stack

Answer: B

20. The index register are used to hold _____

A. memory register

B. offset address

C. segment memory

D. offset memory

Answer: A

21. The BIU contains FIFO register of size _____ bytes

A. 8

B. 6

C. 4

D. 12

Answer: B

22. The BIU prefetches the instruction from memory and store them in _____

A. queue

B. register

C. memory

D. stack

Answer: A

23. The 1 MB byte of memory can be divided into _____ segment

A. 1 Kbyte

B. 64 Kbyte

C. 33 Kbyte

D. 34 Kbyte

Answer: B

24. The DS is called as _____

A. data segment

B. digital segment

C. divide segment

D. decode segment

Answer: A

25. The CS register stores instruction _____ in code segment

A. stream

B. path

C. codes

D. stream line

Answer: C

26. The IP is _____ bits in length

A. 8 bits

B. 4 bits

C. 16 bits

D. 32 bits

Answer: C

27. The push source copies a word from source to _____

A. stack

B. memory

C. register

D. destination

Answer: A

28. LDs copies to consecutive words from memory to register and _____

A. ES

B. DS

C. SS

D. CS

Answer: B

29. INC destination increments the content of destination by _____

A. 1

B. 2

C. 30

D. 41

Answer: A

30. IMUL source is a signed _____

A. multiplication

B. addition

C. subtraction

D. division

Answer: A

31. _____destination inverts each bit of destination

A. NOT

B. NOR

C. AND

D. OR

Answer: A

32. The JS is called as _____

A. jump the signed bit

B. jump single bit

C. jump simple bit

D. jump signal it

Answer: A

33. Instruction providing both segment base and offset address are called _____

A. below type .

B. far type

C. low type

D. high type

Answer: B

34. The conditional branch instruction specify _____ for branching

A. conditions

B. instruction

C. address

D. memory

Answer: A

35. The microprocessor determines whether the specified condition exists or not by testing the _____

A. carry flag

B. conditional flag

C. common flag

D. sign flag

Answer: B

36. The LES copies to words from memory to register and _____

A. DS

B. CS

C. ES

D. DS

Answer: C

37. The _____ translates a byte from one code to another code

A. XLAT

B. XCHNG

C. POP

D. PUSH

Answer: A

38. The _____ contains an offset instead of actual address

A. SP

B. IP

C. ES

D. SS

Answer: B

39. The 8086 fetches instruction one after another from _____ of memory

A. code segment

B. IP

C. ES

D. SS

Answer: A

40. The BIU contains FIFO register of size 6 bytes called _____.

A. queue

B. stack

C. segment

D. register

Answer: A

41. The _____ is required to synchronize the internal operands in the processor CLK Signal

A. UR Signal

B. Vcc

C. AIE

D. Ground

Answer: A

42. The pin of minimum mode AD0-AD15 has _____ address

A. 16 bit

B. 20 bit

C. 32 bit

D. 4 bit

Answer: B

43. The pin of minimum mode AD0- AD15 has _____ data bus

A. 4 bit

B. 20 bit

C. 16 bit

D. 32 bit

Answer: C

44. The address bits are sent out on lines through _____

A. A16-19

B. A0-17

C. D0-D17

D. C0-C17

Answer: A

45. _____ is used to write into memory

A. RD

B. WR

C. RD / WR

D. CLK

Answer: B

46. The functions of Pins from 24 to 31 depend on the mode in which _____ is operating

A. 8085

B. 8086

C. 80835

D. 80845

Answer: B

47. The RD, WR, M/IO is the heart of control for a _____ mode

A. minimum

B. maximum

C. compatibility mode

D. control mode

Answer: A

48. In a minimum mode there is a _____ on the system bus

A. single

B. double

C. multiple

D. triple

Answer: A

49. If MN/MX is low the 8086 operates in _____ mode

A. Minimum

B. Maximum

C. both (A) and (B)

D. medium

Answer: B

50. In max mode, control bus signal So,S1 and S2 are sent out in _____ form

A. decoded

B. encoded

C. shared

D. unshared

Answer: B

51. The ___ bus controller device decodes the signals to produce the control bus signal

A. internal

B. data

C. external

D. address

Answer: C

52. A _____ Instruction at the end of interrupt service program takes the execution back to the interrupted program

A. forward

B. return

C. data

D. line

Answer: B

53. The main concerns of the _____ are to define a flexible set of commands

A. memory interface

B. peripheral interface

C. both (A) and (B)

D. control interface

Answer: A

54. Primary function of memory interfacing is that the _____ should be able to read from and write into register

A. multiprocessor

B. microprocessor

C. dual Processor

D. coprocessor

Answer: B

55. To perform any operations, the Mp should identify the _____

A. register

B. memory

C. interface

D. system

Answer: A

56. The Microprocessor places _____ address on the address bus

A. 4 bit

B. 8 bit

C. 16 bit

D. 32 bit

Answer: C

57. The Microprocessor places 16 bit address on the add lines from that address by _____

register should be selected

A. address

B. one

C. two

D. three

Answer: B

58. The _____of the memory chip will identify and select the register for the EPROM

A. internal decoder

B. external decoder

C. address decoder

D. data decoder

Answer: A

59. Microprocessor provides signal like ____ to indicate the read operatio

A. LOW

B. MCMW

C. MCMR

D. MCMWR

Answer: C

60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the _____ chip.

A. single

B. memory

C. multiple

D. triple

Answer: B

61. The remaining address line of _____ bus is decoded to generate chip select signal

A. data

B. address

C. control bus

D. both (a) and (b)

Answer: B

62. _____ signal is generated by combining RD and WR signals with IO/M

A. control

B. memory

C. register

D. system

Answer: A

63. Memory is an integral part of a _____ system

A. supercomputer

B. microcomputer

C. mini computer

D. mainframe computer

Answer: B

64. _____ has certain signal requirements write into and read from its registers

A. memory

B. register

C. both (a) and (b)

D. control

Answer: A

65. An _____ is used to fetch one address

A. internal decoder

B. external decoder

C. encoder

D. register

Answer: A

66. The primary function of the _____ is to accept data from I/P devices

A. multiprocessor

B. microprocessor

C. peripherals

D. interfaces

Answer: B

67. _____ signal prevent the microprocessor from reading the same data more than one

A. pipelining

B. handshaking

C. controlling

D. signaling

Answer: B

68. Bits in IRR interrupt are _____

A. reset

B. set

C. stop

D. start

Answer: B

69. _____ generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver

B. control logic

C. interrupt request register

D. interrupt register

Answer: B

70. The _____ pin is used to select direct command word

A. A0

B. D7-D6

C. A12

D. AD7-AD6

Answer: A

71. The _____ is used to connect more microprocessor

A. peripheral device

B. cascade

C. I/O devices

D. control unit

Answer: B

72. CS connect the output of _____

A. encoder

B. decoder

C. slave program

D. buffer

Answer: B

73. In which year, 8086 was introduced?

A. 1978

B. 1979

C. 1977

D. 1981

Answer: A

74. Expansion for HMOS technology_____

A. high level mode oxygen semiconductor

B. high level metal oxygen semiconductor

C. high performance medium oxide semiconductor

D. high performance metal oxide semiconductor

Answer: D

75. 8086 and 8088 contains _____ transistors

A. 29000

B. 24000

C. 34000

D. 54000

Answer: A

76. ALE stands for _____

A. address latch enable

B. address level enable

C. address leak enable

D. address leak extension

Answer: A

77. What is DEN?

A. direct enable

B. data entered

C. data enable

D. data encoding

Answer: C

78. In 8086, Example for Non maskable interrupts are _____.

A. TRAP

B. RST6.5

C. INTR

D. RST6.6

Answer: A

79. In 8086 the overflow flag is set when _____.

A. the sum is more than 16 bits.

B. signed numbers go out of their range after an arithmetic operation.

C. carry and sign flags are set.

D. subtraction

Answer: B

80. In 8086 microprocessor the following has the highest priority among all type interrupts?

A. NMI

B. DIV 0

C. TYPE 255

D. OVER FLOW

Answer: A

81. In 8086 microprocessor one of the following statements is not true?

A. coprocessor is interfaced in max mode.

B. coprocessor is interfaced in min mode.

C. I /O can be interfaced in max / min mode.

D. supports pipelining

Answer: B

82. Address line for TRAP is?

A. 0023H

B. 0024H

C. 0033H

D. 0099H

Answer: B

83. Access time is faster for _____.

A. ROM

B. SRAM

C. DRAM

D. ERAM

Answer: B

84. The First Microprocessor was_____.

A. Intel 4004

B. 8080

C. 8085

D. 4008

Answer: A

85. Status register is also called as _____.

A. accumulator

B. stack

C. counter

D. flags

Answer: D

86.Which of the following is not a basic element within the microprocessor?

A.Microcontroller

B. Arithmetic logic unit (ALU)

C. Register array

D. Control unit

Answer: A

87.Which method bypasses the CPU for certain types of data transfer?

A.Software interrupts

B. Interrupt-driven I/O

C. Polled I/O

D. Direct memory access (DMA)

Answer: D

88.Which bus is bidirectional?

A.

Address bus

B. Control bus

C. Data bus

D. None of the above

Answer: C

89.The first microprocessor had a(n)_____.

A.1 – bit data bus

B. 2 – bit data bus

C. 4 – bit data bus

D. 8 – bit data bus

Answer: C

90.Which microprocessor has multiplexed data and address lines?

A.8086

B. 80286

C. 80386

D. Pentium

Answer: A

91.Which is not an operand?

A.Variable

B. Register

C. Memory location

D. Assembler

Answer: D

92.Which is not part of the execution unit (EU)?

A.Arithmetic logic unit (ALU)

B. Clock

C. General registers

D. Flags

Answer: B

93.A 20-bit address bus can locate _____.

A.1,048,576 locations

B. 2,097,152 locations

C. 4,194,304 locations

D. 8,388,608 locations

Answer: A

94.Which of the following is not an arithmetic instruction?

A. INC (increment)

B. CMP (compare)

C. DEC (decrement)

D. ROL (rotate left)

Answer: D

95.During a read operation the CPU fetches _____.

A.a program instruction

B. another address

C. data itself

D. all of the above

Answer: D

96.Which of the following is not an 8086/8088 general-purpose register?

A.Code segment (CS)

B. Data segment (DS)

C. Stack segment (SS)

D. Address segment (AS)

Answer: D

97.A 20-bit address bus allows access to a memory of capacity

A.1 MB

B. 2 MB

C. 4 MB

D. 8 MB

Answer: A

98.Which microprocessor accepts the program written for 8086 without any changes?

A.8085

B. 8086

C. 8087

D. 8088

Answer: D

99.Which group of instructions do not affect the flags?

A.Arithmetic operations

B. Logic operations

C. Data transfer operations

D. Branch operations

Answer: C

100.The result of MOV AL, 65 is to store

A.store 0100 0010 in AL

B. store 42H in AL

C. store 40H in AL

D. store 0100 0001 in AL

Answer: D

8086: Microprocessor

Multiple Choice Questions and Answers:-

1. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple

B. single

C. double

D. triple

Answer: B

2. Microprocessor is a/an _____ circuit that functions as the CPU of the compute

A. electronic

B. mechanic

C. integrating

D. processing

Answer: A

3. Microprocessor is the _____ of the computer and it perform all the computational tasks

A. main

B. heart

C. important

D. simple

Answer: B

4. The purpose of the microprocessor is to control _____

A. memory

B. switches

C. processing

D. tasks

Answer: A

5. The first digital electronic computer was built in the year_____

A. 1950

B. 1960

C. 1940

D. 1930

Answer: C

6. In 1960's texas institute invented _____

A. integrated circuits

B. microprocessor

C. vacuum tubes

D. transistors

Answer: A

7. The intel 8086 microprocessor is a _____ processor

A. 8 bit

B. 16 bit

C. 32 bit

D. 4 bit

Answer: B

8. The microprocessor can read/write 16 bit data from or to _____

A. memory

B. I /O device

C. processor

D. register

Answer: A

9. In 8086 microprocessor , the address bus is _____ bit wide

A.1

2 bit

B. 10 bit

C. 16 bit

D. 20 bit

Answer: D

10. The work of EU is _____

A. encoding

B. decoding

C. processing

D. calculations

Answer: B

11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____

A. the condition of result of ALU operation

B. the condition of memory

C. the result of addition

D. the result of subtraction

Answer: A

12. The CF is known as _____

A. carry flag

B. condition flag

C. common flag

D. single flag

Answer: A

13. The SF is called as _____

A. service flag

B. sign flag

C. single flag

D. condition flag

Answer: B

14. The OF is called as _____

A. overflow flag

B. overdue flag

C. one flag

D. over flag

Answer: A

15. The IF is called as _____

A. initial flag

B. indicate flag

C. interrupt flag

D. inter flag

Answer: C

16. The register AX is formed by grouping _____

A. AH & AL

B. BH & BL

C. CH & CL

D. DH & DL

Answer: A

17. The SP is indicated by _____

A. single pointer

B. stack pointer

C. source pointer

D. destination pointer

Answer: B

18. The BP is indicated by _____

A. base pointer

B. binary pointer

C. bit pointer

D. digital pointer

Answer: A

19. The SS is called as _____

A. single stack

B. stack segment

C. sequence stack

D. random stack

Answer: B

20. The index register are used to hold _____

A. memory register

B. offset address

C. segment memory

D. offset memory

Answer: A

21. The BIU contains FIFO register of size _____ bytes

A. 8

B. 6

C. 4

D. 12

Answer: B

22. The BIU prefetches the instruction from memory and store them in _____

A. queue

B. register

C. memory

D. stack

Answer: A

23. The 1 MB byte of memory can be divided into _____ segment

A. 1 Kbyte

B. 64 Kbyte

C. 33 Kbyte

D. 34 Kbyte

Answer: B

24. The DS is called as _____

A. data segment

B. digital segment

C. divide segment

D. decode segment

Answer: A

25. The CS register stores instruction _____ in code segment

A. stream

B. path

C. codes

D. stream line

Answer: C

26. The IP is _____ bits in length

A. 8 bits

B. 4 bits

C. 16 bits

D. 32 bits

Answer: C

27. The push source copies a word from source to _____

A. stack

B. memory

C. register

D. destination

Answer: A

28. LDs copies to consecutive words from memory to register and _____

A. ES

B. DS

C. SS

D. CS

Answer: B

29. INC destination increments the content of destination by _____

A. 1

B. 2

C. 30

D. 41

Answer: A

30. IMUL source is a signed _____

A. multiplication

B. addition

C. subtraction

D. division

Answer: A

31. _____destination inverts each bit of destination

A. NOT

B. NOR

C. AND

D. OR

Answer: A

32. The JS is called as _____

A. jump the signed bit

B. jump single bit

C. jump simple bit

D. jump signal it

Answer: A

33. Instruction providing both segment base and offset address are called _____

A. below type .

B. far type

C. low type

D. high type

Answer: B

34. The conditional branch instruction specify _____ for branching

A. conditions

B. instruction

C. address

D. memory

Answer: A

35. The microprocessor determines whether the specified condition exists or not by testing the _____

A. carry flag

B. conditional flag

C. common flag

D. sign flag

Answer: B

36. The LES copies to words from memory to register and _____

A. DS

B. CS

C. ES

D. DS

Answer: C

37. The _____ translates a byte from one code to another code

A. XLAT

B. XCHNG

C. POP

D. PUSH

Answer: A

38. The _____ contains an offset instead of actual address

A. SP

B. IP

C. ES

D. SS

Answer: B

39. The 8086 fetches instruction one after another from _____ of memory

A. code segment

B. IP

C. ES

D. SS

Answer: A

40. The BIU contains FIFO register of size 6 bytes called _____.

A. queue

B. stack

C. segment

D. register

Answer: A

41. The _____ is required to synchronize the internal operands in the processor CLK Signal

A. UR Signal

B. Vcc

C. AIE

D. Ground

Answer: A

42. The pin of minimum mode AD0-AD15 has _____ address

A. 16 bit

B. 20 bit

C. 32 bit

D. 4 bit

Answer: B

43. The pin of minimum mode AD0- AD15 has _____ data bus

A. 4 bit

B. 20 bit

C. 16 bit

D. 32 bit

Answer: C

44. The address bits are sent out on lines through _____

A. A16-19

B. A0-17

C. D0-D17

D. C0-C17

Answer: A

45. _____ is used to write into memory

A. RD

B. WR

C. RD / WR

D. CLK

Answer: B

46. The functions of Pins from 24 to 31 depend on the mode in which _____ is operating

A. 8085

B. 8086

C. 80835

D. 80845

Answer: B

47. The RD, WR, M/IO is the heart of control for a _____ mode

A. minimum

B. maximum

C. compatibility mode

D. control mode

Answer: A

48. In a minimum mode there is a _____ on the system bus

A. single

B. double

C. multiple

D. triple

Answer: A

49. If MN/MX is low the 8086 operates in _____ mode

A. Minimum

B. Maximum

C. both (A) and (B)

D. medium

Answer: B

50. In max mode, control bus signal So,S1 and S2 are sent out in _____ form

A. decoded

B. encoded

C. shared

D. unshared

Answer: B

51. The ___ bus controller device decodes the signals to produce the control bus signal

A. internal

B. data

C. external

D. address

Answer: C

52. A _____ Instruction at the end of interrupt service program takes the execution back to the interrupted program

A. forward

B. return

C. data

D. line

Answer: B

53. The main concerns of the _____ are to define a flexible set of commands

A. memory interface

B. peripheral interface

C. both (A) and (B)

D. control interface

Answer: A

54. Primary function of memory interfacing is that the _____ should be able to read from and write into register

A. multiprocessor

B. microprocessor

C. dual Processor

D. coprocessor

Answer: B

55. To perform any operations, the Mp should identify the _____

A. register

B. memory

C. interface

D. system

Answer: A

56. The Microprocessor places _____ address on the address bus

A. 4 bit

B. 8 bit

C. 16 bit

D. 32 bit

Answer: C

57. The Microprocessor places 16 bit address on the add lines from that address by _____

register should be selected

A. address

B. one

C. two

D. three

Answer: B

58. The _____of the memory chip will identify and select the register for the EPROM

A. internal decoder

B. external decoder

C. address decoder

D. data decoder

Answer: A

59. Microprocessor provides signal like ____ to indicate the read operatio

A. LOW

B. MCMW

C. MCMR

D. MCMWR

Answer: C

60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the _____ chip.

A. single

B. memory

C. multiple

D. triple

Answer: B

61. The remaining address line of _____ bus is decoded to generate chip select signal

A. data

B. address

C. control bus

D. both (a) and (b)

Answer: B

62. _____ signal is generated by combining RD and WR signals with IO/M

A. control

B. memory

C. register

D. system

Answer: A

63. Memory is an integral part of a _____ system

A. supercomputer

B. microcomputer

C. mini computer

D. mainframe computer

Answer: B

64. _____ has certain signal requirements write into and read from its registers

A. memory

B. register

C. both (a) and (b)

D. control

Answer: A

65. An _____ is used to fetch one address

A. internal decoder

B. external decoder

C. encoder

D. register

Answer: A

66. The primary function of the _____ is to accept data from I/P devices

A. multiprocessor

B. microprocessor

C. peripherals

D. interfaces

Answer: B

67. _____ signal prevent the microprocessor from reading the same data more than one

A. pipelining

B. handshaking

C. controlling

D. signaling

Answer: B

68. Bits in IRR interrupt are _____

A. reset

B. set

C. stop

D. start

Answer: B

69. _____ generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver

B. control logic

C. interrupt request register

D. interrupt register

Answer: B

70. The _____ pin is used to select direct command word

A. A0

B. D7-D6

C. A12

D. AD7-AD6

Answer: A

71. The _____ is used to connect more microprocessor

A. peripheral device

B. cascade

C. I/O devices

D. control unit

Answer: B

72. CS connect the output of _____

A. encoder

B. decoder

C. slave program

D. buffer

Answer: B

73. In which year, 8086 was introduced?

A. 1978

B. 1979

C. 1977

D. 1981

Answer: A

74. Expansion for HMOS technology_____

A. high level mode oxygen semiconductor

B. high level metal oxygen semiconductor

C. high performance medium oxide semiconductor

D. high performance metal oxide semiconductor

Answer: D

75. 8086 and 8088 contains _____ transistors

A. 29000

B. 24000

C. 34000

D. 54000

Answer: A

76. ALE stands for _____

A. address latch enable

B. address level enable

C. address leak enable

D. address leak extension

Answer: A

77. What is DEN?

A. direct enable

B. data entered

C. data enable

D. data encoding

Answer: C

78. In 8086, Example for Non maskable interrupts are _____.

A. TRAP

B. RST6.5

C. INTR

D. RST6.6

Answer: A

79. In 8086 the overflow flag is set when _____.

A. the sum is more than 16 bits.

B. signed numbers go out of their range after an arithmetic operation.

C. carry and sign flags are set.

D. subtraction

Answer: B

80. In 8086 microprocessor the following has the highest priority among all type interrupts?

A. NMI

B. DIV 0

C. TYPE 255

D. OVER FLOW

Answer: A

81. In 8086 microprocessor one of the following statements is not true?

A. coprocessor is interfaced in max mode.

B. coprocessor is interfaced in min mode.

C. I /O can be interfaced in max / min mode.

D. supports pipelining

Answer: B

82. Address line for TRAP is?

A. 0023H

B. 0024H

C. 0033H

D. 0099H

Answer: B

83. Access time is faster for _____.

A. ROM

B. SRAM

C. DRAM

D. ERAM

Answer: B

84. The First Microprocessor was_____.

A. Intel 4004

B. 8080

C. 8085

D. 4008

Answer: A

85. Status register is also called as _____.

A. accumulator

B. stack

C. counter

D. flags

Answer: D

86.Which of the following is not a basic element within the microprocessor?

A.Microcontroller

B. Arithmetic logic unit (ALU)

C. Register array

D. Control unit

Answer: A

87.Which method bypasses the CPU for certain types of data transfer?

A.Software interrupts

B. Interrupt-driven I/O

C. Polled I/O

D. Direct memory access (DMA)

Answer: D

88.Which bus is bidirectional?

A.

Address bus

B. Control bus

C. Data bus

D. None of the above

Answer: C

89.The first microprocessor had a(n)_____.

A.1 – bit data bus

B. 2 – bit data bus

C. 4 – bit data bus

D. 8 – bit data bus

Answer: C

90.Which microprocessor has multiplexed data and address lines?

A.8086

B. 80286

C. 80386

D. Pentium

Answer: A

91.Which is not an operand?

A.Variable

B. Register

C. Memory location

D. Assembler

Answer: D

92.Which is not part of the execution unit (EU)?

A.Arithmetic logic unit (ALU)

B. Clock

C. General registers

D. Flags

Answer: B

93.A 20-bit address bus can locate _____.

A.1,048,576 locations

B. 2,097,152 locations

C. 4,194,304 locations

D. 8,388,608 locations

Answer: A

94.Which of the following is not an arithmetic instruction?

A. INC (increment)

B. CMP (compare)

C. DEC (decrement)

D. ROL (rotate left)

Answer: D

95.During a read operation the CPU fetches _____.

A.a program instruction

B. another address

C. data itself

D. all of the above

Answer: D

96.Which of the following is not an 8086/8088 general-purpose register?

A.Code segment (CS)

B. Data segment (DS)

C. Stack segment (SS)

D. Address segment (AS)

Answer: D

97.A 20-bit address bus allows access to a memory of capacity

A.1 MB

B. 2 MB

C. 4 MB

D. 8 MB

Answer: A

98.Which microprocessor accepts the program written for 8086 without any changes?

A.8085

B. 8086

C. 8087

D. 8088

Answer: D

99.Which group of instructions do not affect the flags?

A.Arithmetic operations

B. Logic operations

C. Data transfer operations

D. Branch operations

Answer: C

100.The result of MOV AL, 65 is to store

A.store 0100 0010 in AL

B. store 42H in AL

C. store 40H in AL

D. store 0100 0001 in AL

Answer: D

COMPUTER ORGANIZATION AND ARCHITECTURE

BCA

Multiple choice questions

1. In Reverse Polish notation, expression A*B+C*D is written as
   (A) AB*CD*+ (B) A*BCD*+ (C) AB*CD+* (D) A*B*CD+
   Ans: A
2. SIMD represents an organization that _____.
   (A) refers to a computer system capable of processing several programs at the same time.
   (B) represents organization of single computer containing a control unit, processor unit and a memory unit.
   (C) includes many processing units under the supervision of a common control unit
   (D) none of the above.
   Ans: C
3. Floating point representation is used to store
   (A) Boolean values (B) whole numbers (C) real integers (D) integers
   Ans: C
4. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?
   (A) 1 Megabyte/sec (B) 4 Megabytes/sec
   (C) 8 Megabytes/sec (D) 2 Megabytes/sec
   Ans: D
5. Assembly language
   (A) uses alphabetic codes in place of binary numbers used in machine language
   (B) is the easiest language to write programs
   (C) need not be translated into machine language
   (D) None of these
   Ans: A
6. In computers, subtraction is generally carried out by
   (A) 9's complement (B) 10's complement
   (C) 1's complement (D) 2's complement
   Ans: D
7. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to
   (A) the time its takes for the platter to make a full rotation
   (B) the time it takes for the read-write head to move into position over the appropriate track
   (C) the time it takes for the platter to rotate the correct sector under the head
   (D) none of the above

Ans: A

8. What characteristic of RAM memory makes it not suitable for permanent storage?
   (A) too slow (B) unreliable (C) it is volatile (D) too bulky
   Ans: C
9. Computers use addressing mode techniques for _____.
   (A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
   (B) to reduce no. of bits in the field of instruction
   (C) specifying rules for modifying or interpreting address field of the instruction
   (D) All the above
   Ans: D
10. The circuit used to store one bit of data is known as
    (A) Register (B) Encoder (C) Decoder (D) Flip Flop
    Ans: D
11. (2FAOC) 16 is equivalent to
    (A) (195 084) 10 (B) (001011111010 0000 1100) 2
    (C) Both (A) and (B) (D) None of these
    Ans: B
12. The average time required to reach a storage location in memory and obtain its contents is called the
    (A) seek time (B) turnaround time (C) access time (D) transfer time
    Ans: C
13. Which of the following is not a weighted code?
    (A) Decimal Number system (B) Excess 3-cod
    (C) Binary number System (D) None of these
    Ans: B
14. The idea of cache memory is based
    (A) on the property of locality of reference (B) on the heuristic 90-10 rule
    (C) on the fact that references generally tend to cluster (D) all of the above
    Ans: A
15. Which of the following is lowest in memory hierarchy?
    (A) Cache memory
    (B) Secondary memory
    (C) Registers
    (D) RAM
    (E) None of these
    Ans (B) Secondary memory

16. The addressing mode used in an instruction of the form ADD X Y, is
    (A) Absolute (B) indirect (C) index (D) none of these
    Ans: C
17. If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is

(A) 93% (B) 90% (C) 88% (D) 87%

Ans: B

18. In a memory-mapped I/O system, which of the following will not be there?

(A) LDA (B) IN (C) ADD (D) OUT

Ans: A

19. In a vectored interrupt.

(A) the branch address is assigned to a fixed location in memory.

(B) the interrupting source supplies the branch information to the processor through an interrupt vector.

(C) the branch address is obtained from a register in the processor

(D) none of the above

Ans: B

20. Von Neumann architecture is

(A) SISD (B) SIMD (C) MIMD (D) MISD

Ans: A

21. The circuit used to store one bit of data is known as

(A) Encoder (B) OR gate (C) Flip Flop (D) Decoder

Ans: C

22. Cache memory acts between

(A) CPU and RAM (B) RAM and ROM (C) CPU and Hard Disk (D) None of these

Ans: A

23. Write Through technique is used in which memory for updating the data

(A) Virtual memory (B) Main memory

(C) Auxiliary memory (D) Cache memory

Ans: D

24. Generally Dynamic RAM is used as main memory in a computer system as it

(A) Consumes less power (B) has higher speed

(C) has lower cell density (D) needs refreshing circuitary

Ans: B

25. In signed-magnitude binary division, if the dividend is (11100) 2 and divisor is (10011) 2 then the result is

(A) (00100) 2 (B) (10100) 2 (C) (11001) 2 (D) (01100) 2

Ans: B

26. Virtual memory consists of

(A) Static RAM (B) Dynamic RAM

(C) Magnetic memory (D) None of these

Ans: A

27. In a program using subroutine call instruction, it is necessary

(A) initialise program counter (B) Clear the accumulator

(C) Reset the microprocessor (D) Clear the instruction register

Ans: D

28. A Stack-organised Computer uses instruction of

(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressing

Ans: C

29. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be

(A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits

Ans: C

30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit

(A) n TQD =• (B) T D = (C) D = T . Q n (D) n TQD =⊕

Ans: D

31. Logic X-OR operation of (4ACO) H & (B53F) H results

(A) AACB (B) 0000 (C) FFFF (D) ABCD

Ans: C

32. When CPU is executing a Program that is part of the Operating System, it is said to be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mode

Ans: B

33. An n-bit microprocessor has

(A) n-bit program counter (B) n-bit address register

(C) n-bit ALU (D) n-bit instruction register

Ans: D

34. Cache memory works on the principle of

(A) Locality of data (B) Locality of memory

(C) Locality of reference (D) Locality of reference & memory

Ans: C

35. The main memory in a Personal Computer (PC) is made of

(A) cache memory. (B) static RAM

(C) Dynamic Ram (D) both (A) and (B) .

Ans: D

36. In computers, subtraction is carried out generally by

(A) 1's complement method (B) 2's complement method

(C) signed magnitude method (D) BCD subtraction method

Ans: B

37. PSW is saved in stack when there is a

(A) interrupt recognised (B) execution of RST instruction

(C) Execution of CALL instruction (D) All of these

Ans: A

38. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be

(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10

Ans: A

39. The circuit converting binary data in to decimal is

(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter

Ans: D

40. A three input NOR gate gives logic high output only when
(A) one input is high (B) one input is low
(C) two input are low (D) all input are high
Ans: D

41. n bits in operation code imply that there are _____ possible distinct operators (A) 2n (B) 2n (C) n/2 (D) n2
Ans: B

42. _____ register keeps tracks of the instructions stored in program stored in memory.
(A) AR (Address Register) (B) XR (Index Register)
(C) PC (Program Counter) (D) AC (Accumulator)
Ans: C

43. Memory unit accessed by content is called
(A) Read only memory (B) Programmable Memory
(C) Virtual Memory (D) Associative Memory
Ans: D

44. 'Aging registers' are
(A) Counters which indicate how long ago their associated pages have been referenced.
(B) Registers which keep track of when the program was last accessed.
(C) Counters to keep track of last accessed instruction.
(D) Counters to keep track of the latest data structures referred.
Ans: A

45 The instruction 'ORG O' is a
(A) Machine Instruction. (B) Pseudo instruction.
(C) High level instruction. (D) Memory instruction.
Ans: B

46 Translation from symbolic program into Binary is done in
(A) Two passes. (B) Directly (C) Three passes. (D) Four passes.
Ans: A

47 A floating point number that has a O in the MSB of mantissa is said to have
(A) Overflow (B) Underflow (C) Important number (D) Undefined
Ans: B

48 The BSA instruction is
(A) Branch and store accumulator (B) Branch and save return address
(C) Branch and shift address (D) Branch and show accumulator
Ans: B

49 State whether True or False.
(i) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers.
Ans: True.
(ii) An arithmetic shift left multiplies a signed binary number by 2.

Ans: False.

50 Logic gates with a set of input and outputs is arrangement of

(A) Combinational circuit (B) Logic circuit (C) Design circuits (D) Register

Ans: A

51. MIMD stands for

(A) Multiple instruction multiple data (B) Multiple instruction memory data

(C) Memory instruction multiple data (D) Multiple information memory data

Ans: A

52 A k-bit field can specify any one of

(A) 3k registers (B) 2k registers

(C) K2 registers (D) K3 registers

Ans: B

53 The time interval between adjacent bits is called the

(A) Word-time (B) Bit-time (C) Turn around time (D) Slice time

Ans: B

54 A group of bits that tell the computer to perform a specific operation is known as

(A) Instruction code (B) Micro-operation (C) Accumulator (D) Register

Ans: A

55 The load instruction is mostly used to designate a transfer from memory to a processor register known as

(A) Accumulator (B) Instruction Register

(C) Program counter (D) Memory address Register

Ans: A

56 The communication between the components in a microcomputer takes place via the address and

(A) I/O bus (B) Data bus (C) Address bus (D) Control lines

Ans: B

57 An instruction pipeline can be implemented by means of

(A) LIFO buffer (B) FIFO buffer (C) Stack (D) None of the above

Ans: B

58 Data input command is just the opposite of a

(A) Test command (B) Control command (C) Data output (D) Data channel

Ans: C

59 A microprogram sequencer

(A) generates the address of next micro instruction to be executed.

(B) generates the control signals to execute a microinstruction.

(C) sequentially averages all microinstructions in the control memory.

(D) enables the efficient handling of a micro program subroutine.

Ans: A

60 . A binary digit is called a

(A) Bit (B) Byte (C) Number (D) Character

Ans: A

61 A flip-flop is a binary cell capable of storing information of

(A) One bit (B) Byte (C) Zero bit (D) Eight bit

Ans: A

62 The operation executed on data stored in registers is called

(A) Macro-operation (B) Micro-operation

(C) Bit-operation (D) Byte-operation

Ans: B

63 MRI indicates

(A) Memory Reference Information. (B) Memory Reference Instruction.

(C) Memory Registers Instruction. (D) Memory Register information

Ans: B

64 Self-contained sequence of instructions that performs a given computational task is called

(A) Function (B) Procedure (C) Subroutine (D) Routine

Ans: A

65 Microinstructions are stored in control memory groups, with each group specifying a

(A) Routine (B) Subroutine (C) Vector (D) Address

Ans: A

66 An interface that provides a method for transferring binary information between internal storage and external devices is called

(A) I/O interface (B) Input interface (C) Output interface (D) I/O bus

Ans: A

67 Status bit is also called

(A) Binary bit (B) Flag bit (C) Signed bit (D) Unsigned bit

Ans: B

68 An address in main memory is called

(A) Physical address (B) Logical address (C) Memory address (D) Word address

Ans: A

69 If the value V(x) of the target operand is contained in the address field itself, the addressing mode is

(A) immediate. (B) direct. (C) indirect. (D) implied.

Ans: B

70 can be represented in a signed magnitude format and in a 1's complement format as

(A) 111011 & 100100 (B) 100100 & 111011

(C) 011011 & 100100 (D) 100100 & 011011

Ans: A

71 The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

(A) Data transfer instructions. (B) Program control instructions.

(C) Input-output instructions. (D) Logical instructions.

Ans: A

72 A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called

(A) register (B) flip-flop (C) transistor. (D) counter.

Ans: D

73. The performance of cache memory is frequently measured in terms of a quantity called

(A) Miss ratio. (B) Hit ratio. (C) Latency ratio. (D) Read ratio.

Ans: C

74. The information available in a state table may be represented graphically in a

(A) simple diagram. (B) state diagram. (C) complex diagram. (D) data flow diagram.

Ans: B

75 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.

(A) relative address mode. (B) index addressing mode.

(C) register mode. (D) implied mode.

Ans: A

76 An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

(A) DDA. (B) Serial interface. (C) BR. (D) DMA.

Ans: D

77 The 2s compliment form (Use 6 bit word) of the number 1010 is

(A) 111100. (B) 110110. (C) 110111. (D) 1011.

Ans: B

78 A register capable of shifting its binary information either to the right or the left is called a

(A) parallel register. (B) serial register. (C) shift register. (D) storage register.

Ans: C

79 What is the content of Stack Pointer (SP)?

(A) Address of the current instruction (B) Address of the next instruction

(C) Address of the top element of the stack (D) Size of the stack.

Ans: C

80 Which of the following interrupt is non maskable

(A) INTR. (B) RST 7.5. (C) RST 6.5. (D) TRAP.

Ans: D

81 Which of the following is a main memory

(A) Secondary memory. (B) Auxiliary memory.

(C) Cache memory. (D) Virtual memory.

Ans: C

82 Which of the following are not a machine instructions

(A) MOV. (B) ORG. (C) END. (D) (B) & (C) .

Ans: D

83 In Assembly language programming, minimum number of operands required for an instruction is/are

(A) Zero. (B) One. (C) Two. (D) Both (B) & (C) .

Ans: A

84 The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is

(A) 64 K. (B) 4 GB. (C) both (A) & (B) . (D) None of these.

Ans: B

85 The memory unit that communicates directly with the CPU is called the

(A) main memory (B) Secondary memory

(C) shared memory (D) auxiliary memory.

Ans: A

86 The average time required to reach a storage location in memory and obtain its contents is called

(A) Latency time. (B) Access time.

(C) Turnaround time. (D) Response time.

Ans: B

State True or False

87 A byte is a group of 16 bits.

Ans: False

88 A nibble is a group of 16 bits.

Ans: False

89 When a word is to be written in an associative memory, address has got to be given.

Ans: False

90 When two equal numbers are subtracted, the result would be _____and not_____.

Ans: +ZERO, -ZERO.

91 A _____development system and an _____are essential tools for writing large assembly language programs.

Ans: Microprocessor, assembler

92 In an operation performed by the ALU, carry bit is set to 1 if the end carry C 8 is _____. It is cleared to 0 (zero) if the carry is _____ _____.

Ans: One, zero

93 A successive A/D converter is

(A) a high-speed converter. (B) a low speed converter.

(C) a medium speed converter. (D) none of these.

Ans: C

94 When necessary, the results are transferred from the CPU to main memory by

(A) I/O devices. (B) CPU. (C) shift registers. (D) none of these.

Ans: C

96 A combinational logic circuit which sends data coming from a single source to two or more separate destinations is

(A) Decoder. (B) Encoder. (C) Multiplexer. (D) Demultiplexer.

Ans: D

97 In which addressing mode the operand is given explicitly in the instruction

(A) Absolute. (B) Immediate . (C) Indirect. (D) Direct.

Ans: B

98 A stack organized computer has

(A) Three-address Instruction. (B) Two-address Instruction.

(C) One-address Instruction. (D) Zero-address Instruction.

Ans: D

99 A Program Counter contains a number 825 and address part of the instruction contains the number 24. The effective address in the relative address mode, when an instruction is read from the memory is

(A) 849. (B) 850. (C) 801. (D) 802.

Ans: B

102 A page fault

(A) Occurs when there is an error in a specific page.

(B) Occurs when a program accesses a page of main memory.

(C) Occurs when a program accesses a page not currently in main memory.

(D) Occurs when a program accesses a page belonging to another program.

Ans: C

103. The load instruction is mostly used to designate a transfer from memory to a processor register known as____.

A. Accumulator B. Instruction Register

C. Program counter D. Memory address Register

Ans: A

104. A group of bits that tell the computer to perform a specific operation is known as____.

A. Instruction code B. Micro-operation

C. Accumulator D. Register

Ans: A

105. The time interval between adjacent bits is called the_____.

A. Word-time B. Bit-time

C. Turn around time D. Slice time

Ans: B

106. A k-bit field can specify any one of_____.

A. 3k registers B. 2k registers

C. K2 registers D. K3 registers

Ans: B

107. MIMD stands for _____.

A. Multiple instruction multiple data

B. Multiple instruction memory data

C. Memory instruction multiple data

D. Multiple information memory data

Ans: A

108. Logic gates with a set of input and outputs is arrangement of_____.

A. Computational circuit
B. Logic circuit
C. Design circuits
D. Register

Ans: A

109. The average time required to reach a storage location in memory and obtain its contents is called_____.

A. Latency time. B. Access time.
C. Turnaround time. D. Response time.

Ans: B

110. The BSA instruction is_____.

A. Branch and store accumulator B. Branch and save return address
C. Branch and shift address D. Branch and show accumulator

Ans: B

111. A floating point number that has a O in the MSB of mantissa is said to have_____.

A. Overflow B. Underflow
C. Important number D. Undefined

Ans: B

112. Translation from symbolic program into Binary is done in_____.

A. Two passes. B. Directly
C. Three passes. D. Four passes.

Ans: A

113. The instruction 'ORG O' is a_____.

A. Machine Instruction. B. Pseudo instruction.
C. High level instruction. D. Memory instruction.

Ans: B

114. 'Aging registers' are _____.

A. Counters which indicate how long ago their associated pages have been referenced.
B. Registers which keep track of when the program was last accessed.
C. Counters to keep track of last accessed instruction.
D. Counters to keep track of the latest data structures referred.

Ans: A

115. Memory unit accessed by content is called_____.

A. Read only memory B. Programmable Memory
C. Virtual Memory D. Associative Memory

Ans: D

116. _____ register keeps tracks of the instructions stored in program stored in memory.

A. AR (Address Register) B. XR (Index Register)
C. PC (Program Counter) D. AC (Accumulator)

Ans: C

117. n bits in operation code imply that there are _____ possible distinct operators.

A. 2n B. 2n
C. n/2 D. n2

Ans: B

118. A three input NOR gate gives logic high output only when_____.

A. one input is high B. one input is low

C. two input are low D. all input are high

Ans: D

119. The circuit converting binary data in to decimal is_____.

A. Encoder B. Multiplexer

C. Decoder D.Code converter

Ans: D

120. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be _____.

A. (812)10 B. (-12)10

C. (12)10 D. (-812)10

Ans: A

121. PSW is saved in stack when there is a _____.

A. interrupt recognized B. execution of RST instruction

C. Execution of CALL instruction D. All of these

Ans: A

122. In computers, subtraction is carried out generally by____.

A. 1's complement method B. 2's complement method

C. signed magnitude method D. BCD subtraction method

Ans: B

123. The main memory in a Personal Computer (PC) is made of_____.

A. cache memory. B. static RAM

C. Dynamic Ram D. bothA.and (B).

Ans: D

124. Cache memory works on the principle of_____.

A. Locality of data B. Locality of memory

C. Locality of reference D. Locality of reference & memory

Ans: C

125. An n-bit microprocessor has_____.

A. n-bit program counter B. n-bit address register

C. n-bit ALU D. n-bit instruction register

Ans: D

126. When CPU is executing a Program that is part of the Operating System, it is said to be in _____.

A. Interrupt mode B. System mode

C. Half mode D. Simplex mode

Ans: B

127. Logic X-OR operation of (4ACO)H& (B53F)H results _____.

A. AACB B. 0000

C. FFFF D. ABCD

Ans: C

128. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be_____.

A. 11 bits B. 21 bits

C. 16 bits D. 20 bits

Ans: C

129. A Stack-organised Computer uses instruction of _____.

A. Indirect addressing B. Two-addressing
C. Zero addressing D. Index addressing

Ans: C

130. In a program using subroutine call instruction, it is necessary_____.

A. initialize program counter B. Clear the accumulator
C. Reset the microprocessor D. Clear the instruction register

Ans: D

131. Virtual memory consists of _____.

A. Static RAM B. Dynamic RAM
C. Magnetic memory D. None of these

Ans: A

132. In signed-magnitude binary division, if the dividend is (11100)2 and divisor is (10011)2 then the result is _____.

A. (00100)2 B. (10100)2
C. (11001)2 D. (01100)2

Ans: B

133. Generally Dynamic RAM is used as main memory in a computer system as it_____.

A. Consumes less power B. has higher speed
C. has lower cell density D. needs refreshing circuitry

Ans: B

134. Write Through technique is used in which memory for updating the data _____.

A. Virtual memory B. Main memory
C. Auxiliary memory D. Cache memory

Ans: D

135. Cache memory acts between_____.

A. CPU and RAM B. RAM and ROM
C. CPU and Hard Disk D. None of these

Ans: A

136. The circuit used to store one bit of data is known as _____.

A. Encoder B. OR gate
C. Flip Flop D. Decoder

Ans: C

137. Von Neumann architecture is _____.

A. SISD B. SIMD
C. MIMD D. MISD

Ans: A

138. In a vectored interrupt.

A. the branch address is assigned to a fixed location in memory.
B. the interrupting source supplies the branch information to the processor through an interrupt vector.
C. the branch address is obtained from a register in the processor
D. none of the above

Ans: B

139. . In a memory-mapped I/O system, which of the following will not be there?

A. LDA B. IN

C. ADD D. OUT

Ans: A

140. If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is _____.

A. 93% B. 90%

C. 88% D. 87%

Ans: B

141. The addressing mode used in an instruction of the form ADD X Y, is _____.

A. Absolute B. indirect

C. index D. none of these

Ans: C

142. _____ register keeps track of the instructions stored in program stored in memory.

A. AR (Address Register) B. XR (Index Register)

C. PC (Program Counter) D. AC (Accumulator)

Ans: C

143. The idea of cache memory is based _____.

A. on the property of locality of reference

B. on the heuristic 90-10 rule

C. on the fact that references generally tend to cluster

D. all of the above

Ans: A

144. Which of the following is not a weighted code?

A. Decimal Number system B. Excess 3-cod

C. Binary number System D. None of these

Ans: B

145. The average time required to reach a storage location in memory and obtain its contents is called the _____.

A. seek time B. turnaround time

C. access time D. transfer time

Ans: C

146. (2FAOC)16 is equivalent to _____.

A. (195 084)10 B. (001011111010 0000 1100)2

C. Both A.and (B) D. None of these

Ans: B

147. The circuit used to store one bit of data is known as_____.

A. Register B. Encoder

C. Decoder D. Flip Flop

Ans: D

148. . Computers use addressing mode techniques for _____.

A. giving programming versatility to the user by providing facilities as pointers to memory counters for loop control

B. to reduce no. of bits in the field of instruction

C. specifying rules for modifying or interpreting address field of the instruction

D. All the above

Ans: D

149. What characteristic of RAM memory makes it not suitable for permanent storage?

A. too slow
B. unreliable
C. it is volatile
D. too bulky

Ans: C

150. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to _____.

A. the time its takes for the platter to make a full rotation
B. the time it takes for the read-write head to move into position over the appropriate track
C. the time it takes for the platter to rotate the correct sector under the head
D. none of the above

Ans: A

151. In computers, subtraction is generally carried out by _____.

A. 9's complement
B. 10's complement
C. 1's complement
D. 2's complement

Ans: D

152. Assembly language _____.

a. uses alphabetic codes in place of binary numbers used in machine language
b. is the easiest language to write programs
c. need not be translated into machine language
d. None of these

Ans: A

153. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?

A. 1 Megabyte/sec
B. 4 Megabytes/sec
C. 8 Megabytes/sec
D. 2 Megabytes/sec

Ans: D

154. Floating point representation is used to store _____.

A. Boolean values
B. whole numbers
C. real integers
D. integers

Ans: C

155. SIMD represents an organization that _____.

a. refers to a computer system capable of processing several programs at the same time.
b. represents organization of single computer containing a control unit, processor unit and a memory unit.
c. includes many processing units under the supervision of a common control unit
d. none of the above.

Ans: C

156. In Reverse Polish notation, expression A*B+C*D is written as

A. AB*CD*+
B. A*BCD*+
C. AB*CD+*
D. A*B*CD+

Ans: A

157. Processors of all computers, whether micro, mini or mainframe must have
a. ALU b. Primary Storage
c. Control unit d. All of above

Ans b

158. What is the control unit's function in the CPU?
a. To transfer data to primary storage
b. to store program instruction
c. to perform logic operations
d. to decode program instruction

Ans e

159. What is meant by a dedicated computer?
a. which is used by one person only
b. which is assigned to one and only one task
c. which does one kind of software
d. which is meant for application software only

Ans f

160. The most common addressing techiniques employed by a CPU is
a. immediate b. direct
c. indirect d. register e. all of the above

Ans d

161. Pipeline implement
a. fetch instruction b. decode instruction
c. fetch operand d. calculate operand
e. execute instruction f. all of abve

Ans d

162. Which of the following code is used in present day computing was developed by IBM corporation?
a. ASCII b. Hollerith Code
c. Baudot code d. EBCDIC code

Ans d

163. When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the
a. stack pointer b. accumulator
c. program counter d. stack

Ans d

164. A microprogram written as string of 0's and 1's is a
a. symbolic microinstruction b. binary microinstruction
c. symbolic microprogram d. binary microprogram

Ans d

165. Interrupts which are initiated by an instruction are
a. internal b. external c. hardware d. software

Ans b

166. Memory access in RISC architecture is limited to instructions

a. CALL and RET b. PUSH and POP
c. STA and LDA d. MOV and JMP

Ans c

167. A collection of lines that connects several devices is called .....
A) bus B) peripheral connection wires
C) Both a and b D) internal wires

Ans A

168. A complete microcomputer system consist of .....
A) microprocessor B) memory
C) peripheral equipment D) all of the above

Ans D

169. PC Program Counter is also called .....
A) instruction pointer B) memory pointer
C) data counter D) file pointer

Ans A

170. In a single byte how many bits will be there?
A) 8 B) 16 C) 4 D) 32

Ans A

171. CPU does not perform the operation .....
A) data transfer B) logic operation
C) arithmetic operation D) all of the above

Ans A

172. The access time of memory is ..... the time required for performing any single CPU operation.
A) Longer thanB) Shorter than
C) Negligible than D) Same as

Ans A

173. Memory address refers to the successive memory words and the machine is called as .....
A) word addressable B) byte addressable
C) bit addressable D) Tera byte addressable

Ans A

174. A microprogram written as string of 0's and 1's is a .....
A) Symbolic microinstruction B) binary microinstruction
C) symbolic microinstruction D) binary microprogram

Ans D

175. A pipeline is like .....
A) an automobile assembly line B) house pipeline
C) both a and b D) a gas line

Ans A

176. Data hazards occur when .....
A) Greater performance loss
B) Pipeline changes the order of read/write access to operands

C) Some functional unit is not fully pipelined

D) Machine size is limited

Ans B

177. Where does a computer add and compare data?

A. Hard disk B. Floppy disk

C. CPU chip D:Memory chip

Ans C

178. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?

A. Memory Address Register

B. Memory Data Register

C. Instruction Register

D. Program Register

Ans D

179. A complete microcomputer system consists of

A) microprocessor

B) memory

C) peripheral equipment

D) all of above

Ans D

180. CPU does not perform the operation

A. data transfer

B. logic operation

C. arithmetic operation

D. all of above

Ans B

181. Pipelining strategy is called implement

A. instruction execution

B. instruction prefetch

C. instruction decoding

D. instruction manipulation

Ans C

182. A stack is

A. an 8-bit register in the microprocessor

B. a 16-bit register in the microprocessor

C. a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer

D. a 16-bit memory address stored in the program counter

Ans A

183. A stack pointer is

A. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.

B. a register that decodes and executes 16-bit arithmetic expression.
C. The first memory location where a subroutine address is stored.
D. a register in which flag bits are stored

Ans A

184. The branch logic that provides decision making capabilities in the control unit is known as

A. controlled transfer
B. conditional transfer
C. unconditional transfer
D. none of above

Ans C

185. Interrupts which are initiated by an instruction are

A. internal
B. external
C. hardware
D. software

Ans D

186. A time sharing system imply

A. more than one processor in the system
B. more than one program in memory
C. more than one memory in the system
D. None of above

Ans B

187.Virtual memory is –
(1) an extremely large main memory
(2) an extremely large secondary memory
(3) an illusion of an extremely large memory
(4) a type of memory used in super computers

(5) None of these

Answers:
3

188.Fragmentation is -
(1) dividing the secondary memory into equal sized f ragments
(2) dividing the main memory into equal size f ragments
(3) f ragments of memory words used in a page
(4) f ragments of memory words unused in a page
(5) None of these

Answers:: 2

189.Which memory unit has lowest access time?
(1) Cache (2) Registers
(3) Magnetic Disk (4) Main Memory
(5) Pen drive

Answer :2

190.Cache memory-
(1) has greater capacity than RAM
(2) is f aster to access than CPU Registers
(3) is permanent storage
(4) f aster to access than RAM
(5) None of these
Answer 4
191.When more than one processes are running concurrently on a system-
(1) batched system
(2) real-time system
(3) multi programming system
(4) multiprocessing system
(5) None of these
Answers:
3

192.Which of the following memories must be refreshed many times per second?
a. Static RAM b. Dynamic RAM c. EPROM
d. ROM e. None of these
ans Static RAM
193.RAM stands for
a. Random origin money b. Random only memory
c. Read only memory d. Random access memory
e. None of these
ans Random access memory

194.CPU fetches the instruction from memory according to the value of
a) program counter
b) status register
c) instruction register
d) program status word

Answer:a.
195.A memory buffer used to accommodate a speed differential is called
a) stack pointer
b) cache

c) accumulator
d) disk buffer

Answer:b.
196.Which one of the following is the address generated by CPU?
a) physical address
b) absolute address
c) logical address
d) none of the mentioned
Answer:c.
197.Run time mapping from virtual to physical address is done by
a) memory management unit
b) CPU
c) PCI
d) none of the mentioned
Answer:a.
198.Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called
a) fragmentation
b) paging
c) mapping
d) none of the mentioned
Answer:b

199.The address of a page table in memory is pointed by
a) stack pointer
b) page table base register
c) page register
d) program counter

200.Program always deals with
a) logical address
b) absolute address
c) physical address
d) relative address

Answer:a

COMPUTER ORGANIZATION AND ARCHITECTURE

BCA

Multiple choice questions

1. In Reverse Polish notation, expression A*B+C*D is written as
   (A) AB*CD*+ (B) A*BCD*+ (C) AB*CD+* (D) A*B*CD+
   Ans: A
2. SIMD represents an organization that _____.
   (A) refers to a computer system capable of processing several programs at the same time.
   (B) represents organization of single computer containing a control unit, processor unit and a memory unit.
   (C) includes many processing units under the supervision of a common control unit
   (D) none of the above.
   Ans: C
3. Floating point representation is used to store
   (A) Boolean values (B) whole numbers (C) real integers (D) integers
   Ans: C
4. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?
   (A) 1 Megabyte/sec (B) 4 Megabytes/sec
   (C) 8 Megabytes/sec (D) 2 Megabytes/sec
   Ans: D
5. Assembly language
   (A) uses alphabetic codes in place of binary numbers used in machine language
   (B) is the easiest language to write programs
   (C) need not be translated into machine language
   (D) None of these
   Ans: A
6. In computers, subtraction is generally carried out by
   (A) 9's complement (B) 10's complement
   (C) 1's complement (D) 2's complement
   Ans: D
7. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to
   (A) the time its takes for the platter to make a full rotation
   (B) the time it takes for the read-write head to move into position over the appropriate track
   (C) the time it takes for the platter to rotate the correct sector under the head
   (D) none of the above

Ans: A

8. What characteristic of RAM memory makes it not suitable for permanent storage?
   (A) too slow (B) unreliable (C) it is volatile (D) too bulky
   Ans: C
9. Computers use addressing mode techniques for _____.
   (A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
   (B) to reduce no. of bits in the field of instruction
   (C) specifying rules for modifying or interpreting address field of the instruction
   (D) All the above
   Ans: D
10. The circuit used to store one bit of data is known as
    (A) Register (B) Encoder (C) Decoder (D) Flip Flop
    Ans: D
11. (2FAOC) 16 is equivalent to
    (A) (195 084) 10 (B) (001011111010 0000 1100) 2
    (C) Both (A) and (B) (D) None of these
    Ans: B
12. The average time required to reach a storage location in memory and obtain its contents is called the
    (A) seek time (B) turnaround time (C) access time (D) transfer time
    Ans: C
13. Which of the following is not a weighted code?
    (A) Decimal Number system (B) Excess 3-cod
    (C) Binary number System (D) None of these
    Ans: B
14. The idea of cache memory is based
    (A) on the property of locality of reference (B) on the heuristic 90-10 rule
    (C) on the fact that references generally tend to cluster (D) all of the above
    Ans: A
15. Which of the following is lowest in memory hierarchy?
    (A) Cache memory
    (B) Secondary memory
    (C) Registers
    (D) RAM
    (E) None of these
    Ans (B) Secondary memory

16. The addressing mode used in an instruction of the form ADD X Y, is
    (A) Absolute (B) indirect (C) index (D) none of these
    Ans: C
17. If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is

(A) 93% (B) 90% (C) 88% (D) 87%

Ans: B

18. In a memory-mapped I/O system, which of the following will not be there?

(A) LDA (B) IN (C) ADD (D) OUT

Ans: A

19. In a vectored interrupt.

(A) the branch address is assigned to a fixed location in memory.

(B) the interrupting source supplies the branch information to the processor through an interrupt vector.

(C) the branch address is obtained from a register in the processor

(D) none of the above

Ans: B

20. Von Neumann architecture is

(A) SISD (B) SIMD (C) MIMD (D) MISD

Ans: A

21. The circuit used to store one bit of data is known as

(A) Encoder (B) OR gate (C) Flip Flop (D) Decoder

Ans: C

22. Cache memory acts between

(A) CPU and RAM (B) RAM and ROM (C) CPU and Hard Disk (D) None of these

Ans: A

23. Write Through technique is used in which memory for updating the data

(A) Virtual memory (B) Main memory

(C) Auxiliary memory (D) Cache memory

Ans: D

24. Generally Dynamic RAM is used as main memory in a computer system as it

(A) Consumes less power (B) has higher speed

(C) has lower cell density (D) needs refreshing circuitary

Ans: B

25. In signed-magnitude binary division, if the dividend is (11100) 2 and divisor is (10011) 2 then the result is

(A) (00100) 2 (B) (10100) 2 (C) (11001) 2 (D) (01100) 2

Ans: B

26. Virtual memory consists of

(A) Static RAM (B) Dynamic RAM

(C) Magnetic memory (D) None of these

Ans: A

27. In a program using subroutine call instruction, it is necessary

(A) initialise program counter (B) Clear the accumulator

(C) Reset the microprocessor (D) Clear the instruction register

Ans: D

28. A Stack-organised Computer uses instruction of

(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressing

Ans: C

29. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be

(A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits

Ans: C

30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit

(A) n TQD =• (B) T D = (C) D = T . Q n (D) n TQD =⊕

Ans: D

31. Logic X-OR operation of (4ACO) H & (B53F) H results

(A) AACB (B) 0000 (C) FFFF (D) ABCD

Ans: C

32. When CPU is executing a Program that is part of the Operating System, it is said to be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mode

Ans: B

33. An n-bit microprocessor has

(A) n-bit program counter (B) n-bit address register

(C) n-bit ALU (D) n-bit instruction register

Ans: D

34. Cache memory works on the principle of

(A) Locality of data (B) Locality of memory

(C) Locality of reference (D) Locality of reference & memory

Ans: C

35. The main memory in a Personal Computer (PC) is made of

(A) cache memory. (B) static RAM

(C) Dynamic Ram (D) both (A) and (B) .

Ans: D

36. In computers, subtraction is carried out generally by

(A) 1's complement method (B) 2's complement method

(C) signed magnitude method (D) BCD subtraction method

Ans: B

37. PSW is saved in stack when there is a

(A) interrupt recognised (B) execution of RST instruction

(C) Execution of CALL instruction (D) All of these

Ans: A

38. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be

(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10

Ans: A

39. The circuit converting binary data in to decimal is

(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter

Ans: D

40. A three input NOR gate gives logic high output only when

(A) one input is high (B) one input is low

(C) two input are low (D) all input are high

Ans: D

41. n bits in operation code imply that there are _____ possible distinct operators (A) 2n (B) 2n (C) n/2 (D) n2

Ans: B

42. _____ register keeps tracks of the instructions stored in program stored in memory.

(A) AR (Address Register) (B) XR (Index Register)

(C) PC (Program Counter) (D) AC (Accumulator)

Ans: C

43. Memory unit accessed by content is called

(A) Read only memory (B) Programmable Memory

(C) Virtual Memory (D) Associative Memory

Ans: D

44. 'Aging registers' are

(A) Counters which indicate how long ago their associated pages have been referenced.

(B) Registers which keep track of when the program was last accessed.

(C) Counters to keep track of last accessed instruction.

(D) Counters to keep track of the latest data structures referred.

Ans: A

45 The instruction 'ORG O' is a

(A) Machine Instruction. (B) Pseudo instruction.

(C) High level instruction. (D) Memory instruction.

Ans: B

46 Translation from symbolic program into Binary is done in

(A) Two passes. (B) Directly (C) Three passes. (D) Four passes.

Ans: A

47 A floating point number that has a O in the MSB of mantissa is said to have

(A) Overflow (B) Underflow (C) Important number (D) Undefined

Ans: B

48 The BSA instruction is

(A) Branch and store accumulator (B) Branch and save return address

(C) Branch and shift address (D) Branch and show accumulator

Ans: B

49 State whether True or False.

(i) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers.

Ans: True.

(ii) An arithmetic shift left multiplies a signed binary number by 2.

Ans: False.

50 Logic gates with a set of input and outputs is arrangement of

(A) Combinational circuit (B) Logic circuit (C) Design circuits (D) Register

Ans: A

51. MIMD stands for

(A) Multiple instruction multiple data (B) Multiple instruction memory data

(C) Memory instruction multiple data (D) Multiple information memory data

Ans: A

52 A k-bit field can specify any one of

(A) 3k registers (B) 2k registers

(C) K2 registers (D) K3 registers

Ans: B

53 The time interval between adjacent bits is called the

(A) Word-time (B) Bit-time (C) Turn around time (D) Slice time

Ans: B

54 A group of bits that tell the computer to perform a specific operation is known as

(A) Instruction code (B) Micro-operation (C) Accumulator (D) Register

Ans: A

55 The load instruction is mostly used to designate a transfer from memory to a processor register known as

(A) Accumulator (B) Instruction Register

(C) Program counter (D) Memory address Register

Ans: A

56 The communication between the components in a microcomputer takes place via the address and

(A) I/O bus (B) Data bus (C) Address bus (D) Control lines

Ans: B

57 An instruction pipeline can be implemented by means of

(A) LIFO buffer (B) FIFO buffer (C) Stack (D) None of the above

Ans: B

58 Data input command is just the opposite of a

(A) Test command (B) Control command (C) Data output (D) Data channel

Ans: C

59 A microprogram sequencer

(A) generates the address of next micro instruction to be executed.

(B) generates the control signals to execute a microinstruction.

(C) sequentially averages all microinstructions in the control memory.

(D) enables the efficient handling of a micro program subroutine.

Ans: A

60 . A binary digit is called a

(A) Bit (B) Byte (C) Number (D) Character

Ans: A

61 A flip-flop is a binary cell capable of storing information of

(A) One bit (B) Byte (C) Zero bit (D) Eight bit

Ans: A

62 The operation executed on data stored in registers is called

(A) Macro-operation (B) Micro-operation

(C) Bit-operation (D) Byte-operation

Ans: B

63 MRI indicates

(A) Memory Reference Information. (B) Memory Reference Instruction.

(C) Memory Registers Instruction. (D) Memory Register information

Ans: B

64 Self-contained sequence of instructions that performs a given computational task is called

(A) Function (B) Procedure (C) Subroutine (D) Routine

Ans: A

65 Microinstructions are stored in control memory groups, with each group specifying a

(A) Routine (B) Subroutine (C) Vector (D) Address

Ans: A

66 An interface that provides a method for transferring binary information between internal storage and external devices is called

(A) I/O interface (B) Input interface (C) Output interface (D) I/O bus

Ans: A

67 Status bit is also called

(A) Binary bit (B) Flag bit (C) Signed bit (D) Unsigned bit

Ans: B

68 An address in main memory is called

(A) Physical address (B) Logical address (C) Memory address (D) Word address

Ans: A

69 If the value V(x) of the target operand is contained in the address field itself, the addressing mode is

(A) immediate. (B) direct. (C) indirect. (D) implied.

Ans: B

70 can be represented in a signed magnitude format and in a 1's complement format as

(A) 111011 & 100100 (B) 100100 & 111011

(C) 011011 & 100100 (D) 100100 & 011011

Ans: A

71 The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

(A) Data transfer instructions. (B) Program control instructions.

(C) Input-output instructions. (D) Logical instructions.

Ans: A

72 A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called

(A) register (B) flip-flop (C) transistor. (D) counter.

Ans: D

73. The performance of cache memory is frequently measured in terms of a quantity called

(A) Miss ratio. (B) Hit ratio. (C) Latency ratio. (D) Read ratio.

Ans: C

74. The information available in a state table may be represented graphically in a

(A) simple diagram. (B) state diagram. (C) complex diagram. (D) data flow diagram.

Ans: B

75 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.

(A) relative address mode. (B) index addressing mode.

(C) register mode. (D) implied mode.

Ans: A

76 An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

(A) DDA. (B) Serial interface. (C) BR. (D) DMA.

Ans: D

77 The 2s compliment form (Use 6 bit word) of the number 1010 is

(A) 111100. (B) 110110. (C) 110111. (D) 1011.

Ans: B

78 A register capable of shifting its binary information either to the right or the left is called a

(A) parallel register. (B) serial register. (C) shift register. (D) storage register.

Ans: C

79 What is the content of Stack Pointer (SP)?

(A) Address of the current instruction (B) Address of the next instruction

(C) Address of the top element of the stack (D) Size of the stack.

Ans: C

80 Which of the following interrupt is non maskable

(A) INTR. (B) RST 7.5. (C) RST 6.5. (D) TRAP.

Ans: D

81 Which of the following is a main memory

(A) Secondary memory. (B) Auxiliary memory.

(C) Cache memory. (D) Virtual memory.

Ans: C

82 Which of the following are not a machine instructions

(A) MOV. (B) ORG. (C) END. (D) (B) & (C) .

Ans: D

83 In Assembly language programming, minimum number of operands required for an instruction is/are

(A) Zero. (B) One. (C) Two. (D) Both (B) & (C) .

Ans: A

84 The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is

(A) 64 K. (B) 4 GB. (C) both (A) & (B) . (D) None of these.

Ans: B

85 The memory unit that communicates directly with the CPU is called the

(A) main memory (B) Secondary memory

(C) shared memory (D) auxiliary memory.

Ans: A

86 The average time required to reach a storage location in memory and obtain its contents is called

(A) Latency time. (B) Access time.

(C) Turnaround time. (D) Response time.

Ans: B

State True or False

87 A byte is a group of 16 bits.

Ans: False

88 A nibble is a group of 16 bits.

Ans: False

89 When a word is to be written in an associative memory, address has got to be given.

Ans: False

90 When two equal numbers are subtracted, the result would be _____and not_____.

Ans: +ZERO, -ZERO.

91 A _____development system and an _____are essential tools for writing large assembly language programs.

Ans: Microprocessor, assembler

92 In an operation performed by the ALU, carry bit is set to 1 if the end carry C 8 is _____. It is cleared to 0 (zero) if the carry is _____ _____.

Ans: One, zero

93 A successive A/D converter is

(A) a high-speed converter. (B) a low speed converter.

(C) a medium speed converter. (D) none of these.

Ans: C

94 When necessary, the results are transferred from the CPU to main memory by

(A) I/O devices. (B) CPU. (C) shift registers. (D) none of these.

Ans: C

96 A combinational logic circuit which sends data coming from a single source to two or more separate destinations is

(A) Decoder. (B) Encoder. (C) Multiplexer. (D) Demultiplexer.

Ans: D

97 In which addressing mode the operand is given explicitly in the instruction

(A) Absolute. (B) Immediate . (C) Indirect. (D) Direct.

Ans: B

98 A stack organized computer has

(A) Three-address Instruction. (B) Two-address Instruction.

(C) One-address Instruction. (D) Zero-address Instruction.

Ans: D

99 A Program Counter contains a number 825 and address part of the instruction contains the number 24. The effective address in the relative address mode, when an instruction is read from the memory is

(A) 849. (B) 850. (C) 801. (D) 802.

Ans: B

102 A page fault

(A) Occurs when there is an error in a specific page.

(B) Occurs when a program accesses a page of main memory.

(C) Occurs when a program accesses a page not currently in main memory.

(D) Occurs when a program accesses a page belonging to another program.

Ans: C

103. The load instruction is mostly used to designate a transfer from memory to a processor register known as____.

A. Accumulator B. Instruction Register

C. Program counter D. Memory address Register

Ans: A

104. A group of bits that tell the computer to perform a specific operation is known as____.

A. Instruction code B. Micro-operation

C. Accumulator D. Register

Ans: A

105. The time interval between adjacent bits is called the_____.

A. Word-time B. Bit-time

C. Turn around time D. Slice time

Ans: B

106. A k-bit field can specify any one of_____.

A. 3k registers B. 2k registers

C. K2 registers D. K3 registers

Ans: B

107. MIMD stands for _____.

A. Multiple instruction multiple data

B. Multiple instruction memory data

C. Memory instruction multiple data

D. Multiple information memory data

Ans: A

108. Logic gates with a set of input and outputs is arrangement of_____.

A. Computational circuit
B. Logic circuit
C. Design circuits
D. Register

Ans: A

109. The average time required to reach a storage location in memory and obtain its contents is called_____.

A. Latency time. B. Access time.
C. Turnaround time. D. Response time.

Ans: B

110. The BSA instruction is_____.

A. Branch and store accumulator B. Branch and save return address
C. Branch and shift address D. Branch and show accumulator

Ans: B

111. A floating point number that has a O in the MSB of mantissa is said to have_____.

A. Overflow B. Underflow
C. Important number D. Undefined

Ans: B

112. Translation from symbolic program into Binary is done in_____.

A. Two passes. B. Directly
C. Three passes. D. Four passes.

Ans: A

113. The instruction 'ORG O' is a_____.

A. Machine Instruction. B. Pseudo instruction.
C. High level instruction. D. Memory instruction.

Ans: B

114. 'Aging registers' are _____.

A. Counters which indicate how long ago their associated pages have been referenced.
B. Registers which keep track of when the program was last accessed.
C. Counters to keep track of last accessed instruction.
D. Counters to keep track of the latest data structures referred.

Ans: A

115. Memory unit accessed by content is called_____.

A. Read only memory B. Programmable Memory
C. Virtual Memory D. Associative Memory

Ans: D

116. _____ register keeps tracks of the instructions stored in program stored in memory.

A. AR (Address Register) B. XR (Index Register)
C. PC (Program Counter) D. AC (Accumulator)

Ans: C

117. n bits in operation code imply that there are _____ possible distinct operators.

A. 2n B. 2n
C. n/2 D. n2

Ans: B

118. A three input NOR gate gives logic high output only when_____.

A. one input is high B. one input is low

C. two input are low D. all input are high

Ans: D

119. The circuit converting binary data in to decimal is_____.

A. Encoder B. Multiplexer

C. Decoder D.Code converter

Ans: D

120. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be _____.

A. (812)10 B. (-12)10

C. (12)10 D. (-812)10

Ans: A

121. PSW is saved in stack when there is a _____.

A. interrupt recognized B. execution of RST instruction

C. Execution of CALL instruction D. All of these

Ans: A

122. In computers, subtraction is carried out generally by____.

A. 1's complement method B. 2's complement method

C. signed magnitude method D. BCD subtraction method

Ans: B

123. The main memory in a Personal Computer (PC) is made of_____.

A. cache memory. B. static RAM

C. Dynamic Ram D. bothA.and (B).

Ans: D

124. Cache memory works on the principle of_____.

A. Locality of data B. Locality of memory

C. Locality of reference D. Locality of reference & memory

Ans: C

125. An n-bit microprocessor has_____.

A. n-bit program counter B. n-bit address register

C. n-bit ALU D. n-bit instruction register

Ans: D

126. When CPU is executing a Program that is part of the Operating System, it is said to be in _____.

A. Interrupt mode B. System mode

C. Half mode D. Simplex mode

Ans: B

127. Logic X-OR operation of (4ACO)H& (B53F)H results _____.

A. AACB B. 0000

C. FFFF D. ABCD

Ans: C

128. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be_____.

A. 11 bits B. 21 bits

C. 16 bits D. 20 bits

Ans: C

129. A Stack-organised Computer uses instruction of _____.

A. Indirect addressing B. Two-addressing
C. Zero addressing D. Index addressing

Ans: C

130. In a program using subroutine call instruction, it is necessary_____.

A. initialize program counter B. Clear the accumulator
C. Reset the microprocessor D. Clear the instruction register

Ans: D

131. Virtual memory consists of _____.

A. Static RAM B. Dynamic RAM
C. Magnetic memory D. None of these

Ans: A

132. In signed-magnitude binary division, if the dividend is (11100)2 and divisor is (10011)2 then the result is _____.

A. (00100)2 B. (10100)2
C. (11001)2 D. (01100)2

Ans: B

133. Generally Dynamic RAM is used as main memory in a computer system as it_____.

A. Consumes less power B. has higher speed
C. has lower cell density D. needs refreshing circuitry

Ans: B

134. Write Through technique is used in which memory for updating the data _____.

A. Virtual memory B. Main memory
C. Auxiliary memory D. Cache memory

Ans: D

135. Cache memory acts between_____.

A. CPU and RAM B. RAM and ROM
C. CPU and Hard Disk D. None of these

Ans: A

136. The circuit used to store one bit of data is known as _____.

A. Encoder B. OR gate
C. Flip Flop D. Decoder

Ans: C

137. Von Neumann architecture is _____.

A. SISD B. SIMD
C. MIMD D. MISD

Ans: A

138. In a vectored interrupt.

A. the branch address is assigned to a fixed location in memory.
B. the interrupting source supplies the branch information to the processor through an interrupt vector.
C. the branch address is obtained from a register in the processor
D. none of the above

Ans: B

139. . In a memory-mapped I/O system, which of the following will not be there?

A. LDA B. IN

C. ADD D. OUT

Ans: A

140. If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is _____.

A. 93% B. 90%

C. 88% D. 87%

Ans: B

141. The addressing mode used in an instruction of the form ADD X Y, is _____.

A. Absolute B. indirect

C. index D. none of these

Ans: C

142. _____ register keeps track of the instructions stored in program stored in memory.

A. AR (Address Register) B. XR (Index Register)

C. PC (Program Counter) D. AC (Accumulator)

Ans: C

143. The idea of cache memory is based _____.

A. on the property of locality of reference

B. on the heuristic 90-10 rule

C. on the fact that references generally tend to cluster

D. all of the above

Ans: A

144. Which of the following is not a weighted code?

A. Decimal Number system B. Excess 3-cod

C. Binary number System D. None of these

Ans: B

145. The average time required to reach a storage location in memory and obtain its contents is called the _____.

A. seek time B. turnaround time

C. access time D. transfer time

Ans: C

146. (2FAOC)16 is equivalent to _____.

A. (195 084)10 B. (001011111010 0000 1100)2

C. Both A.and (B) D. None of these

Ans: B

147. The circuit used to store one bit of data is known as_____.

A. Register B. Encoder

C. Decoder D. Flip Flop

Ans: D

148. . Computers use addressing mode techniques for _____.

A. giving programming versatility to the user by providing facilities as pointers to memory counters for loop control

B. to reduce no. of bits in the field of instruction

C. specifying rules for modifying or interpreting address field of the instruction

D. All the above

Ans: D

149. What characteristic of RAM memory makes it not suitable for permanent storage?

A. too slow
B. unreliable
C. it is volatile
D. too bulky

Ans: C

150. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to _____.

A. the time its takes for the platter to make a full rotation
B. the time it takes for the read-write head to move into position over the appropriate track
C. the time it takes for the platter to rotate the correct sector under the head
D. none of the above

Ans: A

151. In computers, subtraction is generally carried out by _____.

A. 9's complement
B. 10's complement
C. 1's complement
D. 2's complement

Ans: D

152. Assembly language _____.

a. uses alphabetic codes in place of binary numbers used in machine language
b. is the easiest language to write programs
c. need not be translated into machine language
d. None of these

Ans: A

153. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?

A. 1 Megabyte/sec
B. 4 Megabytes/sec
C. 8 Megabytes/sec
D. 2 Megabytes/sec

Ans: D

154. Floating point representation is used to store _____.

A. Boolean values
B. whole numbers
C. real integers
D. integers

Ans: C

155. SIMD represents an organization that _____.

a. refers to a computer system capable of processing several programs at the same time.
b. represents organization of single computer containing a control unit, processor unit and a memory unit.
c. includes many processing units under the supervision of a common control unit
d. none of the above.

Ans: C

156. In Reverse Polish notation, expression A*B+C*D is written as

A. AB*CD*+
B. A*BCD*+
C. AB*CD+*
D. A*B*CD+

Ans: A

157. Processors of all computers, whether micro, mini or mainframe must have
a. ALU b. Primary Storage
c. Control unit d. All of above

Ans b

158. What is the control unit's function in the CPU?
a. To transfer data to primary storage
b. to store program instruction
c. to perform logic operations
d. to decode program instruction

Ans e

159. What is meant by a dedicated computer?
a. which is used by one person only
b. which is assigned to one and only one task
c. which does one kind of software
d. which is meant for application software only

Ans f

160. The most common addressing techiniques employed by a CPU is
a. immediate b. direct
c. indirect d. register e. all of the above

Ans d

161. Pipeline implement
a. fetch instruction b. decode instruction
c. fetch operand d. calculate operand
e. execute instruction f. all of abve

Ans d

162. Which of the following code is used in present day computing was developed by IBM corporation?
a. ASCII b. Hollerith Code
c. Baudot code d. EBCDIC code

Ans d

163. When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the
a. stack pointer b. accumulator
c. program counter d. stack

Ans d

164. A microprogram written as string of 0's and 1's is a
a. symbolic microinstruction b. binary microinstruction
c. symbolic microprogram d. binary microprogram

Ans d

165. Interrupts which are initiated by an instruction are
a. internal b. external c. hardware d. software

Ans b

166. Memory access in RISC architecture is limited to instructions

a. CALL and RET b. PUSH and POP
c. STA and LDA d. MOV and JMP

Ans c

167. A collection of lines that connects several devices is called .....
A) bus B) peripheral connection wires
C) Both a and b D) internal wires

Ans A

168. A complete microcomputer system consist of .....
A) microprocessor B) memory
C) peripheral equipment D) all of the above

Ans D

169. PC Program Counter is also called .....
A) instruction pointer B) memory pointer
C) data counter D) file pointer

Ans A

170. In a single byte how many bits will be there?
A) 8 B) 16 C) 4 D) 32

Ans A

171. CPU does not perform the operation .....
A) data transfer B) logic operation
C) arithmetic operation D) all of the above

Ans A

172. The access time of memory is ..... the time required for performing any single CPU operation.
A) Longer thanB) Shorter than
C) Negligible than D) Same as

Ans A

173. Memory address refers to the successive memory words and the machine is called as .....
A) word addressable B) byte addressable
C) bit addressable D) Tera byte addressable

Ans A

174. A microprogram written as string of 0's and 1's is a .....
A) Symbolic microinstruction B) binary microinstruction
C) symbolic microinstruction D) binary microprogram

Ans D

175. A pipeline is like .....
A) an automobile assembly line B) house pipeline
C) both a and b D) a gas line

Ans A

176. Data hazards occur when .....
A) Greater performance loss
B) Pipeline changes the order of read/write access to operands

C) Some functional unit is not fully pipelined

D) Machine size is limited

Ans B

177. Where does a computer add and compare data?

A. Hard disk B. Floppy disk

C. CPU chip D:Memory chip

Ans C

178. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?

A. Memory Address Register

B. Memory Data Register

C. Instruction Register

D. Program Register

Ans D

179. A complete microcomputer system consists of

A) microprocessor

B) memory

C) peripheral equipment

D) all of above

Ans D

180. CPU does not perform the operation

A. data transfer

B. logic operation

C. arithmetic operation

D. all of above

Ans B

181. Pipelining strategy is called implement

A. instruction execution

B. instruction prefetch

C. instruction decoding

D. instruction manipulation

Ans C

182. A stack is

A. an 8-bit register in the microprocessor

B. a 16-bit register in the microprocessor

C. a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer

D. a 16-bit memory address stored in the program counter

Ans A

183. A stack pointer is

A. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.

B. a register that decodes and executes 16-bit arithmetic expression.
C. The first memory location where a subroutine address is stored.
D. a register in which flag bits are stored

Ans A

184. The branch logic that provides decision making capabilities in the control unit is known as

A. controlled transfer
B. conditional transfer
C. unconditional transfer
D. none of above

Ans C

185. Interrupts which are initiated by an instruction are

A. internal
B. external
C. hardware
D. software

Ans D

186. A time sharing system imply

A. more than one processor in the system
B. more than one program in memory
C. more than one memory in the system
D. None of above

Ans B

187.Virtual memory is –
(1) an extremely large main memory
(2) an extremely large secondary memory
(3) an illusion of an extremely large memory
(4) a type of memory used in super computers

(5) None of these

Answers:
3

188.Fragmentation is -
(1) dividing the secondary memory into equal sized f ragments
(2) dividing the main memory into equal size f ragments
(3) f ragments of memory words used in a page
(4) f ragments of memory words unused in a page
(5) None of these

Answers:: 2

189.Which memory unit has lowest access time?
(1) Cache (2) Registers
(3) Magnetic Disk (4) Main Memory
(5) Pen drive

Answer :2

190.Cache memory-
(1) has greater capacity than RAM
(2) is f aster to access than CPU Registers
(3) is permanent storage
(4) f aster to access than RAM
(5) None of these
Answer 4
191.When more than one processes are running concurrently on a system-
(1) batched system
(2) real-time system
(3) multi programming system
(4) multiprocessing system
(5) None of these
Answers:
3

192.Which of the following memories must be refreshed many times per second?
a. Static RAM b. Dynamic RAM c. EPROM
d. ROM e. None of these
ans Static RAM
193.RAM stands for
a. Random origin money b. Random only memory
c. Read only memory d. Random access memory
e. None of these
ans Random access memory

194.CPU fetches the instruction from memory according to the value of
a) program counter
b) status register
c) instruction register
d) program status word

Answer:a.
195.A memory buffer used to accommodate a speed differential is called
a) stack pointer
b) cache

c) accumulator
d) disk buffer

Answer:b.
196.Which one of the following is the address generated by CPU?
a) physical address
b) absolute address
c) logical address
d) none of the mentioned
Answer:c.
197.Run time mapping from virtual to physical address is done by
a) memory management unit
b) CPU
c) PCI
d) none of the mentioned
Answer:a.
198.Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called
a) fragmentation
b) paging
c) mapping
d) none of the mentioned
Answer:b

199.The address of a page table in memory is pointed by
a) stack pointer
b) page table base register
c) page register
d) program counter

200.Program always deals with
a) logical address
b) absolute address
c) physical address
d) relative address

Answer:a

✗ What fraction of the execution time involves code that is parallel to achieve an overall speedup of 2. Assume 10 numbers of parallel processors? * ···/1

0.45 ✗

✗ 2.3.A doctor in a hospital observes that on average 10 patients per hour arrive and there are typically 4 patient in the hospital. What is the average range of time each patient spend in the hospital? * ···/1

0.4 ✗

✓ Which registers are responsible in cpu when data transmission is takes place between cpu and memory. * 1/1

- ○ PC
- ○ IR
- ○ I/O AR
- ◉ non of the above ✓

✓ Which registers are responsible in cpu when data transmission is takes place between cpu and I/O. * 1/1

- ○ I/OAR
- ○ I/OBR
- ○ only first
- ◉ both first and second ✓

✓ Which action is not performed by the processor * 1/1

- ○ processor-memory
- ○ processor - I/O
- ○ dataprocessing
- ○ control
- ◉ non of the above ✓

✓ In the cpu which register value always increment whenever each instruction fetch from memory * 1/1

- ○ IR
- ○ MAR
- ◉ PC ✓
- ○ I/OBR

✓ Instruction cycle contain---- * 1/1

- ○ Fetch cycle
- ○ Execute cycle
- ◉ both 1st and 2nd ✓
- ○ none

✓ Fetch the operand from memory or read it in from I/O is called --- * 1/1

- ○ data operation
- ○ instruction fetch
- ◉ operand fetch ✓
- ○ operand store

In second generation of computer which technology was used. * 1 point

- ○ vaccum tube
- ○ vlsi
- ◉ transistor
- ○ ulsi

Which is not a function of computer * 1 point

- data processing
- data storage
- pipelining
- control

✓ In second generation of computer which technology was used. * 1/1

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✓ Which is not a function of computer * 1/1

- ○ data processing
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- ◉ pipelining ✓
- ○ control

✓ Mechanism that provides communication between cpu, memory and I/O in computer is * 1/1

- ○ internal bus
- ◉ system bus ✓
- ○ address bus
- ○ none

✓ Which is not a part of a CPU * 1/1

- ( ) ALU
- ( ) Registers
- ( ) Control unit
- (•) Cache ✓

✓ Which is not a ARM product * 1/1

- ○ CORTEX-A50
- ○ CORTEM-M
- ◉ CORTEX-N ✓
- ○ CORTEX-M4

DEDICATED PROCESSOR USED IN SMART PHONE. *

0/1

- (•) YES
- ( ) NO
- ( ) I do not know

Correct answer

- (•) NO

✓ The collection of paths connecting the various modules is called ------ in computer system. * 1/1

- cable
- flat path
- interconnection structure ✓
- none

✓ Interrupts initiated by an instruction is called as _____. * 1/1

- ○ Internal
- ◉ External ✓
- ○ hardware
- ○ Software

✓ Which is not a control line signal * 1/1

- ○ clock
- ○ bus grant
- ○ transfer ACK
- ◉ data transfer ✓

✓ Data lines collectively called ----- * 1/1

- ○ control bus
- ○ address bus
- ◉ data bus ✓
- ○ power distribution bus

✓ Which is not a part of cloud services. * 1/1

- saas
- paas
- jaas ✓
- iaas

✓ Among the techniques which is not followed during design of microprocessor * 1/1

- pipelining
- branch prediction
- data flow analysis
- performance balance ✓

✓ Which is not belongs to QPI architecture layer * 1/1

- ○ physical
- ○ link
- ○ protocol
- ◉ transaction ✓

✓ Which is not a characteristics of point to point interconnection. * 1/1

- multiple direct connections
- layered protocol architecture
- packetized data transfer
- interrupt request ✓

✓ By increasing of clock speed and logic density in the chip which factor is not a obstacles in the computer system * 1/1

- power
- rc delay
- processor speed ✓
- memory latency

✓ In computer system GPUs stand for------ * 1/1

- ○ graphics protocol units
- ○ geographic position units
- ○ gyroscopic processing units
- ◉ none of the above ✓

✓ Amdahl's law states that the maximum speedup S achievable by a parallel computer with 'p' processors is given by: * 1/1

- ○ $S \leq f+(1-f)/p$
- ○ $S \leq f/p+(1-f)$
- ○ $S \leq 1/[f+(1-f)/p]$
- ◉ $S \leq 1/[1-f+f/p]$ ✓

✓ Performance balance can done * 1/1

- ○ by using wider data path
- ○ including cache in DRAM chip
- ○ incorporating complex and efficient cache structures between processor and main memory
- ◉ all of the above ✓

✓ Identify which is not an access method for memory. * 1/1

- ○ Direct
- ○ Sequential
- ◉ Indirect ✓
- ○ Random

✓ Which parameter is belongs to performance of memory. * 1/1

- ○ Direct access
- ○ word
- ○ capacity
- ◉ Transfer rate ✓

✗ Define CPI *

···/1

Cycles per instruction is one aspect of a processor's performance: the average number of clock cycles per instruction for a program or program fragment ✗

✗ Define MIPS *

···/1

MIPS stands for Million Instructions Per Second. It is another measure of performance. It is also referred as rate of instruction execution per unit time. ✗

✓ Which is more appropriate for performance rate analysis * 1/1

- AM
- SM
- HM ✓
- ZM

✓ What will be the overall speed up if N =10 and f =0.9 in a system. * 1/1

- 4.2
- 6.2
- 5.2 ✓
- 3.2

✗ Write meaning of mov ax,3024h * ⋯/1

3020h(immediate data) is moved to ax register ✗

✗ Write meaning of mov [4000h],dx * ⋯/1

[4000h] is offset/ address the content of which is moved to dx ✗

✓ 8086 can access up to? * 1/1

- ○ 512KB
- ◉ 1Mb ✓
- ○ 2Mb
- ○ 256KB

✓ Which flag represents the result when the system capacity is exceeded? 1/1

*

- ○ Carry flag
- ○ Auxiliary flag
- ○ Trap flag
- ◉ Overflow flag ✓

✓ If the offset of the operand is stored in one of the index registers, then it is * 1/1

- ○ based indexed addressing mode
- ○ relative based indexed addressing mode
- ◉ indexed addressing mode ✓
- ○ none of the mentioned

✓ The contents of a base register are added to the contents of index register in * 1/1

- ○ indexed addressing mode
- ○ based indexed addressing mode
- ○ relative based indexed addressing mode
- ◉ based indexed and relative based indexed addressing mode ✓

MOV is a which type of instruction. * 1/1

- Arithmetic Instructions
- Bit Manipulation Instructions
- String Instructions
- Data Transfer Instructions ✓

✓ ADC is a which type of instruction. * 1/1

- ○ Iteration Control Instructions
- ○ Bit Manipulation Instructions
- ○ Processor Control Instructions
- ◉ none of the above ✓

✓ If the data is present in a register and it is referred using the particular register, then it is * 1/1

- ○ direct addressing mode
- ◉ register addressing mode ✓
- ○ indexed addressing mode
- ○ immediate addressing mode

✓ The instruction that pushes the contents of the specified register/memory location on to the stack is * 1/1

- ○ PUSHF
- ○ POPF
- ◉ PUSH ✓
- ○ POP

✓ 8086 is a ------bit microprocessor. * 1/1

- ○ 4
- ○ 2
- ○ 8
- ◉ 16 ✓

✓ How many 16 bit registers are there inside 8086 microprocessor ? * 1/1

- 12
- 14 ✓
- 8
- 16