

QUESTIONS

(Practise)

Question No. 1

What, in general terms, is the distinction between computer organization and computer architecture?

Answer:

- Computer architecture refers to those attributes or features or parts of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program.
- Computer Architecture is concerned with the structure and behavior of the computer as seen by the user.
- Computer organization refers to the operational units and their interconnections that realize the architectural specifications.
- Computer Organization is concerned with the way the hardware components operate and the way they are connected together to form the computer system.

Question No. 2

Explain Moore's law.

Answer:

- Moore's law: Moore (Gordon Moore, cofounder of Intel) observed that the number of transistors that could be put on a single chip was doubling every year, and correctly predicted that this pace would continue into the near future.
- To the surprise of many, including Moore, the pace continued year after year and decade after decade. The pace slowed to a doubling every 18 months in the 1970s but has sustained that rate ever since.

Question No. 3

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

- Determine the effective CPI, MIPS rate, and execution time for each machine.
- Comment on the results.

Answer:

a.

$$CPI_A = \frac{\sum CPI_i \times I_i}{I_c} = \frac{(8 \times 1 + 4 \times 3 + 2 \times 4 + 4 \times 3) \times 10^6}{(8 + 4 + 2 + 4) \times 10^6} \approx 2.22$$

$$MIPS_A = \frac{f}{CPI_A \times 10^6} = \frac{200 \times 10^6}{2.22 \times 10^6} = 90$$

$$CPU_A = \frac{I_c \times CPI_A}{f} = \frac{18 \times 10^6 \times 2.2}{200 \times 10^6} = 0.2 \text{ s}$$

$$CPI_B = \frac{\sum CPI_i \times I_i}{I_c} = \frac{(10 \times 1 + 8 \times 2 + 2 \times 4 + 4 \times 3) \times 10^6}{(10 + 8 + 2 + 4) \times 10^6} \approx 1.92$$

$$MIPS_B = \frac{f}{CPI_B \times 10^6} = \frac{200 \times 10^6}{1.92 \times 10^6} = 104$$

$$CPU_B = \frac{I_c \times CPI_B}{f} = \frac{24 \times 10^6 \times 1.92}{200 \times 10^6} = 0.23 \text{ s}$$

- b. Although machine B has a higher MIPS than machine A, it requires a longer CPU time to execute the same set of benchmark programs.

Question No. 4

Four benchmark programs are executed on three computers with the following results:

	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

The table shows the execution time in seconds, with 100,000,000 instructions executed in each of the four programs. Calculate the MIPS values for each computer for each program. Then calculate the arithmetic and harmonic means assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean.

Answer:

$\text{MIPS} = I_c / (T \times 10^6) = 100/T$. The MIPS values

	Computer A	Computer B	Computer C
Program 1	100	10	5
Program 2	0.1	1	5
Program 3	0.2	0.1	2
Program 4	1	0.125	1

	Arithmetic mean	Rank	Harmonic mean	Rank
Computer A	25.325	1	0.25	2
Computer B	2.8	3	0.21	3
Computer C	3.25	2	2.1	1

Question No.5

Two benchmark programs are executed on three computers with the following results:

Benchmark	Processor		
	X	Y	Z
1	20	10	40
2	40	80	20

- a. Compute the arithmetic mean value for each system using X as the reference machine and then using Y as the reference machine. Argue that intuitively the three machines have roughly equivalent performance and that the arithmetic mean gives misleading results.
- b. Compute the geometric mean value for each system using X as the reference machine and then using Y as the reference machine. Argue that the results are more realistic than with the arithmetic mean.

Answer:

a. Normalized to X:

Benchmark	Processor		
	X	Y	Z
1	1	2.0	0.5
2	1	0.5	2.0
Arithmetic mean	1	1.25	1.25
Geometric mean	1	1	1

Normalized to Y:

Benchmark	Processor		
	X	Y	Z
1	0.5	1	0.25
2	2.0	1	4.0
Arithmetic mean	1.25	1	2.125
Geometric mean	1	1	1

Machine Y is twice as fast as machine X for benchmark 1, but half as fast for benchmark 2. Similarly machine Z is half as fast as X for benchmark 1, but twice as fast for benchmark 2. Intuitively, these three machines have equivalent performance. However, if we

normalize to X and compute the arithmetic mean of the speed metric, we find that Y and Z are 25% faster than X. Now, if we normalize to Y and compute the arithmetic mean of the speed metric, we find that X is 25% faster than Y and Z is more than twice as fast as Y. Clearly, the arithmetic mean is worthless in this context.

- b. When the geometric mean is used, the three machines are shown to have equal performance when normalized to X, and also equal performance when normalized to Y. These results are much more in line with our intuition.

Question No.6

Convert the following hexadecimal numbers to their decimal equivalents:

- (a) C.8 (b) A9.A**

Answer:

- (a) 12.5 (b) 169.625**

Question 7.

Convert the following hexadecimal numbers to their decimal equivalents:

- (a) 5D (b) B32**

Answer:

- (a) 93 (b) 2866**

Question 8.

Convert the following binary numbers to their hexadecimal equivalents:

- (a) 101101.1001 (b) 1100.1101**

Answer:

- (a) 2D.9 (b) C.D**

Question No. 9

Simplify the following expression

$$(A + C)(AD + AD') + AC + C$$

Answer:

$$(A + C)A(D + D') + AC + C$$

$$(A + C)A + AC + C$$

$$A((A + C) + C) + C$$

$$A(A + C) + C$$

$$AA + AC + C$$

$$A + (A + 1)C$$

$$A + C$$

Question No. 10

Simplify the following expression

$$A'(A + B) + (B + AA)(A + B')$$

Answer:

$$A'A + A'B + (B + A)A + (B + A)B'$$

$$A'B + (B + A)A + (B + A)B'$$

$$A'B + BA + AA + BB' + AB'$$

$$A'B + BA + A + AB'$$

$$A'B + A(B + 1 + B')$$

$$A'B + A$$

$$A + A'B$$

$$(A + A')(A + B)$$

$$A + B$$

Question No. 11

Show the structure of a PLA with three inputs (C, B, A) and five outputs (F_1, F_2, F_3, F_4) with the outputs defined as follows:

$$F_1 = ABC$$

$$F_2 = A + B + C$$

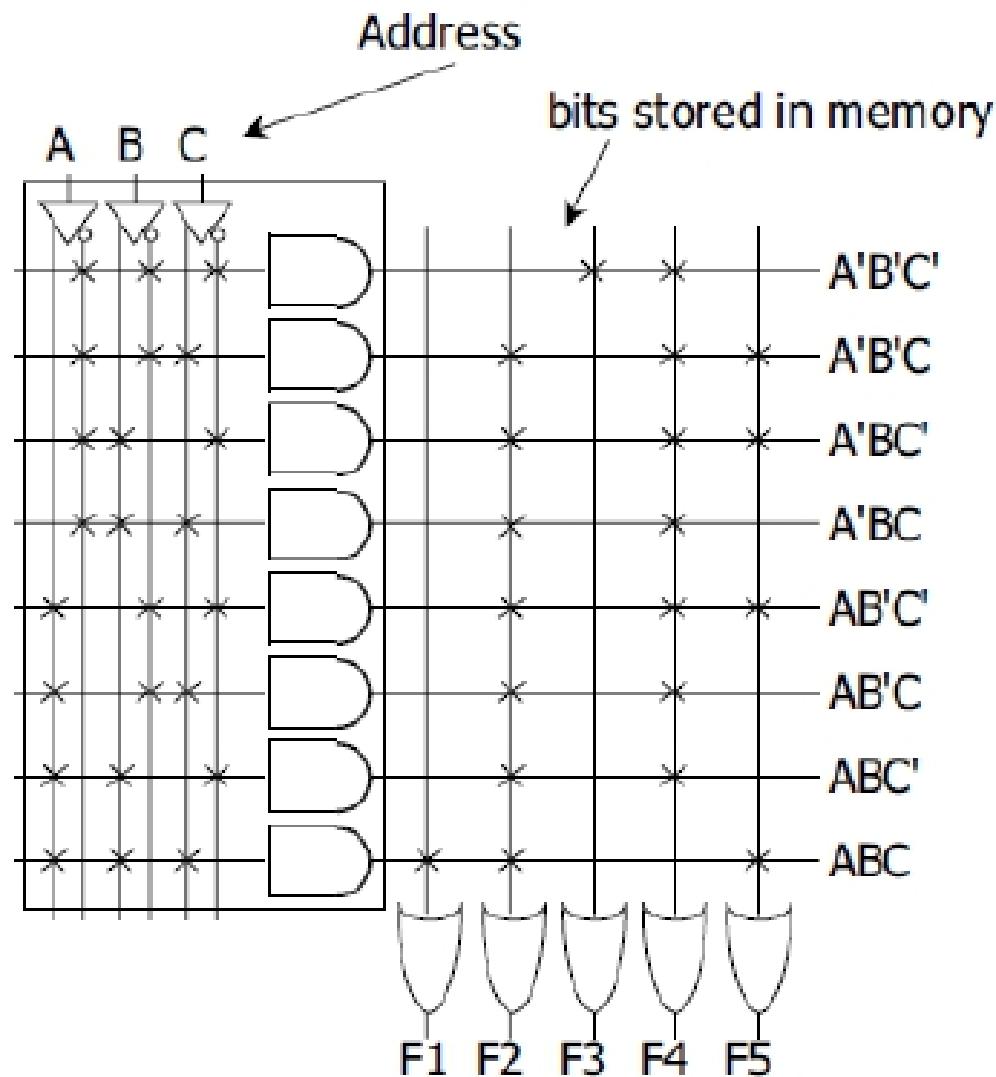
$$F_3 = A' B' C'$$

$$F_4 = A' + B' + C'$$

$$F_5 = A \text{ xor } B \text{ xor } C$$

Answer:

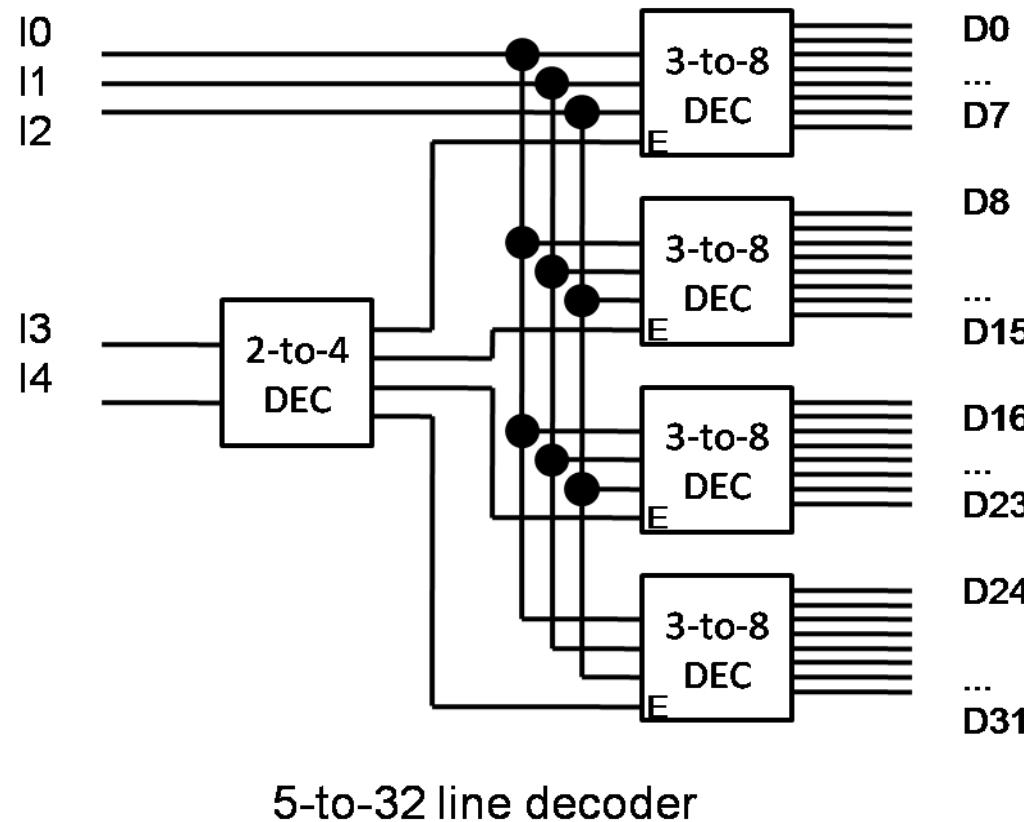
A	B	C	F1	F2	F3	F4	F5
0	0	0	0	0	1	1	0
0	0	1	0	1	0	1	1
0	1	0	0	1	0	1	1
0	1	1	0	1	0	1	0
1	0	0	0	1	0	1	1
1	0	1	0	1	0	1	0
1	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1



Question12:

Design a 5x32 decoder using four 3x 8 decoders (with enable inputs) and one 2X4 decoder.

Answer:



Question No. 13

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

- a. What is the maximum directly addressable memory capacity (in bytes)?
- b. Discuss the impact on the system speed if the microprocessor bus has
 - 1. a 32-bit local address bus and a 16-bit local data bus, or
 - 2. a 16-bit local address bus and a 16-bit local data bus.
- c. How many bits are needed for the program counter and the instruction register?

Answer:

a. $2^{(32-8)} = 2^{24} = 16,777,216$ bytes = 16 MB.

b.1. a 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data. Since If the address bus is 32 bits, the whole address can be transferred to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (accesses to memory) to fetch the 32-bit instruction or operand.

b.2. a 16-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take four bus cycles each, two for the address and two for the data. Therefore, that will have the processor perform two transmissions in order to send to memory the whole 32-bit address; this will require more complex memory interface control to latch the two halves of the address before it performs an access to it. In addition to this two-step address issue, since the data bus is also 16 bits, the microprocessor will need 2 bus cycles to fetch the 32-bit instruction or operand.

c. For the PC needs 24 bits (24-bit addresses), and for the IR needs 32 bits (32-bit addresses).

Question 14

Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

Answer:

By assuming that we have a mix of 100 instructions and operands.

From the question:

- 20% of the operands and instructions are 32-bits long, so it is 20 32-bit.
- 40% of the operands and instructions are 16-bits long, so it is 40 16-bit.
- 40% of the operands and instructions are only 8-bits = 1 byte long, so it is 40 bytes.

The number of bus cycles needed for the 16-bit microprocessor will equal to:

$$(20 * 2) + 40 + 40 = 120 \text{ bus cycles.}$$

The number of bus cycles needed for the 32-bit microprocessor will equal to:

$$20 + 40 + 40 = 100 \text{ bus cycles.}$$

By calculating the improvement achieved with the 32-bit microprocessor to the 16-bit microprocessor will equal to $20/120 = 16.6\%$.

Question 15

A set associative cache consists of 64 lines, or slots, divided into four line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

Answer:

Number of block in main memory = size of memory / size of block

Size of memory = Number of block in main memory × size of block

Size of memory = $2^2 \times 2^{10} \times 2^7$

Size of memory = 2^{19}

Tag	Set	Size of block

Size of block = $128 = 2^7$ -> so size of block = 7

Tag = size of memory - set - size of block

Tag = $19 - 4 - 7$

Tag = 8

Tag	Set	Size of block
8	4	7

Question 16:

Consider a processor that includes a base with indexing addressing mode. Suppose an instruction is encountered that employs this addressing mode and specifies a displacement of 1970, in decimal. Currently the base and index register contain the decimal numbers 48,022 and 8, respectively. What is the address of the operand?

Answer:

For base with indexing address mode:-

$$\begin{aligned}\text{Address of operand} &= (\text{contents of base register} + \text{contents of index register} + \text{displacement}) \\ &= 48022 + 8 + 1970 = 50000\end{aligned}$$

If displacement is not taken into consideration then address will be (base + index)

$$= 48022 + 8 = 48030$$

For scaled indexing (factor=4)

$$\begin{aligned}\text{Address of operand} &= (\text{base} + \text{index} * \text{factor} + \text{displacement}) \\ &= 48022 + (8 \times 4) + 1970 = 50024\end{aligned}$$

Question 17:

WAP to perform the following operation on bytes data given in the memory location 4000h, and 4002h and store the results of the given operation [$\{(data1 + 5) \text{and} (data2 - 5)\} \text{or} (data1 * 2)$] in the memory location 4004h.

Answer:

MOV AX,[4000H]

MOV BX,[4002H]

ADD AX,05H

SUB BX,05H

AND BX,AX

MOV [5000H],BX

MOV AX, [5000H]

MOV BX,02H

MUL BX

NOT AX

MOV BX,[5000H]

OR AX,BX

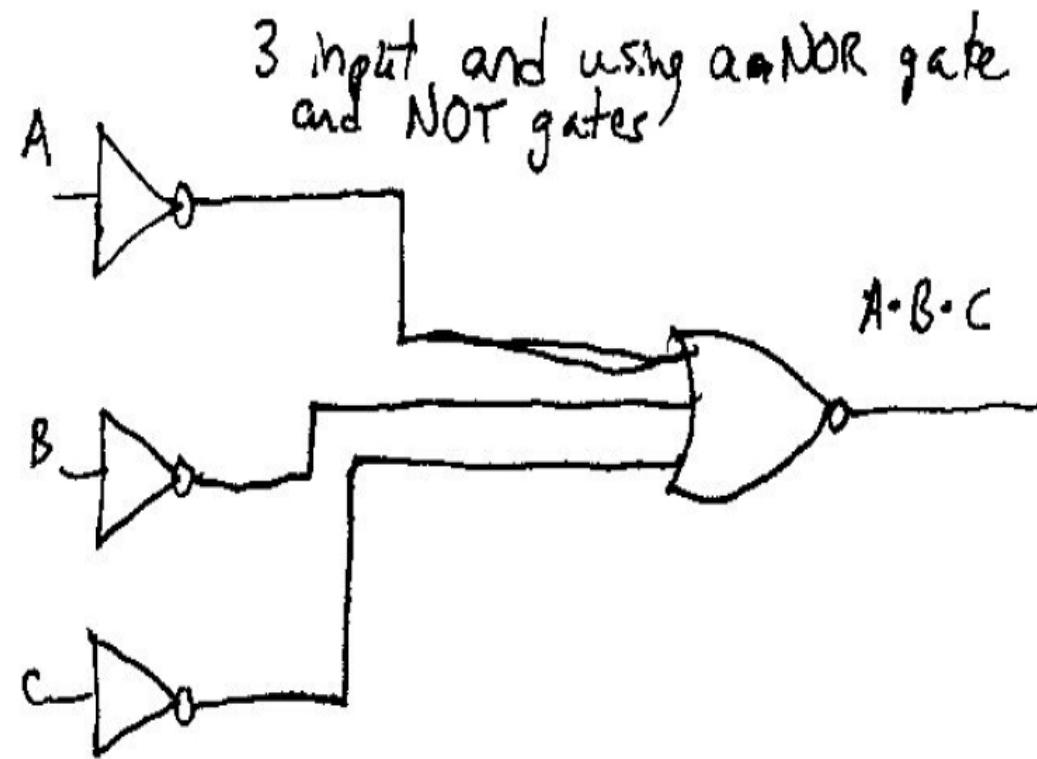
MOV [4004H],AX

HLT

Question 18:

Given a NOR gate and NOT gates, draw a logic diagram that will perform the three input AND function.

Answer:



Question 19:

What is the difference between DRAM and SRAM?

Answer:

- **Dynamic RAM (DRAM)** is made with cells that store data as charge on capacitors. The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0. Because capacitors have a natural tendency to discharge, dynamic RAMs require periodic charge refreshing to maintain data storage.
- **Static RAM (SRAM)** is a digital device that uses the same logic elements used in the processor. In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations. A static RAM will hold its data as long as power is supplied to it.
- Both static and dynamic RAMs are volatile; that is, power must be continuously supplied to the memory to preserve the bit values.
- A dynamic memory cell is simpler and smaller than a static memory cell. Thus, a DRAM is more dense (smaller cells = more cells per unit area) and less expensive than a corresponding SRAM.
- A DRAM requires the supporting refresh circuitry. For larger memories, the fixed cost of the refresh circuitry is more than compensated for by the smaller variable cost of DRAM cells. Thus, DRAMs tend to be favored for large memory requirements.
- A final point is that SRAMs are somewhat faster than DRAMs. Because of these relative characteristics, SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory.

Question 20:

Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer

Answer:

Data bits with value 1 are in bit positions 12, 11, 5, 4, 2, and 1:

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	1	1	0	0		0	0	1		0		
Codes	1100	1011						0101				

The check bits are in bit numbers 8, 4, 2, and 1.

Check bit 8 calculated by values in bit numbers: 12, 11, 10 and 9

Check bit 4 calculated by values in bit numbers: 12, 7, 6, and 5

Check bit 2 calculated by values in bit numbers: 11, 10, 7, 6 and 3

Check bit 1 calculated by values in bit numbers: 11, 9, 7, 5 and 3

Thus, the check bits are: 0 0 1 0

Question 21:

For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?

Answer:

The Hamming Word initially calculated was:

bit number:

12	11	10	9	8	7	6	5	4	3	2	1
0	0	1	1	0	1	0	0	1	1	1	1

Doing an exclusive-OR of 0111 and 1101 yields 1010 indicating an error in bit 10 of the Hamming Word. Thus, the data word read from memory was 00011001.

Question 22:

How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 1024-bit data word?

Answer:

Need K check bits such that $2K - 1 \geq 1024 + K$

The minimum value of K that satisfies this condition is 11

Question No. 23

What common characteristics are shared by all RAID levels?

Answer:

RAID (Redundant Array of Independent Disks) scheme consists of seven levels (0-6). These levels do not imply a hierarchical relationship but designate different design architectures that share three common characteristics:

- a. RAID is a set of physical disk drivers viewed by the operating system as a single logical drive.
- b. Data are distributed across the physical drives of an array in a scheme known as striping, described subsequently.
- c. Redundant disk capacity is used to store parity information which guarantees data recoverability in case of a disk failure.

Question No. 24

Briefly define the seven RAID levels.

Answer:

Category	Level	Description	Disks Required	Data Availability	Large I/O Data Transfer Capacity	Small I/O Request Rate
Striping	0	Nonredundant	N	Lower than single disk	Very high	Very high for both read and write
Mirroring	1	Mirrored	$2N$	Higher than RAID 2, 3, 4, or 5; lower than RAID 6	Higher than single disk for read; similar to single disk for write	Up to twice that of a single disk for read; similar to single disk for write
Parallel access	2	Redundant via Hamming code	$N + m$	Much higher than single disk; comparable to RAID 3, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
	3	Bit-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
Independent access	4	Block-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 5	Similar to RAID 0 for read; significantly lower than single disk for write	Similar to RAID 0 for read; significantly lower than single disk for write
	5	Block-interleaved distributed parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 4	Similar to RAID 0 for read; lower than single disk for write	Similar to RAID 0 for read; generally lower than single disk for write
	6	Block-interleaved dual distributed parity	$N + 2$	Highest of all listed alternatives	Similar to RAID 0 for read; lower than RAID 5 for write	Similar to RAID 0 for read; significantly lower than RAID 5 for write

Note: N = number of data disks; m proportional to $\log N$

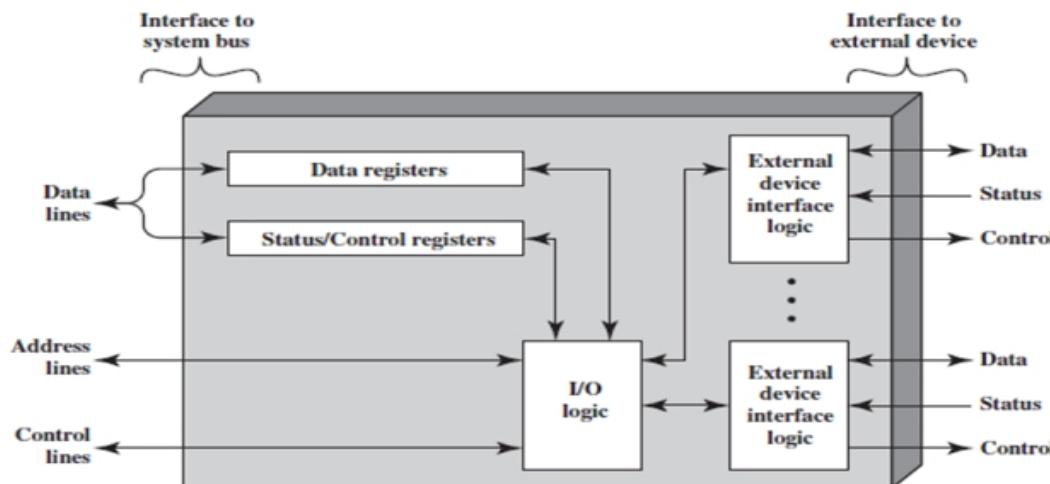
Question No. 25

What are the major functions of an I/O module? Draw the block diagram of I/O module.

Answer:

The major functions or requirements for an I/O module fall into the following categories:

- Control and timing
- Processor communication
- Device communication
- Data buffering
- Error detection



Question No. 26

What is an operating system? List the key services provided by the OS.

Answer

An OS is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware. It can be thought of as having two objectives:

- **Convenience:** An OS makes a computer more convenient to use.
- **Efficiency:** An OS allows the computer system resources to be used in an efficient manner.

The key services provided by an OS include:

- **Program creation:** The OS provides a variety of facilities and services, such as editors and debuggers, to assist the programmer in creating programs.
- **Program execution:** A number of steps need to be performed to execute a program.
- **Access to I/O devices:** Each I/O device requires its own specific set of instructions or control signals for operation.
- **Controlled access to files:** In the case of files, control must include an understanding of not only the nature of the I/O device (disk drive, tape drive) but also the file format on the storage medium.
- **System access:** In the case of a shared or public system, the OS controls access to the system as a whole and to specific system resources.
- **Error detection and response:** A variety of errors can occur while a computer system is running.
- **Accounting:** A good OS collects usage statistics for various resources and monitors performance parameters such as response time.