Computer Organization and Architecture (EET2211)

Syllabus

- Basic Concepts and Computer Evolution
- Performance Issue
- Top Level View of Computer Function and Interconnection
- Cache Memory
- Internal Memory
- External Memory
- Input/Output
- Operating System Support
- Number Systems
- ComputerArithmetic
- DigitalLogic
- Instruction Sets: Characteristics andFunctions
- Instruction Sets: Addressing Modes andFormats
- Processor Structure and Function
- Reduced Instruction SetComputers
- Instruction Level Parallelism and Superscalar Processors
- Parallel Processing
- Multicore Computers

Textbook:

Computer Organization and Architecture by William Stalling, Pearson, 10th Edition

Course Format:

- 3 Classes/week,1hr/Class,
- 1 Lab/Week, 2hr/Lab, 4Credits

Prerequisite

EET1211 – Digital Logic Design

Evaluation Scheme

InternalCom ponent	Marks	External Component	Marks
Mid – Semester Exam	15	End – Semester Exam	45
Assignments	10	External Project	15
Quiz and Viva	10		
Attendance	05		
Total	**40**		**60**

Lecture Wise Lesson Planning

Lect. No.	Topics Covered	References
L1-L4	**Basic Concepts and Computer Evolution**	**Chapter 1**
Lect. 1.	Organization and Architecture Structure and Function	1.1 1.2
Lect. 2.	A Brief History of Computers	1.3
Lect. 3.	The Evolution of the Intel x86 Architecture Embedded Systems ARM Architecture	1.4 1.5 1.6
Lect. 4.	Cloud Computing	1.7
L5-L8	**Performance Issue**	**Chapter 2**
Lect. 5.	Designing for Performance Multicore, MICs, and GPGPUs Two Laws that Provide Insight: Amdahl's Law and Little's Law	2.1 2.2 2.3
Lect. 6.	Basic Measures of Computer Performance	2.4
Lect.7. Lect.8.	Calculating the Mean Problem Solving	2.5
L9-L14	**A Top-Level View of Computer Function and Interconnection**	**Chapter 3**
Lect. 9	Computer Components Computer Function	3.1 3.2
Lect. 10.	Computer Function	3.2
Lect. 11.	Interconnection Structures Bus Interconnection	3.3 3.4
Lect. 12.	Point-to-Point Interconnect	3.5
Lect. 13.-14	PCI Express	**3.6**
L15-L19	**Cache Memory**	**Chapter 4**
Lect. 15.	Computer Memory System Overview	4.1
Lect. 16.	Cache Memory Principles	4.2
Lect. 17.-19	Elements of Cache Design	4.3
L20-L21	**Internal Memory**	**Chapter 5**
	Semiconductor Main Memory	5.1 assignment
Lect. 20.-21	Error Correction	5.2
	Newer Nonvolatile Solid-State Memory Technologies	5.3 5.4,5.5 assignment
L22-L25	**External Memory**	**Chapter 6**
Lect.22-23	RAID	6.2
Lect.24-25	Optical Memory	6.4
	Magnetic Disk , Solid State Drives, Magnetic Tape	assignment
L26-L28	**Input/Output**	**Chapter 7**
Lect. 26	External Devices I/O Modules Programmed I/O	7.1 7.2 7.3
Lect. 27	Direct Memory Access	7.5
Lect. 28	Direct Cache Access	7.6
L29-L30	**Operating System Support**	**Chapter 8**

Lect.29	Operating System Overview Scheduling	8.1 8.2
Lect.30	Memory Management	8.3
L31-L32	**Reduced Instruction Set Computers**	**Chapter 15**
Lect.31	Instruction Execution Characteristics The Use of a Large Register File Compiler-Based Register Optimization	15.1 15.2 15.3
Lect.32	RISC Pipelining	15.5
	Reduced Instruction Set Architecture, MIPS R4000 ,SPARC ,RISC versus CISC Controversy	15.4,15.6,15.7,15.8 (lab)
L33-L35	**Parallel Processing**	**Chapter 17**
Lect.33	Multiple Processor Organizations 6 Symmetric Multiprocessors	17.1 17.2
Lect.34	Cache Coherence and the MESI Protocol Multithreading and Chip Multiprocessors	17.3 17.4
Lect.35	Clusters Non-uniform Memory Access	17.5 17.6
L36-L37	**Multicore Computers**	**Chapter 18**
Lect.36	Hardware Performance Issues Software Performance Issues	18.1 18.2
Lect.37	Multicore Organization Heterogeneous Multicore Organization	18.3 18.4
L38-L39	**ARITHMETIC AND LOGIC**	**Chapter 9-11**
L40	Overview of 8086 Microprocessor and ARM Processor	**Chapter 12-14**