## **COA MCQ CHAPTER 7**

Q1. The main importance of ARM micro-processors is providing operation with		
A.	Low cost and low power consumption	
В.	Higher degree of multi-tasking	
C.	Lower error or glitches	
D.	Efficient memory management	
ANS 1. A		
Q2. ARM processors are basically designed for		
A.	Mainframe systems	
	Distributed systems	
	Mobile systems	
D.	Super computers	
ANS2. C		
Q3. The add	dress system supported by ARM system(s) is / are	
A.	Little Endian	
В.	Big Endian	
C.	X-liitle Endian	
D.	Both Little and Big Endian	
ANS 3. D		
Q4. In the A	ARM, PC is implemented using	
A.	Caches	
В.	Heaps	
C.	General Purpose registers	
D.	Stack	
ANS 4. C		
Q5. How m	any registers are there in ARM7?	
A.	35 registers (28 GPR & 7 SPR)	
В.	37 registers (28 GPR & 9 SPR)	
	37 registers (31 GPR & 6 SPR)	
D.	35 registers (30 GPR & 5 SPR)	
ANS 5. C		
Q6. Which processor requires more number of registers?		
A.	CISC	

B. ISA

C. R D. A	RISC ANNA
ANS 6. C	
Q7. The meth	nod which offers higher speeds of I/O transfers is
B. N	nterrupts Memory mapping Program-controlled I/O DMA
ANS 7. D	
Q8. In memo	ry-mapped I/O
B. T C. <i>A</i>	The I/O devices have a separate address space The I/O devices and the memory share the same address space A part of the memory is specifically set aside for the I/O operation The memory and I/O devices have an associated address space
	circuit is basically used to extend the processor BUS to connect devices.
B. R C. B	Router Repeater Bridge All of the above
ANS 9. C	
Q10. Keyboai	rd and Mouse comes under
B. C C. I,	nput peripherals  Output peripherals  /O devices  None of the above.
ANS 10. A	
Q11. RAM is a	a memory.
B. II C. N	External nternal Main Auxiliary
ANS 11. C	
Q12	is the permanent memory unit built into the computer systems.

	A.	ROM
	В.	CPU
	C.	DVD-ROM
	D.	RAM
А	NS 12. A	
Q	13. Hard-	disk drives are considered as storage medium.
	A.	Flash
	В.	Non-volatile
	C.	Temporary
	D.	Permanent
А	NS 13. B	
Q	14. The st	orage element of a SRAM is
	A.	Diode
	В.	Resistor
	C.	Capacitor
	D.	Flip-flop
А	NS 14. D	
Q	15. Capac	ity of hard-disk is measured in
	A.	Gigabytes
	В.	Megabytes
	C.	Kilobytes
	D.	Bytes
А	NS 15. A	

## 8086 MICROPROCESSOR

Q1. 8086 mid	croprocessor supports modes of operation.
A. 2 B. 3 C. 4 D. 9	3 4
ANS1. A	
Q2. 8086 car	n access up to memory.
B. 1 C. 2	512 KB 1 MB 2 MB 256 KB
ANS1. B	
Q3. 8086 has	s address bus.
B. 1 C. 2	16-bit 18-bit 20-bit 24-bit
ANS1. C	
Q4. Which fla	ag is set to 1 when the result of arithmetic or logical operation is zero else it is set to zero?
B. 7 C. 0	Trap flag Zero flag Carry flag Overflow flag
ANS1. B	
Q5. Which fla	ag represents the result when the system capacity is exceeded?
B. <i>i</i>	Trap flag Auxiliary flag Carry flag Overflow flag
ANS1. B	
Q6. It is used signal.	I to write the data into the memory or the output device depending on the status of M/IO

A. IR

	HR
D.	WR
ANS1. D	
Q7. Which	instruction is used to load the address of operand into the provided register?
A.	LEA
В.	LDS
	LES
D.	LAHF
ANS1. A	
Q8. The dif	ferent ways in which a source operand is denoted in an instruction is known as:
A.	Instruction Set
В.	Interrupts
C.	Architecture
D.	Addressing Modes
ANS1. D	
Q9. A micr	oprocessor is a chip integrating all the functions of a CPU of a computer.
A.	multiple
В.	single
C.	double
D.	triple
ANS1. B	
Q10. The v	vork of EU is
A.	encoding
В.	decoding
C.	processing
D.	calculations
ANS1. B	
Q11. The r	egister used to store the flags is called as
A.	Flag register
В.	Status register
C.	Test register
D.	Log register
ANS 11. B	
Q12. The 1	6 bit flag of 8086 microprocessor is responsible to indicate

B. HLDA

	В. С.	The condition of result of ALU operation The condition of memory The result of addition The result of subtraction
ANS 12	. A	
Q13. Th	ne CF	is known as
	В. С.	Carry flag Condition flag Common flag Single flag
ANS 13	. A	
Q14. Th	ne SF	is known as
	В. С.	Service flag Sign flag Single flag Condition flag
ANS 14	. В	
Q15. Th	ne IF	is known as
	В. С.	Initial flag Indicate flag Interrupt flag Inter flag
ANS 15	. C	
Q16. Th	ne IF	is known as
	A. B. C. D.	Interrupt flag
ANS 16	. C	
Q17. Th	ne IF	is known as
	A. B. C. D.	Interrupt flag

#### ANS 17. C

Q18. The instruction that is used to transfer the data from source operand to destination operand is :

- A. Data copy / transfer instruction
- B. Branch instruction
- C. Arithmetic / logical instruction
- D. String instructions

ANS 17. C

C. IR

### **CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION**

Q1		bus structure is usually used to connect I/O devices
	A.	Single bus
	В.	Multiple bus
	C.	Star bus
	D.	RAM bus
ANS 1.	Α	
Q2. The main advantage of using single bus structure is		
	В. С.	Fast data transfers Cost effective connectivity and speed Cost effective connectivity and ease of attaching peripheral devices None of the above
ANS 2.	С	
Q3. The ISA standard buses are used to connect		
	A.	RAM and Processor
	В.	GPU and Processor
	C.	Hard-disk and Processor
	D.	CD / DVD drives and Processor
ANS 3.	С	
Q4. Which registers can interact with the secondary storage?		
	A.	MAR
	В.	PC

D.	AC
ANS 4. A	
Q5. To exte	end the connectivity of the processor bus we use
A.	PCI Bus
В.	SCSI Bus
C.	Controllers
D.	Multiple Bus
ANS 5. A	
Q6. A sour	ce program is usually written in
A.	Assembly language
В.	Machine-level language
C.	High-level language
D.	Natural language
ANS 6. C	
Q7	_ are numbers and encoded characters which are generally used as operands.
A.	Input
В.	Data
C.	Information
D.	Stored values
ANS 7. B	
Q8. The AL	U stores the immediate result in
A.	Accumulator
В.	Queue
C.	Stack
D.	Memory locations
ANS 8. A	
Q9. The co	ntrol unit controls other units by generating
A.	Control signals
В.	Timing signals
C.	Transfer signals
D.	Command signals
ANS 9. B	
Q10. The e	xtremely small and fast RAM is known as
A.	Cache

В.	Heaps
C.	Accumulators
D.	Stacks
ANS 10. A	
Q11. The si	mallest entity of memory is called
A.	Cell
В.	Block
C.	Instance
D.	Unit
ANS 11. A	
Q12. The b known as:	ranch of study that deals with the computer system's conceptual design and basic overview is
A.	Computer Anatomy
В.	Computer Architecture
C.	Computer OS
D.	Computer Interface
ANS12. B	
Q13. Which	n of the following technologies was used in second generation computer?
A.	Vacuum Tubes
В.	Transistors
C.	Integrated Circuits
D.	VLSI Circuits
ANS13. B	
	CHAPTER 2: PERFORMANCE ISSUES
01.	are used to overcome the difference in data transfer speeds of various devices.

A. Speed enhancing circuitry

- B. Bridge circuits
- C. Multiple buses
- D. Buffer registers

ANS 1. D

Q2. Two processors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?		
<ul><li>A. A</li><li>B. B</li><li>C. Both takes equal amount of time</li><li>D. None of the above</li></ul>		
ANS 2. A		
Q3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called		
<ul><li>A. Super-scaling</li><li>B. Pipelining</li><li>C. Parallel computation</li><li>D. Architecture</li></ul>		
ANS 3. B		
Q4. The clock rate of the processor can be improved by		
<ul> <li>A. Improving the IC technology of the logic circuits</li> <li>B. Reducing the amount of processing done in one step</li> <li>C. By using the over-clocking method</li> <li>D. All of the above</li> </ul>		
ANS 4. D		
Q5. SPEC stands for		
<ul> <li>A. Standard Performance Evaluation Code</li> <li>B. System Processing Enhancing Code</li> <li>C. System Performance Evaluation Corporation</li> <li>D. Standard Processing Enhancement Corporation</li> </ul>		
ANS 5. C		
Q6. CISC stands for		
<ul> <li>A. Complete Instruction Sequential Compilation</li> <li>B. Computer Integrated Sequential Compiler</li> <li>C. Complex Instruction Set Computer</li> <li>D. Complex Instruction Sequential Compilation</li> </ul>		
ANS 6. C		
Q7. Which instruction is used to load the address of operand into the provided register?		
Δ ΙΕΔ		

		LES LAHF
ANS1.	4	
Q8. The	e diff	Ferent ways in which a source operand is denoted in an instruction is known as:
	В. С.	Instruction Set Interrupts Architecture Addressing Modes
ANS1. [	)	
29. A n	nicro	processor is a chip integrating all the functions of a CPU of a computer.
	В. С.	multiple single double triple
ANS1. E	3	
Q10. Tł	ne w	ork of EU is
	В. С.	encoding decoding processing calculations
ANS10.	В	
Q11. W	hich'	of the following is the important characteristics of computers?
	F.	speed accuracy storage all of the above
ANS11.	D	
Q12. W	hich'	of the following is not a hardware component of computer?
	В. С.	memory scanner operating system CPU
ANS12.	С	

B. LDS

# CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

Q1. During the execution of a program which gets initialized first?		
A. B.	MDR IR PC	
	MAR	
ANS1. C		
Q2. The de	coded instruction is stored in	
A.	IR	
	PC	
	Registers AC	
	AC	
ANS1. A		
Q3. Which of the register(s) of the processor is / are connected to Memory Bus?		
A.	PC	
В.	MAR	
-	IR	
D.	Both PC AND MAR	
ANS1. B		
Q4. ISP stands for		
В. С.	Instruction Set Processor Information Standard Processing Interchange Standard Protocol Interrupt Service Procedure	
ANS1. A		
Q5. The interrupt request line is a part of the		
Α.	Data line	

B. Control line

D.	None of the above
ANS1. B	
Q6. The sig	nal set to the device from the processor to the device after receiving an interrupt is
·	
A.	Interrupt acknowledge
	Return signal
	Service signal
D.	Permission signal
ANS1. A	
	CHAPTER 4: CACHE MEMORY
	CHAPTER 4. CACHE MEMORI
Q1. To redu	uce the memory access time we generally make use of
A.	Heaps
В.	SSD
	SDRAMs
D.	Cache memory
ANS 1. D	
Q2	is usually used to increase the size of physical memory.
A.	Secondary memory
В.	Virtual memory
	Hard-disk
D.	Disks
ANS 2. B	
Q3. The int	ernal components of the processor are connected by
A.	Processor intra-connectivity circuitry
В.	Processor bus
C.	Memory bus
D.	Single bus
ANS 3. B	
Q4. During	the execution of instructions, a copy of the instructions is placed in the

C. Address line

		Register RAM
		Main memory
		Cache
ANS 4. [	)	
Q5. To g	get 1	the physical address from the logical address generated by CPU we use
	A.	MAR
	В.	MMU
	C.	Overlays
	D.	TLB
ANS 5. E	3	
Q6. Dur	ing	the transfer of data between the processor and memory we use
	A.	Cache
	В.	TLB
		Buffers
	D.	Registers
ANS 6. [	)	
Q7		_ method is used to map logical address of variable length onto physical memory.
	A.	Paging
		Paging Overlays
	В.	
	В. С.	Overlays
	B. C. D.	Overlays Segmentation
ANS1. C	B. C. D.	Overlays Segmentation
ANS1. C Q8. Phy	B. C. D.	Overlays Segmentation Paging with segmentation
ANS1. C Q8. Phy	B. C. D.	Overlays Segmentation Paging with segmentation  Il memory is divided into sets of finite size called as
ANS1. C Q8. Phy	B. C. D. sica A. B.	Overlays Segmentation Paging with segmentation  Il memory is divided into sets of finite size called as  Frames
ANS1. C Q8. Phy	B. C. D. Ssica A. B.	Overlays Segmentation Paging with segmentation  Il memory is divided into sets of finite size called as  Frames Pages
ANS1. C Q8. Phy	B. C. D. sica A. B. C.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks
ANS1. C Q8. Phy ANS1. A	B. C. D. sica A. B. C.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks
ANS1. C Q8. Phy ANS1. A Q9. Wha	B. C. D. sica A. B. C.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks Vectors
ANS1. C Q8. Phy ANS1. A Q9. Wha	B. C. D. Sica A. B. C. D.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks Vectors  If the high speed memory between the main memory and the CPU called?
ANS1. C Q8. Phy ANS1. A Q9. Wha	B. C. D. C. D. A. A. A. A.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks Vectors  If the high speed memory between the main memory and the CPU called?  Registers Cache memory
ANS1. C Q8. Phy ANS1. A Q9. Wha	B. C. D. Sical A. B. C. D. A. B. C. D.	Overlays Segmentation Paging with segmentation  If memory is divided into sets of finite size called as  Frames Pages Blocks Vectors  If the high speed memory between the main memory and the CPU called?  Registers Cache memory

Q10. Wher	never the data is found in the cache memory it is called a
A. B.	HIT MISS
Б. С.	FOUND
	ERROR
ANS 10. A	
Q11. The t	ransfer between CPU and Cache is called
A.	Block transfer
В.	Word transfer
	Set transfer
D.	Associative transfer
ANS 11. B	
Q12. LRU s	tands for
A.	Low Rate Usage
В.	Least Rate Usage
C.	Least Recently Used
D.	Low Required Usage
ANS 12. C	
Q13. Wher called	the data at a location in cache is different from the data in the main memory, the cache is
A.	Unique
	Inconsistent
C.	Variable
D.	Fault
ANS 13. B	
Q14. Whic	n of the following is not a write policy to avoid Cache Coherence?
A.	Write through
В.	Write within
C.	Write back
D.	Write buffer
ANS 14. B	
Q15. In	mapping, the data can be mapped anywhere in the Cache Memory.
A.	Associative
В.	Direct
C.	Set-associative

	D.	Indirect	
ANS 15	. A		
Q16. Ca	Q16. Cache Memory is implemented using the DRAM chips.		
	A. B.	True False	
ANS 16	. В		
		<b>COA MCQ CHAPTER 5 &amp; 6</b>	
Q1. Wh	at is	the permanent memory built into your computer called?	
ANS 1.	В		
Q2. Sto	rage	which stores or retains data after power off is called	
	В. С.	Volatile storage Non-volatile storage Sequential storage Direct storage	
ANS2. E	3		
Q3. The	cor	tents of memory into blocks of the same size is called as	
	A. B. C. D.	El NOW	
ANS 3.	D		
Q4. Ma	in m	emory of computer is	
		Internal External Both Auxilliary	
ANS 4.	A		
Q5. Wh	ich d	of the following memories must be refreshed many times per second?	

A	
	. ROM Static RAM
	. Dynamic RAM
ANS 5. D	,
Q6. A half	-byte is known as
Α	. data
	. bit
	half-byte
D	. nibble
ANS 6. D	
Q7. USB t	ype storage device is
А	Secondary
В	. Auxiliary
	Tertiary
D	. Primary
ANS 7. A	
Q8. Which	n device is used to back-up the data?
Α	. Floppy disk
В	. Таре
	Network drive
D	. All of the above
ANS 8. D	
Q9. With	a CD you can perform
Α	. read
В	write
	read and write
D	. none of these
ANS 9. A	
Q10. Flasl	n memory is also known as
А	Flash RAM
	Flash ROM
	Flash DRAM
D	. Flash DROM

ANS 10. A

Q11. RAM	is a memory.
A.	External
В.	
	Main
D.	Auxiliary
ANS 11. C	
Q12	_ is the permanent memory unit built into the computer systems.
A.	ROM
	CPU
	DVD-ROM
D.	RAM
ANS 12. A	
Q13. Hard-	disk drives are considered as storage medium.
A.	Flash
В.	Non-volatile
C.	Temporary
D.	Permanent
ANS 13. B	
Q14. The s	torage element of a SRAM is
A.	Diode
В.	Resistor
C.	Capacitor
D.	Flip-flop
ANS 14. D	
Q15. Capac	city of hard-disk is measured in
A.	Gigabytes
В.	Megabytes
C.	Kilobytes
D.	Bytes
ANS 15. A	

### **COA MCQ CHAPTER 8**

Q1. Which of the following is not a type of Operating System?

A. Batch Processing

- B. Multi-programming
- C. Latch Programming
- D. Real time programming

#### ANS 1. C

- Q2. BIOS programs are embedded on a chip called
  - A. Firmware
  - B. IC
  - C. Hardware
  - D. Application programs

#### ANS 1. A

## **COA MCQ CHAPTER 5 & 6**

Q1. Wh	at is	the permanent memory built into your computer called?
	C.	RAM ROM CPU CD-ROM
ANS 1.	В	
Q2. Sto	rage	e which stores or retains data after power off is called
	B. C.	Volatile storage Non-volatile storage Sequential storage Direct storage
ANS2. E	3	
Q3. The	cor	ntents of memory into blocks of the same size is called as
	В. С.	ROM EPROM EEPROM All of the above
ANS 3.	D	
Q4. Ma	in m	nemory of computer is
	В. С.	Internal External Both Auxilliary
ANS 4.	Α	
Q5. Wh	ich (	of the following memories must be refreshed many times per second?
	A. B. C. D.	EPROM ROM Static RAM Dynamic RAM
ANS 5.	D	
Q6. A h	alf-k	pyte is known as
	A.	data

	half-byte nibble
ANS 6. D	
Q7. USB typ	pe storage device is
В. С.	Secondary Auxiliary Tertiary Primary
ANS 7. A	
Q8. Which	device is used to back-up the data?
В. С.	Floppy disk Tape Network drive All of the above
ANS 8. D	
Q9. With a	CD you can perform
В. С.	read write read and write none of these
ANS 9. A	
Q10. Flash	memory is also known as
В. С.	Flash RAM Flash ROM Flash DRAM Flash DROM
ANS 10. A	
Q11. RAM i	is a memory.
В. С.	External Internal Main Auxiliary
ANS 11. C	
Q12	_ is the permanent memory unit built into the computer systems.

C.	ROM CPU DVD-ROM RAM
ANS 12. A	
Q13. Hard-	disk drives are considered as storage medium.
В. С.	Flash Non-volatile Temporary Permanent
ANS 13. B	
Q14. The st	corage element of a SRAM is
C.	Diode Resistor Capacitor Flip-flop
ANS 14. D	
Q15. Capac	city of hard-disk is measured in
B. C. D.	Gigabytes Megabytes Kilobytes Bytes
ANS 15. A	

## **COA MCQ CHAPTER 4**

Q1. LRU sta	ands for
В. С.	Low Rate Usage Least Rate Usage Least Recently Used Low Required Usage
ANS 1. C	
Q2. When t	the data at a location in cache is different from the data in the main memory, the cache is
A.	Unique
	Inconsistent
C.	Variable
D.	Fault
ANS 2. B	
Q3. Which	of the following is not a write policy to avoid Cache Coherence?
A.	Write through
В.	Write within
C.	Write back
D.	Write buffer
ANS 3. B	
Q4. In	mapping, the data can be mapped anywhere in the Cache Memory.
A.	Associative
В.	Direct
C.	Set-associative
D.	Indirect
ANS 4. A	
Q5. To get	the physical address from the logical address generated by CPU we use
A.	MAR
В.	MMU
C.	Overlays
D.	TLB
ANS 5. B	
Q6. During	the transfer of data between the processor and memory we use
A.	Cache

В	. TLB
C	. Buffers
0	o. Registers
ANS 6. D	
Q7	method is used to map logical address of variable length onto physical memory.
A	Paging
В	. Overlays
C	. Segmentation
	Paging with segmentation
ANS1. C	
Q8. Physi	cal memory is divided into sets of finite size called as
A	Frames
Е	. Pages
C	. Blocks
0	o. Vectors
ANS1. A	
Q9. What	is the high speed memory between the main memory and the CPU called?
A	Registers
Е	. Cache memory
C	. Secondary storage memory
0	. Virtual memory
ANS 9. B	
Q10. Wh	enever the data is found in the cache memory it is called a
A	. HIT
В	. MISS
C	
	o. ERROR
ANS 10.	A
Q11. The	transfer between CPU and Cache is called
A	Block transfer
Е	. Word transfer
C	. Set transfer
	. Associative transfer

ANS 11. B

## 8086 MICROPROCESSOR

Q1. 8086 microprocessor supports modes of operation.
A. 2 B. 3 C. 4 D. 5
ANS1. A
Q2. 8086 can access up to memory.
A. 512 KB B. 1 MB C. 2 MB D. 256 KB
ANS1. B
Q3. 8086 has address bus.
<ul><li>A. 16-bit</li><li>B. 18-bit</li><li>C. 20-bit</li><li>D. 24-bit</li></ul>
ANS1. C
Q4. Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to zero?
<ul><li>A. Trap flag</li><li>B. Zero flag</li><li>C. Carry flag</li><li>D. Overflow flag</li></ul>
ANS1. B
Q5. Which flag represents the result when the system capacity is exceeded?
<ul><li>A. Trap flag</li><li>B. Auxiliary flag</li><li>C. Carry flag</li><li>D. Overflow flag</li></ul>
ANS1. B
Q6. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

A. IR

	HR WR
ANS1. D	
Q7. Which	instruction is used to load the address of operand into the provided register?
В. С.	LEA LDS LES LAHF
ANS1. A	
Q8. The dif	ferent ways in which a source operand is denoted in an instruction is known as:
В. С.	Instruction Set Interrupts Architecture Addressing Modes
ANS1. D	
Q9. A micro	oprocessor is a chip integrating all the functions of a CPU of a computer.
В. С.	multiple single double triple
ANS1. B	
Q10. The w	ork of EU is
В. С.	encoding decoding processing calculations
ANS1. B	
Q11. The re	egister used to store the flags is called as
B. C. D.	Flag register Status register Test register Log register
ANS 11. B	

B. HLDA

## **CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION**

Q1	bus structure is usually used to connect I/O devices
	Single bus Multiple bus
	Star bus
	RAM bus
Ο.	17 1171 503
ANS 1. A	
Q2. The m	ain advantage of using single bus structure is
A.	Fast data transfers
В.	Cost effective connectivity and speed
C.	Cost effective connectivity and ease of attaching peripheral devices
D.	None of the above
ANS 2. C	
Q3. The IS	A standard buses are used to connect
A.	RAM and Processor
В.	GPU and Processor
C.	Hard-disk and Processor
D.	CD / DVD drives and Processor
ANS 3. C	
Q4. Which	registers can interact with the secondary storage?
Α.	MAR
В.	PC
C.	IR
D.	AC
ANS 4. A	
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A.	PCI Bus
В.	SCSI Bus
C.	Controllers
D.	Multiple Bus
ANS 5. A	
Q6. A sou	ce program is usually written in

A.	Assembly language
В.	Machine-level language
C.	High-level language
D.	Natural language
ANS 6. C	
Q7	_ are numbers and encoded characters which are generally used as operands.
A.	Input
В.	Data
C.	Information
D.	Stored values
ANS 7. B	
Q8. The AL	U stores the immediate result in
A.	Accumulator
В.	Queue
	Stack
D.	Memory locations
ANS 8. A	
Q9. The co	ntrol unit controls other units by generating
A.	Control signals
В.	Timing signals
C.	Transfer signals
D.	Command signals
ANS 9. B	
Q10. The e	xtremely small and fast RAM is known as
A.	Cache
В.	Heaps
C.	Accumulators
D.	Stacks
ANS 10. A	
Q11. The s	mallest entity of memory is called
A.	Cell
В.	Block
C.	Instance
D.	Unit
ANS 11. A	

## **CHAPTER 2: PERFORMANCE ISSUES**

Q1	are used to overcome the difference in data transfer speeds of various devices.
A.	Speed enhancing circuitry
В.	Bridge circuits
C.	Multiple buses
D.	Buffer registers
ANS 1. D	
execute an	rocessors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can instruction with an average of 3 steps and B can execute with an average of 5 steps. For the of the same instruction which processor is faster?
A.	A
В.	В
	Both takes equal amount of time
D.	None of the above
ANS 2. A	
	essor performing fetch or decoding of different instruction during the execution of another is called
A.	Super-scaling
В.	Pipelining
	Parallel computation
D.	Architecture
ANS 3. B	
Q4. The clo	ock rate of the processor can be improved by
A.	Improving the IC technology of the logic circuits
В.	Reducing the amount of processing done in one step
C.	By using the over-clocking method
D.	All of the above
ANS 4. D	
Q5. SPEC st	tands for
A.	Standard Performance Evaluation Code
В.	System Processing Enhancing Code
C.	-1
D.	Standard Processing Enhancement Corporation

ANS 5. C

Q6. CISC stands for		
В. С.	Complete Instruction Sequential Compilation Computer Integrated Sequential Compiler Complex Instruction Set Computer Complex Instruction Sequential Compilation	
ANS 6. C		
Q7. Which i	nstruction is used to load the address of operand into the provided register?	
В. С.	LEA LDS LES LAHF	
ANS1. A		
Q8. The diff	erent ways in which a source operand is denoted in an instruction is known as:	
В. С.	Instruction Set Interrupts Architecture Addressing Modes	
ANS1. D		
Q9. A micro	processor is a chip integrating all the functions of a CPU of a computer.	
В. С.	multiple single double triple	
ANS1. B		
Q10. The work of EU is		
В. С.	encoding decoding processing calculations	

## CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

Q1. During the execution of a program which gets initialized first?		
	A. MDR	
	B. IR	
	C. PC	
	D. MAR	
ANS1. C		
Q2. The	decoded instruction is stored in	
	A. IR	
I	B. PC	
(	C. Registers	
	D. AC	
ANS1. A		
Q3. Whi	ch of the register(s) of the processor is / are connected to Memory Bus?	
	A. PC	
	B. MAR	
(	C. IR	
	D. Both PC AND MAR	
ANS1. B		
Q4. ISP s	tands for	
	A. Instruction Set Processor	
	B. Information Standard Processing	
(	C. Interchange Standard Protocol	
	D. Interrupt Service Procedure	
ANS1. A		
Q5. The interrupt request line is a part of the		
	A. Data line	
1	B. Control line	
(	C. Address line	
	D. None of the above	

ANS1. B

	Α.	Interrupt acknowledge
		Return signal
		Service signal
		Permission signal
ANS1.	Α	
		CHAPTER 4: CACHE MEMORY
O1 T-	راء ما،	
Q1. 10		uce the memory access time we generally make use of
		Heaps
		SSD SDRAMs
		Cache memory
		cache memory
ANS 1.	D	
Q2		is usually used to increase the size of physical memory.
	A.	Secondary memory
		Virtual memory
		Hard-disk
	D.	Disks
ANS 2.	В	
Q3. Th	e int	ernal components of the processor are connected by
	A.	Processor intra-connectivity circuitry
	В.	Processor bus
		Memory bus
	D.	Single bus
ANS 3.	В	
Q4. Du	ıring	the execution of instructions, a copy of the instructions is placed in the
	A.	Register
		RAM
		Main memory
	1)	Cache

Q6. The signal set to the device from the processor to the device after receiving an interrupt is

ANS 4. D	
Q5. To get	the physical address from the logical address generated by CPU we use
A.	MAR
В.	MMU
C.	Overlays
D.	TLB
ANS 5. B	
Q6. During	the transfer of data between the processor and memory we use
A.	Cache
В.	TLB
C.	Buffers
D.	Registers
ANS 6. D	
Q7	method is used to map logical address of variable length onto physical memory
A.	Paging
В.	Overlays
C.	Segmentation
D.	Paging with segmentation
ANS1. C	
Q8. Physic	al memory is divided into sets of finite size called as
A.	Frames
В.	Pages
C.	Blocks
D.	Vectors

ANS1. A

1.	What is DEN in 8086 microprocessor?	
	A. direct enable	
	B. data entered	
	C. data enable	
	D. data encountered	
	ANS- C	
2.	Status register is also called as	
	A. Accumulator	
	B. Stack	
	C. Counter	
	D. Flags	
	ANS- D	
3.	Which method bypasses CPU for certain type of data transfer?	
	A. software interrupts	
	B. interrupt-driven I/O	
	C. Direct memory Access	
	D. Polled I/O	
	ANS- C	
4.	A 20 bit address bus allows access to a memory of capacity	
	A. 1 MB	
	B. 2 MB	
	C. 4 MB	
	D. 8 MB	
	ANS- A	
5.	Which group of instructions do not affect the flags?	
	A. Arithmetic	
	B. Logical	
	C. Data transfer	
	D. Branch	
	ANS- C	
6.	If the offset of the operand is stored in one of the index registers, then it is known as	
	_	
	A. base index addressing mode	
	B. indexed addressing mode	
	C. relative base indexed addressing mode	
	D. none of these	
	ANS- B	
7.	Which of the following is not a data copy/transfer instruction?	
	A. MOV	
	B. PUSH	
	C. POP	
	D. DAS	
	ANS- D	
8.	Which is not a valid one?	

	B.	MOV DS, 5000H
	C.	MOV AX, 5000H
	D.	PUSH AX
		ANS- B
9.	Wh	nich register is used to get input data and send output data when I/O instructions
	are	e executed in 8086?
	A.	AX
	B.	BX
	C.	DX
	D.	SI
		ANS- A
10.	QP	I in point to point stands as
	A.	quick process interconnect
	B.	quick path interconnect
	C.	quick peripheral interconnect
	D.	none of these
		ANS- B
11.	Coı	mputer bus line consists of
	A.	Registers
		Accumulators
	C.	set of parallel lines
	D.	computer clock
		ANS- C
		y in which computer components are connected with each other is called
		computer layout
	B.	computer architecture
		computer parts
	D.	computer hardware
	_	ANS- B
		mputer system mainly consists of
		CPU
		Memory
		I/O Unit
	D.	All of the above
	_	ANS- D
		mputer instructions are divided into
		function code
		instruction code
		operand
	υ.	both a and c
4-	\ A ''	ANS- D
		nich is not part of the execution unit?
	Α.	Clock

A. MOV AX, BX

В.	ALU
C.	General registers
	Flags
	ANS- A
16. WI	nich Bus is bidirectional?
A.	Address bus
В.	control bus
C.	Data bus
D.	All of the above
	ANS- C
17. Th	e primary function of is to accept data from I/O devices.
A.	Multiprocessor
В.	Microprocessor
C.	Peripherals
D.	Interfaces
	ANS- B
18. Th	e microprocessor can read/write 16 bit data from or to
A.	Memory
В.	I/O devices
C.	Processor
D.	none of the above
	ANS- A
	20 bit address bus can locate
	1048576 locations
	2097152 locations
	419304 locations
D.	none of these
	ANS- A
20	generate interrupt signal to microprocessor and receive acknowledgement.
	Decoder
	control logic
	interrupt register
D.	all of the above
24 D.	ANS- B
	ring read operation, CPU fetches Data
	Instruction
	another address
	all of the above
υ.	ANS- D
22 DC	I stands for
	Peripheral Component Interconnect
	Peripheral Computer Interconnect  Peripheral Computer Internet
υ.	r enpheral compater internet

	C.	Processor Computer Interconnect
	D. I	Processor Cable Interconnect
	AN	S- A
23.	Wh	nat will be the contents of AL register after the following instructions have been
	exe	ecuted? MOV BL, 8C
	MC	OV AL, 7E
	ΑD	DD AL, BL
	A.	OA and carry flag is set
	B.	0A and carry flag is reset
	C.	6A and carry flag is set
	D.	6A and carry flag is reset
		ANS- A
24.	A s	cheme in which the register given in the instruction specifies the memory address
	of t	the operand is called
	A.	immediate addressing
	B.	base addressing
	C.	direct addressing
	D.	indirect addressing
		ANS-D
25.	The	e flag which is to be set for enabling single step or trap interrupt in the 8086
		·
		CF
	B.	DF
	C.	TF
	D.	IF
		ANS- C
26.	If tl	he base address of stack segment in 8086 is 4FFF0H, the value in SS register is
		8FFFH
		4FFEH
		5FFEH
	υ.	4FFFH
27	CI.	ANS- D
2/.		ck frequencies of two processors A and B are 700 MHz and 900 MHz respectively.
		executes an instruction with an average of 3 steps. B executes the same instruction
		h an average of 5 steps. Which processor is faster?
	Α.	
	В.	
		Botha are same
	υ.	Cannot be predicted
20	Λ	ANS- A
۷۵.	-	processor is performing fetch or decoding of different instructions during the
		ecution of another instruction is called as
	н.	super scaling

	В.	pipe-lining
	C.	parallel processing
	D.	none of these
		ANS- B
29.	If a	processor clock rate is 1250 million cycles per second, then its clock period
	is_	
	A.	1.9×10 <sup>-10</sup> sec
	В.	1.6×10 <sup>-6</sup> sec
	C.	1.2×10 <sup>-10</sup> sec
	D.	8×10 <sup>-10</sup> sec
		ANS- D
30.	CIS	C stands for
	A.	complete instruction sequential compilation
	В.	computer integrated sequential compiler
		complex instruction set computer
	D.	complex instruction sequential compilation
		ANS- C
31.		EC stands for
		standard performance evaluation criteria
		standard performance evaluation corporation
		Anyone from above
	D.	None of the above
		ANS- B
32.		nich is not a characteristics of benchmark program?
		wide distribution
		easy measurement
		representative of a particular kind of programming domain
	D.	low level language
22		ANS- D
33.		d speed up if N =10 and f=0.9.
		5.123
		5.2632
		5.0
	υ.	4.9
2.4	Th.	ANS-B
34.		e owner of a shop observes that on average 18 customers per hour arrive and
		ere are typically 8 customers in the shop. What is the average length of time each
		tomer spends in the shop? 0.44 hour
		1.2 hour 0.64 hour
		none of these
	υ.	ANS- A
25	Tor	chniques used in contemporary processors to increase speed are
JJ.	150	anniques used in contemporary processors to increase speed are

	A. Pipelining
	B. branch prediction
	C. super scalar execution
	D. all of the above
	ANS- D
36.	Which one is a performance metrics?
	A. Mean
	B. Clock Speed
	C. CPU Cycles
	D. All of the above
	ANS- D
37.	The Arithmetic mean rate of computer A, B and C are 0.12, 0.38 and 0.625
	respectively. Which one is faster?
	A. A
	B. B
	C. C
	D. All are equally faster
	ANS- C
38.	Classification of computers based on computing applications and their characteristics
	are
	A. Desktop
	B. Server
	C. Super computer
	D. All of the above
20	ANS- D
39.	8086 microprocessor is atype of processor.
	A. 8 bit B. 16 bit
	C. 32 bit D. None of the above
	ANS- B
40	. What is the basic functions of a computer?
40.	A. Processing
	B. Storage
	C. Output
	D. All of the above
	ANS- D
41.	The instructions that are used for reading an input port and writing an output port
	respectively are
	a) MOV, XCHG
	b) MOV, IN
	c) IN, MOV
	d) IN, OUT
	ANS- D

42. The instruction that loads effective address formed by destination operand into the
specified source register is
a) LEA
b) LDS
c) LES
d) LAHF
ANS- A
43. The instruction that supports addition when carry exists is
a) ADD
b) ADC
c) ADD & ADC
d) None of the mentioned
ANS- B
44. A machine language instruction format consists of
a) Operand field
b) Operation code field
c) Operation code field & operand field
d) none of the mentioned
ANS- C
45. The instruction, "INC" increases the contents of the specified register or memory
location by
a) 2
b) 0
c) 1
d) 3
ANS- C
46. 3. The instruction that enables subtraction with borrow is
a) DEC
b) SUB
c) SBB
d) None of the mentioned
ANS- C
47. In general, the source operand of an instruction can be
a) memory location
b) register
c) immediate data
d) all of the mentioned
ANS- D
48. The number of address bits in a 32K×12 memory is
A. 10
B. 12
C. 15
D. 16
ANS- C

49.	The	e number of index bits in a direct mapping of 32K×12 main memory and 512
	×12	2cache memory is
	A.	6
	В.	7
	C.	8
	D.	9
		ANS- D

## 8086: Microprocessor

## **Multiple Choice Questions and Answers:-**

1. A microprocessor is a	_ chip integrating all the functions of a CPU of a computer.
A. multiple	
B. single	
C. double	OT,
D. triple	5
Answer: B	
2. Microprocessor is a/an	circuit that functions as the CPU of the compute
A. electronic	
B. mechanic	
C. integrating	
D. processing	
Answer: A	
3. Microprocessor is the	of the computer and it perform all the computational tasks
A. main	
B. heart	
C. important	

D. simple
Answer: B
4. The purpose of the microprocessor is to control
A. memory
B. switches
C. processing
D. tasks
Answer: A
5. The first digital electronic computer was built in the year
A. 1950
B. 1960
C. 1940
D. 1930
Answer: C
6. In 1960's texas institute invented

A. integrated circuits

B. microprocessor
C. vacuum tubes
D. transistors
Answer: A
7. The intel 8086 microprocessor is a processor
A. 8 bit
B. 16 bit
C. 32 bit
D. 4 bit
Answer: B
8. The microprocessor can read/write 16 bit data from or to
A. memory B. I /O device
C. processor
D. register
Answer: A
9. In 8086 microprocessor , the address bus is bit wide

A.1
2 bit
B. 10 bit
C. 16 bit
D. 20 bit
Answer: D
10. The work of EU is
A. encoding
B. decoding
C. processing
D. calculations
Answer: B
11. The 16 bit flag of 8086 microprocessor is responsible to indicate
A. the condition of result of ALU operation
B. the condition of memory
C. the result of addition
D. the result of subtraction

Answer: A
12. The CF is known as
A. carry flag
B. condition flag
C. common flag
D. single flag
Answer: A
13. The SF is called as
A. service flag
B. sign flag
C. single flag
D. condition flag
Answer: B  14. The OF is called as
A. overflow flag
B. overdue flag

C. one flag

D. over flag
Answer: A
15. The IF is called as
A. initial flag
B. indicate flag
C. interrupt flag
D. inter flag
Answer: C  16. The register AX is formed by grouping
A. AH & AL  B. BH & BL
C. CH & CL
D. DH & DL
Answer: A
17. The SP is indicated by

A. single pointer

B. stack pointer
C. source pointer
D. destination pointer
Answer: B
18. The BP is indicated by
44
A. base pointer
B. binary pointer
C. bit pointer
D. digital pointer
Answer: A
19. The SS is called as
A. single stack
B. stack segment
C. sequence stack
D. random stack
Answer: B
20. The index register are used to hold

A. memory register
B. offset address
C. segment memory
D. offset memory
Answer: A
21. The BIU contains FIFO register of size bytes
A. 8
B. 6
C. 4
D. 12
Answer: B
22. The BIU prefetches the instruction from memory and store them in
A. queue
B. register
C. memory
D. stack
Answer: A

23. The 1 MB byte of memory can be divided into _	segment
A. 1 Kbyte	
B. 64 Kbyte	
C. 33 Kbyte	
D. 34 Kbyte	
Answer: B	54
24. The DS is called as	
A. data segment	9.5
B. digital segment	
C. divide segment	
D. decode segment	
Answer: A	
25. The CS register stores instruction	in code segment
A. stream	
B. path	
C. codes	
D. stream line	

Answer: C
26. The IP is bits in length
A. 8 bits
B. 4 bits
C. 16 bits
D. 32 bits
Answer: C
27. The push source copies a word from source to
A. stack
B. memory
C. register
D. destination
Answer: A
28. LDs copies to consecutive words from memory to register and
A. ES

B. DS

C. SS
D. CS
Answer: B
29. INC destination increments the content of destination by
A. 1
B. 2
C. 30
D. 41
Answer: A
30. IMUL source is a signed
A. multiplication
B. addition
C. subtraction
D. division
Answer: A
31destination inverts each bit of destination

A. NOT
B. NOR
C. AND
D. OR
Answer: A
32. The JS is called as
A. jump the signed bit
B. jump single bit
C. jump simple bit
D. jump signal it
Answer: A
33. Instruction providing both segment base and offset address are called
A. below type.
B. far type
C. low type
D. high type
Answer: B

34. The conditional bra	nch instruction specify	for branching	
A. conditions			
B. instruction			
C. address			
D. memory			
Answer: A			A.
35. The microprocesso	r determines whether the spec	cified condition exists or no	ot by testing the
A. carry flag		Χ,	
B. conditional flag			
C. common flag	(4.	,	
D. sign flag			
Answer: B			
36. The LES copies to w	vords from memory to register	and	
A. DS			
B. CS			
C. ES			
D. DS			

Answer: C
37. The translates a byte from one code to another code
A. XLAT
B. XCHNG
C. POP
D. PUSH
Answer: A
38. The contains an offset instead of actual address
A. SP
B. IP
C. ES
D. SS
Answer: B
39. The 8086 fetches instruction one after another from of memory
A. code segment

B. IP

C. ES
D. SS
Answer: A
40. The BIU contains FIFO register of size 6 bytes called
A. queue
B. stack
C. segment
D. register
Answer: A
41. The is required to synchronize the internal operands in the processor CLK
Signal
A. UR Signal
B. Vcc
C. AIE
D. Ground
Answer: A
42. The pin of minimum mode AD0-AD15 has address

A. 16 bit
B. 20 bit
C. 32 bit
D. 4 bit
Answer: B
43. The pin of minimum mode AD0- AD15 has data bus
A. 4 bit
B. 20 bit
C. 16 bit
D. 32 bit
Answer: C
44. The address bits are sent out on lines through
A. A16-19 B. A0-17 C. D0-D17
D. C0-C17
Answer: A

45 is used to write into memory
A. RD
B. WR
C. RD / WR
D. CLK
Answer: B
46. The functions of Pins from 24 to 31 depend on the mode in which is operating
A. 8085
B. 8086
C. 80835
D. 80845
Answer: B
47. The RD, WR, M/IO is the heart of control for a mode
A. minimum
B. maximum
C. compatibility mode

D. control mode

Answer: A
48. In a minimum mode there is a on the system bus
A. single
B. double
C. multiple
D. triple
Answer: A
49. If MN/MX is low the 8086 operates in mode
A. Minimum
B. Maximum
C. both (A) and (B)
D. medium
Answert B  50. In max mode, control bus signal So,S1 and S2 are sent out in form
A. decoded

B. encoded

C. shared
D. unshared
Answer: B
51. The bus controller device decodes the signals to produce the control bus signal
A. internal
B. data
C. external
D. address
Answer: C
52. A Instruction at the end of interrupt service program takes the execution back to the
interrupted program
A. forward
B. return
C. data
D. line
Answer: B
53. The main concerns of the are to define a flexible set of commands

A. memory interface	
B. peripheral interface	
C. both (A) and (B)	
D. control interface	<b>A</b>
Answer: A	94
54. Primary function of memory interfacing is that the	should be able to read from
and write into register	
	$\sim$
A. multiprocessor	<b>J</b> .
B. microprocessor	
C. dual Processor	
D. coprocessor	
Answer: B	
55. To perform any operations, the Mp should identify the	
A. register	
B. memory	
C. interface	
D. system	

Answer: A

B. external decoder

C. address decoder
D. data decoder
Answer: A
59. Microprocessor provides signal like to indicate the read operatio
A. LOW
B. MCMW
C. MCMR
D. MCMWR
Answer: C
60. To interface memory with the microprocessor, connect register the lines of the address bus
must be added to address lines of the chip.
A. single
B. memory
C. multiple
D. triple
Answer: B
61. The remaining address line of bus is decoded to generate chip select signal

A. data
B. address
C. control bus
D. both (a) and (b)
Answer: B
62 signal is generated by combining RD and WR signals with IO/M
A. control
B. memory
C. register
D. system
Answer: A
63. Memory is an integral part of a system
A. supercomputer
B. microcomputer
C. mini computer
D. mainframe computer
Answer: B

64 has certain signal requirements write into and read from its registers
A. memory
B. register
C. both (a) and (b)
D. control
Answer: A
65. An is used to fetch one address
A. internal decoder
B. external decoder
C. encoder
D. register
Answer: A
66. The primary function of the is to accept data from I/P devices  A. multiprocessor
B. microprocessor
C. peripherals
D. interfaces

B. control logic

C. interrupt request register

D. interrupt register
Answer: B
70. The pin is used to select direct command word
A. A0
B. D7-D6
C. A12
D. AD7-AD6
Answer: A
71. The is used to connect more microprocessor
A. peripheral device
B. cascade
C. I/O devices
D. control unit
Answer: B
72. CS connect the output of

A. encoder

B. decoder	
C. slave program	
D. buffer	
Answer: B	
73. In which year, 8086 was introduced?	
94.	
A. 1978	
B. 1979	
C. 1977	
D. 1981	
Answer: A	
74. Expansion for HMOS technology	
A. high level mode oxygen semiconductor	
B. high level metal oxygen semiconductor	
C. high performance medium oxide semiconductor	
D. high performance metal oxide semiconductor	
STITE PERIOD TO A TO	
Answer: D	
75. 8086 and 8088 contains transistors	

A. 29000
B. 24000
C. 34000
D. 54000
Answer: A
76. ALE stands for
A. address latch enable
B. address level enable
C. address leak enable
D. address leak extension
Answer: A
77. What is DEN?
A. direct enable
B. data entered
C. data enable
D. data encoding

Answer: C

78. In 8086, Example for Non maskable interrupts are
A. TRAP
B. RST6.5
C. INTR
D. RST6.6
Answer: A
79. In 8086 the overflow flag is set when
A. the sum is more than 16 bits.
B. signed numbers go out of their range after an arithmetic operation.
C. carry and sign flags are set.
D. subtraction
Answer: B
80. In 8086 microprocessor the following has the highest priority among all type interrupts?
A. NMI
B. DIV 0
C. TYPE 255
D. OVER FLOW

A. ROM

B. SRAM

81. In 8086 microprocessor one of the following statements is not true?
A. coprocessor is interfaced in max mode.
B. coprocessor is interfaced in min mode.
C. I /O can be interfaced in max / min mode.
D. supports pipelining
Answer: B
82. Address line for TRAP is?
A. 0023H
B. 0024H
C. 0033H
D. 0099H
Answer: B  83. Access time is faster for

C. DRAM
D. ERAM
Answer: B
84. The First Microprocessor was
A. Intel 4004
B. 8080
C. 8085
D. 4008
Answer: A
85. Status register is also called as
A. accumulator
B. stack
C. counter
D. flags
Answer: D

86. Which of the following is not a basic element within the microprocessor?

A.Microcontroller
B. Arithmetic logic unit (ALU)
C. Register array
D. Control unit
Answer: A
87.Which method bypasses the CPU for certain types of data transfer?
A.Software interrupts
B. Interrupt-driven I/O
C. Polled I/O
D. Direct memory access (DMA)
Answer: D
88.Which bus is bidirectional?
A.
Address bus
B. Control bus
C. Data bus
D. None of the above
Answer: C

89.The first microprocessor had a(n)	
A.1 – bit data bus	
B. 2 – bit data bus	
C. 4 – bit data bus	
D. 8 – bit data bus	
Answer: C	
90.Which microprocessor has multiplexed data and address lines?	
A.8086  B. 80286  C. 80386  D. Pentium	
Answer: A	
91.Which is not an operand?  A.Variable	
B. Register	
C. Memory location	
D. Assembler	

Answer: D
92.Which is not part of the execution unit (EU)?
A.Arithmetic logic unit (ALU)
B. Clock
C. General registers
D. Flags
Answer: B
93.A 20-bit address bus can locate
A.1,048,576 locations
B. 2,097,152 locations
C. 4,194,304 locations
D. 8,388,608 locations
Answer: A  94.Which of the following is not an arithmetic instruction?
A. INC (increment)
B. CMP (compare)

C. DEC (decrement)
D. ROL (rotate left)
Answer: D
95.During a read operation the CPU fetches
A.a program instruction
B. another address
C. data itself
D. all of the above
Answer: D
96.Which of the following is not an 8086/8088 general-purpose register?
A.Code segment (CS)
B. Data segment (DS)
C. Stack segment (\$S)
D. Address segment (AS)
Answer: D
97.A 20-bit address bus allows access to a memory of capacity

A.1 MB
B. 2 MB
C. 4 MB
D. 8 MB
Answer: A
98.Which microprocessor accepts the program written for 8086 without any changes?
A.8085
B. 8086
C. 8087
D. 8088
Answer: D
99.Which group of instructions do not affect the flags?
A.Arithmetic operations
B. Logic operations
C. Data transfer operations
D. Branch operations
Answer: C

A.store 0100 0010 in AL

B. store 42H in AL

C. store 40H in AL

D. store 0100 0001 in AL

Answer: D

## 8086: Microprocessor

## **Multiple Choice Questions and Answers:-**

1. A microprocessor is a	_ chip integrating all the functions of a CPU of a computer.
A. multiple	
B. single	
C. double	OT,
D. triple	5
Answer: B	
2. Microprocessor is a/an	circuit that functions as the CPU of the compute
A. electronic	
B. mechanic	
C. integrating	
D. processing	
Answer: A	
3. Microprocessor is the	of the computer and it perform all the computational tasks
A. main	
B. heart	
C. important	

D. simple
Answer: B
4. The purpose of the microprocessor is to control
A. memory
B. switches
C. processing
D. tasks
Answer: A
5. The first digital electronic computer was built in the year
A. 1950
B. 1960
C. 1940
D. 1930
Answer: C
6. In 1960's texas institute invented

A. integrated circuits

B. microprocessor
C. vacuum tubes
D. transistors
Answer: A
7. The intel 8086 microprocessor is a processor
A. 8 bit
B. 16 bit
C. 32 bit
D. 4 bit
Answer: B
8. The microprocessor can read/write 16 bit data from or to
A. memory B. I /O device
C. processor
D. register
Answer: A
9. In 8086 microprocessor , the address bus is bit wide

A.1
2 bit
B. 10 bit
C. 16 bit
D. 20 bit
Answer: D
10. The work of EU is
A. encoding
B. decoding
C. processing
D. calculations
Answer: B
11. The 16 bit flag of 8086 microprocessor is responsible to indicate
A. the condition of result of ALU operation
B. the condition of memory
C. the result of addition
D. the result of subtraction

Answer: A
12. The CF is known as
A. carry flag
B. condition flag
C. common flag
D. single flag
Answer: A
13. The SF is called as
A. service flag
B. sign flag
C. single flag
D. condition flag
Answer: B  14. The OF is called as
A. overflow flag
B. overdue flag

C. one flag

D. over flag
Answer: A
15. The IF is called as
A. initial flag
B. indicate flag
C. interrupt flag
D. inter flag
Answer: C  16. The register AX is formed by grouping
A. AH & AL  B. BH & BL
C. CH & CL
D. DH & DL
Answer: A
17. The SP is indicated by

A. single pointer

B. stack pointer
C. source pointer
D. destination pointer
Answer: B
18. The BP is indicated by
44
A. base pointer
B. binary pointer
C. bit pointer
D. digital pointer
Answer: A
19. The SS is called as
A. single stack
B. stack segment
C. sequence stack
D. random stack
Answer: B
20. The index register are used to hold

A. memory register
B. offset address
C. segment memory
D. offset memory
Answer: A
21. The BIU contains FIFO register of size bytes
A. 8
B. 6
C. 4
D. 12
Answer: B
22. The BIU prefetches the instruction from memory and store them in
A. queue
B. register
C. memory
D. stack
Answer: A

23. The 1 MB byte of memory can be divided into _	segment
A. 1 Kbyte	
B. 64 Kbyte	
C. 33 Kbyte	
D. 34 Kbyte	
Answer: B	54
24. The DS is called as	
A. data segment	9.5
B. digital segment	
C. divide segment	
D. decode segment	
Answer: A	
25. The CS register stores instruction	in code segment
A. stream	
B. path	
C. codes	
D. stream line	

Answer: C
26. The IP is bits in length
A. 8 bits
B. 4 bits
C. 16 bits
D. 32 bits
Answer: C
27. The push source copies a word from source to
A. stack
B. memory
C. register
D. destination
Answer: A
28. LDs copies to consecutive words from memory to register and
A. ES

B. DS

C. SS
D. CS
Answer: B
29. INC destination increments the content of destination by
A. 1
B. 2
C. 30
D. 41
Answer: A
30. IMUL source is a signed
A. multiplication
B. addition
C. subtraction
D. division
Answer: A
31destination inverts each bit of destination

A. NOT
B. NOR
C. AND
D. OR
Answer: A
32. The JS is called as
A. jump the signed bit
B. jump single bit
C. jump simple bit
D. jump signal it
Answer: A
33. Instruction providing both segment base and offset address are called
A. below type.
B. far type
C. low type
D. high type
Answer: B

34. The conditional bra	nch instruction specify	for branching	
A. conditions			
B. instruction			
C. address			
D. memory			
Answer: A			A.
35. The microprocesso	r determines whether the spec	cified condition exists or no	ot by testing the
A. carry flag		Χ,	
B. conditional flag			
C. common flag	(4.)	,	
D. sign flag			
Answer: B			
36. The LES copies to w	vords from memory to register	and	
A. DS			
B. CS			
C. ES			
D. DS			

Answer: C
37. The translates a byte from one code to another code
A. XLAT
B. XCHNG
C. POP
D. PUSH
Answer: A
38. The contains an offset instead of actual address
A. SP
B. IP
C. ES
D. SS
Answer: B
39. The 8086 fetches instruction one after another from of memory
A. code segment

B. IP

C. ES
D. SS
Answer: A
40. The BIU contains FIFO register of size 6 bytes called
A. queue
B. stack
C. segment
D. register
Answer: A
41. The is required to synchronize the internal operands in the processor CLK
Signal
A. UR Signal
B. Vcc
C. AIE
D. Ground
Answer: A
42. The pin of minimum mode AD0-AD15 has address

A. 16 bit
B. 20 bit
C. 32 bit
D. 4 bit
Answer: B
43. The pin of minimum mode AD0- AD15 has data bus
A. 4 bit
B. 20 bit
C. 16 bit
D. 32 bit
Answer: C
44. The address bits are sent out on lines through
A. A16-19 B. A0-17 C. D0-D17
D. C0-C17
Answer: A

45 is used to write into memory
A. RD
B. WR
C. RD / WR
D. CLK
Answer: B
46. The functions of Pins from 24 to 31 depend on the mode in which is operating
A. 8085
B. 8086
C. 80835
D. 80845
Answer: B
47. The RD, WR, M/IO is the heart of control for a mode
A. minimum
B. maximum
C. compatibility mode

D. control mode

Answer: A
48. In a minimum mode there is a on the system bus
A. single
B. double
C. multiple
D. triple
Answer: A
49. If MN/MX is low the 8086 operates in mode
A. Minimum
B. Maximum
C. both (A) and (B)
D. medium
Answert B  50. In max mode, control bus signal So,S1 and S2 are sent out in form
A. decoded

B. encoded

C. shared
D. unshared
Answer: B
51. The bus controller device decodes the signals to produce the control bus signal
A. internal
B. data
C. external
D. address
Answer: C
52. A Instruction at the end of interrupt service program takes the execution back to the
interrupted program
A. forward
B. return
C. data
D. line
Answer: B
53. The main concerns of the are to define a flexible set of commands

A. memory interface	
B. peripheral interface	
C. both (A) and (B)	
D. control interface	<b>A</b>
Answer: A	94
54. Primary function of memory interfacing is that the	should be able to read from
and write into register	
	$\sim$
A. multiprocessor	<b>J</b> .
B. microprocessor	
C. dual Processor	
D. coprocessor	
Answer: B	
55. To perform any operations, the Mp should identify the	
A. register	
B. memory	
C. interface	
D. system	

Answer: A

B. external decoder

C. address decoder
D. data decoder
Answer: A
59. Microprocessor provides signal like to indicate the read operatio
A. LOW
B. MCMW
C. MCMR
D. MCMWR
Answer: C
60. To interface memory with the microprocessor, connect register the lines of the address bus
must be added to address lines of the chip.
A. single
B. memory
C. multiple
D. triple
Answer: B
61. The remaining address line of bus is decoded to generate chip select signal

A. data
B. address
C. control bus
D. both (a) and (b)
Answer: B
62 signal is generated by combining RD and WR signals with IO/M
A. control
B. memory
C. register
D. system
Answer: A
63. Memory is an integral part of a system
A. supercomputer
B. microcomputer
C. mini computer
D. mainframe computer
Answer: B

64 has certain signal requirements write into and read from its registers
A. memory
B. register
C. both (a) and (b)
D. control
Answer: A
65. An is used to fetch one address
A. internal decoder
B. external decoder
C. encoder
D. register
Answer: A
66. The primary function of the is to accept data from I/P devices  A. multiprocessor
B. microprocessor
C. peripherals
D. interfaces

B. control logic

C. interrupt request register

D. interrupt register
Answer: B
70. The pin is used to select direct command word
A. A0
B. D7-D6
C. A12
D. AD7-AD6
Answer: A
71. The is used to connect more microprocessor
A. peripheral device
B. cascade
C. I/O devices
D. control unit
Answer: B
72. CS connect the output of

A. encoder

B. decoder
C. slave program
D. buffer
Answer: B
73. In which year, 8086 was introduced?
dr,
A. 1978
B. 1979
C. 1977
D. 1981
Answer: A
74. Expansion for HMOS technology
A. high level mode oxygen semiconductor
B. high level metal oxygen semiconductor
C. high performance medium oxide semiconductor
D. high performance metal oxide semiconductor
Answer: D
75. 8086 and 8088 contains transistors

A. 29000
B. 24000
C. 34000
D. 54000
Answer: A
76. ALE stands for
A. address latch enable
B. address level enable
C. address leak enable
D. address leak extension
Answer: A
77. What is DEN?
A. direct enable
B. data entered
C. data enable
D. data encoding

Answer: C

78. In 8086, Example for Non maskable interrupts are
A. TRAP
B. RST6.5
C. INTR
D. RST6.6
Answer: A
79. In 8086 the overflow flag is set when
A. the sum is more than 16 bits.
B. signed numbers go out of their range after an arithmetic operation.
C. carry and sign flags are set.
D. subtraction
Answer: B
80. In 8086 microprocessor the following has the highest priority among all type interrupts?
A. NMI
B. DIV 0
C. TYPE 255
D. OVER FLOW

A. ROM

B. SRAM

81. In 8086 microprocessor one of the following statements is not true?
A. coprocessor is interfaced in max mode.
B. coprocessor is interfaced in min mode.
C. I /O can be interfaced in max / min mode.
D. supports pipelining
Answer: B
82. Address line for TRAP is?
A. 0023H
B. 0024H
C. 0033H
D. 0099H
Answer: B  83. Access time is faster for

C. DRAM
D. ERAM
Answer: B
84. The First Microprocessor was
A. Intel 4004
B. 8080
C. 8085
D. 4008
Answer: A
85. Status register is also called as
A. accumulator
B. stack
C. counter
D. flags
Answer: D

86. Which of the following is not a basic element within the microprocessor?

A.Microcontroller
B. Arithmetic logic unit (ALU)
C. Register array
D. Control unit
Answer: A
87.Which method bypasses the CPU for certain types of data transfer?
A.Software interrupts
B. Interrupt-driven I/O
C. Polled I/O
D. Direct memory access (DMA)
Answer: D
88.Which bus is bidirectional?
A.
Address bus
B. Control bus
C. Data bus
D. None of the above
Answer: C

89.The first microprocessor had a(n)	
A.1 – bit data bus	
B. 2 – bit data bus	
C. 4 – bit data bus	
D. 8 – bit data bus	
Answer: C	
90.Which microprocessor has multiplexed data and address lines?	
A.8086  B. 80286  C. 80386  D. Pentium	
Answer: A	
91.Which is not an operand?  A.Variable	
B. Register	
C. Memory location	
D. Assembler	

Answer: D
92.Which is not part of the execution unit (EU)?
A.Arithmetic logic unit (ALU)
B. Clock
C. General registers
D. Flags
Answer: B
93.A 20-bit address bus can locate
A.1,048,576 locations
B. 2,097,152 locations
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B. CMP (compare)

C. DEC (decrement)
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B. another address
C. data itself
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Answer: D
96.Which of the following is not an 8086/8088 general-purpose register?
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B. Data segment (DS)
C. Stack segment (\$S)
D. Address segment (AS)
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97.A 20-bit address bus allows access to a memory of capacity

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C. 4 MB
D. 8 MB
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98.Which microprocessor accepts the program written for 8086 without any changes?
A.8085
B. 8086
C. 8087
D. 8088
Answer: D
99.Which group of instructions do not affect the flags?
A.Arithmetic operations
B. Logic operations
C. Data transfer operations
D. Branch operations
Answer: C

A.store 0100 0010 in AL

B. store 42H in AL

C. store 40H in AL

D. store 0100 0001 in AL

Answer: D

# COMPUTER ORGANIZATION AND ARCHITECTURE BCA

# **Multiple choice questions**

1.	In Reverse Polish notation, expression A*B+C*D is written as						
	(A) AB*CD*+ (	B) A*BCD*+	(C) AB*CD+*	(D) A*B*CD+			
	Ans: A						
2.	SIMD represents an org	ganization that	•				
(A) refers to a computer system capable of processing several programs at the stime.							
	(B) represents organization of single computer containing a control unit, processor unit and a memory unit.						
	(C) includes many proc (D) none of the above.	_	ne supervision of a	common control unit			
	Ans: C						
3.	Floating point represer	ntation is used to sto	re				
	(A) Boolean values	(B) whole number	s (C) real intege	ers (D) integers			
	Ans: C						
4.	4. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle of the bus was reduced to 125 nsecs and the number of cycles required for transstayed the same what would the bandwidth of the bus?						
	(A) 1 Megabyte/sec	(B) 4 Megab	ytes/sec				
	(C) 8 Megabytes/sec	(D) 2 Megaby	ytes/sec				
	Ans: D						
5.	Assembly language						
	(A) uses alphabetic codes in place of binary numbers used in machine language						
	(B) is the easiest language to write programs						
	(C) need not be translated into machine language						
	(D) None of these						
	Ans: A						
6.	In computers, subtract	ion is generally carri	ed out by				
	(A) 9's complement	(B) 10's cor	•				
	(C) 1's complement <b>Ans:</b> D	(D) 2's com	plement				
7.	The amount of time recomposed of seek time	•		•			
	refers to						
	<ul><li>(A) the time its takes for the platter to make a full rotation</li><li>(B) the time it takes for the read-write head to move into position over the</li></ul>						
	appropriate track		au to move into pos	ation over the			

(C) the time it takes for the platter to rotate the correct sector under the head

(D) none of the above

	Ans: A							
8.	What characteristic	of RAM memor	y makes it not suitable	e for permanent storage?				
	(A) too slow (	B) unreliable	(C) it is volatile	(D) too bulky				
	Ans: C							
9.	. Computers use addressing mode techniques for							
	(A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control							
	(B) to reduce no. of bits in the field of instruction							
	(C) specifying rules for modifying or interpreting address field of the instruction							
	(D) All the above							
	Ans: D							
10.	The circuit used to	store one bit of o	lata is known as					
	(A) Register  Ans: D	(B) Encoder	(C) Decoder	(D) Flip Flop				
11.	(2FAOC) 16 is equiv	alent to						
	(A) (195 084) 10 (C) Both (A) and (B		01011111010 0000 11 ne of these	00) 2				
	Ans: B							
12.	The average time recontents is called the	=	a storage location in r	memory and obtain its				
	(A) seek time	(B) turnarour	nd time (C) access t	time (D) transfer time				
	Ans: C							
13.	Which of the follow	ving is not a weig	hted code?					
	(A) Decimal Numb	er system	(B) Excess 3-cod					
	(C) Binary number	System	(D) None of these					
	Ans: B							
14.	The idea of cache n	nemory is based						
			ference (B) or erally tend to cluster	the heuristic 90-10 rule				
	Ans: A	references gene	runy terra to craster	(b) an or the above				
15	Which of the follow	ving is lowest in r	nemory hierarchy?					
	(A) Cache memory	ving is lowest in i	nemory merareny.					
	(B) Secondary mem	nory						
	(C) Registers							
	(D) RAM							
	(E) None of these							
	Ans (B) Secondary	memory						
16.	The addressing mo	de used in an ins	truction of the form A	DD X Y, is				
	(A) Absolute	(B) indirect	(C) index	(D) none of these				
	Ans: C	, ,	, ,	, ,				
17.		akes 20 ns with o	cache and 110 ns with	out it, then the ratio (				
	cache uses a 10 ns							

(A) 93% <b>Ans:</b> B	(B) 90%	(C) 88%	(D) 87%			
18. In a memory	v-mapped I/O	svstem. which	of the following v	vill not b	e there?	
(A) LDA	(B) IN	(C) ADD	(D) OUT			
Ans: A	,	` '	,			
19. In a vectored	l interrupt.					
	•	gned to a fixe	d location in memo	ory.		
	oting source su	_	anch information t	=	cessor through	
(C) the branch a	address is obta	ined from a re	egister in the proc	essor		
(D) none of the	above					
Ans: B						
20. Von Neumar	nn architecture	e is				
(A) SISD	(B) SIMD	(C) MIMD	(D) MISD			
Ans: A						
21. The circuit u	sed to store or	ne bit of data	is known as			
(A) Encoder	· (B) (	OR gate	(C) Flip Flop		(D) Decoder	
Ans: C						
22. Cache memo	ory acts betwe	en				
(A) CPU and	RAM (B) R	AM and ROM	(C) CPU and Hai	rd Disk	(D) None of these	
Ans: A						
			h memory for upd	ating the	e data	
(A) Virtual n	•	. ,	memory			
	memory	(D) Cach	e memory			
Ans: D				_		
24. Generally Dynamic RAM is used as main memory in a computer system as it						
• •	es less power	(B) has high	•	_		
	r cell density	(D) needs r	efreshing circuitar	У		
Ans: B	anituda hinan	, division if th	o dividend is (111	00\ 2 and	d divisor is	
_	en the result is		ne dividend is (111	oo) z and	I UIVISOI IS	
(A) (00100			(C) (11001) 2	(D) (0	1100) 2	
Ans: B	(5)(1	0100,2	(0) (11001) 2	(5) (6	1100, 2	
26. Virtual mem	orv consists of					
(A) Static RA	•		mic RAM			
• •	c memory	` ' '	e of these			
Ans: A		( /				
27. In a program	using subrout	ine call instru	ction, it is necessa	ry		
	_		Clear the accumul	=		
• •		• •	Clear the instructi		er	
Ans: D	•	. ,		J		
28. A Stack-orga	anised Comput	er uses instru	ction of			
_	-					

(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressing	g
Ans: C	
29. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be (A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits	
Ans: C	
30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit	
(A) n TQD = • (B) T D = (C) D = T . Q n (D) n TQD = $\bigoplus$	
Ans: D	
31. Logic X-OR operation of (4ACO) H & (B53F) H results	
(A) AACB (B) 0000 (C) FFFF (D) ABCD	
Ans: C	
32. When CPU is executing a Program that is part of the Operating System, it is said to	
be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mod	е
Ans: B	
33. An n-bit microprocessor has	
(A) n-bit program counter (B) n-bit address register	
(C) n-bit ALU (D) n-bit instruction register	
Ans: D	
34. Cache memory works on the principle of	
(A) Locality of data (B) Locality of memory	
(C) Locality of reference (D) Locality of reference & memory	
Ans: C	
35. The main memory in a Personal Computer (PC) is made of	
(A) cache memory. (B) static RAM	
(C) Dynamic Ram (D) both (A) and (B).	
Ans: D	
36. In computers, subtraction is carried out generally by	
(A) 1's complement method (B) 2's complement method	
(C) signed magnitude method (D) BCD subtraction method	
Ans: B	
37. PSW is saved in stack when there is a	
(A) interrupt recognised (B) execution of RST instruction	
(C) Execution of CALL instruction (D) All of these	
Ans: A	
38. The multiplicand register & multiplier register of a hardware circuit implementing	
booth's algorithm have (11101) & (1100). The result shall be	
(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10	
Ans: A	
39. The circuit converting binary data in to decimal is  (A) Encoder (P) Multipleyer (C) Deceder (D) Code converter	
(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter  Ans: D	

40.	A three input NOR gate give	s logic high	output only when	
	(A) one input is high	(B) one inp	out is low	
	(C) two input are low	(D) all inpu	ut are high	
	Ans: D			
41.	n bits in operation code imp	ly that ther	e are	_ possible distinct
	operators (A) 2n	(B) 2n	(C) n/2	(D) n2
	Ans: B			
42.	register keeps tr	acks of the	instructions stored	I in program stored in
	memory.			
	(A) AR (Address Register)	(B) XR (Ind	dex Register)	
	(C) PC (Program Counter)	(D) AC (Ad	ccumulator)	
	Ans: C			
43.	Memory unit accessed by co	ontent is ca	lled	
	(A) Read only memory	(B) Progra	mmable Memory	
	(C) Virtual Memory	(D) Associ	ative Memory	
	Ans: D			
44.	'Aging registers' are			
	(A) Counters which indicate I referenced.	now long ag	go their associated	pages have been
	(B) Registers which keep trac	k of when t	the program was la	ist accessed.
	(C) Counters to keep track o	f last access	sed instruction.	
	(D) Counters to keep track o	f the latest	data structures re	ferred.
	Ans: A			
45	The instruction 'ORG O' is a			
	(A) Machine Instruction.	(B) Pseud	o instruction.	
	(C) High level instruction.	(D) Memo	ry instruction.	
	Ans: B			
46	Translation from symbolic pr	ogram into	Binary is done in	
	(A) Two passes. (B) Direct	ctly (C)	Three passes.	(D) Four passes.
	Ans: A			
47	A floating point number that	has a O in t	the MSB of mantis	sa is said to have
	(A) Overflow (B) Underf	low (C) I	mportant number	(D) Undefined
	Ans: B			
48	The BSA instruction is			
	(A) Branch and store accumu	ılator (B	) Branch and save i	return address
	(C) Branch and shift address	(D	) Branch and show	accumulator
	Ans: B			
49	State whether True or False.			
	(i) Arithmetic operations with compared to with floating	-		nger time for execution as
	Ans: True.			
	(ii) An arithmetic shift left mu	ultiplies a si	gned binary numb	er by 2.

	Ans: False.					
50	Logic gates wit	th a set of inpu	t and outputs	is arrangemen	t of	
	(A) Combinati	ional circuit (B)	Logic circuit	(C) Design circ	uits (D) Re	egister
	Ans: A					
51.	MIMD stands	for				
	(A) Multiple in	struction multi	iple data	(B) Multiple	instructio	n memory data
		nstruction mult				on memory data
	Ans: A		•	. , .		•
52	A k-bit field ca	n specify any o	ne of			
	(A) 3k register	rs (B) 2k ı	registers			
	(C) K2 register	s (D) K3	registers			
	Ans: B	, ,	J			
53	The time inter	val between ac	ljacent bits is o	called the		
	(A) Word-time		-	urn around tir	ne	(D) Slice time
	Ans: B	. ,	, ,			. ,
54	A group of bits	s that tell the co	omputer to pe	rform a specif	ic operati	on is known as
		n code (B) Mi		-	-	(D) Register
	Ans: A	, ,	•	, ,		. , ,
55	The load instru	uction is mostly	used to desig	nate a transfe	r from me	emory to a
	processor regi	-				•
	(A) Accumula	ntor	(B) Instructio	n Register		
	(C) Program c	ounter	(D) Memory a	address Regist	er	
	Ans: A					
56	The communic	cation between	the compone	nts in a micro	computer	takes place via
	the address ar	nd				
	(A) I/O bus	(B) Data bus	(C) Address b	ous (D) C	ontrol line	es
	Ans: B					
57	An instruction	pipeline can be	e implemented	d by means of		
	(A) LIFO buffe	er (B) FIF	O buffer	(C) Stack	(D) Non	e of the above
	Ans: B					
58	Data input cor	nmand is just t	he opposite of	fa		
	(A) Test comn	nand (B) Co	ntrol comman	d (C) Data o	utput	(D) Data channel
	Ans: C					
59	A microprogra	am sequencer				
	(A) generat	es the address	of next micro	instruction to	be execut	ed.
	(B) generat	es the control s	signals to exec	ute a microins	truction.	
	(C) sequenti	ially averages a	ll microinstruc	tions in the co	ontrol mer	nory.
	(D) enables	the efficient ha	andling of a mi	cro program s	ubroutine	! <b>.</b>
	Ans: A					
60	. A binary digit	is called a				
	(A) Bit	(B) Byte	(C) Number	(D) C	Character	
	Ans: A					

61	A flip-flop is a bina	ary cell capa	ble of storing	informatio	n of	
	(A) One bit (B)	Byte	(C) Zero bit	(D) Eight l	bit	
	Ans: A					
62	The operation exe	cuted on da	ita stored in r	egisters is c	called	
	(A) Macro-opera	tion	(B) Micro-op	eration		
	(C) Bit-operation		(D) Byte-ope	ration		
	Ans: B					
63	MRI indicates					
	(A) Memory Refer	ence Inform	nation. (B) Me	emory Refe	rence Instruc	ction.
	(C) Memory Regis	sters Instruc	tion. (D) M	emory Reg	ister informa	tion
	Ans: B					
64	Self-contained sec called	uence of in	structions tha	t performs	a given com	putational task is
	(A) Function (B)	Procedure	(C) Subroutin	ne (D	) Routine	
	Ans: A					
65	Microinstructions					
		Subroutine	(C) V	'ector	(D) Add	ress
	Ans: A					
66	An interface that p			_	nary informa	tion between
	internal storage a				mtoufooo	(D) 1/O b
	(A) I/O interface	(B) inpu	it interface (	C) Output ii	nterrace	(D) I/O bus
67	Ans: A Status bit is also ca	llod				
07	(A) Binary bit (B)		(C) Signed hit	(D) Unciar	and hit	
	Ans: B	riag bit	(C) Signed bit	(D) Ulisigi	ieu bit	
60	An address in mair	n momory is	called			
08	(A) Physical addre	•		(C) Memor	v address (D	)) Word address
	Ans: A	.33 (D) LOGI	cai addi C33	(C) WICHION	y addicss (b	y word address
69	If the value V(x) of	f the target (	onerand is co	ntained in t	he address fi	ield itself the
03	addressing mode	_	operana is coi	rtainea iir t	ire address ii	era reserr, tric
	(A) immediate.		t. (C) in	direct.	(D) implied.	
	Ans: B	. ,			. , .	
70	can be represented	d in a signed	l magnitude fo	ormat and i	in a 1's comp	lement format as
	(A) 111011 & 100	)100	(B) 100	100 & 111	.011	
	(C) 011011 & 1001	00	(D) 1001	00 & 0110	11	
	Ans: A					
71	The instructions w	hich copy in	formation fro	m one loca	tion to anoth	ner either in the
	processor's intern	_			-	
	(A) Data transfe					
		instructions	s. (D) Logica	l instructio	ns.	
	Ans: A					

72 A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called
(A) register (B) flip-flop (C) transistor. (D) counter.  Ans: D
73. The performance of cache memory is frequently measured in terms of a quantity called
(A) Miss ratio. (B) Hit ratio. (C) Latency ratio. (D) Read ratio.  Ans: C
74. The information available in a state table may be represented graphically in a (A) simple diagram. (B) state diagram. (C) complex diagram. (D) data flow diagram. Ans: B
75 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.
<ul><li>(A) relative address mode.</li><li>(B) index addressing mode.</li><li>(C) register mode.</li><li>(D) implied mode.</li></ul>
Ans: A
76 An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as
(A) DDA. (B) Serial interface. (C) BR. (D) DMA.
Ans: D
77 The 2s compliment form (Use 6 bit word) of the number 1010 is
(A) 111100. (B) 110110. (C) 110111. (D) 1011.
Ans: B
78 A register capable of shifting its binary information either to the right or the left is called a
(A) parallel register. (B) serial register. (C) shift register. (D) storage register.  Ans: C
79 What is the content of Stack Pointer (SP)?  (A) Address of the current instruction (B) Address of the next instruction
(C) Address of the top element of the stack (D) Size of the stack.  Ans: C
80 Which of the following interrupt is non maskable
(A) INTR. (B) RST 7.5. (C) RST 6.5. (D) TRAP.
Ans: D
81 Which of the following is a main memory
(A) Secondary memory. (B) Auxiliary memory.
(C) Cache memory. (D) Virtual memory.
Ans: C
82 Which of the following are not a machine instructions (A) MOV (B) ORC (C) END (D) (D) (D) (C)
(A) MOV. (B) ORG. (C) END. (D) (B) & (C) . <b>Ans: D</b>

83	83 In Assembly language programming, minimum number of operands required for an instruction is/are					
		-		(C) Two.	(D) Bot	th (B) & (C) .
	Ans: A		(=) ==.	(0)	(-,	(-) (-)
84	The ma		_	apacity of a m	icro proce	essor which uses 16 bit database &
	(A) 6	4 K.	(B) 4 GB.	(C) both (A	.) & (B) .	(D) None of these.
	Ans: B					
85	The m	emory u	ınit that comn	nunicates dire	ctly with	the CPU is called the
	(A) ma	ain mem	nory (B) S	econdary mer	mory	
	(C) sha	ared me	mory (D) a	uxiliary memo	ry.	
	Ans: A	1				
86		erage tir nts is cal	· · · · · · · · · · · · · · · · · · ·	o reach a stora	age locatio	on in memory and obtain its
		tency tir		(B) Access t		
	• •		nd time.	(D) Respons	e time.	
	Ans: B					
		True or F				
87	-	_	oup of 16 bits	•		
	Ans: F					
88		_	roup of 16 bit	S.		
	Ans: F					
89	given.		l is to be writ	ten in an asso	ciative me	emory, address has got to be
	Ans: F					
90		two equ		re subtracted,	, the resul	t would beand
		ZERO,				
91				=	an	are essential tools for writing
	_	-	y language pro	_		
02		-	ocessor, asser			at to 4 if the and as C 0 is
92		-	=	=	=	et to 1 if the end carry C 8 is
		ne, zero				
93			/D converter			
				er. (B)	-	
	• •		n speed conve	erter. (D)	none of th	iese.
	Ans: C					
94			· · · ·			he CPU to main memory by
	(A) 1/O		s. (B) C	ru. ((	) Sillit reg	gisters. (D) none of these.
06			al logic circuit	t which condo	data com	ing from a single source to two
90			ate destinatio		uata CUIII	ing from a single source to two

(A) Decoder. (B) End Ans: D	coder. (C) Multiplexe	r. (D) Demultiplexer.
97 In which addressing m	node the operand is giv	en explicitly in the instruction
_		. (C) Indirect. (D) Direct.
Ans: B	,	
98 A stack organized cor	mnuter has	
_	struction. (B) Two-add	ress Instruction
• •	` '	
• •	ruction. (D) Zero-addr	ess instruction.
Ans: D		
_		nd address part of the instruction ess in the relative address mode, when
an instruction is read		ŕ
(A) 849. (B) 85	0. (C) 801.	(D) 802.
Ans: B	,	. ,
102 A page fault		
	re is an error in a speci	fic page.
	ogram accesses a page	
		not currently in main memory.
•		belonging to another program.
Ans: C	ogram accesses a page	belonging to unother program.
	iction is mostly used to	o designate a transfer from memory to a
processor register kno		designate a transfer from memory to a
A. Accumulator		Instruction Register
C. Program counter		Memory address Register
Ans: A		,
104. A group of bits	that tell the compute	r to perform a specific operation is
known as		
A. Instruction code	В.	Micro-operation
C. Accumulator	D.	Register
Ans: A		
	val between adjacent l	
A. Word-time	В.	Bit-time
C. Turn around tim  Ans: B	e D	. Slice time
	n specify any one of	
A. 3k registers	B.	
C. K2 registers	D.	K3 registers
Ans: B	2.	
107. MIMD stands f	for	
A. Multiple instruction	on multiple data	
B. Multiple instruction	on memory data	
C. Memory instruction	on multiple data	
D. Multiple informati	ion memory data	
Ans: A		
108. Logic gates wit	th a set of input and ou	itputs is arrangement of

	Computational circuit						
B. Logic circuit							
C. Design circuits							
D. F	Register						
Ans							
_	The average time required to rea	nch a s	storage location in m	emory and obtain			
its c	ontents is called						
A.	Latency time.	B.	Access time.				
C.	Turnaround time.	D.	Response time.				
Ans	: B						
110.	The BSA instruction is						
A.	Branch and store accumulator	В.	Branch and save r	eturn address			
C.	Branch and shift address	D.	Branch and show a	accumulator			
Ans	: B						
	A floating point number that has	a O ir	n the MSB of mantiss	sa is said to			
		D	I I m d a mf l a				
	Overflow		Underflow				
	Important number	υ.	Undefined				
Ans	· <del>-</del>	:	o Dinamila dana in				
	Translation from symbolic progra			·			
	Two passes.		,				
	Three passes.	υ.	Four passes.				
Ans	• • •						
	The instruction 'ORG O' is a		Dooredo inoterration				
			Pseudo instruction				
	High level instruction.	D.	iviemory instruction	on.			
Ans	· <del>-</del>						
	'Aging registers' are	م ط <b>د</b> م	:	an a bana			
	Counters which indicate how long ag renced.	go the	ir associated pages r	lave been			
B.	Registers which keep track of wher	n the p	orogram was last acc	essed.			
C.	Counters to keep track of last acces	ssed i	nstruction.				
D.	Counters to keep track of the lates	t data	structures referred.				
Ans							
115.	Memory unit accessed by conter	nt is ca	alled				
A.	Read only memory	В.	Programmable Me	emory			
C.	Virtual Memory	D.	Associative Memo	ry			
Ans	: D						
116.	register keeps tracks	of the	instructions stored	in program stored			
in m	emory.						
A.	AR (Address Register)	В.	XR (Index Register)				
C.	PC (Program Counter)	D.	AC (Accumulator)				
Ans			,				
117.	n bits in operation code imply the	at the	re are	possible distinct			
operato			<del></del>				
Α.	2n	В.	2n				
C.	n/2	D.	n2				

Ans	: В	
118.	A three input NOR gate gives I	logic high output only when
A.	one input is high	B. one input is low
C.	two input are low	D. all input are high
Ans	: D	, -
119.	The circuit converting binary of	data in to decimal is .
	Encoder	B. Multiplexer
C.	Decoder	D.Code converter
Ans		
120.		nultiplier register of a hardware circuit
		e (11101) & (1100). The result shall be
Α.	_	B. (-12)10
	(12)10	D. (-812)10
Ans		<i>D.</i> (012)10
	PSW is saved in stack when th	pere is a
		B. execution of RST instruction
	Execution of CALL instruction	
		D. All of these
Ans		and advis as a smaller by
	In computers, subtraction is ca	- · · · · <del></del>
	•	B. 2's complement method
	•	D. BCD subtraction method
Ans		
		nal Computer (PC) is made of
	cache memory.	B. static RAM
C.	Dynamic Ram	D. bothA.and (B).
Ans		
	Cache memory works on the p	· · · · · · · · · · · · · · · · · · ·
A.	Locality of data	B. Locality of memory
C.	Locality of reference	D. Locality of reference & memory
Ans	: C	
125.	An n-bit microprocessor has	·
A.	n-bit program counter	B. n-bit address register
C.	n-bit ALU	D. n-bit instruction register
Ans	: D	
126.	When CPU is executing a Prog	gram that is part of the Operating System, it is
said	to be in	
A.	Interrupt mode	B. System mode
C.	Half mode	D. Simplex mode
Ans	: B	•
127.	Logic X-OR operation of (4ACC	O)H& (B53F)H results .
Α.	AACB	В. 0000
C.	FFFF	D. ABCD
Ans		
128.		ytes and the cache memory is of 2K words. It
		word of cache memory shall be
A.	11 bits	B. 21 bits
C.	16 bits	D. 20 bits
٠.	TO DIE	J. 20 516

An	is: C					
129.	A Stack-organised Computer uses instruction of					
A.	Indirect addressing	В.	Two-addressing			
C.	Zero addressing	D.	Index addressing			
	s: C		-			
130.	In a program using subroutine o	all inst	ruction, it is necessary .			
C.	initialize program counter Reset the microprocessor	D.	Clear the instruction register			
	is: D					
131.	Virtual memory consists of					
	Static RAM		Dynamic RAM			
	Magnetic memory	D.	•			
	s: A					
132.		sion. if	the dividend is (11100)2 and divisor is			
	0011)2 then the result is	,	(			
	(00100)2	В.	(10100)2			
	(11001)2		(01100)2			
	is: B		(======			
	Generally Dynamic RAM is used	as ma	in memory in a computer system as			
			, , a co p co cyclon ac			
		В.	has higher speed			
	has lower cell density	D.				
	s: B		,			
134.	Write Through technique is use	d in wł	nich memory for updating the data			
			,			
A.	Virtual memory	В.	Main memory			
C.	Auxiliary memory	D.	Cache memory			
An	s: D					
135.	Cache memory acts between					
A.	CPU and RAM	В.	RAM and ROM			
C.	CPU and Hard Disk	D.	None of these			
An	s: A					
136.	The circuit used to store one bit	of dat	ta is known as			
A.	Encoder	В.	OR gate			
C.	Flip Flop	D.	Decoder			
An	s: C					
137.	Von Neumann architecture is					
A.	SISD	В.	SIMD			
C.	MIMD	D.	MISD			
An	s: A					
138.	In a vectored interrupt.					
A.	the branch address is assigned to a	fixed I	ocation in memory.			
В.	the interrupting source supplies the	e branc	ch information to the processor through			
	an interrupt vector.					
C.	the branch address is obtained from	n a reg	ister in the processor			

Ans: B

139.	. In a memory-mapped I/O sy	stem, w	which of the following will not be there
A.	LDA	В.	IN
C.	ADD	D.	OUT
An	s: A		
140.	If memory access takes 20 ns w	ith cac	he and 110 ns without it, then the ratio
(ca	che uses a 10 ns memory) is		
A.		В.	90%
C.	88%	D.	87%
An	s: B		
141.	The addressing mode used in a	n instru	iction of the form ADD X Y, is
	Absolute	В.	
C.	index	D.	none of these
An	s: C		
142.	register keeps track	of the	instructions stored in program stored
	memory.		, ,
A.	AR (Address Register)	В.	XR (Index Register)
	PC (Program Counter)		
	s: C		,
143.	The idea of cache memory is ba	ased	
A.	on the property of locality of refer		
В.	on the heuristic 90-10 rule		
C.	on the fact that references general	lly tend	to cluster
D.	all of the above		
An	s: A		
144.	Which of the following is not a	weight	ed code?
	Decimal Number system	_	
C.	Binary number System	D.	None of these
	s: B		
145.	The average time required to re	each a s	storage location in memory and obtain
its	contents is called the		
A.	seek time	В.	turnaround time
C.	access time	D.	transfer time
An	s: C		
146.	(2FAOC)16 is equivalent to		
	(195 084)10	В.	(001011111010 0000 1100)2
C.	Both A.and (B)	D.	None of these
An	s: B		
147.	The circuit used to store one bi	t of dat	a is known as .
A.	Register	В.	Encoder
C.	Decoder	D.	Flip Flop
An	s: D		
148.	. Computers use addressing n	node te	chniques for .
A.			by providing facilities as pointers to
	memory counters for loop control		, , , , , , , , , , , , , , , , , , , ,
В.	to reduce no. of bits in the field of	instruct	tion
	specifying rules for modifying or in		
	All the above		

Ans: D							
149.	149. What characteristic of RAM memory makes it not suitable for permanent						
S	storage?						
Α	. too slow	В.	unreliable				
С	. it is volatile	D.	too bulky				
Α	ns: C						
150.	The amount of time required to recomposed of seek time, rotational late		block of data from a disk into memory				
	efers to .	iley,	and transfer time. Notational laterity				
	. the time its takes for the platter to m	aka a	full rotation				
	the time it takes for the read-write he						
	appropriate track						
С	. the time it takes for the platter to rot	ate tl	ne correct sector under the head				
D	. none of the above						
Α	ns: A						
151.	In computers, subtraction is gene	rally (	carried out by				
Α	. 9's complement	В.	10's complement				
C	. 1's complement	D.	2's complement				
A	ns: D						
152.	Assembly language						
а	<ul> <li>uses alphabetic codes in place of bina</li> </ul>	ary nu	ımbers used in machine language				
b	. is the easiest language to write progr	ams					
C	need not be translated into machine	langu	age				
d	. None of these						
A	ns: A						
153.	• •		nd requires 4 cycles of 250 nsecs each				
	o transfer data. The bandwidth of this b		•				
	me of the bus was reduced to 125 nsec		•				
tı	ansfer stayed the same what would the	band	dwidth of the bus?				
Α	. 1 Megabyte/sec	В.	4 Megabytes/sec				
C	. 8 Megabytes/sec	D.	2 Megabytes/sec				
A	ns: D						
154.	Floating point representation is us	sed to	o store				
Α	. Boolean values	В.	whole numbers				
C	. real integers	D.	integers				
Α	ns: C						
155.	SIMD represents an organization						
а	a. refers to a computer system capable of processing several programs at the same						
	time.						
b	<ul> <li>represents organization of single com unit and a memory unit.</li> </ul>	pute	r containing a control unit, processor				
C		tho	supervision of a common control unit				
_	none of the above.	tile .	supervision of a common control unit				
	ns: C						
156.	In Reverse Polish notation, expres	sion	A*B+C*D is written as				
Α		В.	A*BCD*+				
,	ΛP*CD+*	D.	*B*CD+				

#### Ans: A

- 157. Processors of all computers, whether micro, mini or mainframe must have
  - a. ALU b. Primary Storage
  - c. Control unit d. All of above

## Ans b

- 158. What is the control unit's function in the CPU?
  - a. To transfer data to primary storage
  - b. to store program instruction
  - c. to perform logic operations
  - d. to decode program instruction

#### Ans e

- 159. What is meant by a dedicated computer?
  - a. which is used by one person only
  - b. which is assigned to one and only one task
  - c. which does one kind of software
  - d. which is meant for application software only

#### Ans f

- 160. The most common addressing techniques employed by a CPU is
  - a. immediate b. direct
  - c. indirect d. register
    - d. register e. all of the above

## Ans d

- 161. Pipeline implement
  - a. fetch instructionb. decode instructionc. fetch operandd. calculate operand
  - e. execute instruction f. all of abve

#### Ans d

- 162. Which of the following code is used in present day computing was developed by IBM corporation?
  - a. ASCII b. Hollerith Code c. Baudot code d. EBCDIC code

#### Ans d

- 163. When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the
  - a. stack pointer b. accumulator
  - c. program counter d. stack

# Ans d

- 164. A microprogram written as string of 0's and 1's is a
  - a. symbolic microinstructionb. binary microinstructionc. symbolic microprogramd. binary microprogram

## Ans d

- 165. Interrupts which are initiated by an instruction are
  - a. internal b. external c. hardware d. software

#### Ans b

166. Memory access in RISC architecture is limited to instructions

	c. STA a	and LDA	d. MOV and	d JMP			
	A) bus	A collection of	B) peripher	al connec		is called	
168	A) micr	A complete moprocessor	B) n	nemory	consist of bove		
	A) instr	PC Program Co ruction pointer counter	B) n	nemory po	ointer		
	). A) 8 <b>Ans A</b>	In a single byt B) 16	e how man C) 4				
171			B) lo	ogic opera	tion		
	A) Long	The access tir gle CPU operat ger thanB) Sho ligible than	tion. rter than		the time	required for p	performing
<b>17</b> 3	called a	Memory addrossd addressable ddressable	B) b	yte addre	•	words and th	e machine is
174	A) Sym	A microprogra bolic microinst bolic microinst	ruction	B) bina	f 0's and 1's is a ary microinstru ary microprogr	ıction	
175	A) an a	A pipeline is li utomobile asse a a and b			ise pipeline as line		
176	A) Grea	Data hazards of ater performan line changes th	ce loss		access to ope	rands	

a. CALL and RET b. PUSH and POP

- C) Some functional unit is not fully pipelined
- D) Machine size is limited

#### Ans B

- 177. Where does a computer add and compare data?
  - A. Hard disk B. Floppy disk C. CPU chip D:Memory chip

#### Ans C

- 178. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
  - A. Memory Address Register
  - B. Memory Data Register
  - C. Instruction Register
  - D. Program Register

#### Ans D

- 179. A complete microcomputer system consists of
  - A) microprocessor
  - B) memory
  - C) peripheral equipment
  - D) all of above

#### Ans D

- 180. CPU does not perform the operation
  - A. data transfer
  - B. logic operation
  - C. arithmetic operation
  - D. all of above

# Ans B

- 181. Pipelining strategy is called implement
  - A. instruction execution
  - B. instruction prefetch
  - C. instruction decoding
  - D. instruction manipulation

# Ans C

- 182. A stack is
  - A. an 8-bit register in the microprocessor
  - B. a 16-bit register in the microprocessor
  - **C.** a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer
  - D. a 16-bit memory address stored in the program counter

#### Ans A

- 183. A stack pointer is
  - A. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.

- B. a register that decodes and executes 16-bit arithmetic expression.
- C. The first memory location where a subroutine address is stored.
- D. a register in which flag bits are stored

#### Ans A

- 184. The branch logic that provides decision making capabilities in the control unit is known as
  - A. controlled transfer
  - B. conditional transfer
  - C. unconditional transfer
  - D. none of above

#### Ans C

- 185. Interrupts which are initiated by an instruction are
  - A. internal
  - B. external
  - C. hardware
  - D. software

#### Ans D

- 186. A time sharing system imply
  - A. more than one processor in the system
  - B. more than one program in memory
  - C. more than one memory in the system
  - D. None of above

# Ans B

- 187. Virtual memory is -
- (1) an extremely large main memory
- (2) an extremely large secondary memory
- (3) an illusion of an extremely large memory
- (4) a type of memory used in super computers
- (5) None of these

Answers:

3

- 188. Fragmentation is -
- (1) dividing the secondary memory into equal sized f ragments
- (2) dividing the main memory into equal size f ragments
- (3) f ragments of memory words used in a page
- (4) f ragments of memory words unused in a page
- (5) None of these

Answers:: 2

- 189. Which memory unit has lowest access time?
- (1) Cache (2) Registers
- (3) Magnetic Disk (4) Main Memory
- (5) Pen drive

# Answer:2

- 190. Cache memory-
- (1) has greater capacity than RAM
- (2) is f aster to access than CPU Registers
- (3) is permanent storage
- (4) f aster to access than RAM
- (5) None of these

Answer 4

- 191. When more than one processes are running concurrently on a system-
- (1) batched system
- (2) real-time system
- (3) multi programming system
- (4) multiprocessing system
- (5) None of these

Answers:

3

- 192. Which of the following memories must be refreshed many times per second?
- a. Static RAM
- b. Dynamic RAM
- c. EPROM

- d. ROM
- e. None of these

ans Static RAM

193.RAM stands for

- a. Random origin money b. Random only memory
- c. Read only memory d. Random access memory
- e. None of these

ans Random access memory

- 194.CPU fetches the instruction from memory according to the value of
- a) program counter
- b) status register
- c) instruction register
- d) program status word

### Answer:a.

- 195.A memory buffer used to accommodate a speed differential is called
- a) stack pointer
- b) cache

- c) accumulator
- d) disk buffer

# Answer:b.

196. Which one of the following is the address generated by CPU?

- a) physical address
- b) absolute address
- c) logical address
- d) none of the mentioned

Answer:c.

- 197. Run time mapping from virtual to physical address is done by
- a) memory management unit
- b) CPU
- c) PCI
- d) none of the mentioned

Answer:a.

198.Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called

- a) fragmentation
- b) paging
- c) mapping
- d) none of the mentioned

Answer:b

199. The address of a page table in memory is pointed by

- a) stack pointer
- b) page table base register
- c) page register
- d) program counter

200. Program always deals with

- a) logical address
- b) absolute address
- c) physical address
- d) relative address

Answer:a

# COMPUTER ORGANIZATION AND ARCHITECTURE BCA

# **Multiple choice questions**

1.	In Reverse Polish not	ation, expression	A*B+C*D is written as				
	(A) AB*CD*+	(B) A*BCD*+	(C) AB*CD+*	(D) A*B*CD+			
	Ans: A						
2.	SIMD represents an o	_					
	(A) refers to a computime.	ter system capabl	e of processing severa	I programs at the same			
	(B) represents organiz unit and a memory		nputer containing a co	ntrol unit, processor			
	(C) includes many processing units under the supervision of a common control unit						
(D) none of the above.							
	Ans: C						
3.	Floating point represe	entation is used to	store				
	(A) Boolean values	(B) whole num	bers (C) real integ	ers (D) integers			
	Ans: C						
4.	Suppose that a bus ha		•				
			· .	es/sec. If the cycle time			
	of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?						
	(A) 1 Megabyte/sec						
	(C) 8 Megabytes/sec	, ,					
	Ans: D	. ,	, ,				
5.	Assembly language						
	(A) uses alphabetic co	odes in place of bi	nary numbers used in	machine language			
	(B) is the easiest language to write programs						
	(C) need not be translated into machine language						
	(D) None of these						
	Ans: A						
6.	In computers, subtrac	ction is generally o	arried out by				
	(A) 9's complement	(B) 10's	complement				
	(C) 1's complement	(D) 2's	complement				
	Ans: D						
7.	The amount of time r	•		•			
	composed of seek tin	ne, rotational late	ncy, and transfer time.	Rotational latency			
	(A) the time its takes	for the platter to	make a full rotation				
	• •	•	head to move into po	sition over the			
	appropriate trac		neda to move into po	sidon over the			

(C) the time it takes for the platter to rotate the correct sector under the head

(D) none of the above

	Ans: A			
8.	What characteristic	of RAM memory	makes it not suita	ble for permanent storage?
	(A) too slow (B)	unreliable	(C) it is volatile	(D) too bulky
	Ans: C			
9.	Computers use addr	essing mode tec	nniques for	
	(A) giving programm memory counte	-		ling facilities as pointers to
	(B) to reduce no. of	bits in the field	of instruction	
	(C) specifying rules	for modifying or	interpreting addr	ess field of the instruction
	(D) All the above			
	Ans: D			
10.	The circuit used to st	ore one bit of d	ata is known as	
	(A) Register  Ans: D	(B) Encoder	(C) Decode	(D) Flip Flop
11.	(2FAOC) 16 is equiva	lent to		
	(A) (195 084) 10 (C) Both (A) and (B)	` ' '	10111111010 0000 ne of these	1100) 2
	Ans: B			
12.	The average time recontents is called the	-	storage location	in memory and obtain its
	(A) seek time	(B) turnaround	d time (C) acce	ss time (D) transfer time
	Ans: C			
13.	Which of the followi	ng is not a weigh	ted code?	
	(A) Decimal Number	system	(B) Excess 3-cod	l
	(C) Binary number S	ystem	(D) None of the	se
	Ans: B			
14.	The idea of cache me	emory is based		
				on the heuristic 90-10 rule r (D) all of the above
	Ans: A			
15.	Which of the followi	ng is lowest in m	emory hierarchy?	
	(A) Cache memory			
	(B) Secondary memo	ry		
	(C) Registers			
	(D) RAM			
	` '	emory		
	Alis (b) Secondary III	emory		
16.	The addressing mode	e used in an inst	ruction of the forn	n ADD X Y, is
	(A) Absolute	(B) indirect	(C) index	(D) none of these
	Ans: C			
17.			ache and 110 ns w	ith out it, then the ratio (
	Ans: C	e used in an inst (B) indirect kes 20 ns with ca	(C) index	(D) none of these

(A) 93% <b>Ans:</b> B	(B) 90%	(C) 88%	(D) 87%		
	v-mapped I/O	svstem. which	of the following	will not	be there?
(A) LDA	(B) IN	(C) ADD	(D) OUT		
Ans: A	. ,	( )	. ,		
19. In a vectore	d interrupt.				
(A) the branch	address is assi	gned to a fixed	d location in mem	ory.	
(B) the interru an interru	-	ipplies the bra	nch information t	o the pr	ocessor through
(C) the branch	address is obta	ined from a re	egister in the proc	essor	
(D) none of the	above				
Ans: B					
20. Von Neuma	nn architecture	e is			
(A) SISD	(B) SIMD	(C) MIMD	(D) MISD		
Ans: A					
21. The circuit u		ne bit of data i	s known as		
(A) Encode	r (B) (	OR gate	(C) Flip Flop		(D) Decoder
Ans: C					
22. Cache mem	-				
	RAM (B) R	AM and ROM	(C) CPU and Ha	rd Disk	(D) None of these
Ans: A					
	-		h memory for upo	lating tr	ie data
(A) Virtual r	•	• •	memory		
	, memory	(D) Cach	e memory		
Ans: D	unamic DAM is	usod as main	memory in a com	nutor sv	estam as it
	es less power		-	puter sy	stem as it
, ,	•		efreshing circuita	rv	
Ans: B	ir cell delisity	(D) ficcus i	circaining circuita	' y	
	agnitude binar	v division, if th	e dividend is (111	00) 2 ar	nd divisor is
_	en the result is	•	ie aiviaena is (111	.00, <b>2</b> ui	14 4111301 13
(A) (00100			(C) (11001) 2	(D) (	(01100) 2
Ans: B		•			
26. Virtual mem	ory consists of	:			
(A) Static R	ΔM	(B) Dynai	mic RAM		
(C) Magnet	ic memory	(D) None	of these		
Ans: A					
27. In a progran	n using subrou	tine call instru	ction, it is necessa	ary	
(A) initialise	program coun	ter (B)	Clear the accumu	lator	
(C) Reset the	e microprocess	or (D)	Clear the instruct	ion regis	ster
Ans: D					
28. A Stack-org	anised Comput	ter uses instru	ction of		

(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressin
Ans: C
29. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be <ul> <li>(A) 11 bits</li> <li>(B) 21 bits</li> <li>(C) 16 bits</li> <li>(D) 20 bits</li> </ul> Ans: C
30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit
(A) $n TQD = \bullet$ (B) $T D =$ (C) $D = T \cdot Q n$ (D) $n TQD = \bigoplus$
Ans: D
31. Logic X-OR operation of (4ACO) H & (B53F) H results  (A) AACB  (B) 0000  (C) FFFF  (D) ABCD  Ans: C
32. When CPU is executing a Program that is part of the Operating System, it is said to
be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mode  Ans: B
33. An n-bit microprocessor has
(A) n-bit program counter (B) n-bit address register
(C) n-bit ALU (D) n-bit instruction register
Ans: D
34. Cache memory works on the principle of
(A) Locality of data (B) Locality of memory
(C) Locality of reference (D) Locality of reference & memory
Ans: C
35. The main memory in a Personal Computer (PC) is made of
(A) cache memory. (B) static RAM
(C) Dynamic Ram (D) both (A) and (B).
Ans: D
36. In computers, subtraction is carried out generally by
(A) 1's complement method (B) 2's complement method
(C) signed magnitude method (D) BCD subtraction method
Ans: B
37. PSW is saved in stack when there is a
(A) interrupt recognised (B) execution of RST instruction
(C) Execution of CALL instruction (D) All of these
Ans: A
38. The multiplicand register & multiplier register of a hardware circuit implementing
booth's algorithm have (11101) & (1100). The result shall be
(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10
Ans: A
39. The circuit converting binary data in to decimal is
(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter
Ans: D

40.	A tilree iliput NOR gate give:	s logic fligh	output only when	
	(A) one input is high	(B) one in	put is low	
	(C) two input are low	(D) all inp	ut are high	
	Ans: D			
41.	n bits in operation code imp	ly that the	re are	_ possible distinct
	operators (A) 2n	(B) 2n	(C) n/2	(D) n2
	Ans: B			
42.	register keeps tr	acks of the	instructions stored	d in program stored in
	memory.			
	(A) AR (Address Register)	(B) XR (In	dex Register)	
	(C) PC (Program Counter)	(D) AC (A	ccumulator)	
	Ans: C			
43.	Memory unit accessed by co	ontent is ca	alled	
	(A) Read only memory	(B) Progra	mmable Memory	
	(C) Virtual Memory	(D) Assoc	iative Memory	
	Ans: D			
44.	'Aging registers' are			
	(A) Counters which indicate hereferenced.	now long a	go their associated	pages have been
	(B) Registers which keep trac	k of when	the program was la	ast accessed.
	(C) Counters to keep track of	f last acces	sed instruction.	
	(D) Counters to keep track o	f the latest	: data structures re	ferred.
	Ans: A			
45	The instruction 'ORG O' is a			
	(A) Machine Instruction.	(B) Pseud	lo instruction.	
	(C) High level instruction.	(D) Memo	ory instruction.	
	Ans: B		•	
46	Translation from symbolic pr	ogram into	Binary is done in	
	(A) Two passes. (B) Direct			(D) Four passes.
	Ans: A		·	
47	A floating point number that	has a O in	the MSB of mantis	sa is said to have
	= *			(D) Undefined
	Ans: B		•	
48	The BSA instruction is			
	(A) Branch and store accumu	ılator (E	B) Branch and save	return address
	(C) Branch and shift address	(E	) ) Branch and show	, accumulator
	Ans: B	·	•	
49	State whether True or False.			
	(i) Arithmetic operations with	h fixed poi	nt numbers take lo	nger time for execution as
	compared to with floating	g point nui	mbers.	
	Ans: True.			
	(ii) An arithmetic shift left mu	ultiplies a s	igned binary numb	er by 2.

	Ans: False.					
50	Logic gates with a set of input and outputs is arrangement of					
	(A) Combination	onal circuit (B)	Logic circuit	(C) Design circ	cuits (D) Re	egister
	Ans: A					
51.	MIMD stands	for				
	(A) Multiple ins	struction multi	ple data	(B) Multiple	instructio	n memory data
	(C) Memory in	struction mult	iple data	(D) Multiple	informati	on memory data
	Ans: A					•
52	A k-bit field car	n specify any o	ne of			
	(A) 3k register	s (B) 2k ı	egisters			
	(C) K2 registers	(D) K3	registers			
	Ans: B					
53	The time interval between adjacent bits is called the					
	(A) Word-time	(B) Bit-	time (C) T	urn around tii	me	(D) Slice time
	Ans: B					
54	A group of bits	that tell the co	omputer to pe	rform a specif	ic operati	on is known as
	(A) Instruction	code (B) Mi	cro-operation	(C) Accumula	ator	(D) Register
	Ans: A					
55	The load instru	ction is mostly	used to desig	nate a transfe	r from me	emory to a
	processor regis	ster known as				
	(A) Accumulat	tor	(B) Instruction	n Register		
	(C) Program co	ounter	(D) Memory a	address Regist	er	
	Ans: A					
56	The communic the address an		the compone	ents in a micro	computer	takes place via
	(A) I/O bus		(C) Address h	ous (D) C	ontrol line	ıς
	Ans: B	(5) 2 ata 2 a	(0) / (00)	(2) 0	011610111116	
57	An instruction	pipeline can be	e implemente	d by means of		
0.	(A) LIFO buffe	•	D buffer	(C) Stack	(D) Nor	e of the above
	Ans: B	(=, : : :		(5, 550.50	(= )	
58	Data input com	nmand is iust t	he opposite of	f a		
	(A) Test comm	-	ntrol comman		utput	(D) Data channel
	Ans: C	, ,		. ,	•	. ,
59	A microprogra	m sequencer				
	(A) generate	es the address	of next micro	instruction to	be execut	ed.
	(B) generates the control signals to execute a microinstruction.					
	· · · -	ally averages a	_			nory.
		he efficient ha				•
	Ans: A		J	. 0		
60	. A binary digit i	s called a				
		(B) Byte	(C) Number	(D) (	Character	
	Ans: A					

61	61 A flip-flop is a binary cell capable of sto	oring information of					
	(A) One bit (B) Byte (C) Zero	o bit (D) Eight bit					
	Ans: A						
62	62 The operation executed on data stored in registers is called						
	(A) Macro-operation (B) Micr	cro-operation					
	(C) Bit-operation (D) Byte-	e-operation					
	Ans: B						
63	63 MRI indicates						
	(A) Memory Reference Information. (E	B) Memory Reference Instruction.					
	(C) Memory Registers Instruction. (	(D) Memory Register information					
	Ans: B						
64	64 Self-contained sequence of instruction called	ns that performs a given computational task is					
	(A) Function (B) Procedure (C) Subr	routine (D) Routine					
	Ans: A						
65		ol memory groups, with each group specifying a					
	(A) Routine (B) Subroutine	(C) Vector (D) Address					
	Ans: A						
66	•	or transferring binary information between					
	internal storage and external devices is called						
	, , ,	(A) I/O interface (B) Input interface (C) Output interface (D) I/O bus					
67	Ans: A						
67	67 Status bit is also called	ad hit (D) Unsigned hit					
	(A) Binary bit (B) Flag bit (C) Signed Ans: B	ed bit (b) offsighed bit					
68	68 An address in main memory is called						
00	•	ess (C) Memory address (D) Word address					
	Ans: A	ess (c) Wellioty address (b) Word address					
69		l is contained in the address field itself, the					
03	addressing mode is	is contained in the address field itself, the					
	(A) immediate. (B) direct. (	(C) indirect. (D) implied.					
	Ans: B	., .					
70	70 can be represented in a signed magnitu	ude format and in a 1's complement format as					
		s) 100100 & 111011					
	(C) 011011 & 100100 (D)	100100 & 011011					
	Ans: A						
71	71 The instructions which copy informatio	on from one location to another either in the					
	processor's internal register set or in the external main memory are called						
	(A) Data transfer instructions. (B) Program control instructions.						
	(C) Input-output instructions. (D) Logical instructions.						
	Ans: A						

72 A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called	
(A) register (B) flip-flop (C) transistor. (D) counter.  Ans: D	
73. The performance of cache memory is frequently measured in terms of a quanti called	ty
(A) Miss ratio. (B) Hit ratio. (C) Latency ratio. (D) Read ratio.  Ans: C	
74. The information available in a state table may be represented graphically in a (A) simple diagram. (B) state diagram. (C) complex diagram. (D) data flow diagrams: B	ram.
75 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.	1
<ul><li>(A) relative address mode.</li><li>(B) index addressing mode.</li><li>(C) register mode.</li><li>(D) implied mode.</li></ul>	
Ans: A	
76 An interface that provides I/O transfer of data directly to and form the memory and peripheral is termed as	unit
(A) DDA. (B) Serial interface. (C) BR. (D) DMA.	
Ans: D	
77 The 2s compliment form (Use 6 bit word) of the number 1010 is	
(A) 111100. (B) 110110. (C) 110111. (D) 1011.	
Ans: B	ic
78 A register capable of shifting its binary information either to the right or the left called a	IS
(A) parallel register. (B) serial register. (C) shift register. (D) storage register.	
Ans: C  70. What is the content of Stack Pointer (SD)?	
79 What is the content of Stack Pointer (SP)?  (A) Address of the current instruction (B) Address of the next instruction	
(C) Address of the top element of the stack (D) Size of the stack.  Ans: C	
80 Which of the following interrupt is non maskable	
(A) INTR. (B) RST 7.5. (C) RST 6.5. (D) TRAP.	
Ans: D	
81 Which of the following is a main memory	
(A) Secondary memory. (B) Auxiliary memory.	
(C) Cache memory. (D) Virtual memory.  Ans: C	
82 Which of the following are not a machine instructions (A) MOV. (B) ORG. (C) END. (D) (B) & (C).	
Ans: D	

83	In Assemb instructio		progran	nming, minim	ium num	ber of operands required for an
	(A) Zer	-	ne.	(C) Two.	(D) Bo	th (B) & (C) .
	Ans: A	(-, -		(0)	(-,	(=) (=)
84		num addre ress base i		acity of a mid	cro proce	essor which uses 16 bit database &
	(A) 64 K	(B) 4 (	GB.	(C) both (A)	& (B).	(D) None of these.
	Ans: B					
85	The memo	ory unit tha	it commu	ınicates direc	tly with	the CPU is called the
	(A) main	memory	(B) Sed	condary mem	nory	
	(C) shared	memory	(D) aux	ciliary memor	·y.	
	Ans: A					
86	The average contents i	-	uired to	reach a stora	ge locati	on in memory and obtain its
	(A) Laten	-		(B) Access ti		
	` '	round time	e.	(D) Response	e time.	
	Ans: B					
	State True					
87	•	a group of	16 bits.			
	Ans: False		C 4 C 1 !!			
88		s a group o	f 16 bits.			
00	Ans: False					
89	given.		e writte	n in an assoc	iative me	emory, address has got to be
	Ans: False					
90		equal nun 	nbers are	subtracted,	the resu	lt would beand
		O, -ZERO.	•			
91			=	= =	n	_are essential tools for writing
	_	mbly langu				
02		roprocesso	-			
92	=	=	-		=	set to 1 if the end carry C 8 is
	Ans: One,					
93		ve A/D con				
		-				ed converter.
	` '	dium spee	d convert	ter. (D) n	one of th	nese.
	Ans: C					
94						he CPU to main memory by
	(A) 1/O de <b>Ans: C</b>	VICES.	(B) CPC	). (C)	siiiit re	gisters. (D) none of these.
06		ational logi	c circuit v	which condc	lata com	ing from a single source to two
90		eparate de			iala CUIII	ing from a single source to two

(A) Decoder. (B)  Ans: D	Encoder. (C) Multip	olexer	r. (D) Demultiplexer.
97 In which addressin	g mode the operand	is giv	en explicitly in the instruction
(A) Absolute.		_	. (C) Indirect. (D) Direct.
Ans: B	· /		( )
98 A stack organized	computer has		
_	Instruction. (B) Two	-24d	ress Instruction
, ,	• •		
• •	nstruction. (D) Zero-	auure	ess mstruction.
Ans: D			
contains the numb	er 24. The effective a	addre	nd address part of the instruction ess in the relative address mode, when
	ad from the memory		
(A) 849. (B)	850. (C) 801.		(D) 802.
Ans: B			
102 A page fault			
(A) Occurs when t	there is an error in a s	specit	fic page.
(B) Occurs when a	a program accesses a	page	e of main memory.
(C) Occurs when a	program accesses a	page	not currently in main memory.
(D) Occurs when a	program accesses a	page	belonging to another program.
Ans: C			
103. The load in:	struction is mostly us	sed to	designate a transfer from memory to
processor register			,
A. Accumulator		В.	Instruction Register
C. Program count	ter	D.	Memory address Register
Ans: A			
A group of	bits that tell the com	puter	r to perform a specific operation is
known as			
A. Instruction cod	de	В.	·
C. Accumulator		D.	Register
Ans: A			9-1-10-10-1
	terval between adjac		pits is called the
A. Word-time C. Turn around t	tima	B. D.	Bit-time . Slice time
Ans: B	.iiie	D.	. Slice tille
	can specify any one	of	
A. 3k registers	can specify any one	В.	
C. K2 registers		D.	K3 registers
Ans: B		٥.	No registers
	ds for .		
A. Multiple instru			
· · · · · · · · · · · · · · · · · · ·	ction memory data		
C. Memory instru			
•	nation memory data		
Ans: A			
108. Logic gates	with a set of input ar	nd ou	itputs is arrangement of

	Computational circuit					
B. L	ogic circuit					
C. D	esign circuits					
D. F	Register					
Ans	: A					
109.	The average time required to rea	ach a s	storage location in memory and obtain			
its c	ontents is called					
A.	Latency time.	B.	Access time.			
C.	Turnaround time.	D.	Response time.			
Ans	: B					
110.	The BSA instruction is					
A.	Branch and store accumulator	В.	Branch and save return address			
C.	Branch and shift address	D.	Branch and show accumulator			
Ans	: B					
	A floating point number that has	a O ir	n the MSB of mantissa is said to			
	e	D	Lie de affec.			
	Overflow		Underflow			
	Important number	D.	Undefined			
Ans	· <del>-</del>	om int	a Dinany is dono in			
	Translation from symbolic progra		· ————			
	Two passes.		•			
Ans:	Three passes.	υ.	Four passes.			
	The instruction 'ORG O' is a					
	Machine Instruction.		Pseudo instruction.			
	High level instruction.					
Ans:		υ.	Memory instruction.			
_	'Aging registers' are					
	Counters which indicate how long ag	n the	ir associated nages have been			
	renced.	50 1110	ii ussociatea pages nave been			
	B. Registers which keep track of when the program was last accessed.					
C.	Counters to keep track of last acce	-	_			
D.	Counters to keep track of the lates					
Ans	-	0.0.00				
115.		nt is ca	alled .			
	Read only memory	В.				
C.	Virtual Memory	D.	Associative Memory			
Ans	•		,			
116.	register keeps tracks	of the	e instructions stored in program stored			
in m	emory.					
A.	AR (Address Register)	В.	XR (Index Register)			
C.	PC (Program Counter)		AC (Accumulator)			
Ans	: C					
117.	n bits in operation code imply th	at the	re are possible distinct			
operato	rs.					
A.	2n	В.	2n			
C.	n/2	D.	n2			

Ans	: B		
118.	A three input NOR gate gives logi	c hi	igh output only when
A.	one input is high	В	3. one input is low
C.	two input are low	D	o. all input are high
Ans	-		
119.	The circuit converting binary data	in i	to decimal is .
	Encoder		. Multiplexer
C.	Decoder		Code converter
Ans	: D		
120.	The multiplicand register & multi	plie	er register of a hardware circuit
imp		-	01) & (1100). The result shall be
-	(812)10		. (-12)10
	(12)10		. (-812)10
	: A		
	PSW is saved in stack when there	is a	a .
	interrupt recognized		
	Execution of CALL instruction		
Ans		٠.	7 iii or tirese
	In computers, subtraction is carri	ed c	out generally by
	1's complement method		
	signed magnitude method		
Ans	_		b. Beb subtraction method
_	The main memory in a Personal C	`om	nuter (PC) is made of
			B. static RAM
	Dynamic Ram		bothA.and (B).
Ans	•	υ.	. DottiA.alia (b).
_	Cache memory works on the prin	cinl	lo of
	-	-	. Locality of memory
	Locality of reference		Locality of reference & memory
Ans		υ.	. Locality of reference & memory
	An n-bit microprocessor has		
_			n hit addrace register
Α.			3
C.		).	n-bit instruction register
Ans		a +b	eat is part of the Operating System it is
126.		n un	nat is part of the Operating System, it is
	to be in	D	Contain and
Α.	•	B.	,
		D.	Simplex mode
Ans		0 /5	DEGENI II.
	Logic X-OR operation of (4ACO)H		
Α.	AACB B.		0000
C.	FFFF D.	•	ABCD
Ans			1.1
128.			nd the cache memory is of 2K words. It
	s associative mapping. Then each wo		
Α.	11 bits	В.	
C.	16 bits	D.	. 20 bits

An	s: C		
129.	A Stack-organised Computer use	s inst	ruction of
A.	Indirect addressing	В.	Two-addressing
	Zero addressing		Index addressing
An	s: C		
130.	In a program using subroutine ca	II inst	truction, it is necessary .
	initialize program counter		·
	Reset the microprocessor		
	s: D		· ·
131.	Virtual memory consists of		
			Dynamic RAM
C.			None of these
	s: A		
132.	In signed-magnitude binary divisi	ion, if	the dividend is (11100)2 and divisor is
	011)2 then the result is	·	, ,
	(00100)2	В.	(10100)2
	(11001)2		(01100)2
	s: B		,
133.	Generally Dynamic RAM is used a	as ma	in memory in a computer system as
	·		, , ,
	Consumes less power	В.	has higher speed
	has lower cell density		needs refreshing circuitry
	s: B		,
134.	Write Through technique is used	in wh	nich memory for updating the data
			, ,
A.	Virtual memory	В.	Main memory
C.	Auxiliary memory	D.	Cache memory
An	s: D		
135.	Cache memory acts between		
A.	CPU and RAM	В.	RAM and ROM
C.	CPU and Hard Disk	D.	None of these
An	s: A		
136.	The circuit used to store one bit	of dat	ta is known as
A.	Encoder	В.	OR gate
C.	Flip Flop	D.	Decoder
An	s: C		
137.	Von Neumann architecture is		
A.	SISD	В.	SIMD
C.	MIMD	D.	MISD
An	s: A		
138.	In a vectored interrupt.		
A.	the branch address is assigned to a f	ixed l	ocation in memory.
	_		ch information to the processor through
	an interrupt vector.		
C.	the branch address is obtained from	a reg	ister in the processor
	none of the above	0	,
	s: B		

139.	. In a memory-mappe	ed I/O system, w	nich of the following will not be there?
Δ	A. LDA	В.	IN
C	C. ADD	D.	OUT
Δ	Ans: A		
140.	If memory access takes	s 20 ns with cacl	ne and 110 ns without it, then the ratio
(	cache uses a 10 ns memory) i		
	A. 93%	В.	90%
C	2. 88%	D.	87%
Δ	Ans: B		
141.	The addressing mode u	used in an instru	ction of the form ADD X Y, is
	A. Absolute	В.	indirect
	C. index	D.	
	Ans: C		
		ens track of the	instructions stored in program stored
	n memory.	spo track or tire	motractions stored in program stored
	A. AR (Address Register)	В	XR (Index Register)
	C. PC (Program Counter)		
	Ans: C	Б.	AC (Accumulator)
	The idea of cache mem	ory is based	
	a. on the property of locality	-	<u> </u>
	<ol> <li>on the heuristic 90-10 rule</li> </ol>		
	c. on the fact that references		to cluster
	of the above	generally tenu	to cluster
	Ans: A		
_		is not a waight	Codes be
	Which of the following	_	
	A. Decimal Number system		
	C. Binary number System	D.	None of these
_	Ans: B	:	tanana la antion in manual and alatain
	_		torage location in memory and obtain
	ts contents is called the	_	turno ano una ditima o
_	A. seek time	В.	turnaround time
C		D.	transfer time
	\ns: C		
146.	, , ,		(004044444040,0000,4400)2
	A. (195 084)10	В.	(001011111010 0000 1100)2
C		D.	None of these
-	Ans: B		
147.		e one bit of dat	<del></del>
Δ	A. Register	В.	Encoder
C	C. Decoder	D.	Flip Flop
Δ	Ans: D		
148.	. Computers use addi	ressing mode te	chniques for
Δ	<ul> <li>giving programming versat memory counters for loop</li> </ul>	•	by providing facilities as pointers to
В	3. to reduce no. of bits in the		ion
			ng address field of the instruction
	). All the above	5	

Αı	ns: D						
149.	149. What characteristic of RAM memory makes it not suitable for permanent						
st	storage?						
A.	too slow	В.	unreliable				
C.	it is volatile	D.	too bulky				
Αı	ns: C						
	composed of seek time, rotational late		block of data from a disk into memory and transfer time. Rotational latency				
re	fers to						
A.	the time its takes for the platter to ma	ake a	full rotation				
В.	the time it takes for the read-write he appropriate track	ad to	move into position over the				
C.	the time it takes for the platter to rota	ate th	ne correct sector under the head				
D.	none of the above						
Aı	ns: A						
151.	In computers, subtraction is gener	ally o	carried out by				
A.	9's complement	B.	10's complement				
C.	1's complement	D.	2's complement				
ıΑ	ns: D						
152.	Assembly language						
a.	uses alphabetic codes in place of bina	ry nu	mbers used in machine language				
b.	is the easiest language to write progra	ams					
C.	need not be translated into machine I	angu	age				
d.	None of these						
	ns: A						
153.	• •		nd requires 4 cycles of 250 nsecs each				
	transfer data. The bandwidth of this bu						
	ne of the bus was reduced to 125 nsecs						
tra	ansfer stayed the same what would the	band					
A.	1 Megabyte/sec	В.	4 Megabytes/sec				
C.	8 Megabytes/sec	D.	2 Megabytes/sec				
	ns: D						
154.	Floating point representation is us	ed to					
A.	Boolean values	В.	whole numbers				
C.	real integers	D.	integers				
Aı	ns: C						
155.	SIMD represents an organization t						
a.	a. refers to a computer system capable of processing several programs at the same						
	time.						
b.	represents organization of single com unit and a memory unit.	pute	containing a control unit, processor				
c.	includes many processing units under	the s	supervision of a common control unit				
d.	none of the above.						
Ar	ns: C						
156.	In Reverse Polish notation, expres	sion	A*B+C*D is written as				
A.	AB*CD*+	B.	A*BCD*+				
_	Λ D * C D ⊥ *	D	V*D*CD+				

#### Ans: A

- 157. Processors of all computers, whether micro, mini or mainframe must have
  - a. ALU b. Primary Storage
  - c. Control unit d. All of above

## Ans b

- 158. What is the control unit's function in the CPU?
  - a. To transfer data to primary storage
  - b. to store program instruction
  - c. to perform logic operations
  - d. to decode program instruction

#### Ans e

- 159. What is meant by a dedicated computer?
  - a. which is used by one person only
  - b. which is assigned to one and only one task
  - c. which does one kind of software
  - d. which is meant for application software only

#### Ans f

- 160. The most common addressing techniques employed by a CPU is
  - a. immediate b. direct
  - c. indirect d. register e. all of the above

## Ans d

- 161. Pipeline implement
  - a. fetch instructionb. decode instructionc. fetch operandd. calculate operand
  - e. execute instruction f. all of abve

#### Ans d

- 162. Which of the following code is used in present day computing was developed by IBM corporation?
  - a. ASCII b. Hollerith Code c. Baudot code d. EBCDIC code

#### Ans d

- 163. When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the
  - a. stack pointer b. accumulator
  - c. program counter d. stack

# Ans d

- 164. A microprogram written as string of 0's and 1's is a
  - a. symbolic microinstructionb. binary microinstructionc. symbolic microprogramd. binary microprogram

## Ans d

- 165. Interrupts which are initiated by an instruction are
  - a. internal b. external c. hardware d. software

# Ans b

166. Memory access in RISC architecture is limited to instructions

	STA and LDA ns c	d. MOV and JN	ИΡ
A) C)		B) peripheral of	nects several devices is called connection wires res
C)	A complete m ) microprocessor ) peripheral equipm ns D	B) mer	•
C)	PC Program Co ) instruction pointer ) data counter ns A	B) mer	
A)	In a single byt ) 8 B) 16 ns <b>A</b>	=	ts will be there? D) 32
C)		B) logic	•
A) C)	The access tingle CPU operate  ) Longer thanB) Show  ) Negligible than  ns A	tion. rter than	s the time required for performing
173.	Memory addr	ess refers to th	e successive memory words and the machine is
A) C)	alled as) word addressable bit addressable ns A		e addressable a byte addressable
C)	A microprogra ) Symbolic microinst ) symbolic microinst ns D	ruction	tring of 0's and 1's is a B) binary microinstruction D) binary microprogram
C)	A pipeline is li ) an automobile asse ) both a and b ns A	ke embly line	B) house pipeline D) a gas line
	) Greater performan		d/write access to operands

a. CALL and RET b. PUSH and POP

- C) Some functional unit is not fully pipelined
- D) Machine size is limited

#### Ans B

- 177. Where does a computer add and compare data?
  - A. Hard disk B. Floppy disk C. CPU chip D:Memory chip

#### Ans C

- 178. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
  - A. Memory Address Register
  - B. Memory Data Register
  - C. Instruction Register
  - D. Program Register

#### Ans D

- 179. A complete microcomputer system consists of
  - A) microprocessor
  - B) memory
  - C) peripheral equipment
  - D) all of above

#### Ans D

- 180. CPU does not perform the operation
  - A. data transfer
  - B. logic operation
  - C. arithmetic operation
  - D. all of above

# Ans B

- 181. Pipelining strategy is called implement
  - A. instruction execution
  - B. instruction prefetch
  - C. instruction decoding
  - D. instruction manipulation

# Ans C

- 182. A stack is
  - A. an 8-bit register in the microprocessor
  - B. a 16-bit register in the microprocessor
  - **C.** a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer
  - D. a 16-bit memory address stored in the program counter

### Ans A

- 183. A stack pointer is
  - A. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.

- B. a register that decodes and executes 16-bit arithmetic expression.
- C. The first memory location where a subroutine address is stored.
- D. a register in which flag bits are stored

#### Ans A

- 184. The branch logic that provides decision making capabilities in the control unit is known as
  - A. controlled transfer
  - B. conditional transfer
  - C. unconditional transfer
  - D. none of above

### Ans C

- 185. Interrupts which are initiated by an instruction are
  - A. internal
  - B. external
  - C. hardware
  - D. software

#### Ans D

- 186. A time sharing system imply
  - A. more than one processor in the system
  - B. more than one program in memory
  - C. more than one memory in the system
  - D. None of above

# Ans B

- 187. Virtual memory is -
- (1) an extremely large main memory
- (2) an extremely large secondary memory
- (3) an illusion of an extremely large memory
- (4) a type of memory used in super computers
- (5) None of these

Answers:

3

- 188. Fragmentation is -
- (1) dividing the secondary memory into equal sized f ragments
- (2) dividing the main memory into equal size f ragments
- (3) f ragments of memory words used in a page
- (4) f ragments of memory words unused in a page
- (5) None of these

Answers:: 2

- 189. Which memory unit has lowest access time?
- (1) Cache (2) Registers
- (3) Magnetic Disk (4) Main Memory
- (5) Pen drive

# Answer:2

- 190. Cache memory-
- (1) has greater capacity than RAM
- (2) is f aster to access than CPU Registers
- (3) is permanent storage
- (4) f aster to access than RAM
- (5) None of these

Answer 4

- 191. When more than one processes are running concurrently on a system-
- (1) batched system
- (2) real-time system
- (3) multi programming system
- (4) multiprocessing system
- (5) None of these

Answers:

3

- 192. Which of the following memories must be refreshed many times per second?
- a. Static RAM
- b. Dynamic RAM
- c. EPROM

- d. ROM
- e. None of these

ans Static RAM

193.RAM stands for

- a. Random origin money b. Random only memory
- c. Read only memory d. Random access memory
- e. None of these

ans Random access memory

- 194.CPU fetches the instruction from memory according to the value of
- a) program counter
- b) status register
- c) instruction register
- d) program status word

### Answer:a.

- 195.A memory buffer used to accommodate a speed differential is called
- a) stack pointer
- b) cache

- c) accumulator
- d) disk buffer

# Answer:b.

196. Which one of the following is the address generated by CPU?

- a) physical address
- b) absolute address
- c) logical address
- d) none of the mentioned

Answer:c.

- 197. Run time mapping from virtual to physical address is done by
- a) memory management unit
- b) CPU
- c) PCI
- d) none of the mentioned

Answer:a.

198.Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called

- a) fragmentation
- b) paging
- c) mapping
- d) none of the mentioned

Answer:b

199. The address of a page table in memory is pointed by

- a) stack pointer
- b) page table base register
- c) page register
- d) program counter

200. Program always deals with

- a) logical address
- b) absolute address
- c) physical address
- d) relative address

Answer:a

What fraction of the execution time involves code that is parallel to achieve an overall speedup of 2. Assume 10 numbers of parallel processors? \*

2.3.A doctor in a hospital observes that on average 10 patients per hour "/1 arrive and there are typically 4 patient in the hospital. What is the average range of time each patient spend in the hospital? \*



<b>✓</b>	Which registers are responsible in cpu when data transmission is takes place between cpu and memory. *	1/1
0	PC	
0	IR	
0	I/O AR	
•	non of the above	<b>✓</b>

✓ Which registers are responsible in cpu when data transmission is takes 1/1 place between cpu and I/O. \*

- ) I/OAR
- O I/OBR
- only first
- both first and second

✓ Which action is not performed by the processor *	1/1
processor-memory	
processor - I/O	
dataprocessing	
control	
non of the above	<b>✓</b>

✓ In the cpu which register value always increment whenever each instruction fetch from memory *	1/1
○ IR	
○ MAR	
● PC	<b>✓</b>
O I/OBR	

✓ Instruction cycle contain *	1/1
Fetch cycle	
Execute cycle	
both 1st and 2nd	<b>✓</b>
none	

✓ Fetch the operand from memory or read it in from I/O is called *	1/1
data operation	
instruction fetch	
operand fetch	<b>✓</b>
operand store	

- vaccum tube
- O vlsi
- transistor
- O ul:

- data processing
- data storage
- pipelining
- control

In second generation of computer which technology was used. *	1/1
o vaccum tube	
○ vlsi	
transistor	<b>✓</b>
ulsi	

✓ Which is not a function of computer *	1/1
O data processing	
O data storage	
pipelining	<b>~</b>
control	

<b>✓</b>	Mechanism that provides communication between cpu, memory and I/O 1/1 in computer is *
0	internal bus
•	system bus
0	address bus
0	none

ALU

Registers

Control unit

Cache

✓ Which is not a ARM product \* 1/1 CORTEX-A50 CORTEM-M **CORTEX-N** 

CORTEX-M4

YES

ON (

O I do not know

Correct answer

No

The collection of paths connecting the various modules is called computer system. *	in 1/1
Cable	
flat path	
interconnection structure	<b>✓</b>
none	

<b>✓</b>	Interrupts initiated by an instruction is called as	. *	1/1
	Internal		
$\cup$	internal		
	External		<b>✓</b>
0	hardware		
0	Software		

✓ Which is not a control line signal *	1/1
Clock	
bus grant	
transfer ACK	
data transfer	<b>✓</b>

✓ Data lines collectively called *	1/1
ontrol bus	
address bus	
data bus	<b>✓</b>

power distribution bus

✓ Which is not a part of cloud services. *	1/1
saas	
O paas	
jaas	<b>✓</b>
iaas	

Among the techniques which is not followed during design of microprocessor \*

1/1

pipelining

branch prediction

data flow analysis

performance balance

<b>✓</b>	Which is not belongs to QPI architecture layer *	1/1
0	physical	
$\bigcirc$	link	
$\bigcirc$	protocol	
<b>O</b>	transaction	<b>✓</b>

- multiple direct connections
- layered protocol architecture
- packetized data transfer
- interrupt request

<b>✓</b>	By increasing of clock speed and logic density in the chip which factor is not a obstacles in the computer system *	1/1
	nower	
$\cup$	power	
0	rc delay	
•	processor speed	/
0	memory latency	

In computer system GPUs stand for*	

1/1

- graphics protocol units
- geographic position units
- gyroscopic processing units
- none of the above

Amdahl's law states that the maximum speedup S achievable by a parallel1/1 computer with 'p' processors is given by: \*

- S≤f+(1-f)/p
- S≤f/p+(1-f)
- $S \le 1/[f+(1-f)/p]$
- S≤1/[1-f+f/p]

- by using wider data path
- including cache in DRAM chip
- incorporating complex and efficient cache structures between processor and main memory
- all of the above



Identify which is not an access method for memory. *	1/1
O Direct	
Sequential  Indirect	<b>~</b>
Random	

✓ Which param	neter is belongs to performance of memory. *	1/1
O Direct access		
word		
Capacity		

Transfer rate

★ Define CPI \*

.../1

Cycles per instruction is one aspect of a processor's performance: the average number of clock cycles per instruction for a program or program fragment

X

X Define MIPS \*

.../1

MIPS stands for Million Instructions Per Second. It is another measure of performance. It is also referred as rate of instruction execution per unit time.



✓ Which is more appropriate for performance rate analysis *	1/1
○ AM	
○ SM	
НМ	<b>✓</b>
○ ZM	

✓ What will be the overall speed up if N =10 and f =0.9 in a system. *	1/1
O 4.2	
O 6.2	
5.2	<b>✓</b>
3.2	

X Write meaning of mov ax,3024h *	···/1
3020h(immediate data) is moved to ax register	×

★ Write meaning of mov [4000h],dx *	/1
[4000h] is offset/ address the content of which is moved to dx	×

✓ 8086 can access up to? *	1/1
○ 512KB	
1Mb	<b>✓</b>
O 2Mb	
256KB	

<b>✓</b>	Which flag represents the result when the system capacity is exceeded? 1/1
	Carry flag

- 0 , 3
- Auxiliary flag
- Trap flag
- Overflow flag

<b>✓</b>	If the offset of the operand is stored in one of the index registers, then it is *	1/1
0	based indexed addressing mode	
$\bigcirc$	relative based indexed addressing mode	
•	indexed addressing mode	<b>/</b>
0	none of the mentioned	

The contents of a base register are added to the contents of index register in \*

indexed addressing mode

based indexed addressing mode

relative based indexed addressing mode

based indexed and relative based indexed addressing mode

1/1

- Arithmetic Instructions
- Bit Manipulation Instructions
- String Instructions
- Data Transfer Instructions

- Iteration Control Instructions
- Bit Manipulation Instructions
- Processor Control Instructions
- none of the above

If the data is present in a register and it is referred using the particular register, then it is *	1/1
direct addressing mode	
register addressing mode	<b>✓</b>
indexed addressing mode	
immediate addressing mode	
	register, then it is *  direct addressing mode  register addressing mode  indexed addressing mode

<b>✓</b>	The instruction that pushes the contents of the specified register/memory location on to the stack is *	1/1
0	PUSHF	
0	POPF	
•	PUSH	<b>✓</b>
0	POP	

✓ 8086 is a -----bit microprocessor. \* 1/1 16

•	How many 16 bit registers are there inside 8086 microprocessor ?	*

1/1