8086 MICROPROCESSOR

| Q1. 8086 microprocessor supports modes of operation. |
|---|
| A. 2 B. 3 C. 4 D. 5 |
| ANS1. A |
| Q2. 8086 can access up to memory. |
| A. 512 KB B. 1 MB C. 2 MB D. 256 KB |
| ANS1. B |
| Q3. 8086 has address bus. |
| A. 16-bitB. 18-bitC. 20-bitD. 24-bit |
| ANS1. C |
| Q4. Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to zero |
| A. Trap flagB. Zero flagC. Carry flagD. Overflow flag |
| ANS1. B |
| Q5. Which flag represents the result when the system capacity is exceeded? |
| A. Trap flagB. Auxiliary flagC. Carry flagD. Overflow flag |
| ANS1. B |
| Q6. It is used to write the data into the memory or the output device depending on the status of M/IC signal. |

A. IR

| | HR WR | |
|--|---|--|
| ANS1. D | | |
| Q7. Which i | instruction is used to load the address of operand into the provided register? | |
| A. B. C. | LEA LDS LES LAHF | |
| ANS1. A | | |
| Q8. The dif | ferent ways in which a source operand is denoted in an instruction is known as: | |
| В. С. | Instruction Set Interrupts Architecture Addressing Modes | |
| ANS1. D | | |
| Q9. A micro | oprocessor is a chip integrating all the functions of a CPU of a computer. | |
| В. С. | multiple single double triple | |
| ANS1. B | | |
| Q10. The w | ork of EU is | |
| В. С. | encoding decoding processing calculations | |
| ANS1. B | | |
| Q11. The register used to store the flags is called as | | |
| В. С. | Flag register Status register Test register Log register | |
| ANS 11. B | | |
| Q12. The 16 | 6 bit flag of 8086 microprocessor is responsible to indicate | |
| | | |

B. HLDA

| | В. С. | The condition of result of ALU operation The condition of memory The result of addition The result of subtraction |
|---------|----------------------|---|
| ANS 12. | Α | |
| Q13. Th | e CF | is known as |
| | В. С. | Carry flag Condition flag Common flag Single flag |
| ANS 13. | Α | |
| Q14. Th | e SF | is known as |
| | В. С. | Service flag Sign flag Single flag Condition flag |
| ANS 14. | В | |
| Q15. Th | e IF | is known as |
| | В. С. | Initial flag Indicate flag Interrupt flag Inter flag |
| ANS 15. | С | |
| Q16. Th | e IF | is known as |
| | A. B. C. D. | Initial flag Indicate flag Interrupt flag Inter flag |
| ANS 16. | С | |
| Q17. Th | e IF | is known as |
| | A. B. C. D. | Initial flag Indicate flag Interrupt flag Inter flag |

ANS 17. C

| Q18. The instruction that is used to transfer the data from source of | operand to destination operand is |
|---|-----------------------------------|
|---|-----------------------------------|

- A. Data copy / transfer instruction
- B. Branch instruction
- C. Arithmetic / logical instruction
- D. String instructions

ANS 17. C

CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION

| Q1 | bus structure is usually used to connect I/O devices | |
|---|--|--|
| A. | Single bus | |
| В. | Multiple bus | |
| C. | Star bus | |
| D. | RAM bus | |
| ANS 1. A | | |
| Q2. The main advantage of using single bus structure is | | |
| A. | Fast data transfers | |
| В. | Cost effective connectivity and speed | |
| C. | Cost effective connectivity and ease of attaching peripheral devices | |
| D. | None of the above | |
| ANS 2. C | | |
| Q3. The ISA | A standard buses are used to connect | |
| A. | RAM and Processor | |
| В. | GPU and Processor | |
| C. | Hard-disk and Processor | |
| D. | CD / DVD drives and Processor | |
| ANS 3. C | | |
| Q4. Which | registers can interact with the secondary storage? | |
| A. | MAR | |
| В. | PC | |
| C. | IR | |

| D. | AC |
|-------------|--|
| ANS 4. A | |
| Q5. To exte | end the connectivity of the processor bus we use |
| A. | PCI Bus |
| В. | SCSI Bus |
| C. | Controllers |
| D. | Multiple Bus |
| ANS 5. A | |
| Q6. A sour | ce program is usually written in |
| A. | Assembly language |
| | Machine-level language |
| | High-level language |
| D. | Natural language |
| ANS 6. C | |
| Q7 | are numbers and encoded characters which are generally used as operands. |
| A. | Input |
| | Data |
| | Information |
| D. | Stored values |
| ANS 7. B | |
| Q8. The AL | U stores the immediate result in |
| A. | Accumulator |
| В. | Queue |
| C. | Stack |
| D. | Memory locations |
| ANS 8. A | |
| Q9. The co | ntrol unit controls other units by generating |
| A. | Control signals |
| В. | Timing signals |
| C. | Transfer signals |
| D. | Command signals |
| ANS 9. B | |
| Q10. The e | xtremely small and fast RAM is known as |
| A. | Cache |

| В. | Heaps |
|----------------------|--|
| C. | Accumulators |
| | Stacks |
| ANS 10. A | |
| Q11. The s | mallest entity of memory is called |
| A. | Cell |
| В. | Block |
| C. | Instance |
| D. | Unit |
| ANS 11. A | |
| Q12. The b known as: | ranch of study that deals with the computer system's conceptual design and basic overview is |
| A. | Computer Anatomy |
| В. | Computer Architecture |
| C. | Computer OS |
| D. | Computer Interface |
| ANS12. B | |
| Q13. Which | h of the following technologies was used in second generation computer? |
| A. | Vacuum Tubes |
| В. | Transistors |
| C. | Integrated Circuits |
| D. | VLSI Circuits |
| ANS13. B | |
| | |
| | CHAPTER 2: PERFORMANCE ISSUES |
| Q1 | are used to overcome the difference in data transfer speeds of various devices. |

- A. Speed enhancing circuitry
- B. Bridge circuits
- C. Multiple buses
- D. Buffer registers

ANS 1. D

| Q2. Two processors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster? | | |
|--|--|--|
| A. AB. BC. Both takes equal amount of timeD. None of the above | | |
| ANS 2. A | | |
| Q3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called | | |
| A. Super-scalingB. PipeliningC. Parallel computationD. Architecture | | |
| ANS 3. B | | |
| Q4. The clock rate of the processor can be improved by | | |
| A. Improving the IC technology of the logic circuits B. Reducing the amount of processing done in one step C. By using the over-clocking method D. All of the above | | |
| ANS 4. D | | |
| Q5. SPEC stands for | | |
| A. Standard Performance Evaluation Code B. System Processing Enhancing Code C. System Performance Evaluation Corporation D. Standard Processing Enhancement Corporation | | |
| ANS 5. C | | |
| Q6. CISC stands for | | |
| A. Complete Instruction Sequential Compilation B. Computer Integrated Sequential Compiler C. Complex Instruction Set Computer D. Complex Instruction Sequential Compilation | | |
| ANS 6. C | | |
| Q7. Which instruction is used to load the address of operand into the provided register? | | |
| A. LEA | | |

| | | LES LAHF |
|---------|-------|---|
| 1 NIC 1 | | LATII |
| ANS1. A | | |
| Q8. The | e dif | ferent ways in which a source operand is denoted in an instruction is known as: |
| | | Instruction Set |
| | | Interrupts Architecture |
| | | Addressing Modes |
| | | Addressing Wodes |
| ANS1. [|) | |
| Q9. A n | nicro | oprocessor is a chip integrating all the functions of a CPU of a computer. |
| | A. | multiple |
| | | single |
| | | double |
| | D. | triple |
| ANS1. E | 3 | |
| Q10. Tł | ne w | ork of EU is |
| | A. | encoding |
| | В. | decoding |
| | C. | processing |
| | D. | calculations |
| ANS10. | В | |
| Q11. W | /hich | of the following is the important characteristics of computers? |
| | E. | speed |
| | F. | accuracy |
| | G. | storage |
| | Н. | all of the above |
| ANS11. | D | |
| Q12. W | /hich | of the following is not a hardware component of computer? |
| | A. | memory |
| | В. | scanner |
| | | operating system |
| | D. | CPU |
| ANS12. | С | |

B. LDS

CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

| Q1. During | the execution of a program which gets initialized first? | |
|--------------------|---|--|
| Α. | MDR | |
| В. | IR | |
| C. | PC | |
| | MAR | |
| ANS1. C | | |
| Q2. The de | coded instruction is stored in | |
| A. | IR | |
| В. | PC | |
| C. | Registers | |
| D. | AC | |
| ANS1. A | | |
| Q3. Which | of the register(s) of the processor is / are connected to Memory Bus? | |
| A. | PC | |
| В. | MAR | |
| C. | IR | |
| D. | Both PC AND MAR | |
| ANS1. B | | |
| Q4. ISP stands for | | |
| A. | Instruction Set Processor | |
| В. | Information Standard Processing | |
| C. | Interchange Standard Protocol | |
| D. | Interrupt Service Procedure | |
| ANS1. A | | |
| Q5. The int | errupt request line is a part of the | |
| A. | Data line | |

B. Control line

| | Address line None of the above |
|-------------|--|
| ANS1. B | |
| Q6. The sig | nal set to the device from the processor to the device after receiving an interrupt is |
| В. С. | Interrupt acknowledge Return signal Service signal Permission signal |
| ANS1. A | |
| | |
| | CHAPTER 4: CACHE MEMORY |
| Q1. To red | uce the memory access time we generally make use of |
| В. С. | Heaps SSD SDRAMs Cache memory |
| ANS 1. D | |
| Q2 | is usually used to increase the size of physical memory. |
| В. С. | Secondary memory Virtual memory Hard-disk Disks |
| ANS 2. B | |
| Q3. The int | ernal components of the processor are connected by |
| В. С. | Processor intra-connectivity circuitry Processor bus Memory bus Single bus |
| ANS 3. B | |
| Q4. During | the execution of instructions, a copy of the instructions is placed in the |
| A. | Register |

| В | . RAM |
|-----------|--|
| _ | . Main memory |
| Ľ | . Cache |
| ANS 4. D | |
| Q5. To ge | t the physical address from the logical address generated by CPU we use |
| A | . MAR |
| В | . MMU |
| | . Overlays |
| | . TLB |
| ANS 5. B | |
| Q6. Durir | g the transfer of data between the processor and memory we use |
| A | . Cache |
| | . TLB |
| | . Buffers |
| | . Registers |
| ANS 6. D | |
| Q7 | method is used to map logical address of variable length onto physical memory. |
| | . Paging |
| | . Overlays |
| | . Segmentation |
| Ľ | . Paging with segmentation |
| ANS1. C | |
| Q8. Physi | cal memory is divided into sets of finite size called as |
| A | . Frames |
| В | . Pages |
| _ | . Blocks |
| | . Vectors |
| ANS1. A | |
| Q9. What | is the high speed memory between the main memory and the CPU called? |
| A | Registers |
| | . Cache memory |
| | . Secondary storage memory |
| | . Virtual memory |
| ANS 9. B | |
| Q10. Wh | enever the data is found in the cache memory it is called a |

| В. С. | HIT MISS FOUND ERROR |
|-------------|---|
| ANS 10. A | |
| Q11. The tr | ransfer between CPU and Cache is called |
| В. С. | Block transfer Word transfer Set transfer Associative transfer |
| ANS 11. B | |
| Q12. LRU s | tands for |
| В. С. | Low Rate Usage Least Rate Usage Least Recently Used Low Required Usage |
| ANS 12. C | |
| Q13. When | the data at a location in cache is different from the data in the main memory, the cache is |
| В. С. | Unique Inconsistent Variable Fault |
| ANS 13. B | |
| Q14. Which | n of the following is not a write policy to avoid Cache Coherence? |
| В. С. | Write through Write within Write back Write buffer |
| ANS 14. B | |
| Q15. In | mapping, the data can be mapped anywhere in the Cache Memory. |
| В. С. | Associative Direct Set-associative Indirect |
| | |

| ANS 15. A | | | | | |
|--|---|--|--|--|--|
| Q16. Cache | Memory is implemented using the DRAM chips. | | | | |
| | True False | | | | |
| ANS 16. B | | | | | |
| | | | | | |
| | COA MCQ CHAPTER 5 & 6 | | | | |
| Q1. What is the permanent memory built into your computer called? | | | | | |
| B. C. | RAM ROM CPU CD-ROM | | | | |
| ANS 1. B | | | | | |
| Q2. Storage | e which stores or retains data after power off is called | | | | |
| В. С. | Volatile storage Non-volatile storage Sequential storage Direct storage | | | | |
| ANS2. B | | | | | |
| Q3. The contents of memory into blocks of the same size is called as | | | | | |
| В. С. | ROM EPROM EEPROM All of the above | | | | |
| ANS 3. D | | | | | |
| Q4. Main memory of computer is | | | | | |
| | Internal External Both Auxilliary | | | | |

ANS 4. A

Q5. Which of the following memories must be refreshed many times per second?

A. EPROM

| C. | ROM Static RAM Dynamic RAM |
|---|--|
| ANS 5. D | |
| Q6. A half-l | byte is known as |
| В. С. | data bit half-byte nibble |
| ANS 6. D | |
| Q7. USB typ | pe storage device is |
| В. С. | Secondary Auxiliary Tertiary Primary |
| ANS 7. A | |
| Q8. Which device is used to back-up the c | |
| В. С. | Floppy disk Tape Network drive All of the above |
| ANS 8. D | |
| Q9. With a | CD you can perform |
| C. | read write read and write none of these |
| ANS 9. A | |
| Q10. Flash | memory is also known as |
| В. С. | Flash RAM Flash ROM Flash DRAM Flash DROM |
| ANS 10. A | |
| Q11. RAM i | is a memory. |

| A. | External |
|-------------|--|
| В. | Internal |
| C. | Main |
| D. | Auxiliary |
| ANS 11. C | |
| Q12 | _ is the permanent memory unit built into the computer systems |
| A. | ROM |
| В. | CPU |
| C. | DVD-ROM |
| D. | RAM |
| ANS 12. A | |
| Q13. Hard- | disk drives are considered as storage medium. |
| A. | Flash |
| В. | Non-volatile |
| C. | Temporary |
| D. | Permanent |
| ANS 13. B | |
| Q14. The st | corage element of a SRAM is |
| A. | Diode |
| В. | Resistor |
| C. | Capacitor |
| D. | Flip-flop |
| ANS 14. D | |
| Q15. Capac | ity of hard-disk is measured in |
| A. | Gigabytes |
| В. | Megabytes |
| C. | Kilobytes |
| D. | Bytes |
| ANS 15. A | |

COA MCQ CHAPTER 8

Q1. Which of the following is not a type of Operating System?

- A. Batch Processing
- B. Multi-programming

- C. Latch Programming
- D. Real time programming

ANS 1. C

- Q2. BIOS programs are embedded on a chip called
 - A. Firmware
 - B. IC
 - C. Hardware
 - D. Application programs

ANS 1. A