DAILY ATTENDANCE QUIZ - COA

Q1. First generation computers use---------- *

Vacuum Tubes
Transistor
IC
LSI

Q2. Number of cores in Core 2 Duo processor is --------- *

1
2
3
4

Q3. Which of the following is not a component of CPU *

Main Memory
ALU
Control Unit
Internal Bus

Q4. IAS consists of ----------no of storage locations *

4095
4096
4090
4089

Q5. IAS consists of memory with words of ------- binary digits/bits each). *

40
20
15
10

Q1. ARM Architecture has evolved form --------design principle. *

RISC
CISC
Both
None of these

Q2. All instructions of ARM are ---------- bits long *

20
32
30
10

Q3. Which of the following is not a model of cloud services . *

QaaS
Saa
S
PaaS
IaaS

Q4. Cortex-A50 is a ----------bit machine. *

32
64
16
8

Q5. 8086 has ----------active flags *

9
7
8
10

Q1. ARM Architecture has evolved form --------design principle. *

RISC
CISC
Both
None of these

Q2. power density is expressed in *

Watts/cm4
Watts/cm2
Watts/cm
Watts/cm3

Q3. delay ---------- as the RC product increases. *

increases
decreases
remains constant
none of these

Q4. What is GPGPU *

general-processor computing on GPUs
general-purpose computing on GPUs
general price computing on GPUs
None of these

Q5. For calculation of speedup, When f is small, the use of parallel processors has ---------- *

little effect
More effect
infinite effect
None of these

Q1. According to Amdahl's law ,When f is small, the use of parallel processors has ---------- effect *

little
more
no
None of these

Q2. power density is expressed in *

Watts/cm4
Watts/cm2
Watts/cm
Watts/cm3

Q3. Little’s Law relates these three variables as *

L = λ W
W = λ L
WL= λ
none of these

Q4. What is MIC *

multi integrated core
many integrated core
none of these

Q5. Memory access speed (latency) and transfer speed (throughput) is ---------- compared to processor speeds *

less
more
equal

Q1.A doctor in a hospital observes that on average 6 patients per hour arrive and there are typically 3 patient in the hospital. What is the average range of time each patient spend in the hospital? *

0.75 hour
0.25 hour
0.5 hour
1 hour

Q2. The processor time T needed to execute a given program can be expressed as: *

T= Ic × CPI
T= Ic × CPI × τ
T= CPI × τ
None of these

Q3. We can express the MIPS rate in terms of the clock rate and CPI as follows: *

$Ic/(T$ × 10^6)
$f/(CPI$ × 10^6)
Both of these
None of these

Q4. pulse frequency produced by the clock is measured in *

cycles per hour
cycles per second
cycles per minute
None of these

Q5. Pipelining is used to increase--------- *

Microprocessor Speed
memory Speed
I/O Speed

Q1. 8086 can address a maximum of ------ of memory *

1MB
1G
B
1TB

100GB

Q2. IP (Instruction Pointer) Register is a ----bit register *

8
16
32
20

Q3. find physical address of 8086 if segment address is 0700 and offset is 100 *

07100
7100
0800
800

Q4. EU has -----no of general purpose registers *

10
8
6

Q5. DX is a ----------bit register *

16
8
20

Q1.A doctor in a hospital observes that on average 6 patients per hour arrive and there are typically 3 patient in the hospital. What is the average range of time each patient spend in the hospital? *

0.75 hour
0.25 hour
0.5 hour
1 hour

Q2. What fraction of the execution time involves code that is parallel to achieve an overall speedup of 2.25. Assume 15 numbers of parallel processors? *

f = 0.56
f = 0.59
f = 0.49
None of these

Q3. For computer A, Calculate AM rate if MIPS rate for program 1 and program 2 is 0.2 and 0.1 . *

0.625
0.275
0.15
None of these

Q4. For computer A, Calculate HM rate if MIPS rate for program 1 and program 2 is 0.2 and 0.1 . *

0.09
0.133
0.4
None of these

Q5. Pipelining is used to increase--------- *

Microprocessor Speed
memory Speed
I/O Speed

Q1. program counter is used to store *

address of the current instruction
current data
address of the next instruction to be fetched

next data

Q2. What will be the overall speed up if N =10 and f =0.9 *

0.56
5.263
6.49
None of these

Q3. For computer A, Calculate AM rate if MIPS rate for program 1 and program 2 is 1 and 1. *

0.625
0.5
1
None of these

Q4. For computer A, Calculate GM rate if MIPS rate for program 1 and program 2 is 1 and 1 . *

0.5
1
0.4
None of these

Q5. ---------- Executes each instruction *

processor
memory
I/O

Q1. MAR is a part of--------- *

I/O Module
Main Memory
CPU
None of these

Q2. ----------Holds the address of the next instruction to be fetched. *

IR
PC
MAR
MBR

Q3. According to John Von Neumann model of computer, Instructions are stored in ---------- *

output device
input device
memory
MBR

Q4. I/O AR is a part of--------- *

Main Memory
CPU
I/O Module
None of these

Q5. ---------- Executes each instruction *

processor
memory
I/O

Q1. If the instruction format provides 4 bits for the opcode, then there can be as many as ---------- different opcodes *

2
4
16
8

Q2. How many words of memory can be directly addressed if the instruction format provides 12 bits for the address. *

2K
4K
8K
16K

Q3. States in the lower part of the Instruction Cycle State diagram involve *

output device operations
input device operations
processor operations
memory operations

Q4. Interrupts are provided primarily as a way to improve processing efficiency of *

Main Memory
processor
I/O Module
None of these

Q5. Interrupts that are generated by some conditions that occurs as a result of an instruction execution is called as *

program Interrupt
timmer Interrupt
I/O Interrupt
Hardware Failure Interrupt

Q1. Which of the following case gives more efficiency *

Program Flow of Control and program timing without Interrupts
Program Flow of Control and Program Timing with Interrupts: Short I/O wait
efficiency is equal in both the cases
none of these

Q2. Which of the following is used to effectively handle multiple interrupt *

Disabled interrupt

interrupts handled based on priority

none of these

Q3. The memory used in computer is *

Read only memory

Write only memory

Read/Write memory

none of these

Q4. CPU can *

send interrupt

receive interrupt

both send and receive interrupt

None of these

Q5. Bus can be used to transmit binary digits *

parallelly

serially

both

none of these

Q1.The addressing mode in which the data operand is a part of the instruction itself is known as *

Register addressing mode

immediate addressing mode

Direct addressing mode

indirect addressing mode

Q2. The addressing mode in which the effective address of the memory location is written directly in the instruction is known as *

- immediate addressing mode
- Direct addressing mode
- Register addressing mode
- indirect addressing mode

Q3. The addressing mode in which the operands offset address is found by adding the contents of SI or DI register and 8-bit/16-bit displacements is known as *

- Direct addressing mode
- Base-index addressing mode
- Indexed addressing mode
- indirect addressing mode

Q4. The addressing mode in which the offset address of the operand is computed by summing the base register to the contents of an Index register is known as *

- Direct addressing mode
- Base-index addressing mode
- Indexed addressing mode
- indirect addressing mode

Q5. INC is ----------type of instruction *

- Arithmetic Instructions
- Data Transfer Instructions
- Logical Instructions
- Control Transfer Instructions

Q1.Each line is capable of transmitting --------no of bit *

- 2
- 1
- 3
- 4

Q2. Which control line indicates that data have been accepted from or placed on the bus. *

- Interrupt request
- Transfer ACK
- Bus request
- I/O write

Q3. Which control line is used to synchronize operations *

- Interrupt ACK
- Reset
- Clock
- Bus request

Q4. The ---------- are used to control the access to and the use of the data and address lines *

- Data lines
- control lines
- address lines
- None of these

Q5. A bus that connects major computer components (processor, memory, I/O) is called as *

- system bus
- address lines
- Data lines
- None of these

Q1. Which layer is responsible for reliable transmission and flow control *

- Physical
- Link
- Routing

Protocol

Q2. The Link layer’s unit of transfer is an 80-bit --------- *

Phit
Flit
packets
None of these

Q3. In Protocol layer, ------ is defined as the unit of transfer *

Phit
Flit
packet
None of these

Q4. The peripheral component interconnect (PCI) is a popular high-bandwidth, ---------- bus *

processor-dependent
processor-independent
None of these

Q5. The PCIe protocol architecture includes -------number of layers *

3
4
2
1

Q1. The signal sent to the device from the processor after receiving an interrupt is _____ *

Return signal
Interrupt-acknowledge
Service signal
Permission signal

Q2. CISC stands for _____ *

- Complete Instruction Sequential Compilation
- Complex Instruction Set Computer
- Computer Integrated Sequential Compiler
- None of these

Q3. During the execution of a program which gets initialized first? *

- IR
- MDR
- PC
- MAR

Q4. When dealing with multiple device interrupts, which mechanism is easy to implement? *

- Vectored interrupts
- Polling method
- Interrupt nesting
- None of these

Q5. The stack segment register contains *

- base address of the stack segment
- address of the stack segment
- pointer address of the stack segment
- data in the stack segment

Q1. A system architect can attack the problem of speed mismatch in the following way: *

- Increase the number of bits that are retrieved at one time by making DRAMs “wider” rather than “deeper” and by using wide bus data paths.
- Change the DRAM interface to make it more efficient by including a cache or other buffering scheme on the DRAM chip.
- . Reduce the frequency of memory access by incorporating increasingly complex and efficient cache structures between the processor and main memory.
- All of the above

Q2. The transmission technique used by QPI is known as (LVDS) which stands for: *

- low variable direct signaling
- low voltage differential signaling
- low voltage direct signaling
- low variable differential signaling

Q3. The main function of the root complex is: *

- It acts as a buffering device, to deal with difference in data rates between I/O controllers and memory and processor components.
- It translates between PCIe transaction formats and the processor and memory signal and control requirements.
- Both of the above
- None of the above

Q4. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. Then the maximum directly addressable memory capacity (in bytes) is: *

- 32 MB
- 16 MB
- 8 MB
- 64 MB

Q5. Cache normally sits between: *

- Main memory and CPU
- Primary memory and Secondary memory
- Main memory and I/O module
- Processor and I/O module

Q1. In random access method, Access time ---------- location or previous access *

- depends on
- is independent of
- None of the above

Q2. Type of access method used in tape is---------- *

Direct
Sequential
Random
Associative

Q3. Rate at which data can be transferred into or out of a memory unit is known as *

Memory Cycle time
Access time
Transfer Rate
None of the above

Q4. Unit of transfer for external memory is represented as *

Wor
d
block
bits
none of these

Q5. Speed of Cache is normally ----------speed of main memory *

greater than
less than
equal to that of
none of these

Q1. The transmission technique used by QPI is known as (LVDS) which stands for: *

low variable direct signaling
low voltage differential signaling
low voltage direct signaling
low variable differential signaling

Q2. The main function of the root complex is: *

-It acts as a buffering device, to deal with difference in data rates between I/O controllers and Memory and processor components.

-It translates between PCIe transaction formats and the processor and memory signal and control requirements

-Both of the above

-None of these

Q3. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. Then the maximum directly addressable memory capacity (in bytes) is: *

32MB

64MB

16MB

8MB

Q4. The _____ generally changes with the changing technology. *

Architecture

Organization

none of these

Q5. The processor used in a smartphone is an example of: *

Application Processor

Tiny Processor

Multiprocessor

None of these

Q1. Speed of L2 cache is ----------speed of L1 cache. *

more than

less than

equal to that of
None of these

Q2. Size of L2 cache is ----------size of L1 cache. *

less than
equal to that of
greater than
None of these

Q3. Direct Mapping technique Maps each block of main memory into---------- possible cache line. *

only one
two
multiple
None of these

Q4. Number of address lines required to address 16MByte Main Memory is *

14 bits
24 bits
20 bits
10 bits

Q5. The processor used in a smartphone is an example of: *

Application Processor
Tiny Processor
Multiprocessor
None of these

Q1. During the execution of a program which gets initialized first? *

MDR
PC
IR
MAR

Q2. If a system is 64 bit machine, then the length of each word will be _____ *

- 4 bytes
- 8 bytes
- 16 bytes
- 12 bytes

Q3. In a particular Data segment (DS) the effective address is calculated as *

- DS + Offset
- 10 * DS + Offset
- DS+ offset*10
- None of these

Q4. 24 Bit address line is required to address ---------- Main Memory *

- 8 MByte
- 16 MByte
- 20 MByte
- 24 MByte

Q5. In an IAS computer what Contains the address of the next instruction pair to be fetched from memory. *

- program counter
- Memory buffer register
- Memory address register
- Instruction buffer register

Quiz 23

Total points 10/10

Section D

Email *

1941012406.bikash@gmail.com

Name *

Bikash Kumar Dash

Registration Number *

1941012406

✓ Q1. Speed of L2 cache is ----------speed of L1 cache. * 2/2

- more than
- ✓ less than
- equal to that of
- None of these

✓ Q2. Size of L2 cache is ----------size of L1 cache. * 2/2

- less than
- equal to that of
- ✓ greater than
- None of these

✓ Q3. Direct Mapping technique Maps each block of main memory into---- ------- possible cache line. * 2/2

- ✓ only one
- two
- multiple
- None of these

✓ Q4. Number of address lines required to address 16MByte Main Memory is * 2/2

- 14 bits
- ✓ 24 bits
- 20 bits
- 10 bits

✓ Q5. The processor used in a smartphone is an example of: * 2/2

- ✓ Application Processor
- Tiny Processor
- Multiprocessor
- None of these

Quiz 19

Total points 10/10

Section D

Email *

1941012406.bikash@gmail.com

Name *

Bikash Kumar Dash

Registration Number *

1941012406

✓ Q1. A system architect can attack the problem of speed mismatch in the following way: * 2/2

- Increase the number of bits that are retrieved at one time by making DRAMs "wider" rather than "deeper" and by using wide bus data paths.
- Change the DRAM interface to make it more efficient by including a cache or other buffering scheme on the DRAM chip.
- Reduce the frequency of memory access by incorporating increasingly complex and efficient cache structures between the processor and main memory.
- **All of the above** ✓

✓ Q2. The transmission technique used by QPI is known as (LVDS) which stands for: * 2/2

- low variable direct signaling
- **low voltage differential signaling** ✓
- low voltage direct signaling
- low variable differential signaling

✓ Q3. The main function of the root complex is: * 2/2

- It acts as a buffering device, to deal with difference in data rates between I/O controllers and memory and processor components.
- It translates between PCIe transaction formats and the processor and memory signal and control requirements.
- **Both of the above** ✓
- None of the above

✓ Q4. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. Then the maximum directly addressable memory capacity (in bytes) is: * 2/2

- 32 MB
- **16 MB** ✓
- 8 MB
- 64 MB

✓ Q5. Cache normally sits between: * 2/2

- **Main memory and CPU** ✓
- Primary memory and Secondary memory
- Main memory and I/O module
- Processor and I/O module

Quiz 18

Total points 10/10

Section D

Email *

1941012406.bikash@gmail.com

Name *

Bikash Kumar Dash

Registration Number *

1941012406

✓ Q1. The signal sent to the device from the processor after receiving an interrupt is _____ * 2/2

- ○ Return signal
- ◉ Interrupt-acknowledge ✓
- ○ Service signal
- ○ Permission signal

✓ Q2. CISC stands for _____ * 2/2

- ○ Complete Instruction Sequential Compilation
- ◉ Complex Instruction Set Computer ✓
- ○ Computer Integrated Sequential Compiler
- ○ None of these

✓ Q3. During the execution of a program which gets initialized first? * 2/2

- ○ IR
- ○ MDR
- ◉ PC ✓
- ○ MAR

✓ Q4. When dealing with multiple device interrupts, which mechanism is easy to implement? * 2/2

- ○ Vectored interrupts
- ◉ Polling method ✓
- ○ Interrupt nesting
- ○ None of these

✓ Q5. The stack segment register contains * 2/2

- ◉ base address of the stack segment ✓
- ○ address of the stack segment
- ○ pointer address of the stack segment
- ○ data in the stack segment

Quiz 17

Total points 10/10

Section D

Email *

1941012406.bikash@gmail.com

Name *

Bikash Kumar Dash

Registration Number *

1941012406

✓ Q1. Which layer is responsible for reliable transmission and flow control * 2/2

- ○ Physical
- ◉ Link ✓
- ○ Routing
- ○ Protocol

✓ Q2. The Link layer's unit of transfer is an 80-bit --------- * 2/2

- ○ Phit
- ◉ Flit ✓
- ○ packets
- ○ None of these

✓ Q3. In Protocol layer, ------ is defined as the unit of transfer * 2/2

- ○ Phit
- ○ Flit
- ◉ packet ✓
- ○ None of these

✓ Q4. The peripheral component interconnect (PCI) is a popular high-bandwidth, ---------- bus * 2/2

- ○ processor-dependent
- ◉ processor-independent ✓
- ○ None of these

✓ Q5. The PCIe protocol architecture includes -------number of layers * 2/2

- ◉ 3 ✓
- ○ 4
- ○ 2
- ○ 1

8086 MICROPROCESSOR

Q1. 8086 microprocessor supports _____ modes of operation.

A. 2
B. 3
C. 4
D. 5

ANS1. A

Q2. 8086 can access up to _____ memory.

A. 512 KB
B. 1 MB
C. 2 MB
D. 256 KB

ANS1. B

Q3. 8086 has _____ address bus.

A. 16-bit
B. 18-bit
C. 20-bit
D. 24-bit

ANS1. C

Q4. Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to zero?

A. Trap flag
B. Zero flag
C. Carry flag
D. Overflow flag

ANS1. B

Q5. Which flag represents the result when the system capacity is exceeded?

A. Trap flag
B. Auxiliary flag
C. Carry flag
D. Overflow flag

ANS1. B

Q6. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

A. IR

B. HLDA
C. HR
D. WR

ANS1. D

Q7. Which instruction is used to load the address of operand into the provided register?

A. LEA
B. LDS
C. LES
D. LAHF

ANS1. A

Q8. The different ways in which a source operand is denoted in an instruction is known as:

A. Instruction Set
B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS1. B

Q11. The register used to store the flags is called as _____.

A. Flag register
B. Status register
C. Test register
D. Log register

ANS 11. B

Q12. The 16 bit flag of 8086 microprocessor is responsible to indicate _____.

A. The condition of result of ALU operation
B. The condition of memory
C. The result of addition
D. The result of subtraction

ANS 12. A

Q13. The CF is known as _____.

A. Carry flag
B. Condition flag
C. Common flag
D. Single flag

ANS 13. A

Q14. The SF is known as _____.

A. Service flag
B. Sign flag
C. Single flag
D. Condition flag

ANS 14. B

Q15. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 15. C

Q16. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 16. C

Q17. The IF is known as _____.

A. Initial flag
B. Indicate flag
C. Interrupt flag
D. Inter flag

ANS 17. C

Q18. The instruction that is used to transfer the data from source operand to destination operand is :

A. Data copy / transfer instruction
B. Branch instruction
C. Arithmetic / logical instruction
D. String instructions

ANS 17. C

CHAPTER 1: BASIC CONCEPTS AND COMPUTER EVOLUTION

Q1. _____ bus structure is usually used to connect I/O devices..

A. Single bus
B. Multiple bus
C. Star bus
D. RAM bus

ANS 1. A

Q2. The main advantage of using single bus structure is _____.

A. Fast data transfers
B. Cost effective connectivity and speed
C. Cost effective connectivity and ease of attaching peripheral devices
D. None of the above

ANS 2. C

Q3. The ISA standard buses are used to connect _____.

A. RAM and Processor
B. GPU and Processor
C. Hard-disk and Processor
D. CD / DVD drives and Processor

ANS 3. C

Q4. Which registers can interact with the secondary storage?

A. MAR
B. PC
C. IR

D. AC

ANS 4. A

Q5. To extend the connectivity of the processor bus we use _____.

A. PCI Bus
B. SCSI Bus
C. Controllers
D. Multiple Bus

ANS 5. A

Q6. A source program is usually written in _____.

A. Assembly language
B. Machine-level language
C. High-level language
D. Natural language

ANS 6. C

Q7. _____ are numbers and encoded characters which are generally used as operands.

A. Input
B. Data
C. Information
D. Stored values

ANS 7. B

Q8. The ALU stores the immediate result in _____.

A. Accumulator
B. Queue
C. Stack
D. Memory locations

ANS 8. A

Q9. The control unit controls other units by generating _____.

A. Control signals
B. Timing signals
C. Transfer signals
D. Command signals

ANS 9. B

Q10. The extremely small and fast RAM is known as _____.

A. Cache

B. Heaps
C. Accumulators
D. Stacks

ANS 10. A

Q11. The smallest entity of memory is called _____.

A. Cell
B. Block
C. Instance
D. Unit

ANS 11. A

Q12. The branch of study that deals with the computer system's conceptual design and basic overview is known as:

A. Computer Anatomy
B. Computer Architecture
C. Computer OS
D. Computer Interface

ANS12. B

Q13. Which of the following technologies was used in second generation computer?

A. Vacuum Tubes
B. Transistors
C. Integrated Circuits
D. VLSI Circuits

ANS13. B

CHAPTER 2: PERFORMANCE ISSUES

Q1. _____ are used to overcome the difference in data transfer speeds of various devices.

A. Speed enhancing circuitry
B. Bridge circuits
C. Multiple buses
D. Buffer registers

ANS 1. D

Q2. Two processors A and B have clock frequencies of 700 MHz and 900MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

A. A
B. B
C. Both takes equal amount of time
D. None of the above

ANS 2. A

Q3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____.

A. Super-scaling
B. Pipelining
C. Parallel computation
D. Architecture

ANS 3. B

Q4. The clock rate of the processor can be improved by _____.

A. Improving the IC technology of the logic circuits
B. Reducing the amount of processing done in one step
C. By using the over-clocking method
D. All of the above

ANS 4. D

Q5. SPEC stands for _____.

A. Standard Performance Evaluation Code
B. System Processing Enhancing Code
C. System Performance Evaluation Corporation
D. Standard Processing Enhancement Corporation

ANS 5. C

Q6. CISC stands for _____.

A. Complete Instruction Sequential Compilation
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation

ANS 6. C

Q7. Which instruction is used to load the address of operand into the provided register?

A. LEA

B. LDS
C. LES
D. LAHF

ANS1. A

Q8. The different ways in which a source operand is denoted in an instruction is known as:

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B. Interrupts
C. Architecture
D. Addressing Modes

ANS1. D

Q9. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple
B. single
C. double
D. triple

ANS1. B

Q10. The work of EU is _____.

A. encoding
B. decoding
C. processing
D. calculations

ANS10. B

Q11. Which of the following is the important characteristics of computers?

E. speed
F. accuracy
G. storage
H. all of the above

ANS11. D

Q12. Which of the following is not a hardware component of computer?

A. memory
B. scanner
C. operating system
D. CPU

ANS12. C

CHAPTER 3: A TOP-LEVEL VIEW OF COMPUTERFUNCTION AND INTERCONNECTION

Q1. During the execution of a program which gets initialized first?

A. MDR
B. IR
C. PC
D. MAR

ANS1. C

Q2. The decoded instruction is stored in _____.

A. IR
B. PC
C. Registers
D. AC

ANS1. A

Q3. Which of the register(s) of the processor is / are connected to Memory Bus?

A. PC
B. MAR
C. IR
D. Both PC AND MAR

ANS1. B

Q4. ISP stands for _____.

A. Instruction Set Processor
B. Information Standard Processing
C. Interchange Standard Protocol
D. Interrupt Service Procedure

ANS1. A

Q5. The interrupt request line is a part of the _____.

A. Data line
B. Control line

C. Address line
D. None of the above

ANS1. B

Q6. The signal set to the device from the processor to the device after receiving an interrupt is _____.

A. Interrupt acknowledge
B. Return signal
C. Service signal
D. Permission signal

ANS1. A

CHAPTER 4: CACHE MEMORY

Q1. To reduce the memory access time we generally make use of _____.

A. Heaps
B. SSD
C. SDRAMs
D. Cache memory

ANS 1. D

Q2. _____ is usually used to increase the size of physical memory.

A. Secondary memory
B. Virtual memory
C. Hard-disk
D. Disks

ANS 2. B

Q3. The internal components of the processor are connected by _____.

A. Processor intra-connectivity circuitry
B. Processor bus
C. Memory bus
D. Single bus

ANS 3. B

Q4. During the execution of instructions, a copy of the instructions is placed in the _____.

A. Register

B. RAM
C. Main memory
D. Cache

ANS 4. D

Q5. To get the physical address from the logical address generated by CPU we use _____

A. MAR
B. MMU
C. Overlays
D. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use _____.

A. Cache
B. TLB
C. Buffers
D. Registers

ANS 6. D

Q7. _____ method is used to map logical address of variable length onto physical memory.

A. Paging
B. Overlays
C. Segmentation
D. Paging with segmentation

ANS1. C

Q8. Physical memory is divided into sets of finite size called as _____.

A. Frames
B. Pages
C. Blocks
D. Vectors

ANS1. A

Q9. What is the high speed memory between the main memory and the CPU called?

A. Registers
B. Cache memory
C. Secondary storage memory
D. Virtual memory

ANS 9. B

Q10. Whenever the data is found in the cache memory it is called a _____.

A. HIT
B. MISS
C. FOUND
D. ERROR

ANS 10. A

Q11. The transfer between CPU and Cache is called _____.

A. Block transfer
B. Word transfer
C. Set transfer
D. Associative transfer

ANS 11. B

Q12. LRU stands for _____.

A. Low Rate Usage
B. Least Rate Usage
C. Least Recently Used
D. Low Required Usage

ANS 12. C

Q13. When the data at a location in cache is different from the data in the main memory, the cache is called _____.

A. Unique
B. Inconsistent
C. Variable
D. Fault

ANS 13. B

Q14. Which of the following is not a write policy to avoid Cache Coherence?

A. Write through
B. Write within
C. Write back
D. Write buffer

ANS 14. B

Q15. In _____ mapping, the data can be mapped anywhere in the Cache Memory.

A. Associative
B. Direct
C. Set-associative
D. Indirect

ANS 15. A

Q16. Cache Memory is implemented using the DRAM chips.

A. True
B. False

ANS 16. B

COA MCQ CHAPTER 5 & 6

Q1. What is the permanent memory built into your computer called?

A. RAM
B. ROM
C. CPU
D. CD-ROM

ANS 1. B

Q2. Storage which stores or retains data after power off is called _____.

A. Volatile storage
B. Non-volatile storage
C. Sequential storage
D. Direct storage

ANS2. B

Q3. The contents of memory into blocks of the same size is called as _____.

A. ROM
B. EPROM
C. EEPROM
D. All of the above

ANS 3. D

Q4. Main memory of computer is _____.

A. Internal
B. External
C. Both
D. Auxilliary

ANS 4. A

Q5. Which of the following memories must be refreshed many times per second?

A. EPROM

B. ROM
C. Static RAM
D. Dynamic RAM

ANS 5. D

Q6. A half-byte is known as _____.

A. data
B. bit
C. half-byte
D. nibble

ANS 6. D

Q7. USB type storage device is _____.

A. Secondary
B. Auxiliary
C. Tertiary
D. Primary

ANS 7. A

Q8. Which device is used to back-up the data?

A. Floppy disk
B. Tape
C. Network drive
D. All of the above

ANS 8. D

Q9. With a CD you can perform _____.

A. read
B. write
C. read and write
D. none of these

ANS 9. A

Q10. Flash memory is also known as _____.

A. Flash RAM
B. Flash ROM
C. Flash DRAM
D. Flash DROM

ANS 10. A

Q11. RAM is a _____ memory.

A. External
B. Internal
C. Main
D. Auxiliary

ANS 11. C

Q12. _____ is the permanent memory unit built into the computer systems.

A. ROM
B. CPU
C. DVD-ROM
D. RAM

ANS 12. A

Q13. Hard-disk drives are considered as _____ storage medium.

A. Flash
B. Non-volatile
C. Temporary
D. Permanent

ANS 13. B

Q14. The storage element of a SRAM is _____.

A. Diode
B. Resistor
C. Capacitor
D. Flip-flop

ANS 14. D

Q15. Capacity of hard-disk is measured in _____.

A. Gigabytes
B. Megabytes
C. Kilobytes
D. Bytes

ANS 15. A

COA MCQ CHAPTER 8

Q1. Which of the following is not a type of Operating System?

A. Batch Processing
B. Multi-programming

C. Latch Programming
D. Real time programming

ANS 1. C

Q2. BIOS programs are embedded on a chip called

A. Firmware
B. IC
C. Hardware
D. Application programs

ANS 1. A

COA MCQ CHAPTER 4

Q1. LRU stands for _____.

A. Low Rate Usage
B. Least Rate Usage
C. Least Recently Used
D. Low Required Usage

ANS 1. C

Q2. When the data at a location in cache is different from the data in the main memory, the cache is called _____.

A. Unique
B. Inconsistent
C. Variable
D. Fault

ANS 2. B

Q3. Which of the following is not a write policy to avoid Cache Coherence?

A. Write through
B. Write within
C. Write back
D. Write buffer

ANS 3. B

Q4. In _____ mapping, the data can be mapped anywhere in the Cache Memory.

A. Associative
B. Direct
C. Set-associative
D. Indirect

ANS 4. A

Q5. To get the physical address from the logical address generated by CPU we use _____

A. MAR
B. MMU
C. Overlays
D. TLB

ANS 5. B

Q6. During the transfer of data between the processor and memory we use _____.

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B. TLB
C. Buffers
D. Registers

ANS 6. D

Q7. _____ method is used to map logical address of variable length onto physical memory.

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B. Overlays
C. Segmentation
D. Paging with segmentation

ANS1. C

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B. Pages
C. Blocks
D. Vectors

ANS1. A

Q9. What is the high speed memory between the main memory and the CPU called?

A. Registers
B. Cache memory
C. Secondary storage memory
D. Virtual memory

ANS 9. B

Q10. Whenever the data is found in the cache memory it is called a _____.

A. HIT
B. MISS
C. FOUND
D. ERROR

ANS 10. A

Q11. The transfer between CPU and Cache is called _____.

A. Block transfer
B. Word transfer
C. Set transfer
D. Associative transfer

ANS 11. B

COA MCQ CHAPTER 5 & 6

Q1. What is the permanent memory built into your computer called?

A. RAM
B. ROM
C. CPU
D. CD-ROM

ANS 1. B

Q2. Storage which stores or retains data after power off is called _____.

A. Volatile storage
B. Non-volatile storage
C. Sequential storage
D. Direct storage

ANS2. B

Q3. The contents of memory into blocks of the same size is called as _____.

A. ROM
B. EPROM
C. EEPROM
D. All of the above

ANS 3. D

Q4. Main memory of computer is _____.

A. Internal
B. External
C. Both
D. Auxilliary

ANS 4. A

Q5. Which of the following memories must be refreshed many times per second?

A. EPROM
B. ROM
C. Static RAM
D. Dynamic RAM

ANS 5. D

Q6. A half-byte is known as _____.

A. data
B. bit

C. half-byte
D. nibble

ANS 6. D

Q7. USB type storage device is _____.

A. Secondary
B. Auxiliary
C. Tertiary
D. Primary

ANS 7. A

Q8. Which device is used to back-up the data?

A. Floppy disk
B. Tape
C. Network drive
D. All of the above

ANS 8. D

Q9. With a CD you can perform _____.

A. read
B. write
C. read and write
D. none of these

ANS 9. A

Q10. Flash memory is also known as _____.

A. Flash RAM
B. Flash ROM
C. Flash DRAM
D. Flash DROM

ANS 10. A

Q11. RAM is a _____ memory.

A. External
B. Internal
C. Main
D. Auxiliary

ANS 11. C

Q12. _____ is the permanent memory unit built into the computer systems.

A. ROM
B. CPU
C. DVD-ROM
D. RAM

ANS 12. A

Q13. Hard-disk drives are considered as _____ storage medium.

A. Flash
B. Non-volatile
C. Temporary
D. Permanent

ANS 13. B

Q14. The storage element of a SRAM is _____.

A. Diode
B. Resistor
C. Capacitor
D. Flip-flop

ANS 14. D

Q15. Capacity of hard-disk is measured in _____.

A. Gigabytes
B. Megabytes
C. Kilobytes
D. Bytes

ANS 15. A

COA MCQ CHAPTER 7

Q1. The main importance of ARM micro-processors is providing operation with _____

A. Low cost and low power consumption
B. Higher degree of multi-tasking
C. Lower error or glitches
D. Efficient memory management

ANS 1. A

Q2. ARM processors are basically designed for _____.

A. Mainframe systems
B. Distributed systems
C. Mobile systems
D. Super computers

ANS2. C

Q3. The address system supported by ARM system(s) is / are_____.

A. Little Endian
B. Big Endian
C. X-liitle Endian
D. Both Little and Big Endian

ANS 3. D

Q4. In the ARM, PC is implemented using _____.

A. Caches
B. Heaps
C. General Purpose registers
D. Stack

ANS 4. C

Q5. How many registers are there in ARM7?

A. 35 registers (28 GPR & 7 SPR)
B. 37 registers (28 GPR & 9 SPR)
C. 37 registers (31 GPR & 6 SPR)
D. 35 registers (30 GPR & 5 SPR)

ANS 5. C

Q6. Which processor requires more number of registers?

A. CISC
B. ISA

C. RISC
D. ANNA

ANS 6. C

Q7. The method which offers higher speeds of I/O transfers is _____.

A. Interrupts
B. Memory mapping
C. Program-controlled I/O
D. DMA

ANS 7. D

Q8. In memory-mapped I/O _____.

A. The I/O devices have a separate address space
B. The I/O devices and the memory share the same address space
C. A part of the memory is specifically set aside for the I/O operation
D. The memory and I/O devices have an associated address space

ANS 8. B

Q9. The _____ circuit is basically used to extend the processor BUS to connect devices.

A. Router
B. Repeater
C. Bridge
D. All of the above

ANS 9. C

Q10. Keyboard and Mouse comes under _____.

A. Input peripherals
B. Output peripherals
C. I/O devices
D. None of the above.

ANS 10. A

Q11. RAM is a _____ memory.

A. External
B. Internal
C. Main
D. Auxiliary

ANS 11. C

Q12. _____ is the permanent memory unit built into the computer systems.

A. ROM
B. CPU
C. DVD-ROM
D. RAM

ANS 12. A

Q13. Hard-disk drives are considered as _____ storage medium.

A. Flash
B. Non-volatile
C. Temporary
D. Permanent

ANS 13. B

Q14. The storage element of a SRAM is _____.

A. Diode
B. Resistor
C. Capacitor
D. Flip-flop

ANS 14. D

Q15. Capacity of hard-disk is measured in _____.

A. Gigabytes
B. Megabytes
C. Kilobytes
D. Bytes

ANS 15. A

Chapter 8 – OS – MCQ

1. The systems of _____ generally ran one job at a time. These were called single stream batch processing systems.

Ans: 50's

2. In _____ generation of operating system, operating system designers developed the concept of multiprogramming in which several jobs are in main memory at once.

Ans: Third

3. Which of the following is/are the functions of operating systems? (i) Sharing hardware among users. (ii) Allowing users to share data among themselves. (iii) Recovering from errors. (iv) Preventing users from interfering with one another. (v) Scheduling resources among users.

Ans: All

4. _____ executes most frequently and makes the fine grained decision of which process is to be executed next.

Ans: Short term scheduling

5. With _____ a page is brought into main memory only when the refernce is made to a location on that page.

Ans: Demand paging

6. _____ provides a larger sized of virtual memory but require virtual memory which provides multidimensional memory.

Ans: Segmentation method

7. _____ refers to the ability of an operating system to support multiple threads of execution with a single process.

Ans: Multithreading

8. A special type of programming language used to provide instructions to the monitor in simple batch processing scheme is known as:

Ans: Job control language

9. Process is :

Ans:

i. A program in execution

ii. An instance of a program running on a computer

iii. The entity that can be assigned to and executed

10. The facility that allows programmers to address memory from a ogical point of view, irrespective of the main memory physically available is known as :

Ans: Virtual memory

11. With _____ only one process can execute at a time ; meanwhile all other process are waiting for the processor. With _____ more than one process can be running simultaneously each on a different processor.

Ans: Multiprogramming, Multiprocessing

12. Which of the following are the states of a five state process model? (i) Running (ii) Ready (iii) New (iv) Exit (v) Destroy

Ans: i, ii, iii & iv only

13. Routine is not loaded until it is called. All routines are kept on disk in a relocatable load format. The main program is loaded into memory and is executed. This type of loading is called :

Ans: Dynamic linking

14. The hot repeatedly checks if the controller is busy until it is not. It is in a loop that status register's busy bit becomes clear. This is called _____ and a mechanism for the hardware controller to notify the CPU that it is ready is called _____.

Ans: Polling & Interrupt

15. Real time systems are :

Ans: Used for monitoring events as they occur

✓ Replacement algorithms used in associative and set-associative mapping of cache memory are: * 1/1

- ○ LFU
- ○ LRU
- ○ FIFO
- ◉ All of the above ✓

✗ Cache Memory is implemented using the DRAM chips. * 0/1

- ◉ TRUE ✗
- ○ FALSE

Correct answer

- ◉ FALSE

✓ LRU stands for _____ * 1/1

- ○ Low Rate Usage
- ○ Least Rate Usage
- ◉ Least Recently Used ✓
- ○ Low Required Usage

✗ When the data at a location in cache is different from the data located in the main memory, the cache is called _____ * 0/1

- ○ Unique
- ○ Inconsistent
- ○ Variable
- ◉ Fault ✗
- ○ Other:

Correct answer

- ◉ Inconsistent

✓ Which of the following is not a write policy to avoid Cache Coherence? * 1/1

- ○ Write through
- ◉ Write within ✓
- ○ Write back
- ○ Buffered write

✓ The instruction, “INC” increases the contents of the specified register or memory location by..... * 1/1

- 0
- 1 ✓
- 2
- 3

✓ The instruction that enables subtraction with borrow is..... * 1/1

- DEC
- SUB
- SBB ✓
- ADC

✓ In general, the source operand of an instruction can be..... * 1/1

- memory location
- register
- immediate data
- All of these ✓

✓ In general, the destination operand of an instruction can be..... * 1/1

- memory location
- register
- immediate data
- memory location and register ✓

✓ The instruction, CMP to compare source and destination operands, it performs..... * 1/1

- addition
- subtraction ✓
- division
- multiplication

located in the main memory, the cache is called. *

- ○ Unique
- ◉ Inconsistent ✓
- ○ Variable
- ○ Fault

✓ Which of the following is not a write policy to avoid Cache Coherence? * 1/1

- ○ Write through
- ◉ Write within ✓
- ○ Write back
- ○ Buffered write

✓ In Direct Mapping of a cache the relation holds good is: * 1/1

- ○ i = j modulo k
- ◉ i = j modulo m ✓

✗ The processor used in a smartphone is an example of: * 0/1

- ○ Dedicated Processor
- ○ Application Processor
- ○ Tiny Processor
- ◉ Multiprocessor ✗

Correct answer

- ◉ Application Processor

✓ ARM chips are: * 1/1

- ○ High speed processors and require more power
- ◉ High speed processors and require less power ✓
- ○ Low speed processors and require less power
- ○ Low speed processors and require more power

✓ The first microprocessor to be launched was: * 1/1

- 8008
- 8080
- 4004 ✓
- 4040

✗ Intel's first 32-bit machine was: * 0/1

- 8086
- 80286 ✗
- 80386
- Pentium

Correct answer

- 80386

✗ The processor used in a smartphone is an example of: * 0/1

✓ The main structural components of a computer are: * 1/1

- ○ CPU, VDU, Main Memory, Secondary Memory
- ◉ CPU, I/O, Main Memory, System Interconnections ✓
- ○ CPU, Keyboard, Mouse, Printer
- ○ CPU, CU, ALU, I/O

✓ The Von Neumann architecture consists of: * 1/1

- ○ Main Memory, System interconnections, Speakers, Monitor
- ○ Main Memory, Display Unit, Circuit Board, Power Supply
- ◉ Main Memory, ALU, CU, I/O, System Interconnections ✓
- ○ Main Memory, CPU, Secondary Memory, Speakers

✓ If the offset of the operand is stored in one of the index registers, then it is known as __ * 1/1

- ○ base index addressing mode
- ◉ indexed addressing mode ✓
- ○ relative base indexed addressing mode
- ○ none of these

✓ The microprocessor can read/write 16-bit data from or to ___ * 1/1

- ◉ Memory ✓
- ○ I/O devices
- ○ Processor
- ○ None of these

✓ During read operation, CPU fetches _____ * 1/1

- ○ Data
- ○ Instruction
- ○ another address
- ◉ all of the above ✓

✓ If the base address of stack segment in 8086 is 4FFF0H, the value in SS register is ..... * 1/1

- ○ 8FFFH
- ◉ 4FFEH ✓
- ○ 5FFEH
- ○ 4FFFH

be..... *

- memory location
- register
- immediate data ✗
- memory location and register

Correct answer

- memory location and register

✓ The instruction, CMP to compare source and destination operands, it performs..... * 1/1

- addition
- subtraction ✓
- division
- multiplication

✓ In general, the source operand of an instruction can be..... * 1/1

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- ○ register
- ○ immediate data
- ◉ All of these ✓

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- ○ memory location
- ○ register
- ◉ immediate data ✗
- ○ memory location and register

Correct answer

- ◉ memory location and register

✓ The instruction, “INC” increases the contents of the specified register or memory location by..... * 1/1

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- ○ 2
- ○ 3

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- ○ SUB
- ◉ SBB ✓
- ○ ADC

✓ In general, the source operand of an instruction can be..... * 1/1

✓ An example of non-erasable memory is: * 1/1

- ○ RAM
- ◉ ROM ✓
- ○ CACHE
- ○ MAIN MEMORY

✓ Storage which stores or retains data after power off is called__ * 1/1

- ○ Volatile storage
- ◉ Non-volatile storage ✓
- ○ Sequential Storage
- ○ Direct storage

✓ Which of the following is independent of the address bus? * 1/1

- (●) Secondary memory ✓
- ( ) Main memory
- ( ) Cache memory
- ( ) None of these

✓ An example of non-erasable memory is: * 1/1

- ( ) RAM
- (●) ROM ✓
- ( ) CACHE
- ( ) MAIN MEMORY

✓ Storage which stores or retains data after power off is called__ * 1/1

✓ RAID stands for..... * 1/1

- (●) Redundant Array of Independent Disks ✓
- ( ) Reduced Array of Independent Disks
- ( ) Redundant Array of Independent Devices
- ( ) IR Redundant Array of Interleaved Disks

✓ RAID increases the mean time to failure. * 1/1

- (●) TRUE ✓
- ( ) FALSE

✓ Which of the following is independent of the address bus? * 1/1

✓ Which of the following is not a write policy to avoid Cache Coherence? * 1/1

- ○ Write through
- ◉ Write within ✓
- ○ Write back
- ○ Buffered write

✓ In Direct Mapping of a cache the relation holds good is: * 1/1

- ○ i = j modulo k
- ◉ i = j modulo m ✓
- ○ i = j modulo v
- ○ i = j modulo w

✓ When the data at a location in cache is different from the data located in the main memory, the cache is called. * 1/1

- ○ Unique
- ◉ Inconsistent ✓
- ○ Variable
- ○ Fault

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- ○ Buffered write

✓ In Direct Mapping of a cache the relation holds good is: * 1/1

✓ Replacement algorithms used in associative and set-associative mapping of cache memory are: * 1/1

- ○ LFU
- ○ LRU
- ○ FIFO
- ◉ All the above ✓

✓ For a hamming code of parity bit m=8, what is the total bits and data bits? * 1/1

- ◉ (255, 247) ✓
- ○ (127, 119)
- ○ (31, 26)
- ○ (0, 8)

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