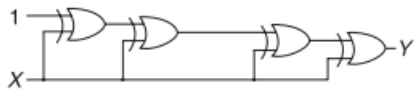
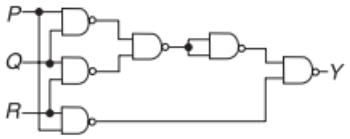
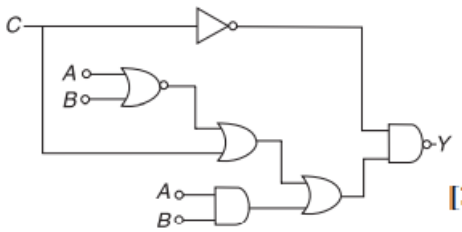
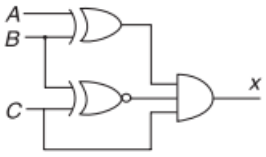
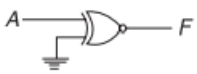
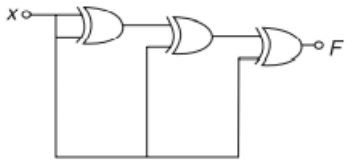
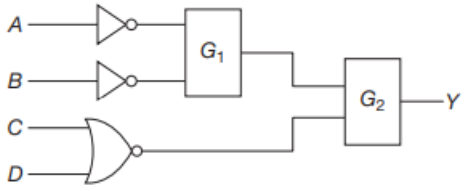
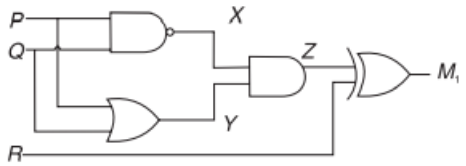
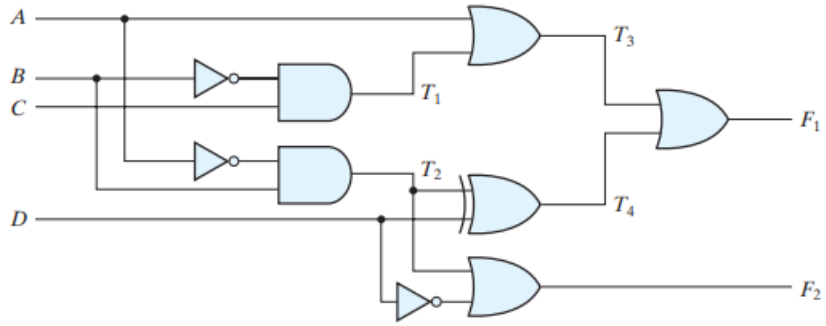
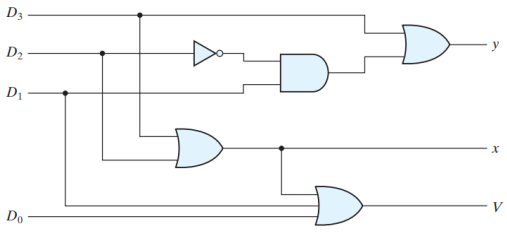
	ITER, SIKSHA 'O' ANUSANDHAN (Deemed to be University)		**Assignment**
Branch	**Computer Science and Engineering**	Programme	**B.Tech**
Course Name	**Digital Logic Design**	Semester	**III**
Course Code	**EET1211**	Academic Year	**2022/Odd**
Assignment-2	**Topic- Gate-level Minimization and Combinational Logic**	**GP-1**	
Learning Level (LL)	**L1**: Remembering	**L3:** Applying	**L5**: Evaluating
	L2: Understanding	**L4**: Analysing	**L6**: Creating

Q's	Questions	COs	LL
1	If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR gates is X, then the output Y is equal to  **[2002]**	**CO2**	**L2**
2	The output Y in the circuit below is always `1' when  **[2011]**	**CO2**	**L4**
3	In the circuit shown in the figure, if $C = 0$, the expression for Y is  **[2014]**	**CO2**	**L2**
4	For the logic circuit shown in the figure, the required input condition (A, B, C) to make the output $(X) = 1$ is  **[2000]**	**CO2**	**L2**
5	The output of the logic gate in figure is  **[1997]**	**CO2**	**L3**
6	The minimum number of NAND gates required to implement the Boolean function $A + A\bar{B} + A\bar{B}C$ is equal to (a) Zero (b) 1 (c) 4 (d) 7 **[1995]**	**CO2**	**L2**

7	For the circuit shown below the output F is given by  **[1988]**	**CO2**	**L3**
8	In the figure shown, the output Y is required to be $Y = AB + \overline{C}\,\overline{D}$. The gates G_1 and G_2 must be, respectively. **[2015]**  (A) NOR, OR (B) OR, NAND (C) NAND, OR (D) AND, NAND	**CO2**	**L2**
9	Which of the following Boolean expressions correctly represents the relation between P, Q, R and M_1?  (a) M_1 = (P OR Q) XOR R (b) M_1 = (P AND Q) XOR R (c) M_1 = (P NOR Q) XOR R (d) M_1=(P XOR Q) XOR R **[2008]**	**CO2**	**L2**
10	The number of product terms in the minimized sum-of-product expression obtained through the following K-map is (where 'd' denotes don't care states) 1 0 0 1 0 d 0 0 0 0 d 1 1 0 0 1 (a) 2 (b) 3 (c) 4 (d) 5 **[2005]**	**CO2**	**L3**
11	The truth table for the output Y in terms of three inputs A, B and C are given in Table. Draw a logic circuit realization using only NOR gates. A 0 1 0 1 1 1 0 1 B 0 0 1 1 0 0 1 1 C 0 0 0 0 1 1 1 1 Y 1 1 1 0 1 0 0 0 **[1993]**	**CO2**	**L3**

12	 Consider the combinational circuit shown above. a. Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs F_1 and F_2 as a function of the four inputs. b. List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.	**CO3**	**L4**
13	Design a combinational circuit with three inputs, x, y , and z , and three outputs, A, B , and C . When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is three less than the input.	**CO3**	**L6**
14	Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use block diagrams	**CO3**	**L6**
15	Design a combinational circuit that converts a four-bit Gray code to a four-bit binary number. Write a Verilog dataflow model of the circuit.	**CO3,CO6**	**L6**
16	Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to4-line decoder. Use block diagrams for the components.	**CO3**	**L6**
17	Using a decoder and external gates, design the combinational circui defined by the following three Boolean functions: (a) $F_1 = x'yz' + xz$ $F_2 = xy'z' + x'y$ $F_3 = x'y'z' + xy$ (b) $F_1 = (y' + x)z$ $F_2 = y'z' + x'y + yz'$ $F_3 = (x + y)z$	**CO3**	**L6**
18	Implement the following Boolean function with a multiplexer (a) $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$ (b) $F(A, B, C, D) = \Pi(2, 6, 11)$	**CO3**	**L3**
19	Write the HDL gate-level description of 4bit priority encoder circuit given below. 	**CO6**	**L4**
20	An 8 × 1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1, and S_0, respectively. The data inputs I_0 through I_7 are as follows: (a)* $I_1 = I_2 = I_7 = 0; I_3 = I_5 = 1; I_0 = I_4 = D$; and $I_6 = D'$. (b) $I_1 = I_2 = 0; I_3 = I_7 = 1; I_4 = I_5 = D$; and $I_0 = I_6 = D'$. Determine the Boolean function that the multiplexer implements.	**CO3**	**L2**

Assignment 2	Topic: Gate-level Minimization and Combinational Logic	Date of Assignment2: 24.11.2022	Date of Submission: 03.12.2022

Note:

1. assignment carries weightage of **20 marks out of 100**
2. Course outcome CO1 to CO2 was covered.

Course Outcomes	CO1	Able to State and explain different number systems, binary codes
	CO2	Able to apply the principles of Boolean algebra and Karnaugh map to simplify logic expressions and implement it using gates
	CO3	Able to Analyse and design various combinational circuits
	CO4	Able to Analyse and design different synchronous and asynchronous sequential circuits
	CO5	Able to Analyse and design various Memory, Programmable Logic circuits and register transfer level
	CO6	Able to implement various digital circuits using HDL and Standard ICs.