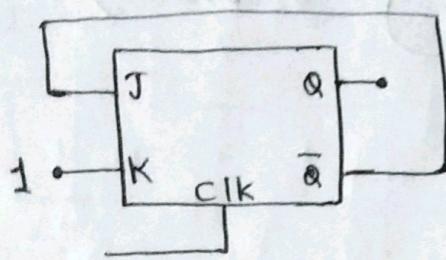


### Assignment - 3.

1) In a J-K Flip-Flop we have  $J = \bar{Q}$  and  $K = 1$ . Assuming the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be.



J	K	$Q_n$	$Q_{n+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

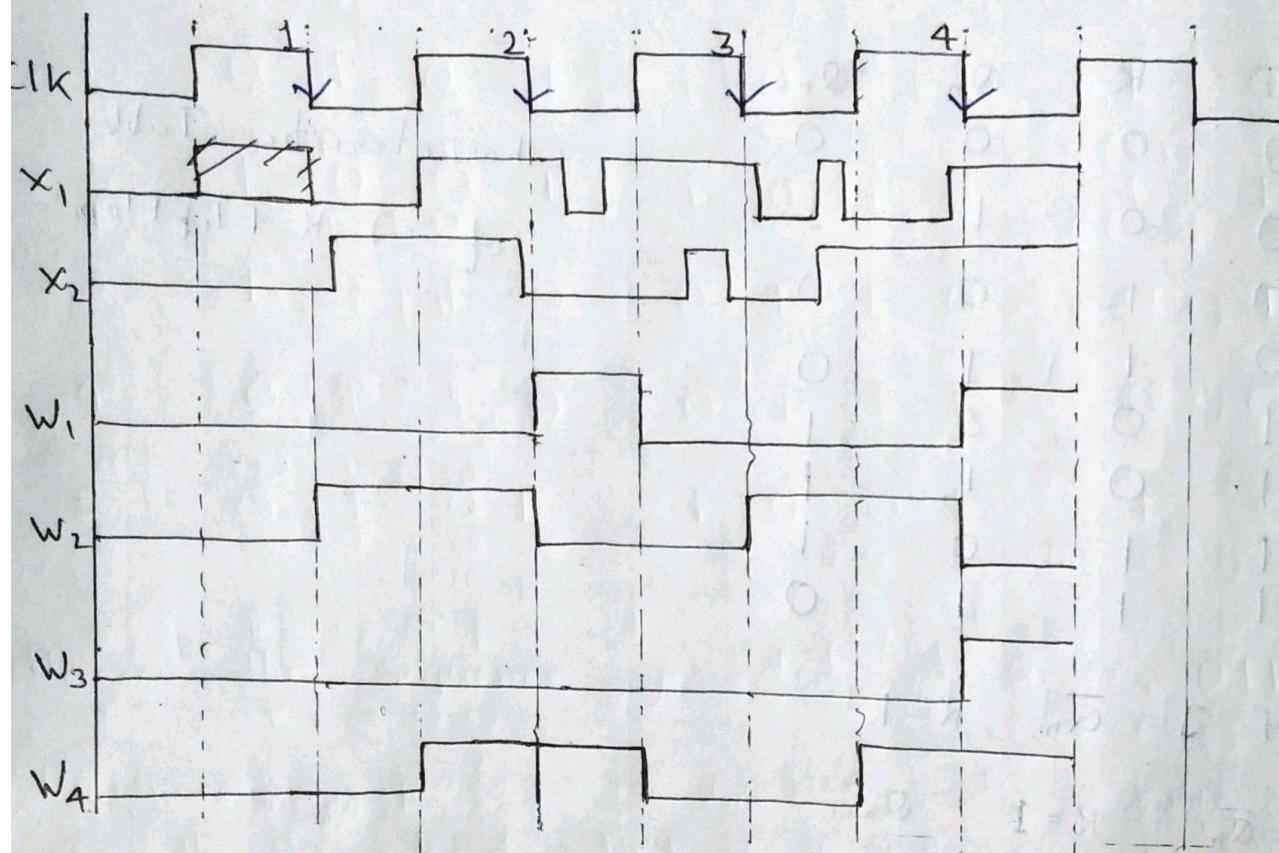
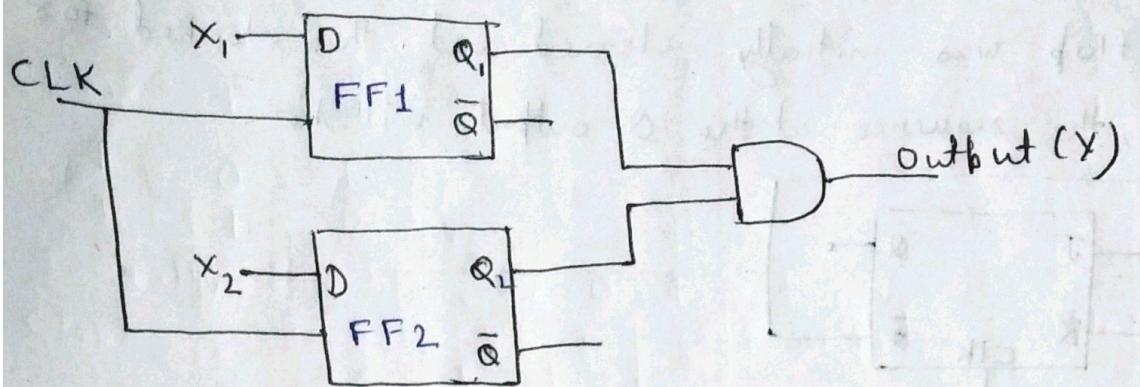
Characteristic Table  
of J-K-Flip Flop.

If  $J = \bar{Q}_n$ ,  $K = 1$ .

clk	$J = \bar{Q}_n$	$K = 1$	$Q_{n+1}$
0	-	-	0
1	1	1	1
2	0	1	0
3	1	1	1
4	0	1	0
5	1	1	1
6	0	1	0

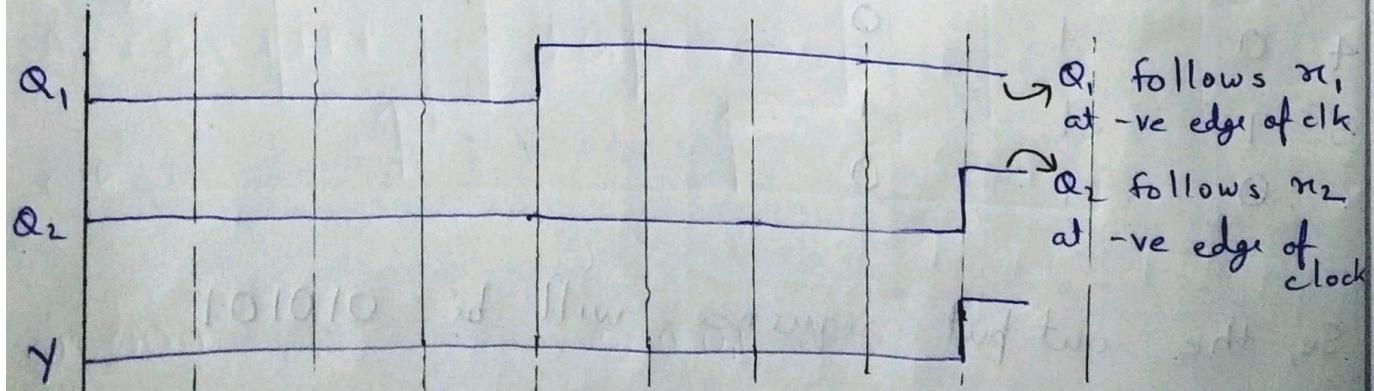
So, the output sequence will be 010101

3) In the circuit shown, choose the correct timing diagram of the output ( $Y$ ) from the given waveforms  $W_1, W_2, W_3$  or  $W_4$ .



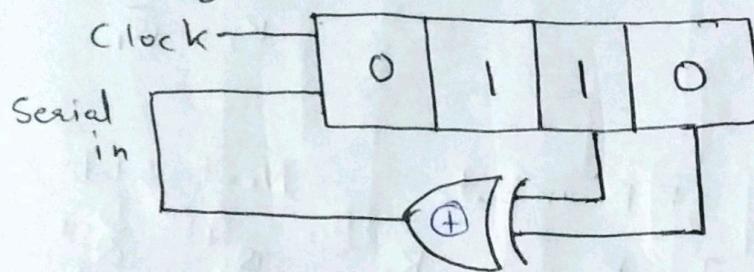
Let  $Q_1$  &  $Q_2$  be output of FF1 and FF2.

The output of flipflop only changes at the negative edge of the clock.



The output  $Y$  is similar to  $W_3$ .

3) The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After 3 clock pulses are applied, the contents of the shift Register will be.



Clock,

0      0 1 1 0

1      1 0 1 1

2      0 1 0 1

3      1 0 1 0

Clock'

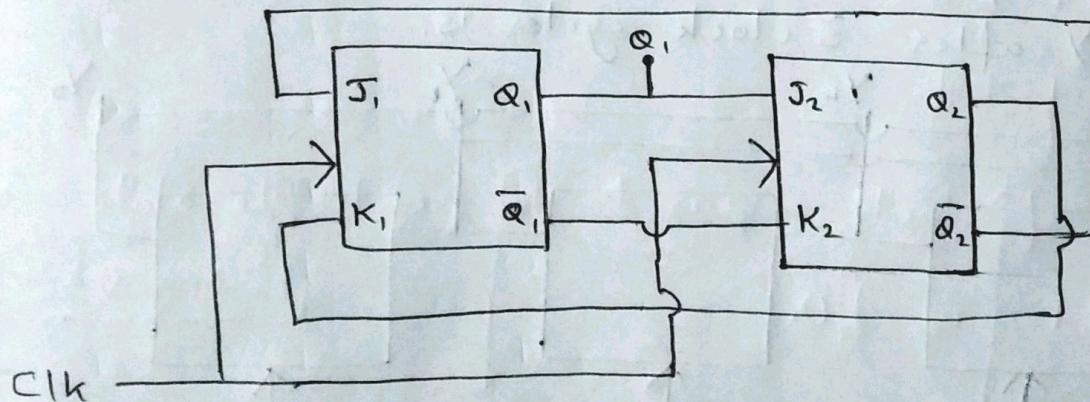
$$1 \quad \text{xor}(1,0)=1$$

$$2 \quad \text{xor}(1,1)=0$$

$$3 \quad \text{xor}(0,1)=1$$

So, the content will be 1010.

4) The outputs of the flip flops  $Q_1$  &  $Q_2$  in the figure shown are initialized to 0, 0. The sequence generated at  $Q_1$  upon application of clock signal is.



a) 01110

b) 01010

c) 00110

d) 01100

$$J_1 = \bar{Q}_2$$

$$K_1 = Q_2$$

$$J_2 = Q_1$$

$$K_2 = \bar{Q}_1$$

The Truth Table of JK Flip Flop is.

J	K	$Q_n$
0	0	Memory.
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$$\begin{aligned} J_1 &= \bar{Q}_2 \\ K_1 &= Q_2 \\ J_2 &= Q_1 \\ K_2 &= \bar{Q}_1 \end{aligned}$$

Initially  $Q_1 = 0, Q_2 = 0$ .

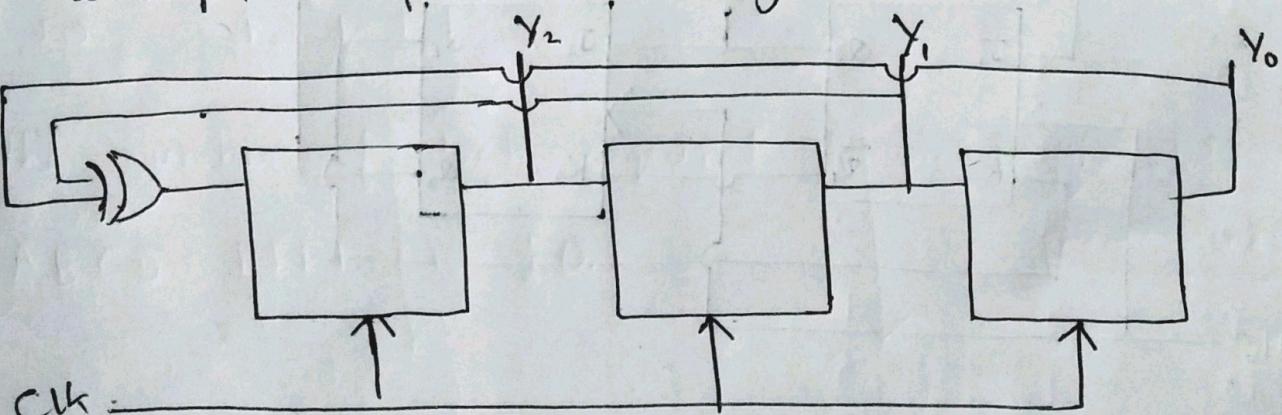
Clock	Present State	FF inputs	Next state
	$Q_1 \quad \bar{Q}_1 \quad Q_2 \quad \bar{Q}_2$	$J_1 \quad K_1 \quad J_2 \quad K_2$	$Q_1^+ \quad Q_2^+$
1	0 1 0 1	1 0 0 1	1 0
2	1 0 0 1	1 0 1 0	1 1
3	1 0 1 0	0 1 1 0	0 1
4	0 1 1 0	0 1 0 1	0 0
5	0 1 0 1	1 0 0 1	1 0

Hence the sequence generated at  $Q_1$  is 01100.

5) A three bit pseudo random number generator is shown.

Initially the value of output  $Y = Y_2 \ Y_1 \ Y_0$  is set 111.

The output  $Y$  after 3 clock cycles is.

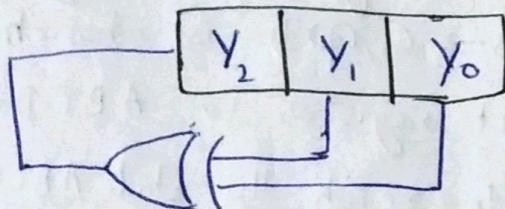


a) 000

b) 001

c) 010

d) 100



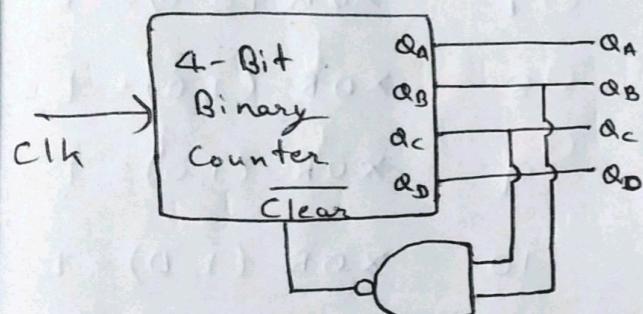
$$Y_2 = Y_1 \oplus Y_0.$$

Clock	$Y_2$	$Y_1$	$Y_0$
0	1	1	1
1	0	1	1
2	0	0	1
3	1	0	0

Clock	$Y_2$
1	$\text{XOR}(1, 1) = 0$
2	$\text{XOR}(1, 1) = 0$
3	$\text{XOR}(0, 1) = 1$

The output  $Y = 100$  after 3 clock cycle.

- b) A mod-'n' counter using a synchronous binary up-counter with synchronous clear input is shown in the figure.  
The value of 'n' is.



$$\overline{\text{Clear}} = \overline{Q_B \cdot Q_C}.$$

When  $Q_B$  &  $Q_C$  is 1

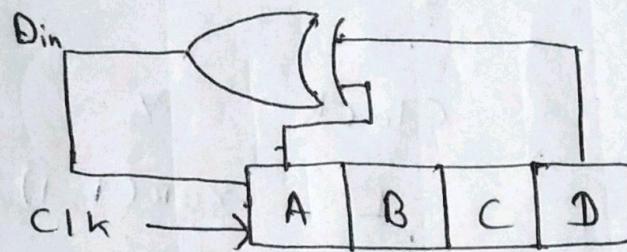
$$\overline{\text{Clear}} = 0.$$

Clock	$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\overline{\text{Clear}}$
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0

$\Rightarrow$  Mod counter is 7.  
as it counts states  
from 0 to 6.

Since it is given that counter have synchronous clear input,  
the output of the counter will be reset at the  $\frac{0110}{7^{\text{th}}}$  clock.

Q) A 4-bit shift register circuit configured for right-shift operation, i.e.,  $D_{in} \rightarrow A$ ,  $A \rightarrow B$ ,  $B \rightarrow C$ ,  $C \rightarrow D$ , is shown. If the present state of the shift register is  $ABCD = 1101$ , the number of clock required to reach the state  $ABCD = 1111$ .



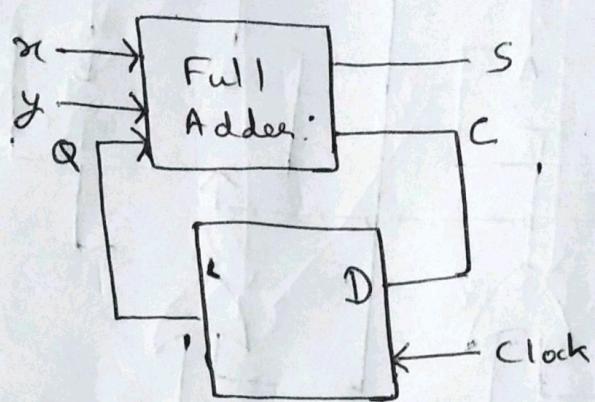
$$D_{in} = A \oplus D.$$

Clock	A	B	C	D
0	1	1	0	1
1	0	1	1	0
2	0	0	1	1
3	1	0	0	1
4	0	1	0	0
5	0	0	1	0
6	0	0	0	1
7	1	0	0	0
8	1	1	0	0
9	1	1	0	0
10	1	1	1	1

Clock	Din
1	$\text{XOR}(1,1) = 0$
2	$\text{XOR}(0,0) = 0$
3	$\text{XOR}(0,1) = 1$
4	$\text{XOR}(1,1) = 0$
5	$\text{XOR}(0,0) = 0$
6	$\text{XOR}(0,0) = 0$
7	$\text{XOR}(0,1) = 1$
8	$\text{XOR}(1,0) = 1$
9	$\text{XOR}(1,0) = 1$
10	$\text{XOR}(1,0) = 1$

The number of clock required to reach the state  $ABCD = 1111$  is 10.

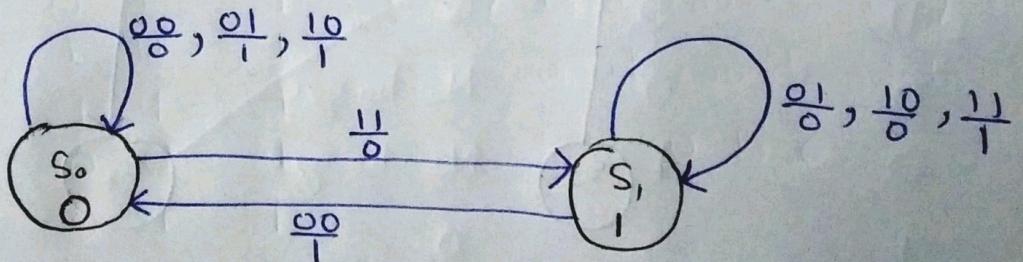
A sequential circuit has one flip-flop  $Q$ , two inputs  $x$  and  $y$ , and one output  $S$ . It consists of a full adder circuit connected to a D flip flop. Derive the state table and state diagram of the sequential circuit.



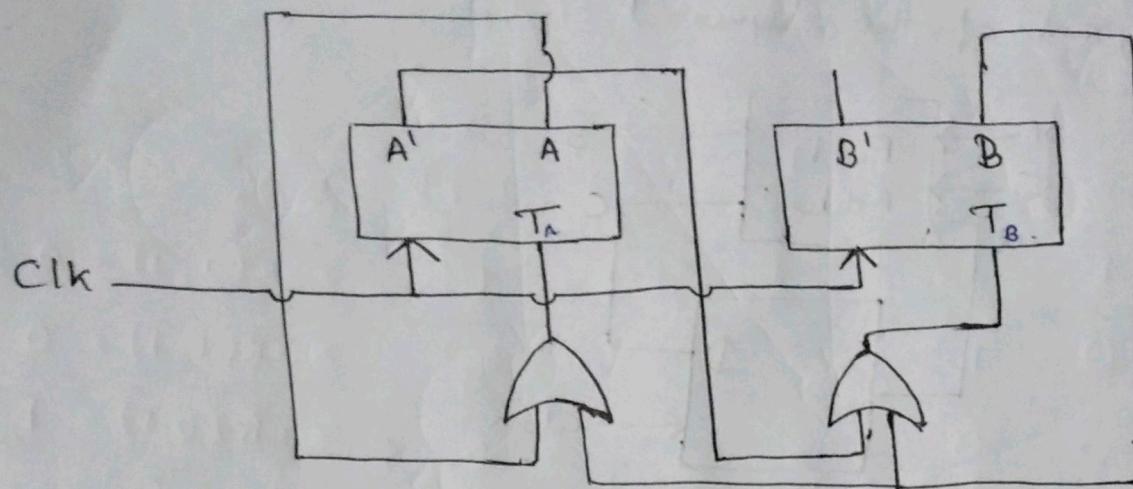
$$S = x \oplus y \oplus Q$$

$$C = xy + xQ + yQ$$

Present State $Q(t)$	Input $x, y$		Next State $Q(t+1)$	Output $S(t+1)$
	$x$	$y$		
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



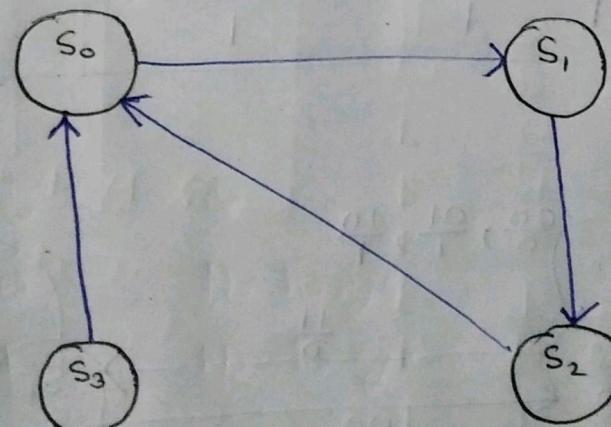
Derive the state table and the state diagram of the sequential circuit shown below. Explain the function of that the circuit performs.



$$T_A = A + B$$

$$T_B = A' + B$$

Present State.		Next State.		Input.	
A(t)	B(t)	A(t+1)	B(t+1)	T <sub>A</sub>	T <sub>B</sub>
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1



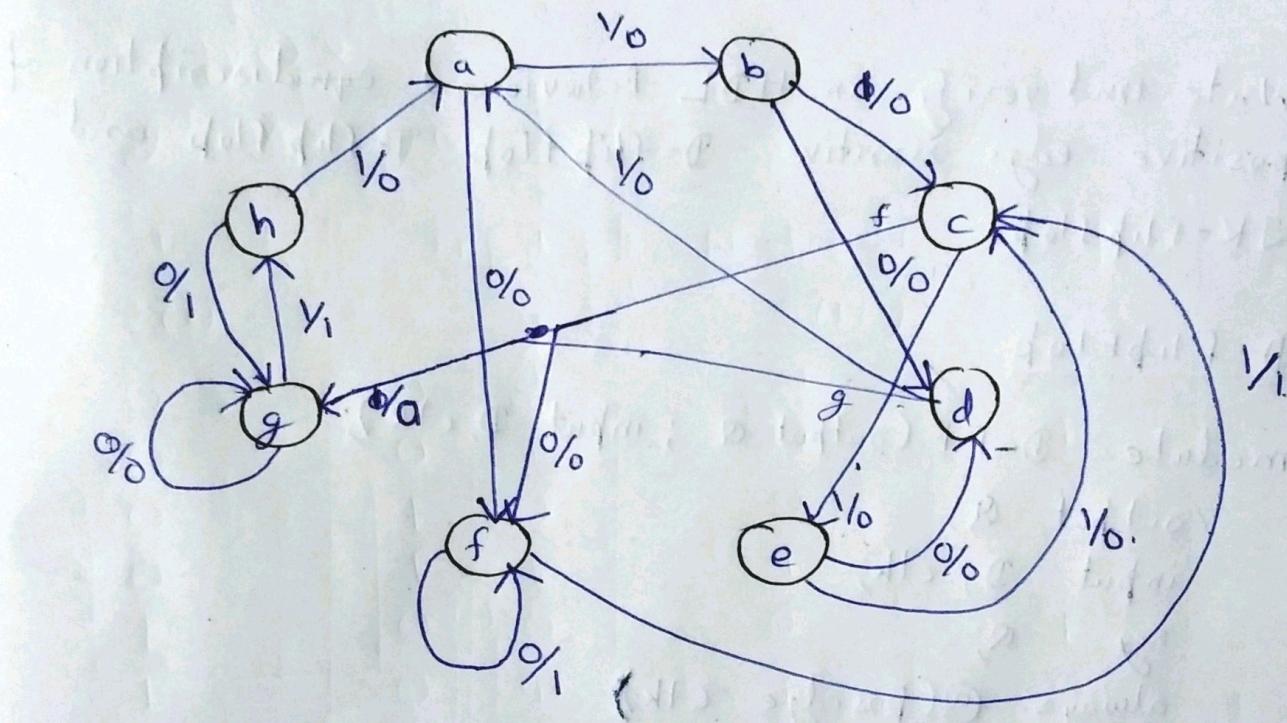
$S_0 \rightarrow S_1 \rightarrow S_2$   
 $00 \rightarrow 01 \rightarrow 10$

This circuit is a counter with repeated sequence 00, 01 and 10.

10) Present state

	Next S state.		Output	
	$n=0$	$n=1$	$n=0$	$n=1$
$\rightarrow a$	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
$\rightarrow e = b$	d	c	0	0
$\rightarrow f = a$	f	b	1	1
g	g	h	0	1
$\rightarrow h = a$	g	a	1	0

a) Draw the corresponding state diagram.

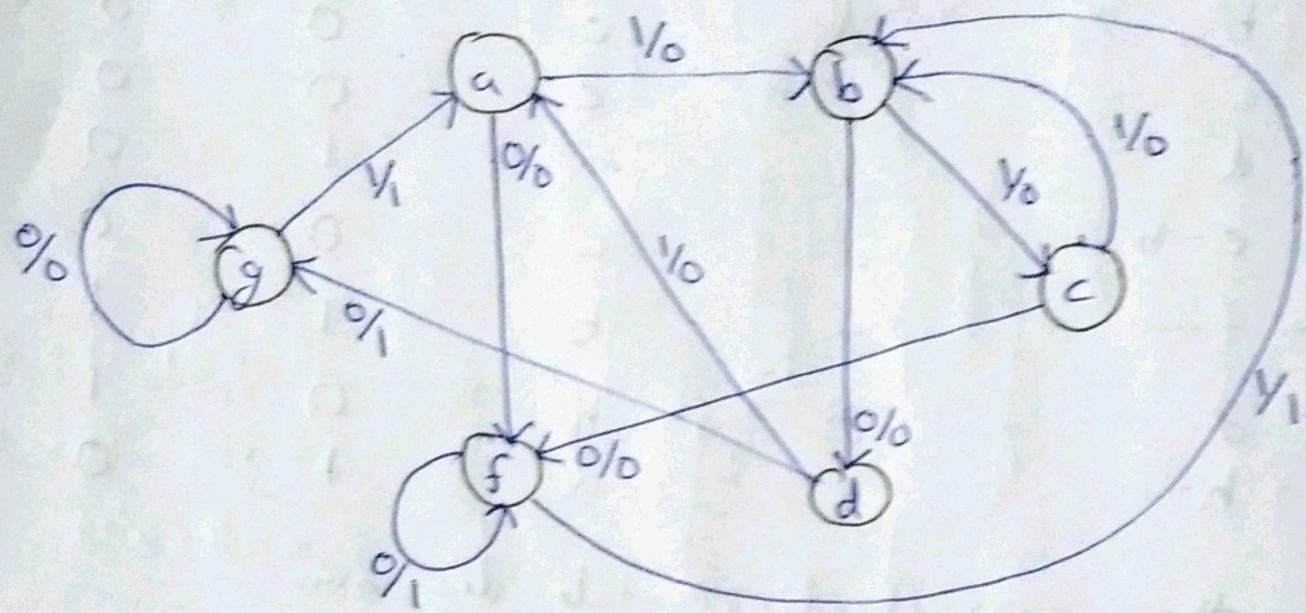


b) Tabulate the reduced state table.

Present state

	Next S state		Output	
	$n=0$	$n=1$	$n=0$	$n=1$
a	f	b	0	0
b	d	c	0	0
c	f	b	0	0
d	g	a	1	0
f	f	b	1	1
g	g	a	0	1

Q) Draw the state diagram corresponding to the reduced state table.



Q) Write and verify an HDL Behavioural description of a positive edge sensitive D-flip flop, T-flip flop and JK-flip flop.