DIGITAL LOGIC DESIGN LAB (EET1211)

LAB II: Examine & Analyze Advantages of Gate Level Minimization for Boolean Function

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Branch:			Section:
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Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE:

1. Construct a circuit using basic gates that implements the Boolean function given below and record the output for all sets of input.

   $F = AB + AB'C$

   a. Simplify the Boolean function using minimization technique.

   b. Construct the circuit for the simplified expression using basic gates & verify the truth table.

2. Simplify the following Boolean functions to minimum number of literals and design the circuit using basic gates.

   a) F= XY +X′Z+YZ

   b) F= (X′Y′+Z) ′+Z+XY+WZ

3. Consider two Boolean functions in sum-of-min terms form:

   F1 (A, B, C, D) = (0, 1, 2, 3, 4, 6, 8, 9, 10, 11)

   F2 (A, B, C, D) = (3, 5, 7, 8, 10, 11, 13, 15)

   a. Implement both the functions using a minimum number of NAND ICs & verify the truth tables.

   b. Implement both the functions using minimum number of basic gates.

II. PRE-LAB

For Obj. 1:

a. Draw the circuit diagram.

b. Obtain the truth table for F as function of 3 inputs.

c. Simplify the Boolean function using Boolean algebra rules & verify the correctness of the simplified expression using truth table.

d. Draw the logic diagram of simplified Boolean expression

For Obj. 2:

a) Draw the circuit diagram and obtain the truth table for all input combinations.

b) Simplify the functions.

c) Draw the circuit & write truth table for minimized functions.

For Obj. 3:

a) Simplify the given expressions using k-map.

b) Obtain a composite logic diagram with four inputs, A, B, C and D, and two outputs, F1, and F2. Obtain truth tables for both the functions.

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

Observation:

Conclusion:

IV. POST LAB:

1. What is the advantage of Boolean laws?

2. What is a K-map? What are its advantages and disadvantages?

 3. What ways can Boolean expressions be represented?

4. Implement two input Ex-NOR gate using minimum number of two input NOR

gates.