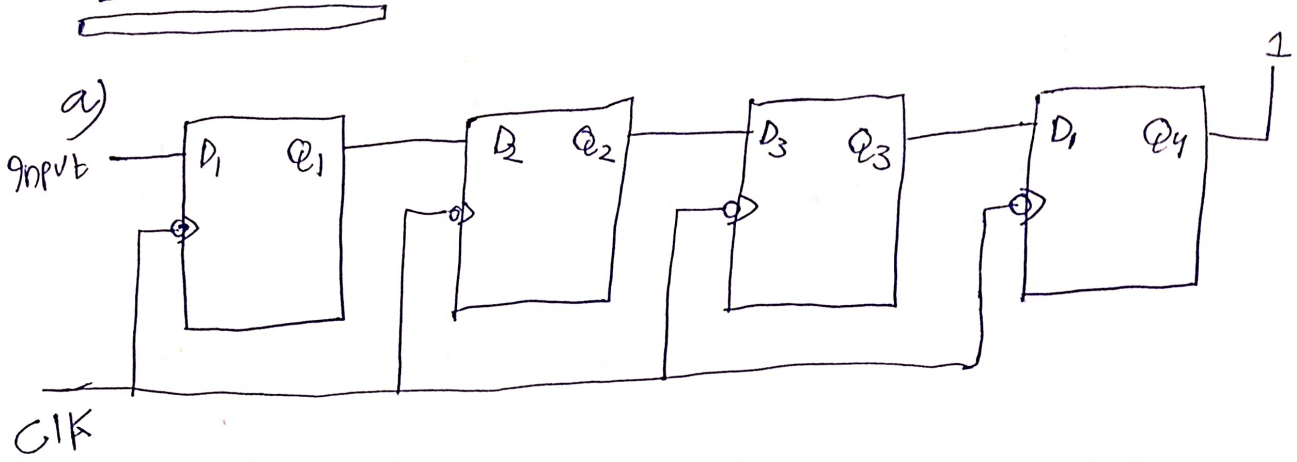
Lab - 8

II. PRE-LAB

a)



b)

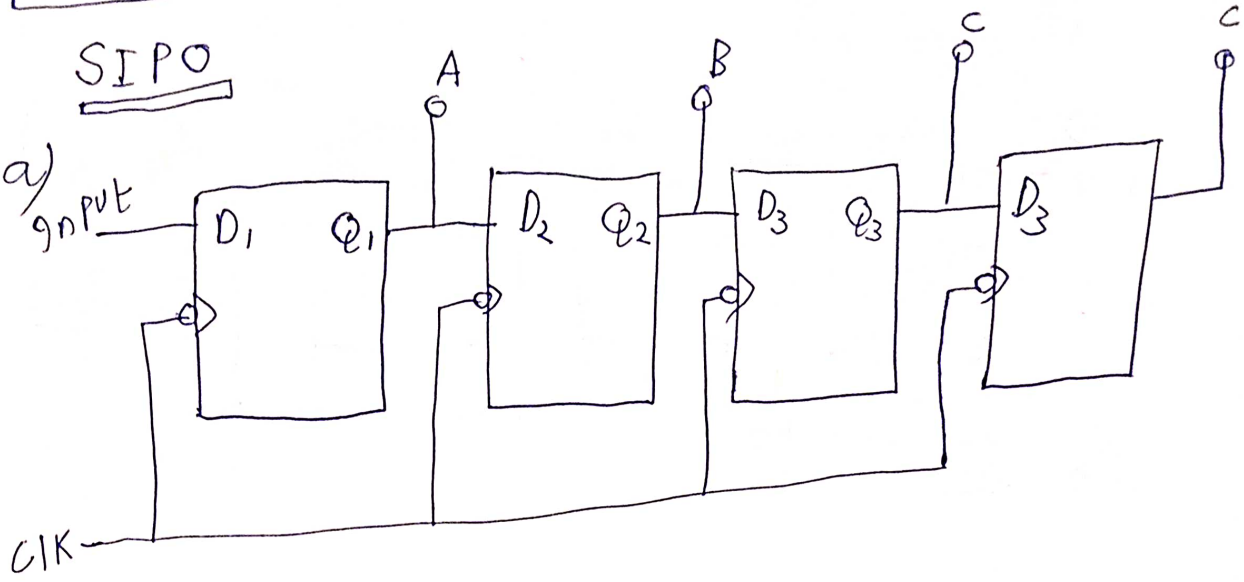
```
module sisomod (CLK, Clear, Si, So);
  input CLK, Si, Clear;
  output So;
  reg So;
  reg [3:0] tmp;
  always @ (posedge CLK)
  begin
  if(Clear)
  tmp <= 4'b0000;
  else
   temp <= tmp << 1;
   temp[0] <= Si;
   So = tmp[3];
  end
  end module
```

(2)

Obj - II

SIPO

a)

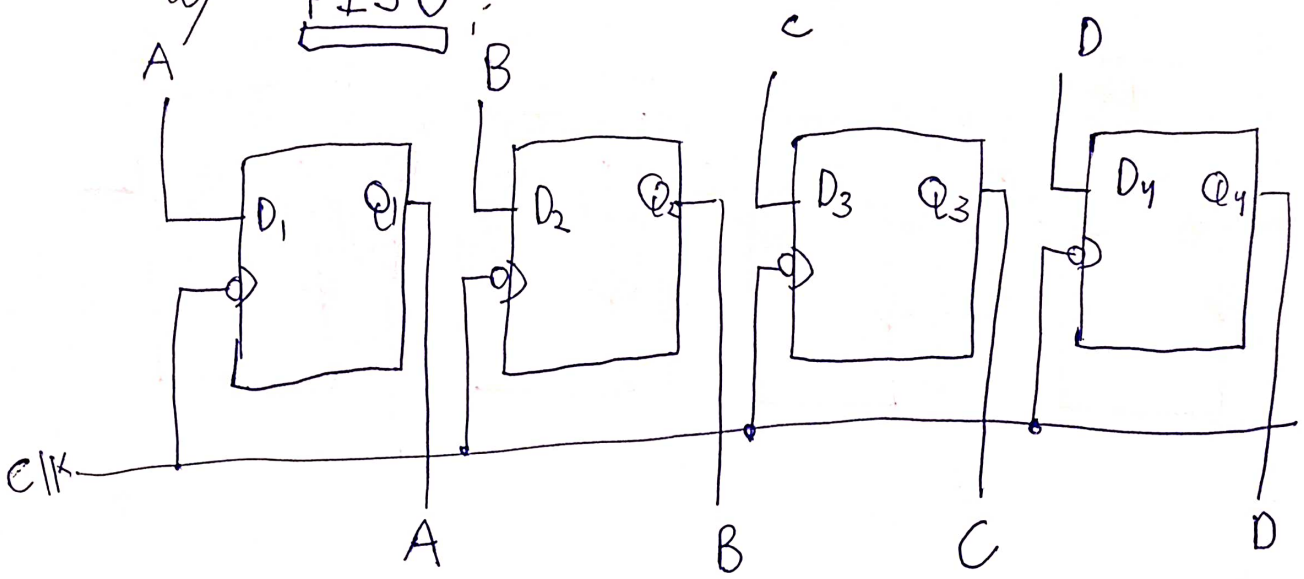


b)

```
module sipomod(clk, clear, si, po);
  input clk, si, clear;
  output[3:0] po;
  reg [3:0] tmp;
  reg [3:0] po;
  always @(posedge clk)
   begin
   if (clear)
   temp<= 4'b0000;
    else
    temp <= tmp << 1;
    tmp[0] <= si;
    po = tmp;
   end
   endmodule.
```

Obj - III :

a) PISO :

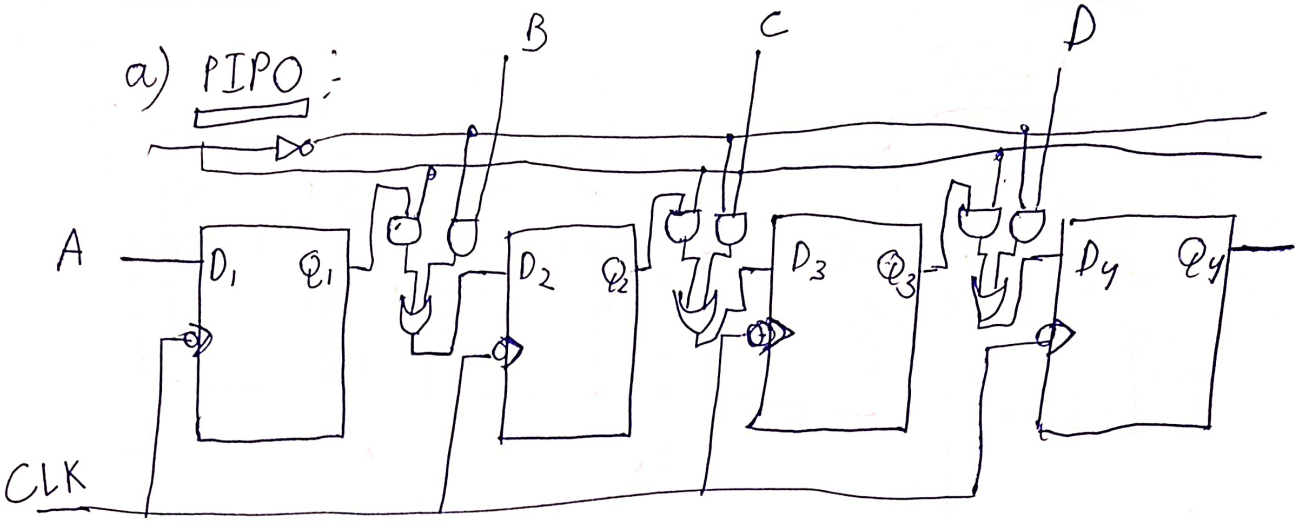


b)
```
module shiftRegister_SIPO(c, SI, PO);
    input c, SI
    output [7:0]PO;
    reg [7:0] tmp;
    always @(posedge c)
    begin
        tmp = {tmp[6:0], SI};
    end
    assign PO = tmp;
endmodule.
```

(4)

Obj - 4

a) PIPO :



b)
```
module ShiftRegister_PIPO (clk, Pi, Po);
    input clk;
    input [3:0] Pi
    output reg [3:0] Po;
    always @(posedge clk)
    begin
        Po = Pi;
    end
endmodule.
```

III LAB;

Components Required;

S. No	Name of the component	specification	Quantity
1	Bread board	–	1
2	D-flip-flop	7474	2
3	AND	7408	2
4	OR	7432	1

CONCLUSION

Obj-I :-

The SISO configuration allows for the serial input of data, which is then shifted through the registers & output in a serial manner.

Obj-II :-

The SIPO configuration allows for the serial input of data, which is then shifted through the registers and output in parallel.

Obj-III :-

The PISO configuration allows for the parallel input of data, which is then shifted through the registers and output in a serial manner.

Obj-IV :-

The PIPO configuration allows for the parallel input of data, which is then shifted through the registers and output in parallel.

IV POST LAB

I) B/0010

II) B/0111

III) C/0000