COURSE HANDBOOK

ON

DIGITAL LOGIC DESIGN (EET 1211)

(3rd Semester)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Faculty of Engineering and Technology,

Institute of Technical Education and Research

SIKSHA 'O' ANUSANDHAN (DEEMED TO BE) UNIVERSITY

Bhubaneswar, Odisha, India

(JULY 2022)

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PREFACE

This course handbook contains all the necessary details of the concerned subject, i.e., Digital Logic Design (EET 1211). It is designed in order keep up with the Outcome Based Education **(OBE)**. The handbook provides necessary details about the Grading Pattern, Grading System, Course Assessment, Assessment Rubrics, the Outcomes (POs, PEOs, PSOs), Bloom's Taxonomy, Graduation CGPA requirements, Minimum Requirements for Passing Grade and Appearing the (Deemed to be University) Examination.

1. Course Details

Name of the Course : Digital Logic Design

Course Code : EET 1211

Course Credits : 4

Grading Pattern : 1

Branch and Semester : Computer Science and Engineering, 3rd Semester

Name of the Instructor: Dr. Meryleen Mohapatra

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<table>
<tr><th>SUBJECT CODE</th><th>SUBJECT NAME</th><th>CREDIT</th><th>GRADING PATTERN</th></tr>
<tr><td>EET 1211</td><td>Digital Logic Design</td><td>4</td><td>1</td></tr>
<tr><td colspan="2" rowspan="2">Digital Systems and binary numbers, Boolean Algebra and logic gates, Gate level minimisation, Combinational Logic, Synchronous Sequential Logic, Registers and Counters, Memory and Programmable Logic : PLA and PLL, Design at the register transfer level
Labs from this textbook : 17 Laboratory Experiments with Standard ICs and FPGAs</td><td colspan="2">Text Book:
– Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog by Mano, 6th Edition, Pearson</td></tr>
<tr><td colspan="2">Course Format:
3 Classes/Week, 1 hr/Class; 1 Lab Session/Week, 2 hrs/ Lab session = 4 Credits</td></tr>
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2. Course Outcomes (COs) and Mapping Course Outcomes with Program Outcomes (POs)

Course Outcomes		Program Outcomes
CO1	Able to State and explain different number systems, binary codes	PO1
CO2	Able to apply the principles of Boolean algebra and Karnaugh map to simplify logic expressions and implement it using gates	PO1, PO2
CO3	Able to Analyse and design various combinational circuits	PO1, PO2, PO3
CO4	Able to Analyse and design different synchronous and asynchronous sequential circuits	PO1,PO2, PO3
CO5	Able to Analyse and design various Memory, Programmable Logic circuits and register transfer level	PO1,PO2, PO3
CO6	Able to implement various digital circuits using HDL and Standard ICs.	PO1, PO2, PO3, PO5,PO9

*Refer Appendix for list of POs

3. Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	0	0	0	0	0	0	0	0	0	0	0	1	0
CO2	3	1	0	0	0	0	0	0	0	0	0	0	1	0
CO3	3	2	2	0	0	0	0	0	0	0	0	0	1	0
CO4	3	2	2	0	0	0	0	0	0	0	0	0	1	0
CO5	3	2	1	0	0	0	0	0	0	0	0	0	1	0
CO6	3	3	3	0	3	0	0	0	1	0	0	0	1	0

*0: No correlation, 1: Slight (Low), 2: Moderate, 3: Substantial (High)

*Refer Appendix for list of POs

4. Grading Pattern and Components of Evaluation

The Subject, Digital Logic Design (EET 1211), has 4 Credits, and belongs to Grading Pattern 1. The **First Grading Pattern** will be for those Subjects which are of 4 credits and which combinations of theory and laboratory components are. The breakdown required for the calculation of the Numeric Score (out of 100) for Grading Pattern 1 is given below.

ATTENDANCE	5
MAJOR LAB / SESSION ASSIGNMENTS / QUIZZES	10
MINOR ASSIGNMENTS	10
MID TERM	15
TOTAL INTERNAL	40

IN LAB EXAM	15
THEORY EXAM	45
TOTAL EXTERNAL	60

5. Tentative Lesson Plan

Lecture/Lab #	Tasks	Mapping with COs
Lecture # 1	Number System: Number Base Conversions - Decimal to other number system conversion and vice versa - Binary to Octal - Binary to Hexadecimal	**CO1**
Lecture # 2	Binary arithmetic(addition and subtraction) - Complements of Numbers (r and r-1complement)	**CO1**
Lecture # 3	Subtraction using complement (1s&2s)	**CO1**
Lab # 1	Introduction to Different ICs and Xilinx Tool	**CO1**
Lecture # 4	Binary Codes	**CO1**
Lecture # 5	Boolean Algebra & Logic Gates: Basic Definitions, Basic Theorems and Properties of Boolean Algebra	**CO2**
Lecture # 6	Boolean functions, Simplification of Boolean functions using Boolean Algebra rules	**CO2**
Lab # 2	Examine the operation of logic gates	**CO2**
Lecture # 7	Introduction to Hardware Description Language	**CO2, CO6**
Lecture # 8	Complement of Boolean Function,	**CO2**
Lecture # 9	Canonical and standard form, HDL Description of Boolean Functions	**CO2, CO6**
Lab # 3	Examine & analyze advantages of gate level minimization for boolean function	**CO2**
Lecture # 10	Other Logic operations, Digital Logic gates,	**CO2**

	Integrated Circuits	
Lecture # 11	Gate Level Minimization Simplification of Boolean functions using Map method (Two variable map method), HDL Description of Simplified Boolean Functions	**CO2, CO6**
Lecture # 12	Gate Level Minimization Simplification of Boolean functions using Map method (Three variable map methods), HDL Description of Simplified Boolean Functions	**CO2, CO6**
Lab # 4	Design, construct & test the combinational circuit to solve a given problem	**CO2**
Lecture # 13	Simplification of Boolean functions: 4 variable maps, Concept of 5 and 6 variable map, HDL Description of Simplified Boolean Functions	**CO2, CO6**
Lecture # 14	Simplification of Boolean functions using K map with don't care conditions, HDL Description of Simplified Boolean Functions	**CO2, CO6**
Lecture # 15	SOP & POS implementation using NAND & NOR gates, HDL Description of the circuit.	**CO2, CO6**
Lab # 5	Construct and test various binary adder and subtractor circuits	**CO2**
Lecture # 16	Multilevel NAND, NOR circuits, Exclusive OR and Equivalence Functions, HDL Description of the circuit.	**CO2, CO6**
Lecture # 17	Introduction to Combinational Logic- Combinational circuit analysis and design procedure, HDL Description of the circuit	**CO3, CO6**
Lecture # 18	Binary Adder, Binary Subtractor, HDL Models for adder and Subtractor	**CO3, CO6**
Lab # 6	Design and test various code converter circuits	**CO3**
Lecture # 19	Code conversion and Analysis Procedure	**CO3**
Lecture # 20	Binary Parallel adder, HDL Models for Binary Parallel Adder	**CO3, CO6**
Lecture # 21	Decimal Adder	**CO3**
Lab # 7	Design of magnitude comparator, decoder and multiplexer circuit	**CO3**
Lecture # 22	Magnitude Comparator, HDL Models of Magnitude Comparator	**CO3, CO6**
Lecture # 23	Decoders, Combinational Logic design using Decoders	**CO3**
Lecture # 24	Encoders HDL Models for Combinational Circuits (Decoder, Encoder)	**CO3, CO6**
Lab # 8	Construct, test and investigate the operation of various flip-flop circuits	**CO3**
Lecture # 25	Multiplexers, Combinational Logic design using Multiplexers, HDL Models for Combinational Circuits using MUX	**CO3, CO6**
Lecture # 26	Introduction to Sequential Circuits, Storage Elements: Latches, HDL Description of Latch	**CO4, CO6**
Lecture # 27	Storage Elements: Flip Flops RS flip-flop (Graphical Symbol, Logic Diagram, Function Table,	**CO4, CO6**

	Characteristics Table, Characteristics Equation, Excitation table) HDL Description of RS Flip Flop	
Lab # 9	Construct, test and investigate the operation of various shift register circuits	**CO4**
Lecture # 28	Storage Elements: Flip Flops JK flip-flop (Graphical Symbol, Logic Diagram, Function Table, Characteristics Table, Characteristics Equation, Excitation table) HDL Description of JK Flip Flop	**CO4, CO6**
Lecture # 29	Storage Elements: Flip Flops D and T flip-flop (Graphical Symbol, Logic Diagram, Function Table, Characteristics Table, Characteristics Equation, Excitation table) HDL Description of Flip Flops	**CO4, CO6**
Lecture # 30	Analysis of clocked Sequential Circuits contd. State Reduction and Assignment	**CO4**
Lab # 10	Design of synchronous sequential circuits	**CO4**
Lecture # 31	Design Procedure of clocked sequential circuit Register, Shift Registers, HDL Models for Shift Register	**CO4, CO6**
Lecture # 32	Design of Ripple Counters with timing sequences	**CO4**
Lecture # 33	Design of Synchronous counters	**CO4**
Lab # 11	Design of various counter circuits	**CO4**
Lecture # 34	Design of Synchronous counters contd. HDL Models for Counters	**CO4, CO6**
Lecture # 35	Memory: Random Access Memory, Read Only Memory, Programmable Logic Array	**CO5**
Lecture # 36	Programmable Array Logic, HDL Description for Read and write operations of memory. Design at the register transfer level.	**CO5, CO6**
Lab # 12	Internal Lab Evaluation	

6. Assessment Rubric for the Course

Method: Assignments, Lab Report and Mid-Semester and End-Semester Exam

Outcomes Assessed:

PO1 – Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 – Problem analysis: Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 – Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate

consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO5 – Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO9 - Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PSO1- The ability to understand, analyse and develop computer programs in the areas related to business intelligence, web design and networking for efficient design of computer-based systems of varying complexities.

PSO2- The ability to apply standard practices and strategies in software development using open-ended programming environments to deliver a quality product for business success.

Mid-Semester and End-Semester Examination Rubrics			
Performance	**High (2 Marks)**	**Medium (1-1.5 Marks)**	**Low (0.5 Marks)**
Theoretical representation of concepts	Properly able to define, represent, and interpret the physical significance.	Minor errors in definition, representation and interpretation of physical significance.	Incomplete or poor definition, representation and interpretation of physical significance.
Pictorial representation of ideas	Circuits are drawn with proper labelling and interpretation.	Circuits are drawn but interpretation of significance is not done or labelling is missing.	The circuits are unclear/not labelled and the interpretation is inappropriate.
Solving mathematical and/or design problems and interpreting the results	Selection of appropriate concepts to formulate. Ability to solve problems, represent them pictorially and interpret the results.	Able to select correct concepts, formulate, represent and solve, but error in interpreting	Erroneous selection of concepts, able to represent and formulate only, but error in solving.

Rubrics for Lab Component			
Performance	**High (9-10 Marks)**	**Medium (7-8 Marks)**	**Low (4-6 Marks)**
Lab Experiments and Report	Student demonstrates an accurate understanding of the lab objectives and concepts. Questions answered completely and correctly. Output waveforms are neat, creative and include complete titles and accurate units. Errors, if any, are minimal.	Student has a basic knowledge of content, but may lack some understanding of the same concepts. Questions are answered fairly well and/or Output waveforms could have been done more neatly, accurately or with more complete information.	Student has problems with both the graphs and the answers. Student appears to have not fully grasped the lab content, and the Output waveforms possess multiple errors. Student turns in lab report late or the report is so incomplete and/or so inaccurate that its unacceptable.
Lab Participation and Presentation	Student demonstrates an accurate understanding of the lab objectives and concepts. The student can correctly answer questions and if appropriate, can explain concepts to fellow classmates. Student is eager to participate and assist when needed. The student has attended all labs.	Student arrives on time to lab, but maybe unprepared. Answers to questions are basic and superficial suggesting that concepts are not fully grasped. The student has missed few (2-3) lab classes.	The unpreparedness of student makes it impossible to fully participate. If able to participate, student has difficulty explaining key lab concepts. The student has missed many (5-6) lab classes.
Viva-voice	The student is able to answer all the asked questions pleasingly, and explains all the concepts reasonably well, and in details.	Is able to answer some of the asked questions satisfactorily, and explains the concepts well.	The student doesn't understand the concepts and hence answers the questions but the logic or is concept explanation provided is improper.

Rubrics for Quiz			
Performance	**High (9-10 Marks)**	**Medium (7-8 Marks)**	**Low (4-6 Marks)**
Short/Long Answer Type Questions	The student has answered all the questions correctly and depicted them in a neat and clean manner, with appropriate explanation.	The student has answered most of the questions correctly and depicted them in a satisfactory manner.	The student has answered some of the questions correctly, though, with improper /erroneous/incomplete justification of the same.
MCQ Type Questions	The student has attended all the quizzes and attempted all the questions correctly.	The student has attended most of the quizzes and attempted most of the questions correctly.	The student has attended some of the quizzes and answers few of the questions correctly.

Rubrics for Assignments			
Performance	**High (9-10 Marks)**	**Medium (7-8 Marks)**	**Low (4-6 Marks)**
Completion and Submission of Assignments	Completed and submitted all assignments within deadline. The answers are depicted correctly, completely and in a neat and clean manner. The answers maybe unique/innovative.	Completed and submitted above 80% of the assignments. Submission is by the due date. The answers were fairly represented.	Completed 60% of the assignments. The submissions were made after repeated reminders, and in the extended deadline period. The answers were fairly represented.

Rubrics for Mini Project			
Performance	**High (9-10 Marks)**	**Medium (7-8 Marks)**	**Low (4-6 Marks)**
Articulate problem statements and identify objectives	Problem statement is clear and objectives are completely defined.	Problem statement is clear and objectives are not in line with problem statement.	Problem statement and objectives are not clear.
Identify engineering systems, variables, and parameters to solve the problems	Engineering systems are identified. Variables, and parameters to solve the problems are completely defined .	Engineering systems are clear. Variables, and parameters to solve the problems are not defined.	Engineering systems are identified but not clear. Variables, and parameters to solve the problems are not defined
Apply formal idea generation tools to develop multiple engineering design solutions	Able to generate engineering designs with justification.	Able to use the tool but not able to generate engineering designs.	Able to identify but not able to use it effectively.
Build models/ prototypes to develop diverse set of design solutions	Able to generate and justify the best solution.	Able to use the tool but not able to generate alternatives.	Able to choose the tool but not able to use it effectively.
Generate information through appropriate tests to improve or revise design	Able to apply information for the improvement.	Able to follow testing procedures but not able to collect information.	Able to identify but not able to follow testing procedure.
Analyze data for trends and correlations, stating possible errors and limitations	Able to identify errors and limitations.	Able to analyze data but not able to correlate them.	Able to understand but not able to analyze data.
Present results as a team, with smooth integration of contributions from all individual efforts.	Contribution from an individual to a team is good and results in an integrated team presentation.	Contributions from an individual to a team is moderate.	Contributions from an individual to a team is minimal.

Note – For specific assessments, specific rubrics may be followed.

7. Course Related Surveys

Pre-requisite Survey: The objective of this survey is to know the basic understanding and different skills relevant to the subject, i.e., Digital Logic Design (EET 1211). Please respond to the questions by clicking any one of the options against each of the following questions.

1. Ability to apply theoretical knowledge in day-to-day life (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

2. Multidisciplinary skills and ability to work in a team (PO9).

(a) Low Understanding (b) Medium (c) Adequate/High

3. Ability to think and solve logical problems (PO1, PO2).

(a) Low Understanding (b) Medium (c) Adequate/High

4. Knowledge about simulation skills (PO5).

(a) Low Understanding (b) Medium (c) Adequate/High

5. Basic knowledge about the Number System and Boolean Algebra (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

6. Basic knowledge about logic gates (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

7. Basic knowledge about Integrated Circuits (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

8. Understanding of basics of combinational circuits (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

9. Knowledge about Encoder and Decoder (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

10. Knowledge about how counter works? (PO1).

(a) Low Understanding (b) Medium (c) Adequate/High

Interim Course Progress Survey: The objective of this survey is to know the students' progress in basic understanding and attaining different outcomes relevant to the subject, i.e., Digital Logic Design (EET 1211). Please respond to the questions by clicking any one of the options against each of the following questions. The outputs will be shared with the respective Faculty Advisors for further necessary actions.

Course End Survey: The objective of this survey is to know the attainment of the outcomes relevant to the subject, i.e., Digital Logic Design (EET 1211). Please respond to the questions by clicking any one of the options against each of the following questions.

APPENDIX I – VISION

The Siksha 'O' Anusandhan will be a leading institution of higher learning in its chosen areas of concentration, preparing future generations through quality teaching and innovative research and will emerge as a comprehensive and socially inclusive University in the country for professional advancements in related disciplines.

APPENDIX II – MISSION

- Educate students to become responsible, enlightened, and productive citizens;
- Conduct scholarship and promote entrepreneurship that improve the human condition;
- Serve business, education, government, health care systems, and community; and
- Enhance the cultural environment of the region.

APPENDIX III – PROGRAM EDUCATIONAL OBJECTIVES (PEO)

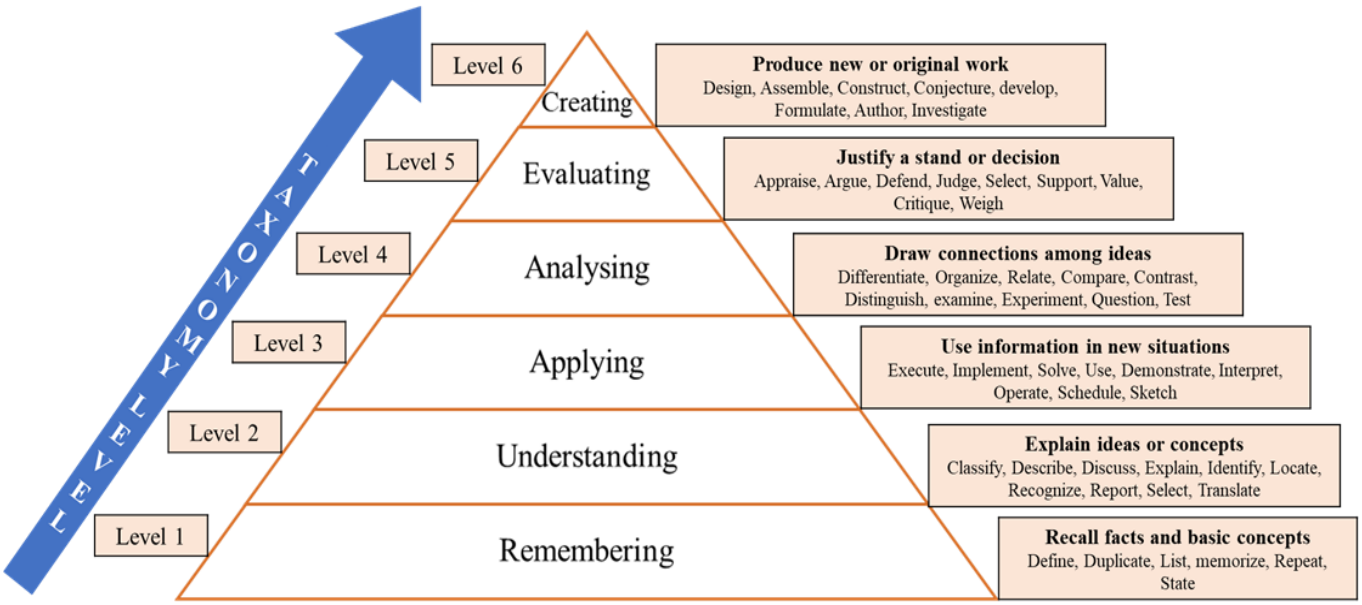
1	Our Graduates will have successful professional careers in industry, government, academia or non-profit organisations.
2	Our Graduates will effectively lead, work and communicate in multidisciplinary teams and apply sound engineering principles and design methodology to solve societal problems.
3	Our Graduates will maintain currency in their chosen field through higher study, through organizational participation and through participation in professional developmental activities.

APPENDIX IV – PROGRAM SPECIFIC OUTCOMES (PSO)	
PSO1	The ability to understand, analyse and develop computer programs in the areas related to business intelligence, web design and networking for efficient design of computer-based systems of varying complexities.
PSO2	The ability to apply standard practices and strategies in software development using open-ended programming environments to deliver a quality product for business success.

APPENDIX V – PROGRAM OUTCOMES (PO)	
POs	**Description**
PO1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the

	limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues, and the consequent responsibilitiesrelevant to the professional engineering practice.
PO7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, andneed for sustainable development.
PO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and teamwork:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and giveand receive clear instructions.
PO11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

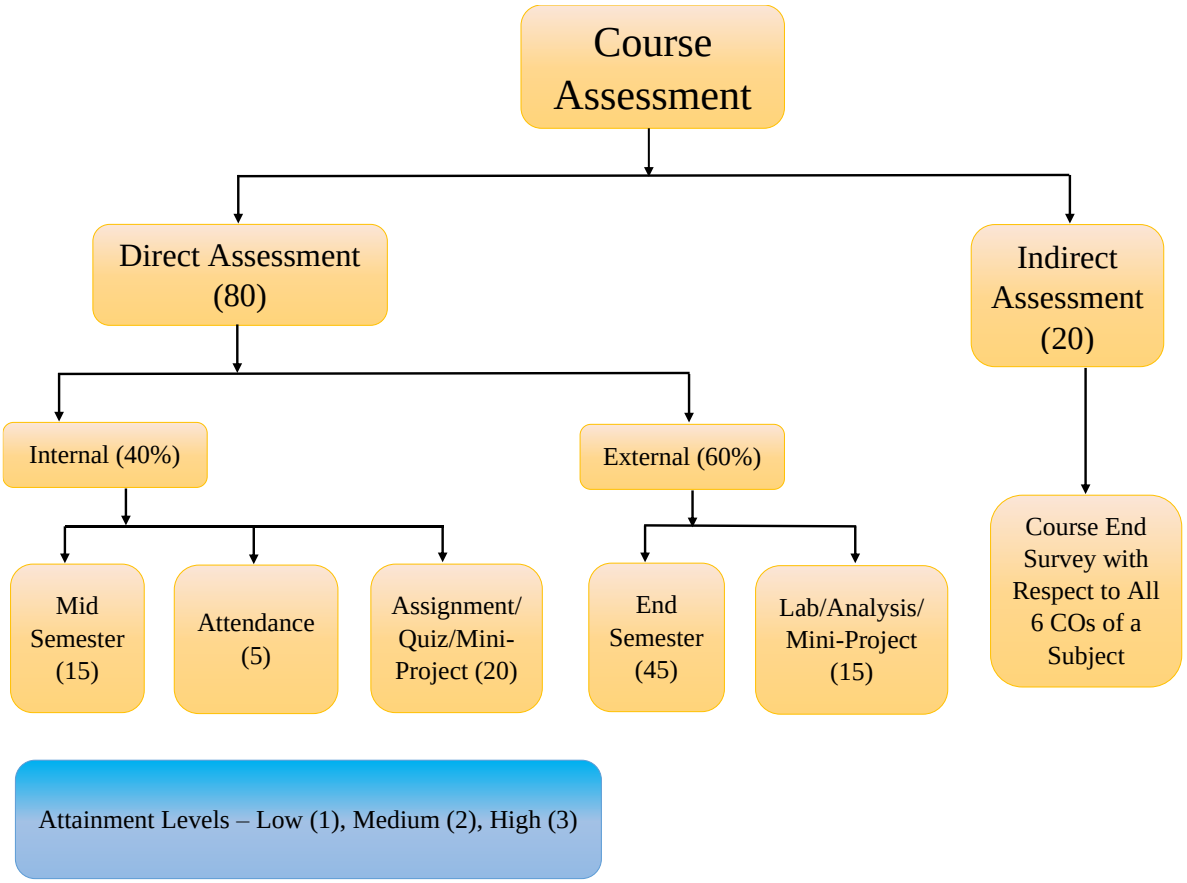
APPENDIX VI – BLOOM'S TAXONOMY



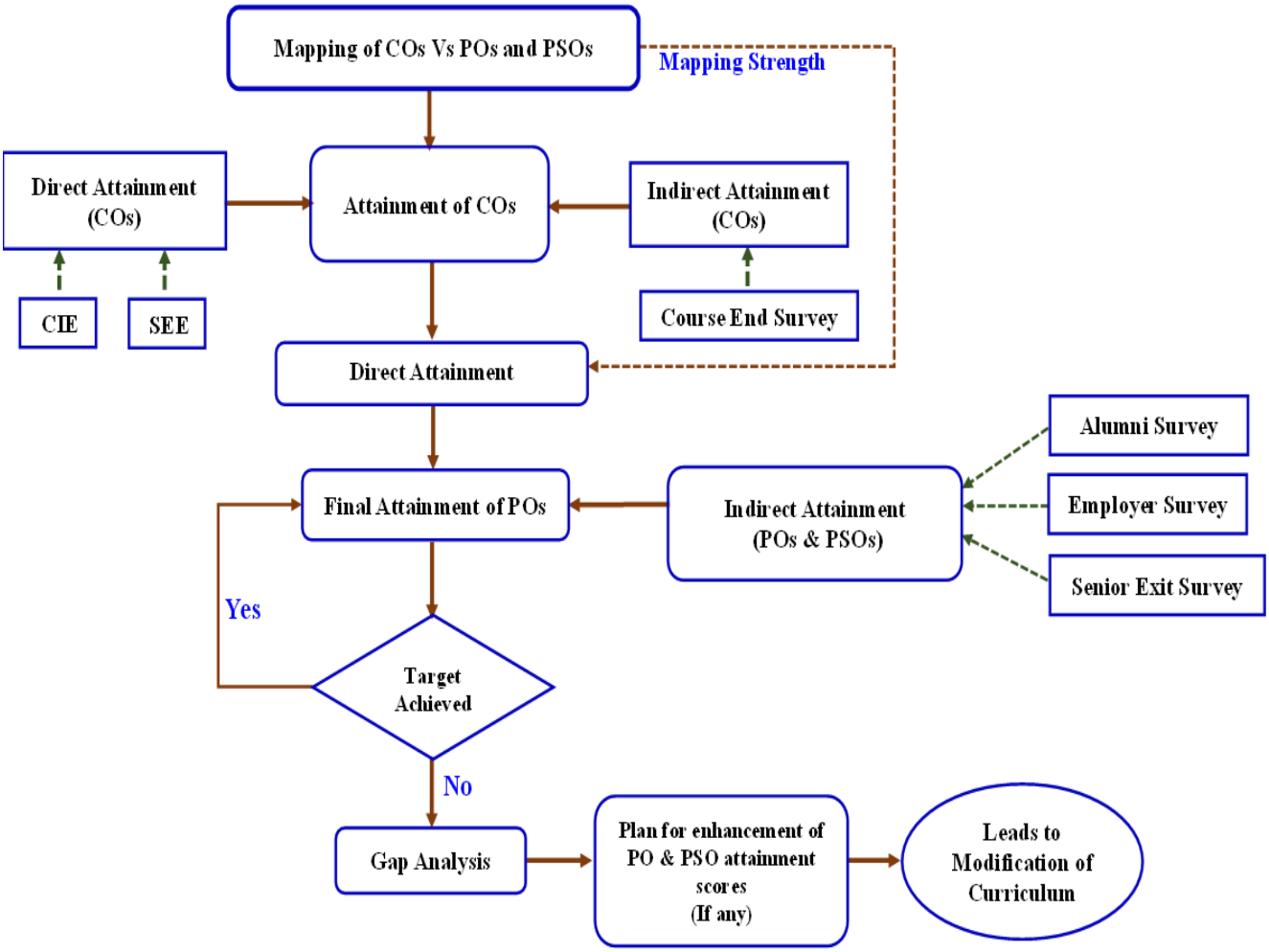
In this subject, Levels 1–4 of Bloom's Taxonomy, i.e., Remembering–Analysing are covered.

APPENDIX VII – COURSE ASSESSMENT

(FOR GRADING PATTERN 1)



APPENDIX VIII – ATTAINMENT OF COs, POs, & PSOs



APPENDIX IX – GRADING SYSTEM

Performance	Letter grade	Grade Point Per Credit
Outstanding	O	10
Accomplished	A	9.5
Impressive	B	8.5
Encouraging	C	7.5
Acceptable	D	6.5
Must do better	E	5.5
Fail	F	0

PERCENTAGE EQUIVALENCE CONVERSION FOR CGPA:

Percentage of Marks = CGPA Multiplied by 10

APPENDIX X – 9.1.2 RELATIVE GRADING

LETTER GRADE	STUDENTS RANGE	GRADE POINT
O	Top 5%	10
A	Next 10%	9.5
B	Next 20%	8.5
C	Next 30%	7.5
D	Next 20%	6.5
E	Remaining Students having Numeric Score >= 40	5.5
F	Numeric Score < 40	0

The minimum possible cutoff used for “E” grade is 40 (Internal + External), i.e., if the marks obtained are less than 40 (Internal + External) then the student won't be given an "E" grade (or above) in a particular instance of the Subject irrespective of value of cutoff for “E” grade.

The Relative Grading System will only be applicable for those subjects which follow Grading Patterns 1, 2, and 6. For Relative grading to be applicable, the number of students in the subject will need to be at least 12. Absolute Grading will be applicable otherwise.

APPENDIX XI – 10. GRADUATION CGPA REQUIREMENTS

The Minimum Cumulative Grade Point Average required for Graduation is **6.0**, i.e., a student can only be considered for graduation if and only if his/her Cumulative Grade Point Average (after complying with all the requirements of the (Deemed to be University) and the Constituent College required for graduation) is **greater than or equal to 6.0 (six point zero)**.

APPENDIX XII – 12. MINIMUM REQUIREMENTS FOR A PASSING GRADE

The Minimum Attendance and Numeric Score Requirements for a passing grade at Institute of Technical Education and Research (ITER), Siksha ‘O’ Anusandhan (Deemed to be University) which will be followed from admission year 2018-2019.

NUMERIC SCORE REQUIREMENTS	
INTERNAL	16
EXTERNAL	24
TOTAL	40

ATTENDANCE REQUIREMENTS	
ATTENDANCE	75%

APPENDIX XIII – 15. APPEARING THE (DEEMED TO BE UNIVERSITY) EXAM

The Minimum Numeric Score and Attendance Requirements for appearing the External Exam of a subject are as mentioned below.

NUMERIC SCORE REQUIREMENTS (For External Exam)	
INTERNAL COMPONENT	16

ATTENDANCE REQUIREMENTS (For External Exam)	
ATTENDANCE	75%