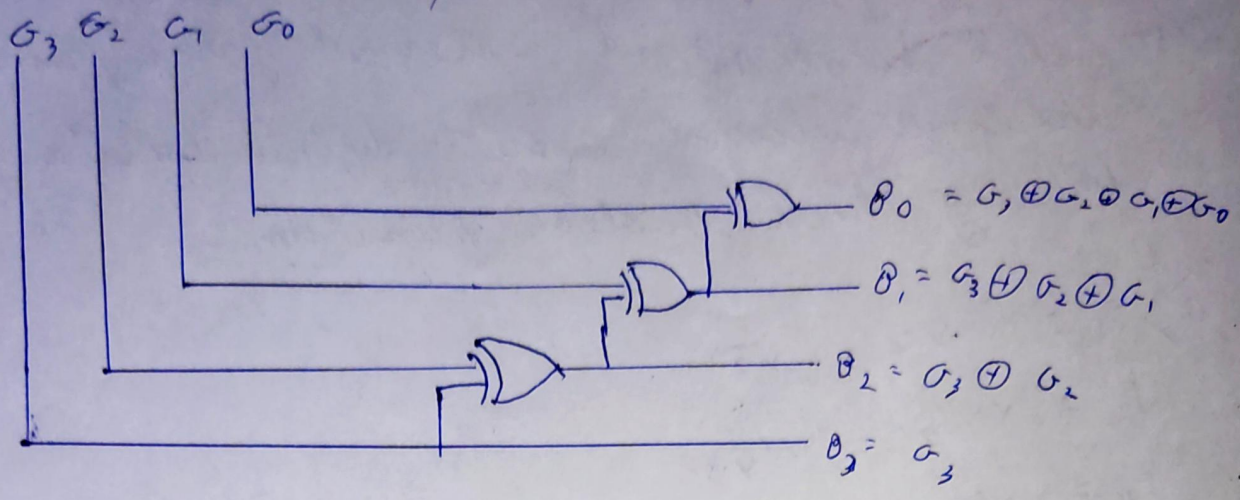
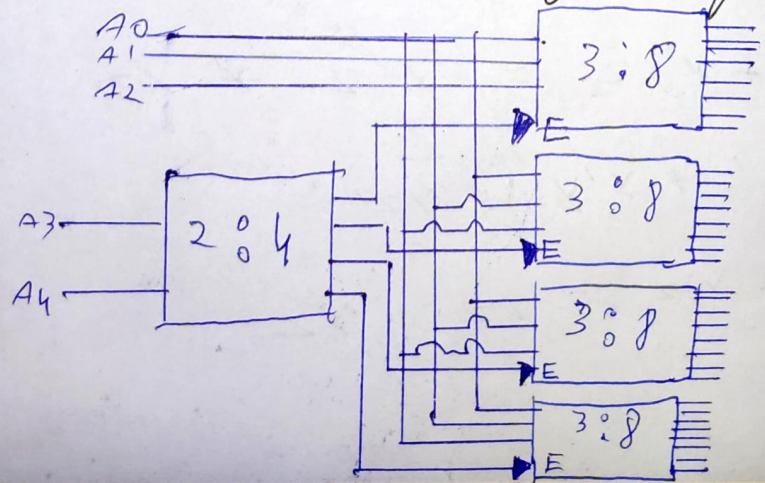
Q15 Design a combinational circuit that converts a 4-bit gray code to a 4-bit binary number. write the verilog data flow model of the circuit




```
module Q_15 (G3, G2, G1, G0, B3, B2, B1, B0);
  input G3, G2, G1, G0;
  output B3, B2, B1, B0;

  assign B3 = G3;
  assign B2 = G3 ^ G2;
  assign B1 = G3 ^ G2 ^ G1;
  assign B0 = G3 ^ G2 ^ G1 ^ G0;
endmodule
```

Q16 Construct a decoder of 5-to-32 with four 3-to-8 line decoder and a 2-to-4 line decoder. Use block diagram for the components

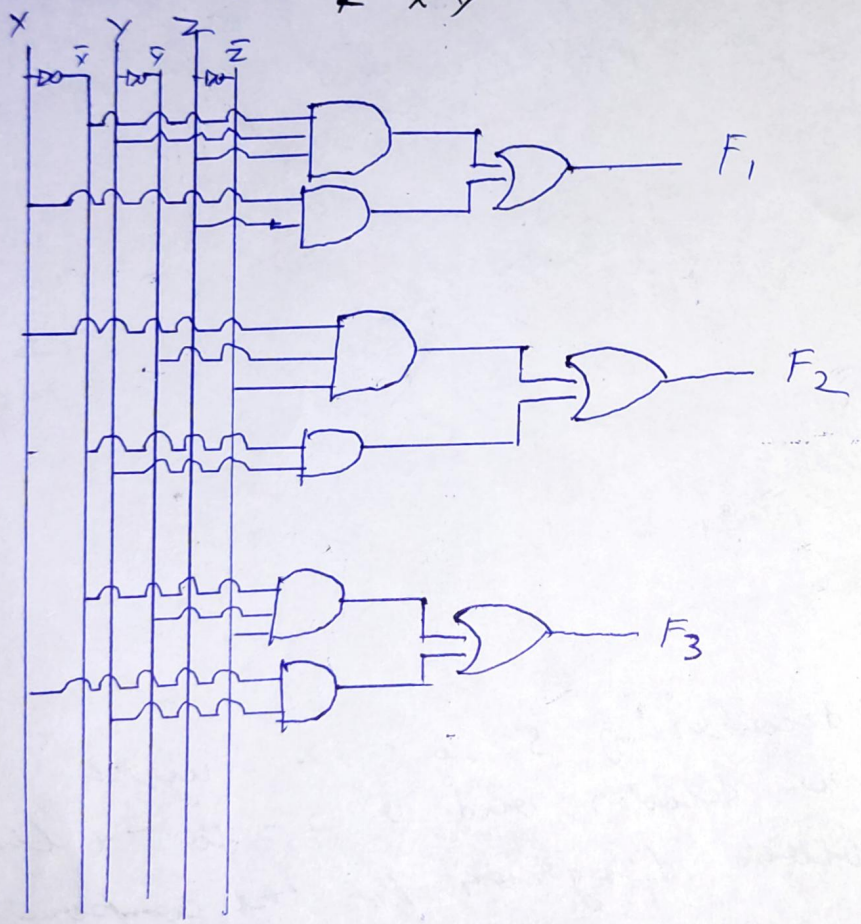


Q17 Use decoder and external gates, design the combinational circuit defined by the following three boolean function

a) $F_1 = x'yz' + xz$

$F_2 = xy'z' + x'y$

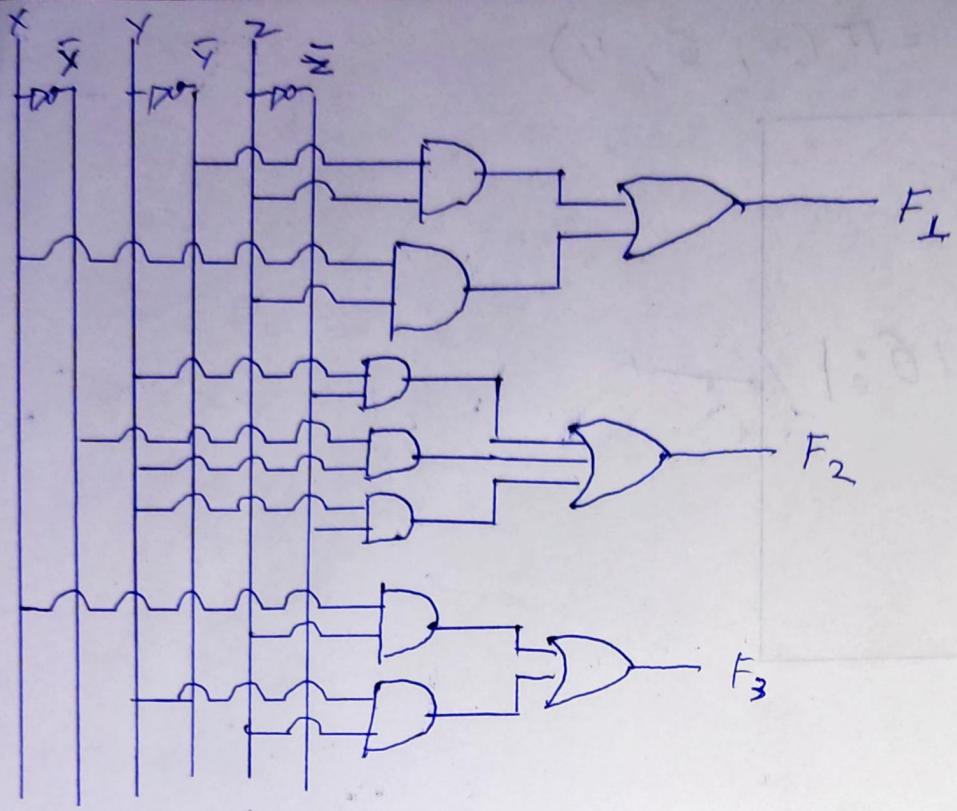
$F_3 = x'y'z' + xy$



b) $F_1 = (y' + x)z = y'z * xz$

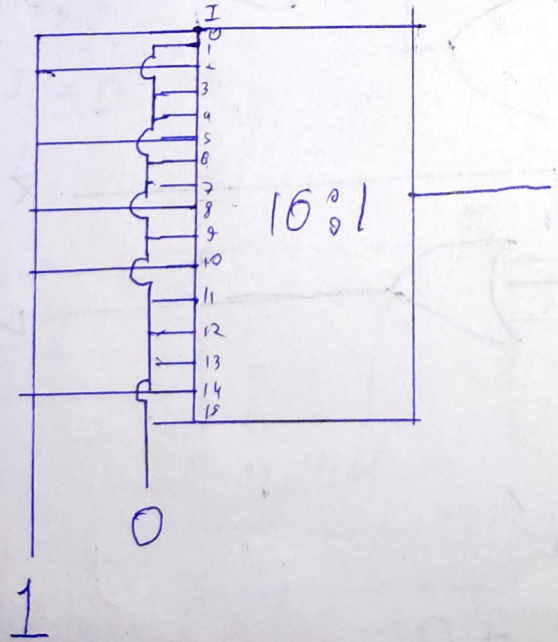
$F_2 = y'z' + x'y + yz'$

$F_3 = (x + y)z = xz + yz$

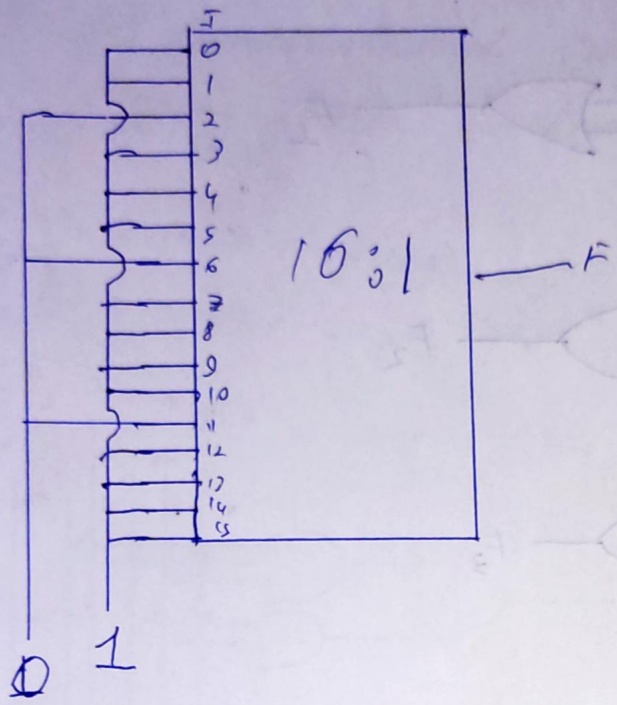


Q18 Implement the following boolean function with a multiplexer.

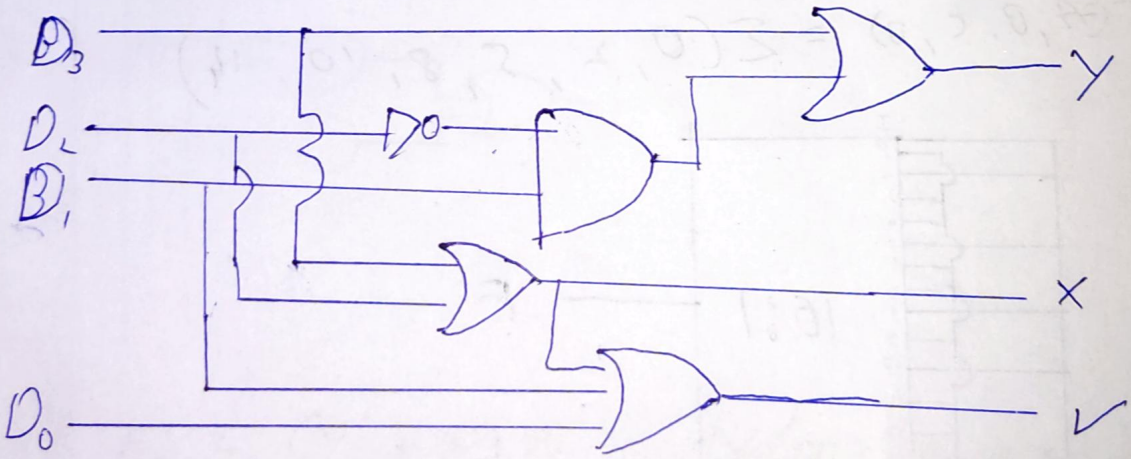
(a) $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$



(b) $F(A, B, C, D) = \Pi(2, 6, 11)$



Q19 Write HDL gate-level description of a 4-bit priority encoder circuit given below.



$x = D_2 + D_3$

$y = D_3 + D_1 D_2'$

$V = D_0 + D_1 + D_2 + D_3$

```
module encoder_gates (output x, y, V, input D0, D1, D2, D3);
    wire w1, D2_not;
    not (D2_not, D2);
    or (x, D2, D3);
    or (V, D0, D1, x);
    and (w1, D2_not, D1);
    or (y, D3, w1);
endmodule
```

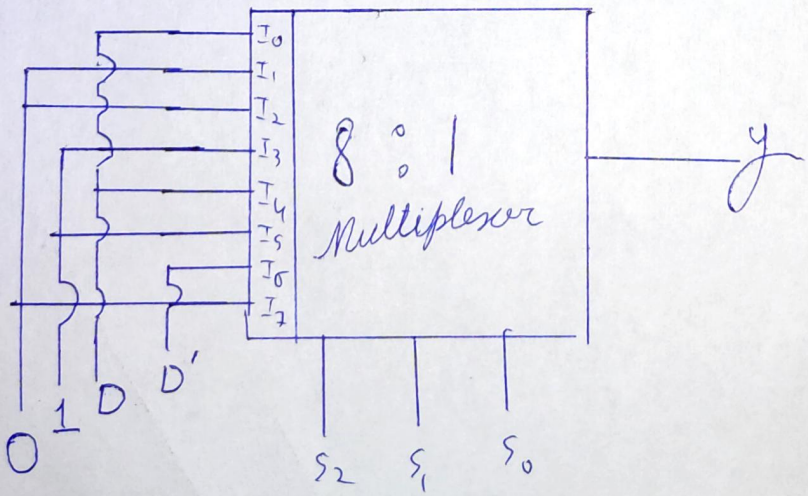
Q20 An 8X1 multiplexer has inputs A, B and C connected to selection input S_2, S_1 and S_0. The data inputs I_0 to I_7 are as follows

(a) $I_1 = I_2 = I_7 = 0$;

$I_3 = I_5 = 1$

$I_0 = I_4 = D$

$I_6 = D'$



(b) $I_1 = I_2 = 0$

$I_3 = I_7 = 1$

$I_4 = I_5 = D$

$I_0 = I_6 = D'$