DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VI: DESIGN OF MAGNITUDE COMPARATOR DECODER, ENCODER AND MULTIPLEXER CIRCUIT

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Marks: _____/10

Remarks:

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I. OBJECTIVE:

1. Design a combinational circuit that compares two 4-bit numbers to check if they are eq
   The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

2. Design a 2 X 1 Multiplexer that will select the binary information from one of the two input lines and direct it to a single output line based on the value of a selection line.

3. Design a 4 bit priority encoder with inputs D_3 (MSB), D_2, D_1 and D_0 (LSB) and outputs X, Y and V. The priority assigned to inputs is $D_3 > D_2 > D_1 > D_0$.The output V shows a value 1 when one or more inputs are equal to one. If all inputs are 0, V is equal to 0. When V=0, then other two outputs are not inspected and are specified as don't care conditions.

4. Design a full adder using 3 to 8 line decoder and external OR gates.

II. PRE-LAB

For Obj. 1:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for the output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 2:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for the output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 3:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 4:

a. Write the truth table for the circuit.
b. Derive the Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

OBJECTIVE - 1

$A \rightarrow A_3\ A_2\ A_1\ A_0$

$B \rightarrow B_3\ B_2\ B_1\ B_0$

$(A=B) \rightarrow (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$

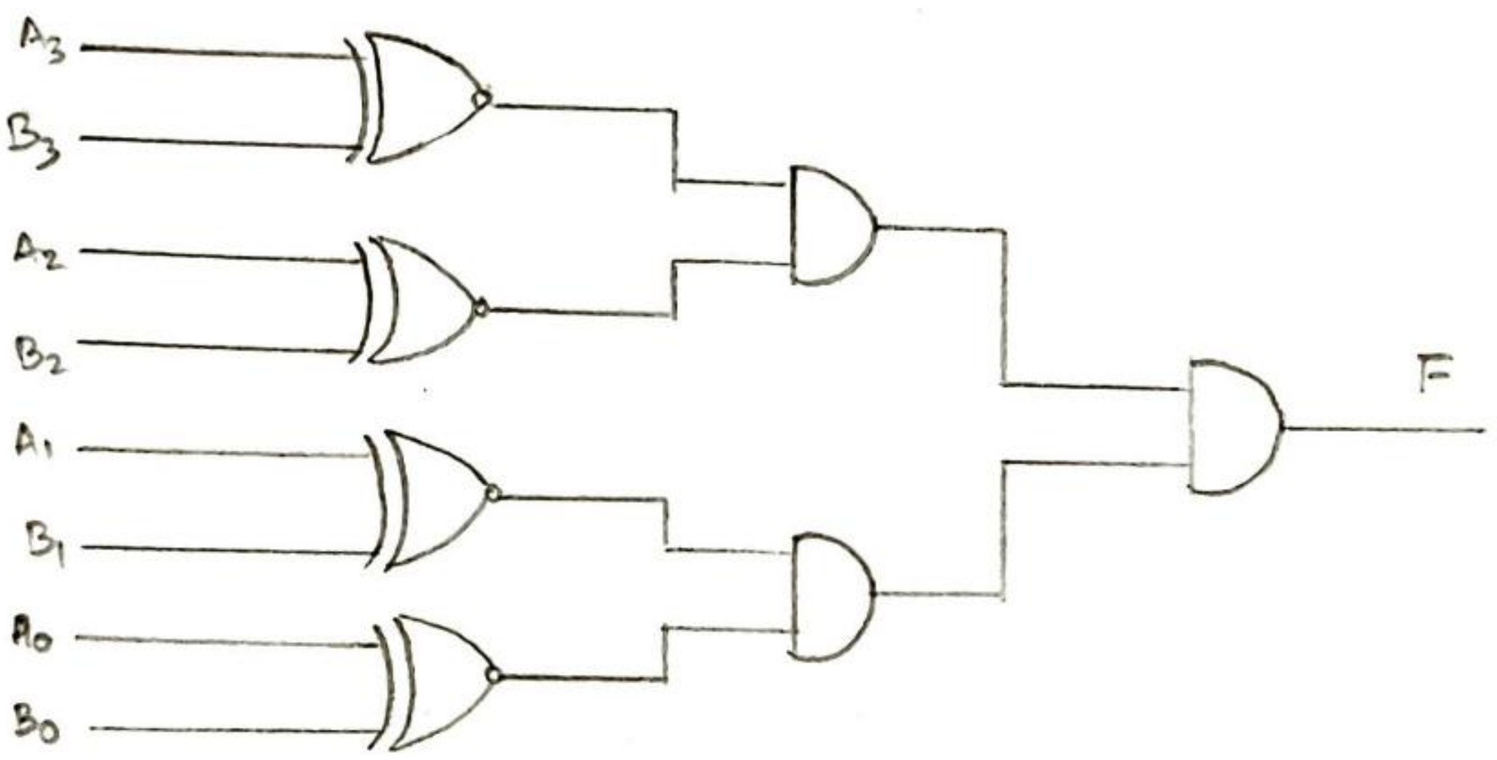
a)

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	$F\ (A=B)$
1	0	0	1	0	0	1	1	0
1	1	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0	1
0	0	0	1	0	1	1	0	0

b) Minimized Eq^n

$(A=B) \Rightarrow (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$

c)



d) HDL Code

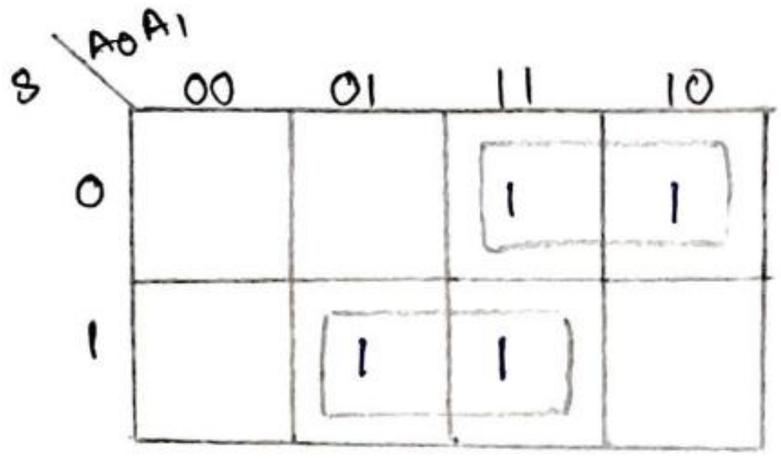
```
module obj1 (A3, A2, A1, A0, B3, B2, B1, B0, F);
input A3, A2, A1, A0, B3, B2, B1, B0;
output F;
assign F = (!(A3^B3)) && (!(A2^B2)) && (!(A1^B1)) && (!(A0^B0));
end module
```

OBJECTIVE - 2

a) $Y = SA_1 + \bar{S}A_0$

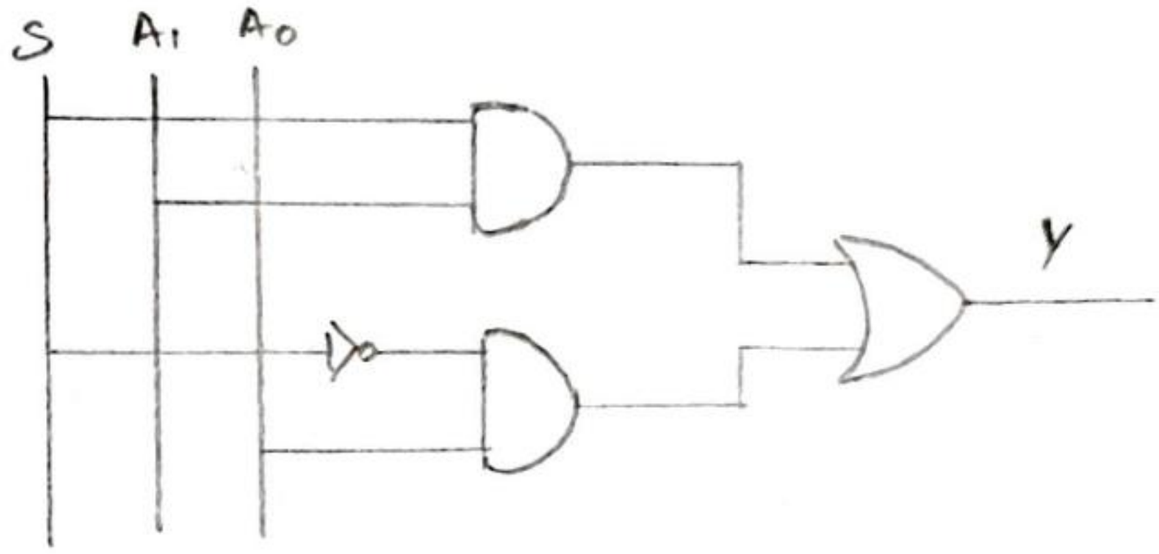
S	A_0	A_1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b)



$Y = SA_1 + \bar{S}A_0$

c)



d) HDL Code

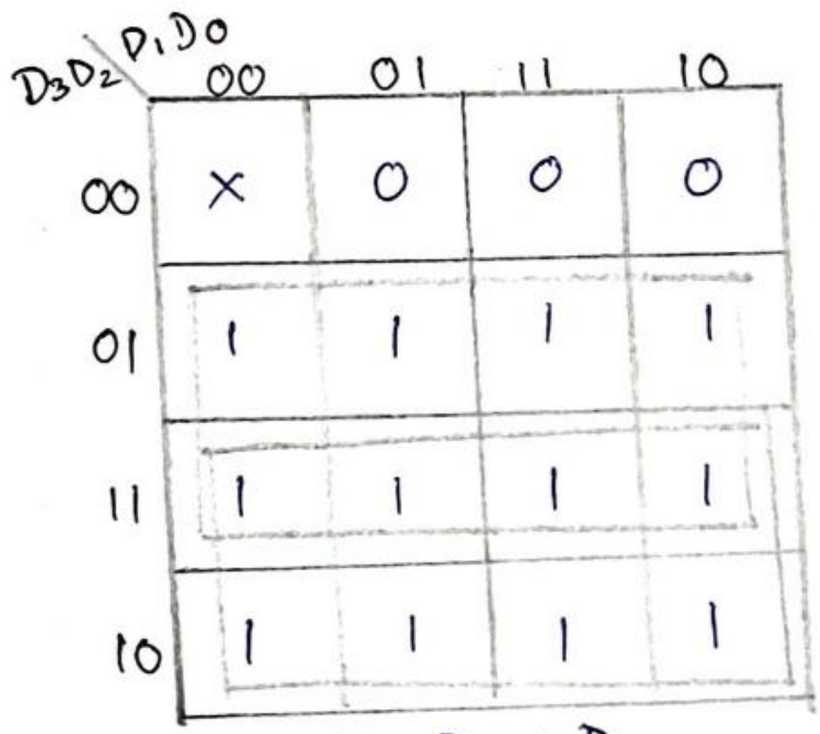
```
module obj2 (S, A0, A, Y);
input S, A0, A1;
output Y;
assign Y = (S&&A1)||(~S&&A0);
end module
```

OBJECTIVE - 3

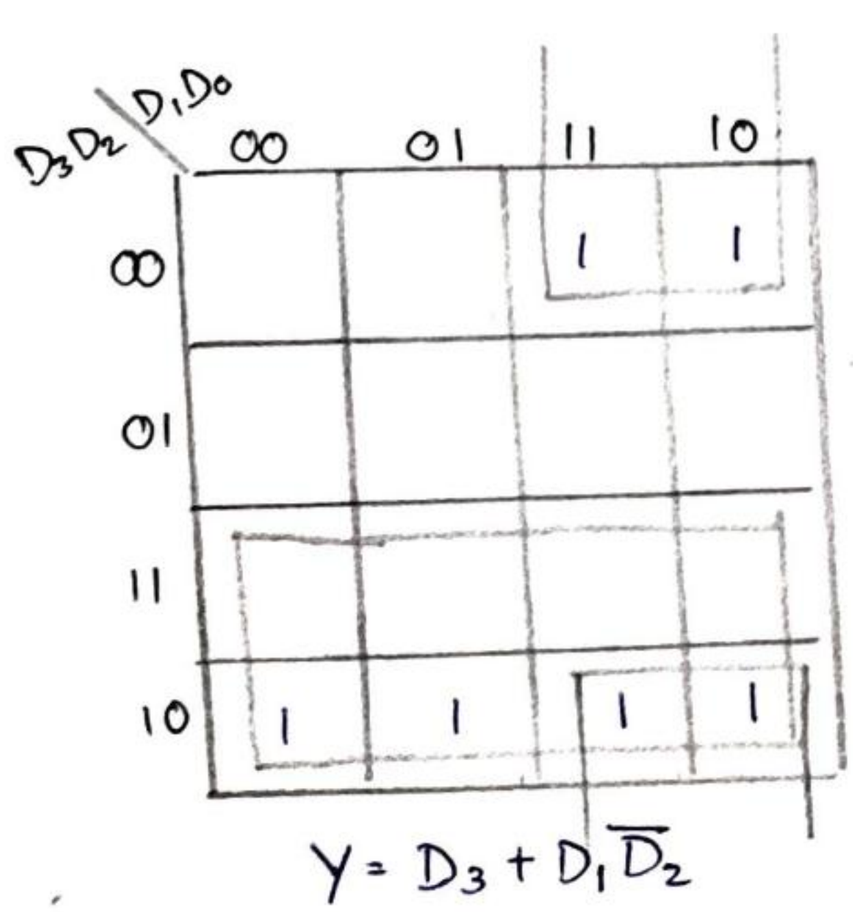
a)

D_3	D_2	D_1	D_0	X	Y	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

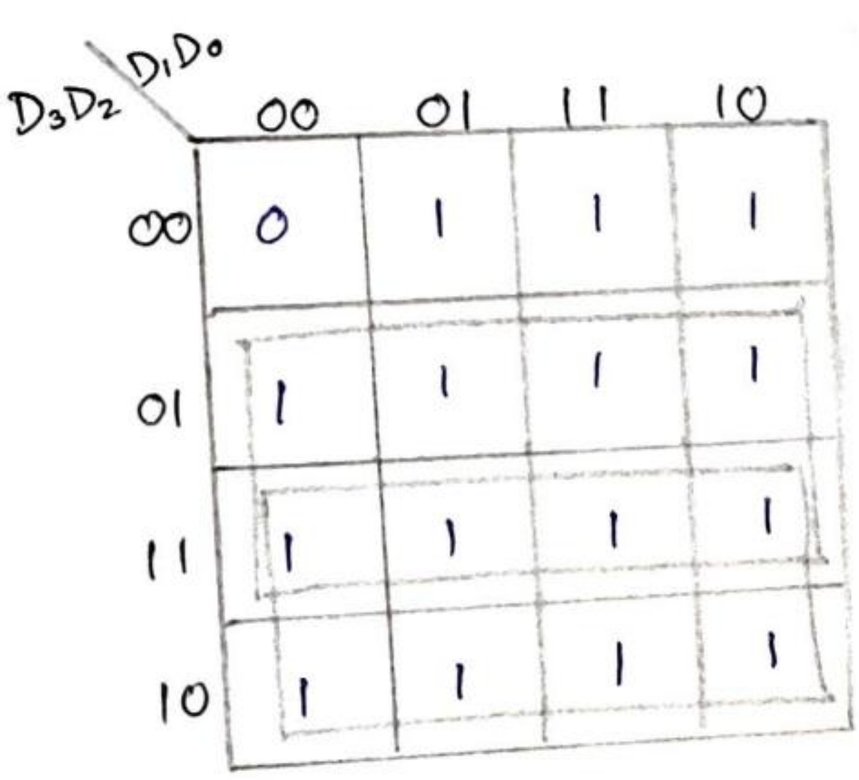
b)



$X = D_3 + D_2$

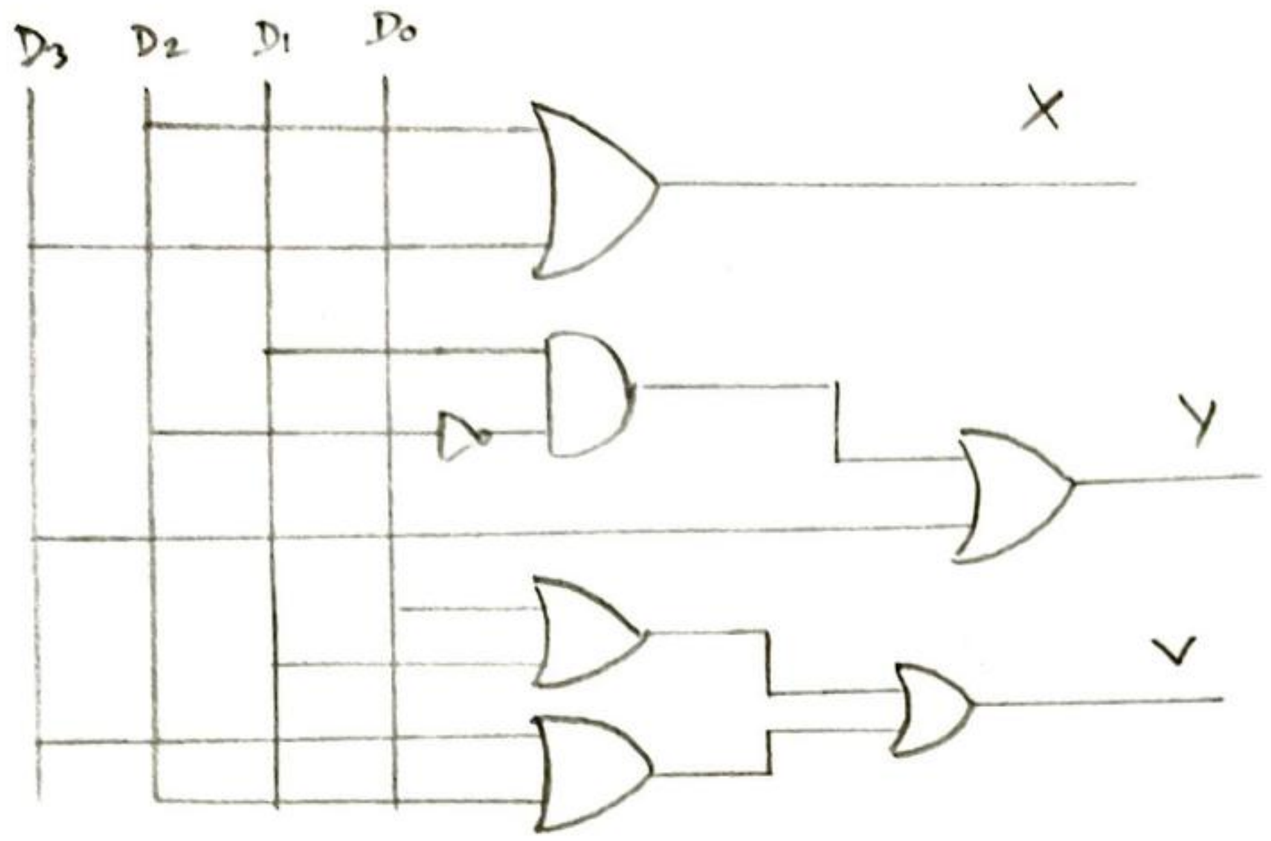


$Y = D_3 + D_1\bar{D_2}$



$V = D_3 + D_2 + D_1 + D_0$

c)



d)

```
module obj3(D0, D1, D2, D3, X, Y, V);
input D0, D1, D2, D3;
output X, Y, V;
assign X = D2 || D3;
assign Y = (D1 && ~D2) || D3;
assign V = D0 || D1 || D2 || D3;
end module
```

OBJECTIVE - 4

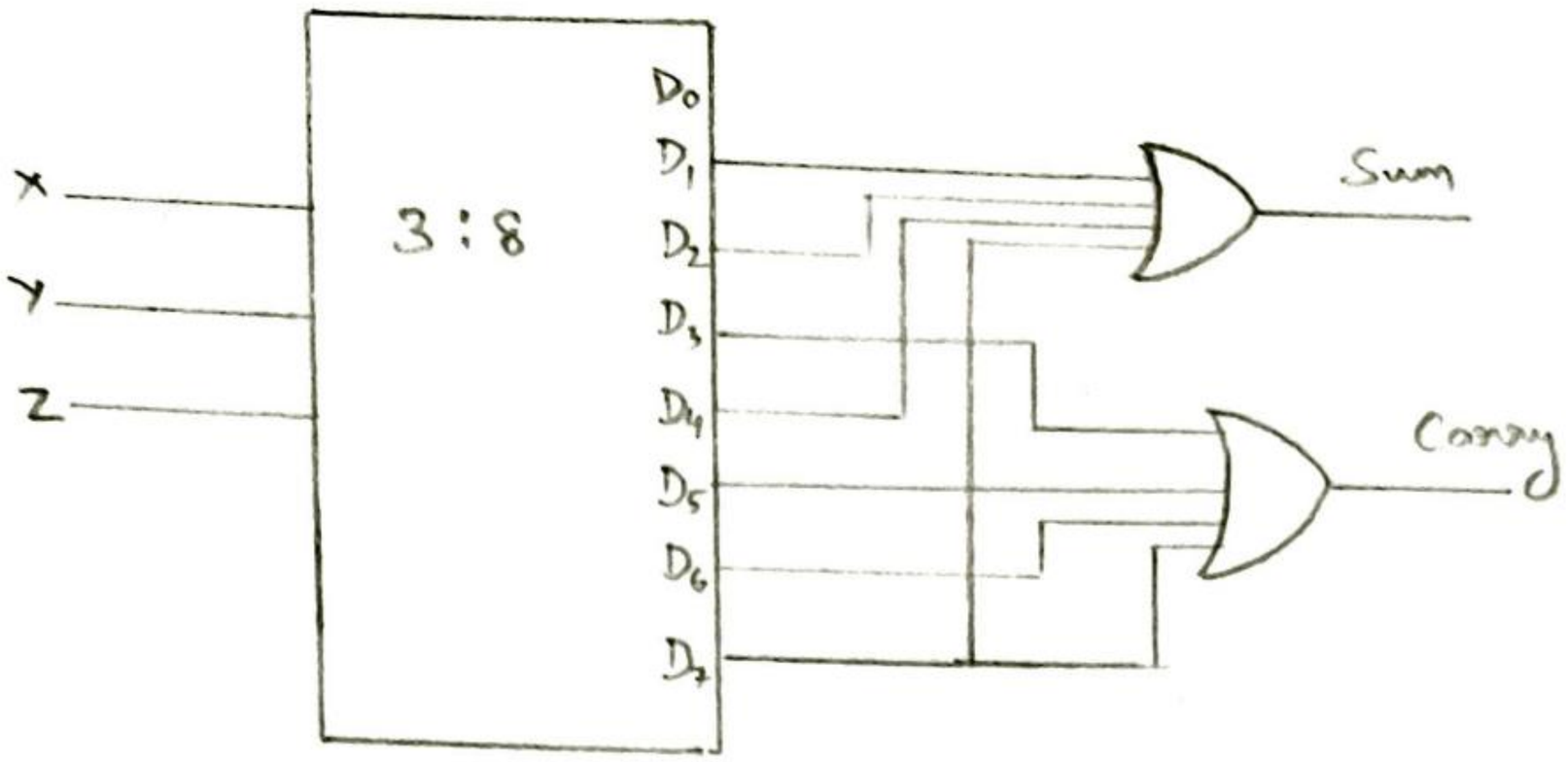
a)

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

X	Y	Z	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

b) $Sum = D_1 + D_2 + D_4 + D_7$

$Carry = D_3 + D_5 + D_6 + D_7$



4) module alg4(x, y, z, sum, carry);
input x, y, z;
output sum, carry;
assign sum = (~x & ~y & z) | (~x & y & ~z) | (x & ~y & ~z) | (x & y & z);
assign carry = (~x & y & z) | (x & ~y & ~z) | (x & y & ~z) | (x & y & z);
endmodule