DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VIII: CONSTRUCT, TEST AND INVESTIGATE THE OPERATION OF VARIOUS SHIFT REGISTER CIRCUITS

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Branch:		Section:	
S. No.	**Name**	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE

1. Design and Test of 4-bit SISO(Serial in Serial out) shift register

2. Design and Test of 4-bit SIPO (Serial in Parallel out) shift register

3. Design and Test of 3-bit PISO (Parallel in Serial out) shift register

4. Design and Test of 4-bit PIPO (Parallel in Parallel out) shift register

II. PRE-LAB

For Obj. 1:

a. Draw the logic diagram for 4-bit SISO shift register.
b. Write HDL code for 4-bit SISO shift register.

For Obj. 2:

a. Draw the logic diagram for 4-bit SIPO shift register.
b. Write HDL code for 4-bit SIPO shift register

For Obj. 3:

a. Draw the logic diagram for 3-bit PISO shift register
b. Write HDL code for 3-bit PISO shift register

For Obj. 4:

a. Draw the logic diagram for 4-bit PIPO shift register
b. Write HDL code for 4-bit PIPO shift register

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

HDL Program:

Observation:

Conclusion:

IV. POST LAB

1. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

   A. 0000
   B. 0010
   C. 1000
   D. 1111

2. A bidirectional 4-bit shift register is storing the nibble 1101. Its $\overline{\text{RIGHT}/\text{LEFT}}$ input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.

   A. 1101
   B. 0111
   C. 0001
   D. 1110

3. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

   A. 1100
   B. 0011
   C. 0000
   D. 1111