For Objective-1:

a)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

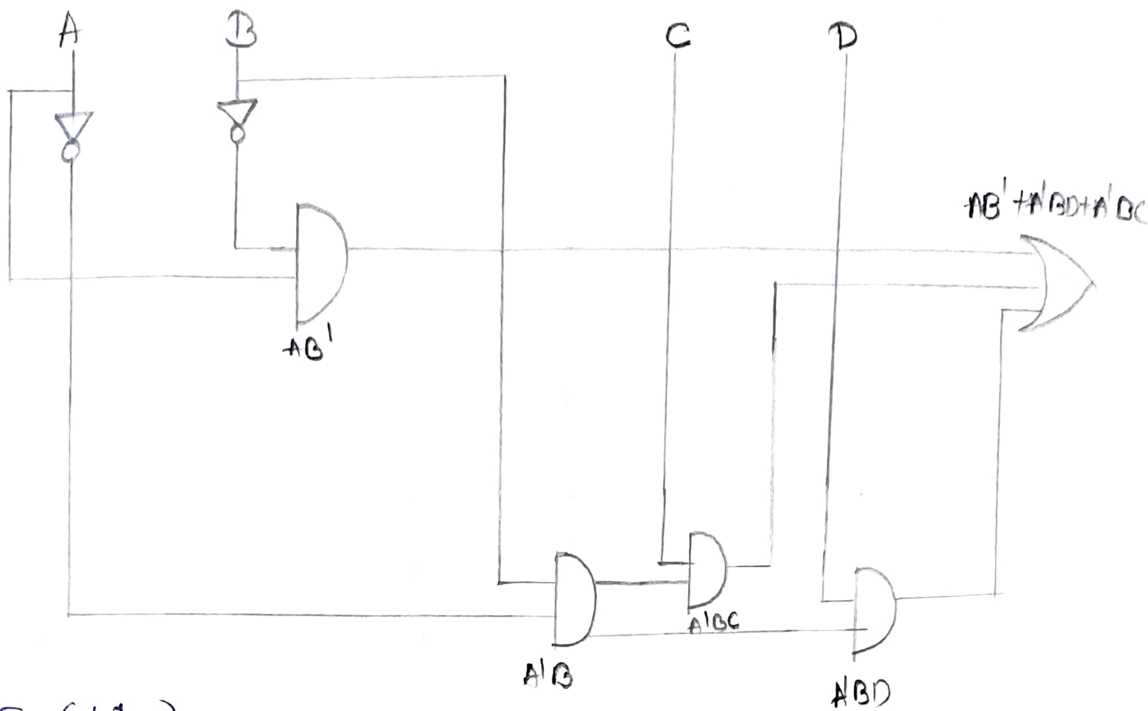
b)

AB \ CD	C'D'	C'D	CD	CD'
A'B'				
A'B		1	1	1
AB				
AB'	1	1	1	1

Simplified expression:

$AB' + A'BD + A'BC.$

c)



For (0b2-2)

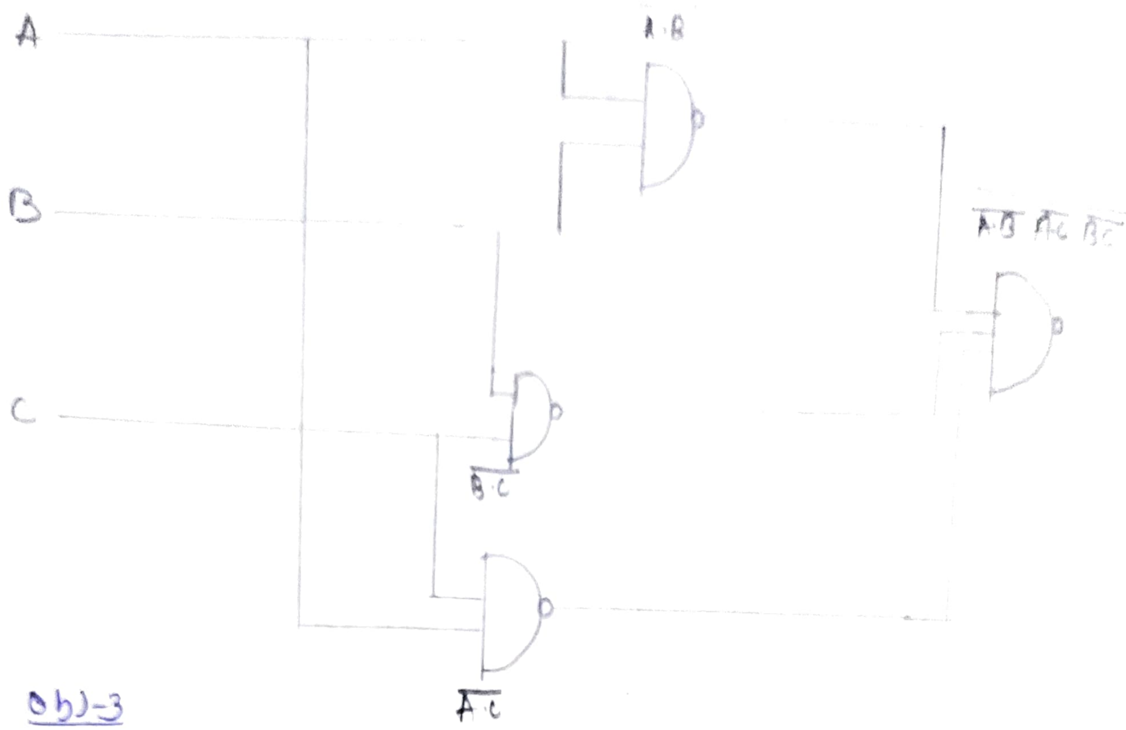
a)

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

b)

A \ BC	B'C'	B'C	BC	BC'
A'			1	
A		1	1	1

Expression:- AB + AC + BC



Obj-3

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

b) $F(A,B,C,D) = \Sigma(1,2,4,7,8,11,13,14)$

AB \ CD	C'D'	C'D	CD	CD'
A'B'		1		1
A'B	1		1	
AB		1		1
AB'	1		1	

$= A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + ABC'D + ABCD' + AB'C'D' + AB'CD$

$= A'B'(C'D + CD') + A'B(C'D' + CD) + AB(C'D + CD') + AB'(C'D' + CD)$

$= A'B'(C \oplus D) + A'B(C \odot D) + AB(C \oplus D) + AB'(C \odot D)$

$= A'B'(C \oplus D) + AB(C \oplus D) + A'B(C \odot D) + AB'(C \odot D)$

$= (C \oplus D)(A'B' + AB) + (C \odot D)(A'B + AB')$

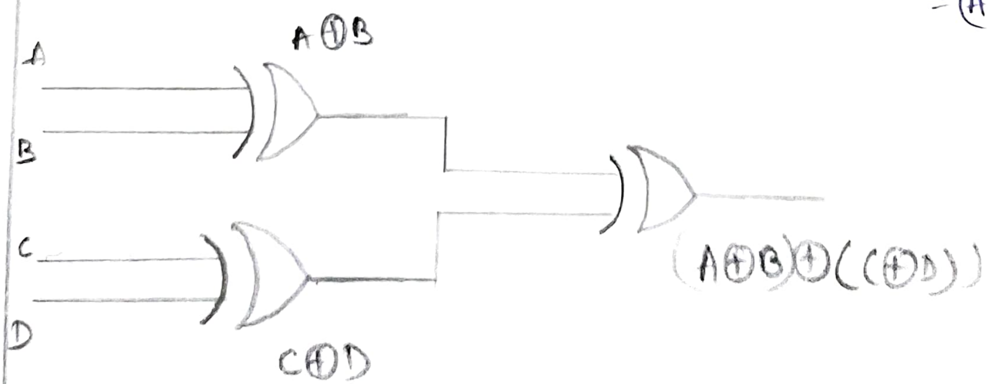
$= (C \oplus D)(A \odot B) + (C \odot D)(A \oplus B)$

Considering $A \oplus B$ as X and $C \oplus D$ as Y

So the expression will be $YX' + XY' = X \oplus Y$

$= (A \oplus B) \oplus (C \oplus D)$

c)



Obj-4

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$F(A,B,C,D) = \Sigma(0,5,10,15)$

AB \ CD	C'D'	C'D	CD	CD'
A'B'	1			
A'B		1		
AB			1	
AB'				1

$F = A'B'C'D' + A'BC'D + ABCD + AB'CD'$

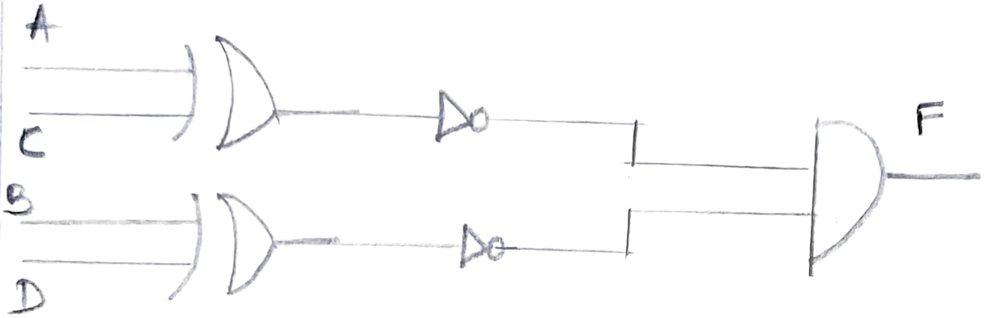
$= A'C'(B'D' + BD) + AC(BD + B'D')$

$= A'C'(B \oplus D)' + AC(B \oplus D)'$

$= (B \oplus D)'(A'C' + AC)$

$= (A \oplus C)'(B \oplus D)'$

c)



Components required

Component	Description	Quantity
IC 7408	Quad 2input AND gate	1
IC 7432	Quad 2input OR gate.	1
IC 7404	Hex Inverter NOT gate	1
IC 7400	Quad 2 input NAND gate	1
IC 7410	~~Quad~~ 3 input NAND gate	1
IC 7486	Quad 2 input XOR gate	1

Connecting wires

Observation

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

obj-2

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

obj-3

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Obs-4

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Conclusion

1. From this observation it can be concluded that for getting the output as per the instruction the combinational circuit leads to the function i.e $AB' + A'BD + A'BC$.

2. 3 input majority circuit leads to the function AB+AC+BC
3. The even parity bit from 4 message bits leads to the function $A \oplus B \oplus C \oplus D$
4. The equality condition leads to the XNOR function $(A \oplus C)'(B \oplus D)'$

Post Lab

1. A majority logic is a digital logic circuit whose output is equal to 1 if the majority of the inputs are 1's i.e. The o/p is '0' otherwise.
2. Take XOR of it with high input i.e 1
3. The function of a magnitude comparator circuit is to determine whether one no. is greater than, less than or equal to the other no.