SUMMER QUARTER EXAMINATION, JUNE - 2018
DIGITAL LOGIC (CSE 1011)

Programme: B. Tech **Semester: 3RD**
Full Marks: 60 **Time: 3 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1, 2	10
Apply concepts of Boolean Algebra.	L3, L4	2, 3	8
Apply Theorems and functions along with logic gates to solve logic operations.	L4	4	6
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) Translate the binary number $(110101)_2$ to its equivalent decimal number. 2

   (b) Using 1's complement method subtract the following binary numbers $(101)_2$-$(1110)_2$ s 2

   (c) Obtain the hexadecimal & octal number for the binary number $(101110)_2$ 2

2. (a) Using 10's complement method subtract the following binary numbers $(26)_{10}$-$(538)_{10}$ 2

   (b) Obtain the gray code and 2421 code for $(1001)_2$. 2

   (c) Simplify the given expression using Boolean algebra 2

$$F = a' + ab'c + bc$$

3. (a) Simplify the given expression using Boolean algebra 2

$$F = x'yz + xy'z' + xyz + xyz'$$

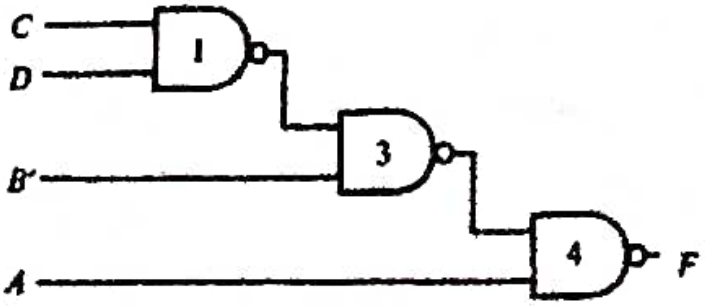
(b) Solve the given expression using k-map 2

$$F(a, b, c) = \Sigma m(0, 1, 4, 6) + d(2, 3)$$

(c) Construct the following function using NAND gates only 2

$$F(a, b, c) = \Sigma m(0, 1, 2, 6)$$

4.



(a) Identify the number of input and output variables used in the following logic diagram and obtain the Boolean function of the circuit 2

(b) Represent the Boolean Function obtained in 3(a) using K-Map and determine the simplified expression. 2

(c) Design a logic circuit to implement the function obtained in 3(b). 2

5. A logic circuit accepts 3-bit binary as input and gives even parity as output

(a) Draw the truth table. 2

(b) Obtain the simplified expressions. 2

(c) Sketch the circuit using minimum number of logic gates. 2

6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

(a) Draw the truth table. 2

(b) Obtain the simplified expressions. 2

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7. (a) What is a priority encoder? 2

(b) Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only. 2

(c) Design a half adder circuit with a decoder and one OR gates. 2

8. (a) What is a MULTIPLEXER? 2

(b) Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER 2

(c) Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer. 2

9. (a) Explain the working of a gated D-latch with circuit diagram. 2

(b) Design a 2-bit down counter using D Flip Flops. 2

(c) How many clock pulse(s) is/are required to transfer the data $(1001)_2$ through a 4-bit (i) SISO (ii) PIPO shift register? 2

10. Design a synchronous MOD 6 down counter using T Flip Flops.

(a) Write the state table 2

(b) Obtain the simplified expressions for FF inputs. 2

(c) Draw the circuit using T FFs 2

End of Questions

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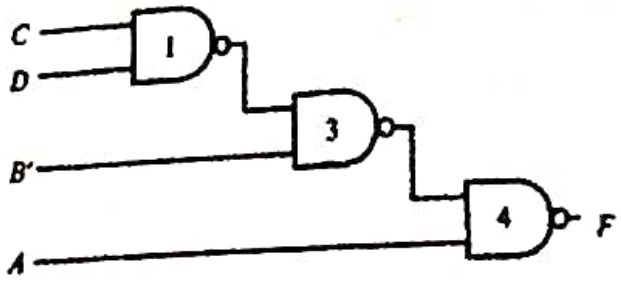

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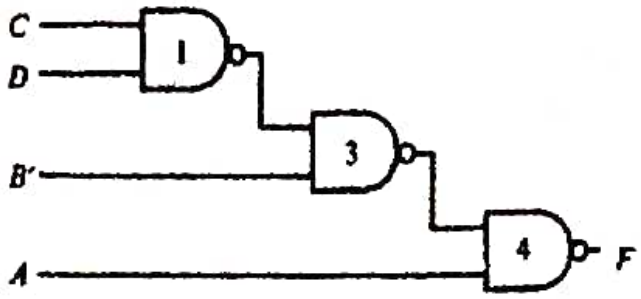

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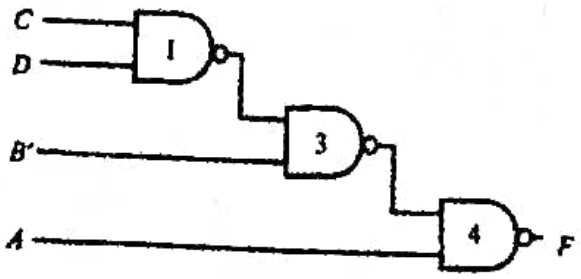

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End of Questions

MID SEMESTER EXAMINATION, OCTOBER-2018
DIGITAL LOGIC (CSE 1011)

Programme: B.Tech **Semester:3RD**

Full Marks: 30 **Time: 2 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1	6
Apply concepts of Boolean Algebra	L3	2(a)	2
Apply Theorems and functions along with logic gates to solve logic operations.	L6	2(b,c)	4
Design and analyze combinational circuits using logic gates and K-map.	L6	3,4	12
Design and analyze clocked sequential circuits using latches and flip-flops.	L6	5	6

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) Construct EX-OR gate using minimum numbers of NAND gates only. 2

(b) Translate the following binary number to corresponding decimal, octal & hexadecimal number: (110111.1011) 2

(c) Obtain the BCD & excess-3 code for 456. 2

2. (a) Determine the simplified expression of the following Boolean function using Boolean algebra rules 2

$(A + B')(A' + B' + D)(B' + C + D')$

(b) Minimize the given expression using k-map 2

$F(a,b,c) = \sum m(0,5,7) + d(1,4)$

(c) Find the complement of the Boolean function and reduce them to a minimum number of literals. 2

$[(AB)'A][(AB)'B]$

3. Design a combinational circuit that converts a decimal digit from the 8,4,-2,-1 code to BCD.

(a) Obtain the truth table for the above circuit. 2

(b) Express the simplified function in sum of products. 2

(c) Draw the logic diagram of the simplified function using NAND gate only. 2

4. (a) Construct a 3-to-8 line decoder circuit using 2-to-4 line decoder only. 2

(b) Construct a **FULL SUBTRACTOR** using 8 to 1 line multiplexers. 2

(c) A combinational circuit has three inputs x, y & z and two outputs F1 & F2. The Boolean expression for two outputs is as given below: 2

F1= XZ + X' Y' Z'
F2= X' Y + X Y' Z'

Implement the combinational circuit using the decoder and external NAND gates.

5. (a) What is the difference between a latch and a flip flop? 2

(b) Compare the behavior of SR Flip Flop with JK Flip Flop.. 2

(c) Convert JK Flip Flop to T Flip Flop and derive its characteristic table. 2

End of Questions

MID SEMESTER EXAMINATION, SEPTEMBER-2019
DIGITAL LOGIC (CSE 1011)

Programme : B.Tech (CSE & CSIT)

Semester:3RD

Full Marks: 30 **Time: 2 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1,2	12
Apply concepts of Boolean Algebra	L3	3	6
Design and analyze combinational circuits using logic gates and K-map.	L6	4,5	12

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) Implement the given function by using only NAND gates. 2

$F = X + Y'Z$

(b) Find (a) the diminished radix and (b) the radix complement of $(235)_{10}$. 2

(c) Represent $(542)_{10}$ in BCD and excess-3 code. 2

2. (a) Find the value of X if 2

$(789)_{16} + (473)_8 = (X)_4$

(b) Given X = 10010 and Y = 10011 (a) find X-Y and (b) find Y-X using 2's complement form. 2

(c) What is the even parity and odd parity of A =0101100 2

3. (a) Prove X.X= X and (X ')'=X using postulates 2

(b) Find the dual of the expression : XY' + (Y+Z) (X+Z') 2

(c) Simplify the following expressions using Boolean theorems and Postulates 2

$AB'C'+CD'+BC'D'$

4. (a) Obtain the Boolean expression that compares two 2 bit numbers A and B to check if A is greater than B. 2

A certain Combinational circuit converts a four bits binary number to a four bits gray code.

(b) Design the above circuit by finding the circuit truth table. 2

(c) Determine the Boolean equations required to design the above circuit 2

5. (a) Construct a 3-to-8 line decoder circuit using 2-to-4 line decoder only. 2

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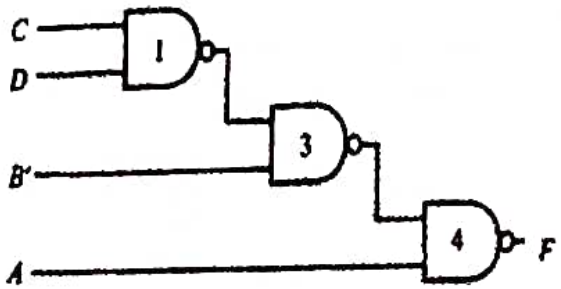

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DIGITAL LOGIC (CSE 1011)

Programme: B. Tech **Semester: 3RD**

Full Marks: 60 **Time: 3 Hours**

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1, 2	10
Apply concepts of Boolean Algebra.	L3, L4	2, 3	8
Apply Theorems and functions along with logic gates to solve logic operations.	L4	4	6
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) Translate the binary number $(110101)_2$ to its equivalent decimal number. 2
   (b) Using 1's complement method subtract the following binary numbers $(101)_2$-$(1110)_2$ s 2
   (c) Obtain the hexadecimal & octal number for the binary number $(101110)_2$ 2
2. (a) Using 10's complement method subtract the following binary numbers $(26)_{10}$-$(538)_{10}$ 2
   (b) Obtain the gray code and 2421 code for $(1001)_2$. 2
   (c) Simplify the given expression using Boolean algebra 2

$$F = a' + ab'c + bc$$

3. (a) Simplify the given expression using Boolean algebra 2

$$F = x'yz + xy'z' + xyz + xyz'$$

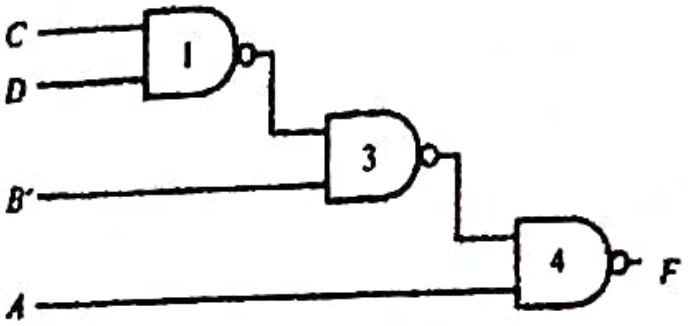
(b) Solve the given expression using k-map 2

$$F(a, b, c) = \Sigma m(0, 1, 4, 6) + d(2, 3)$$

(c) Construct the following function using NAND gates only 2

$$F(a, b, c) = \Sigma m(0, 1, 2, 6)$$

4.



(a) Identify the number of input and output variables used in the following logic diagram and obtain the Boolean function of the circuit 2

(b) Represent the Boolean Function obtained in 3(a) using K-Map and determine the simplified expression. 2

(c) Design a logic circuit to implement the function obtained in 3(b). 2

5. A logic circuit accepts 3-bit binary as input and gives even parity as output

(a) Draw the truth table. 2

(b) Obtain the simplified expressions. 2

(c) Sketch the circuit using minimum number of logic gates. 2

6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

(a) Draw the truth table. 2

(b) Obtain the simplified expressions. 2

(c) Sketch the circuit using minimum number of logic gates. 2

7. (a) What is a priority encoder? 2

(b) Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only. 2

(c) Design a half adder circuit with a decoder and one OR gates. 2

8. (a) What is a MULTIPLEXER? 2

(b) Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER 2

(c) Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer. 2

9. (a) Explain the working of a gated D-latch with circuit diagram. 2

(b) Design a 2-bit down counter using D Flip Flops. 2

(c) How many clock pulse(s) is/are required to transfer the data $(1001)_2$ through a 4-bit (i) SISO (ii) PIPO shift register? 2

10. Design a synchronous MOD 6 down counter using T Flip Flops.

(a) Write the state table 2

(b) Obtain the simplified expressions for FF inputs. 2

(c) Draw the circuit using T FFs 2

End of Questions

(10)

DIGITAL LOGIC
Assignment - 1

Course Code: CSE 1011
Branch: CSE, CSIT

Grading Pattern: 1
Semester: 3rd

1. Convert to hexadecimal, octal and binary
   a. $(123)_{10}$
   b. $(356)_{10}$
   c. $(1063)_{10}$
   d. $(725.25)_{10}$

2. Add and Subtract in binary
   a. $(1111)_2$ and $(1001)_2$
   b. $(1101001)_2$ and $(110110)_2$
   c. $(100010)_2$ and $(11101)_2$

3. Perform the subtraction with the following decimal numbers using 9's complement.
   a. 5250 - 321
   b. 753 - 864

4. Perform the subtraction using 2's complement method
   a. 11010 - 1101
   b. 10010 - 10011
   c. 11010 -10000

5. The solution of the quadratic equation $X^2-11X+22=0$ are X=3 and X=6. What is the base of the number

6 Represent $(542)_{10}$ in BCD and 8421 BCD code

7 Prove Excess 3 Code is a self complementing code

8 Prove X+X= X and X+1=1 using postulates

9 $(16)_{10} = (100)_y$, Find y

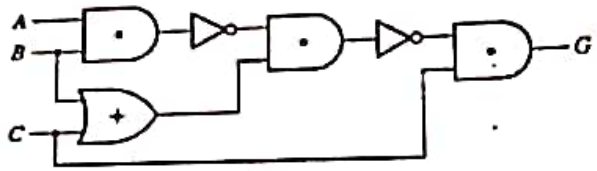
10 Find the value of X

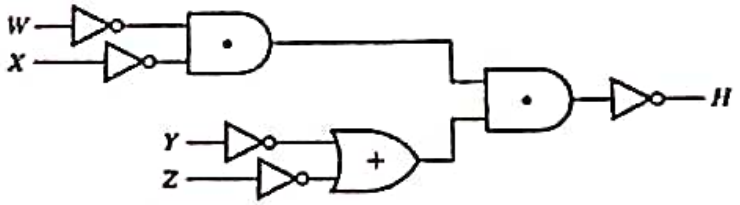
a) $(432)_5 = (X)_7$

b) $(789)_{16} + (473)_8 = (X)_4$

11 Find the 16's complement of $(BABA)_{16}$

11. Find F, G & H and simplify.





12 Minimize the following expression

$$f = A[B + \bar{C}(\overline{A.B + A.\bar{C}})]$$

$$f = A + B[AC + (B + \bar{C})D]$$

$$f = (\overline{A + \overline{BC}})(AB + A\bar{B}C)$$

$$f = (B + BC)(B + B\bar{C})(B + D)$$

13 Simplify each of the following expressions using Boolean theorems and Postulates.

a) $ABCD'+A'B'CD+CD'$
b) $AB'C'+CD'+BC'D'$
c) $(A+B')(A'+B'+D)(B'+C+D')$
d) $xy'+z+(x'+y)z'$
e) $w'x'+x'y'+yz+w'z'$

14 Plot the following functions on a *K-map*

$F(A,B,C,D)=BD'+B'CD+ABC+ABC'D+B'D'$

a) Find the minimum SOP.
b) Find the minimum POS

15 Find the minimized expression for each function

a) $f(a,b,c,d)= \Sigma m(0,2,3,4,7,8,14)$
b) $f(a,b,c,d)= \Sigma m(1,2,4,15)+d(0,3,14)$
c) $f(a,b,c,d)= \Pi M(1,2,3,4,9,15)$
d) $f(a,b,c,d)= \Pi M(0,2,4,6,8)\cdot D(1,9,12,15)$

16 For given table, express F1 and F2 in product of maxterms

A	B	C	F1	F2	
0	0	0	1	0	
0	0	1	0	1	
0	1	0	0	1	
0	1	1	0	1	
1	0	0	0	0	
1	0	1	1	1	
1	1	0	1	0	
1	1	1	1	1	

Obtain the simplified function in SOP and POS

17 Find Min term and Max term of the function

$F_1 = x'y' + yz + x\,z'$

18 Simplify the following functions and implement with NAND gates

$F = (B'+D')(A'+C'+D)(A+B'+C'+D)(A'+B+C'+D')$

19 Implement the function F=X'Y +XY' + Z with NOR gates

20 Implement EX-OR gate using minimum number of NAND and NOR gate