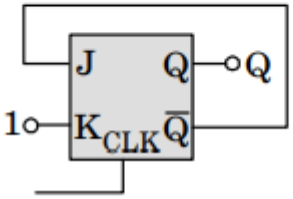
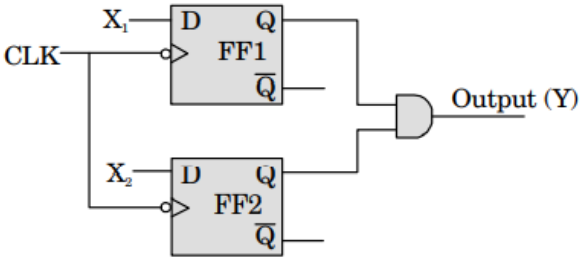
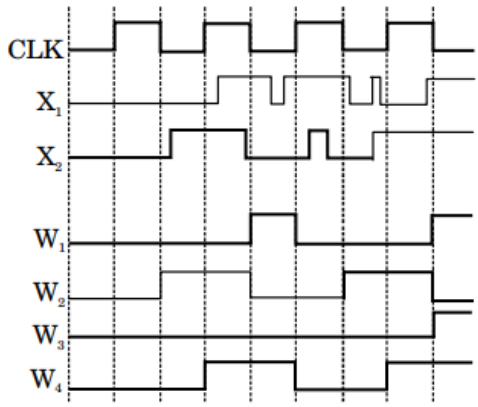
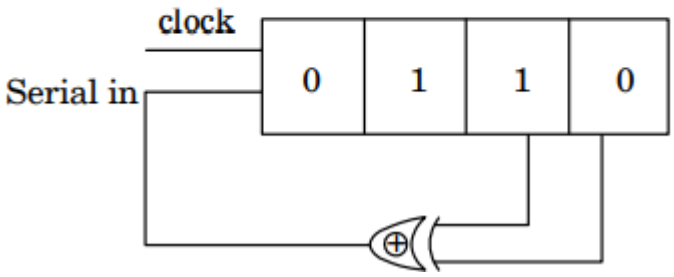
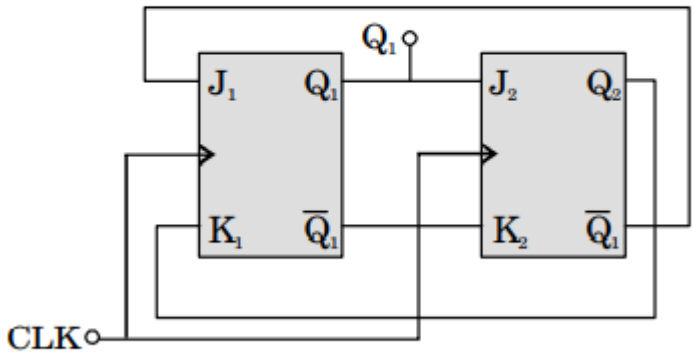
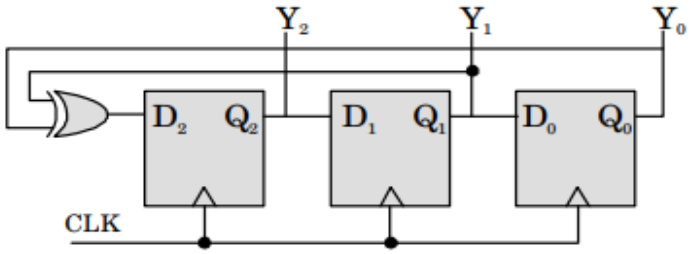
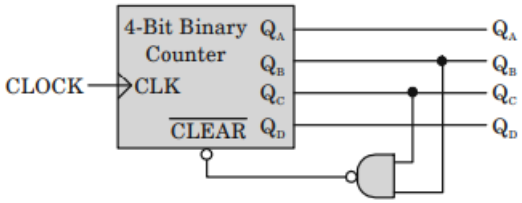
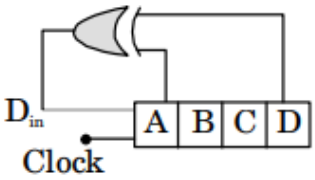
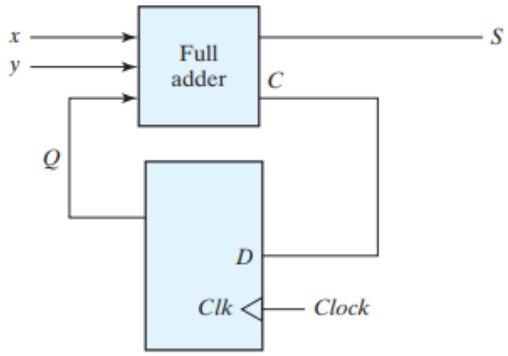
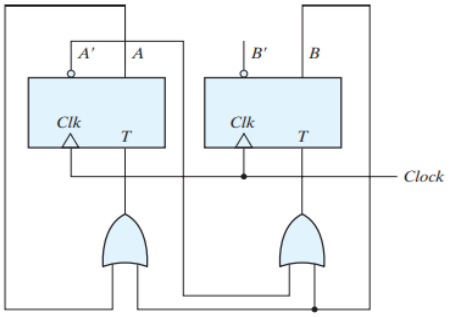
	ITER, SIKSHA 'O' ANUSANDHAN (Deemed to be University)		**Assignment**
Branch	**Computer Science and Engineering**	Programme	**B.Tech**
Course Name	**Digital Logic Design**	Semester	**III**
Course Code	**EET1211**	Academic Year	**2022/Odd**
Assignment-3	**Topic- Synchronous Sequential Logic**	**GP-1**	
Learning Level (LL)	**L1**: Remembering	**L3:** Applying	**L5**: Evaluating
	L2: Understanding	**L4**: Analysing	**L6**: Creating

Q's	Questions	COs	LL
1	In a J-K flip-flop we have $J = \bar{Q}$ and $K = 1$ (see figure) Assuming the flip-flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be  **[1997]**	**CO4**	**L4**
2	In the circuit shown, choose the correct timing diagram of the output (Y) from the given waveforms W_1, W_2, W_3 and W_4.   (a) W_1 (b) W_2 (c) W_3 (d) W_4 **[2014]**	**CO4**	**L2**

3	The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After three clock pulses are applied, the contents of the Shift Register will be 	CO4	L2
4	The outputs of the two flip-flops Q_1, Q_2 in the figure shown are initialized to 0, 0. The sequence generated at Q_1 upon application of clock signal is  (a) 01110... (b) 01010... (c) 00110... (d) 01100.... [2014]	CO4	L2
5	A three bq pseudo random number generator is shown. Initially the value of output Y = Y_2 Y_1Y_0 is set to 111. The value of output Y after three clock cycles is  (a) 000 (b) 001 (c) 010 (d) 100	CO4	L4

6	A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is _____.  **[2015]**	**CO4**	**L2**
7	A 4-bit shift register circuit configured for right-shift operation, i.e. $D_{in} \rightarrow A$, $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$, is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is  **[2017]**	**CO4**	**L2**
8	A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. P5.7. Derive the state table and state diagram of the sequential circuit.  	**CO4**	**L4**
9	Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (IIDL—see Problem 5.36.)  	**CO4**	**L4**
10		**CO4**	**L2**

	For the following state table **Next State** / **Output** **Present State** | **x = 0** | **x = 1** | **x = 0** | **x = 1** *a* | *f* | *b* | 0 | 0 *b* | *d* | *c* | 0 | 0 *c* | *f* | *e* | 0 | 0 *d* | *g* | *a* | 1 | 0 *e* | *d* | *c* | 0 | 0 *f* | *f* | *b* | 1 | 1 *g* | *g* | *h* | 0 | 1 *h* | *g* | *a* | 1 | 0 (a) Draw the corresponding state diagram. (b)* Tabulate the reduced state table. (c) Draw the state diagram corresponding to the reduced state table.		
11	Write and verify an HDL Behavioural description of a positive-edge-sensitive D flip-flop, T flip-flop and JK flip-flop.	**CO6**	**L2**

Assignment 3	**Topic: Synchronous Sequential Logic**	**Date of Assignment3: 11.01.2023**	**Date of Submission: 16.01.2023**

Note:

1. assignment carries weightage of **20 marks out of 100**
2. Course outcome CO4 to CO6 was covered.

Course Outcomes	CO1	Able to State and explain different number systems, binary codes
	CO2	Able to apply the principles of Boolean algebra and Karnaugh map to simplify logic expressions and implement it using gates
	CO3	Able to Analyse and design various combinational circuits
	CO4	Able to Analyse and design different synchronous and asynchronous sequential circuits
	CO5	Able to Analyse and design various Memory, Programmable Logic circuits and register transfer level
	CO6	Able to implement various digital circuits using HDL and Standard ICs.