

November 25  
2022

Digital logic  
Design  
Assignment 2

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Q1 if the input of digital circuit consisting of a cascade of 20 XOR gates in X, Then the output Y is equal to

lets

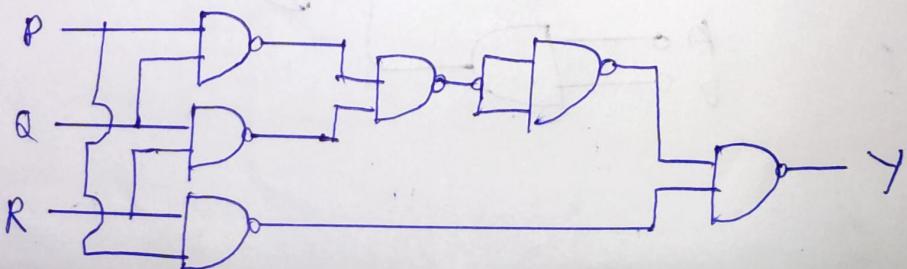
create the truth table for first 4 XOR gate

1	0	1	1	1	1	0	0	1	1	1	1	1	1	0
1	1	0	0	1	1	1	0	0	1	1	1	0	0	1
1	0	1	1	1	1	0	0	1	1	1	1	1	1	0
1	1	0	0	1	1	1	0	0	1	1	1	0	0	1

So, the same output is repeated every 2nd time we execute XOR gate

So,  $y = 0$  after we execute 20th XOR  
gate

Q2 The output y in the circuit given below is always '1' when



$y$  will be 1 for all the combination of input given below

①  $P = 0 \quad Q = 1 \quad R = 1$

②  $P = 1 \quad Q = 0 \quad R = 1$

③  $P = 1 \quad Q = 1 \quad R = 0$

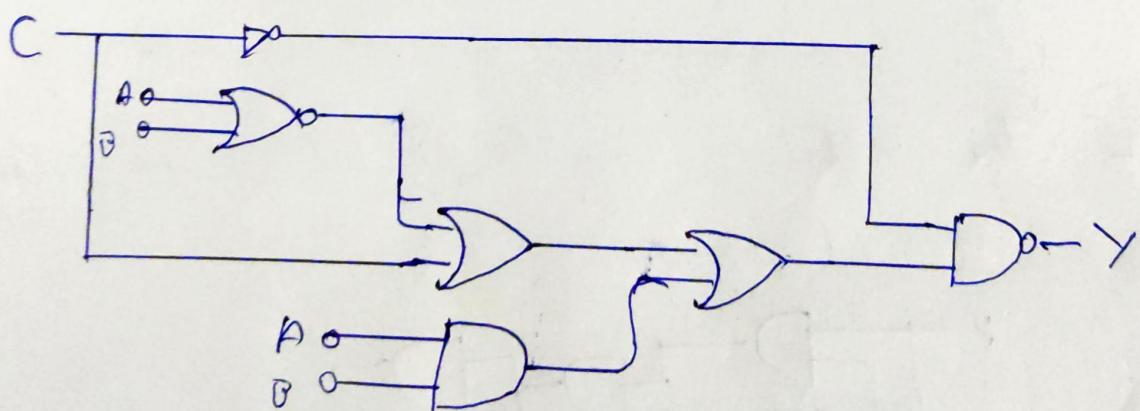
④  $P = 1 \quad Q = 1 \quad R = 1$

$$\therefore F = \left( \overline{\overline{PQ}} \overline{QR} \overline{PR} \right)$$

$$= \left( \overline{PQ} \overline{QR} \overline{PR} \right)$$

$$= \left( \overline{PQ} + \overline{QR} + \overline{PR} \right)$$

③ In the circuit shown below, if  $C = 0$ , the expression for  $Y$  is



The equation for the given circuit is

$$Y = \{[(\bar{A} + \bar{B}) + C] + \bar{A}\bar{B}\} \bar{C}$$

$$= \{[\bar{A}\bar{B}]$$

$$= \{[AB + C] + \bar{A}\bar{B}\} \bar{C}$$

$$= (AB + \bar{A}\bar{B} + C) \bar{C}$$

$$= A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + C\bar{C}$$

$$= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

Given  $C = 0$

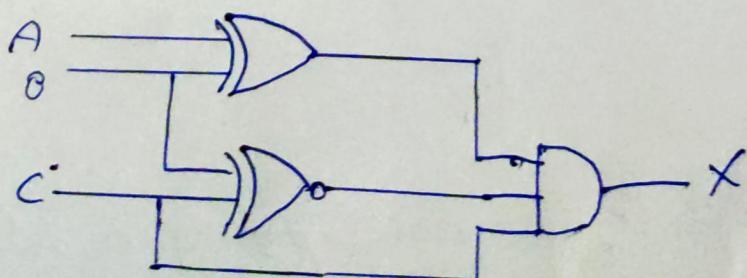
$$( \because C\bar{C} = 0 )$$

$$\therefore Y = \bar{A}\bar{B}(0) + A\bar{B}(0)$$

$$Y = 0 + 0$$

$$\boxed{Y = 0}$$

Q4 For the logic circuit shown in the figure, the required input condition ( $A, B, C$ ) to make output  $X = 1$  is



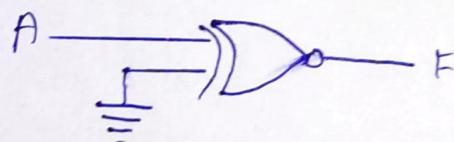
The truth table for the given circuit diagram is

A	B	C	$A \oplus B$	$\bar{B} \oplus C$	$(A \oplus B)(\bar{B} \oplus C)$	X
0	0	0	0	1	0	0
0	0	1	0	0	0	0
0	1	0	1	0	0	0
0	1	+	1	1	1	1
1	0	0	1	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	1	0	1	0	0

Output  $X = 1$  will be true for

$$\underline{A = 0}, \underline{B = 1}, \underline{C = 1}$$

Q5 The output for the logic gate in figure is



$$F = \overline{A + 0}$$

$$= \overline{A}$$

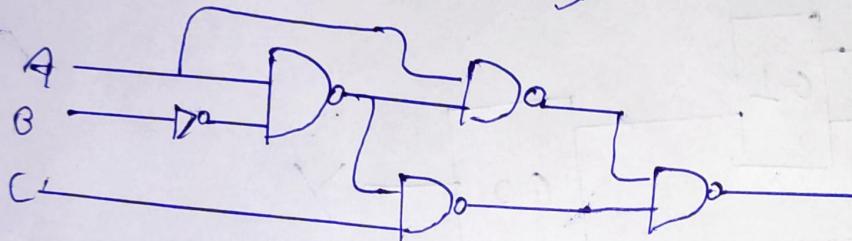
$\therefore$  The output for given logic gate is  $\overline{A}$

Q6 The minimum number of NANO gates required to implement the Boolean function  $A + A\bar{B} + A\bar{B}C$  is equal to

$$\text{let } F = A + A\bar{B} + A\bar{B}C$$

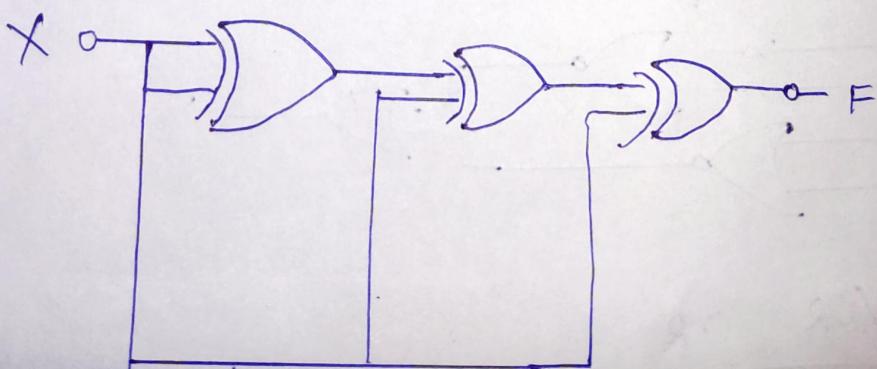
$$\begin{aligned}\bar{F} &= \bar{F} = \overline{\overline{A + A\bar{B} + A\bar{B}C}} \\ &= \overline{\overline{A}(\overline{A\bar{B}})(\overline{A\bar{B}C})}\end{aligned}$$

$$\therefore F = \overline{\overline{A}(\overline{A\bar{B}})(\overline{A\bar{B}C})}$$



$\therefore$  We require 4 NANO gates  
(c)

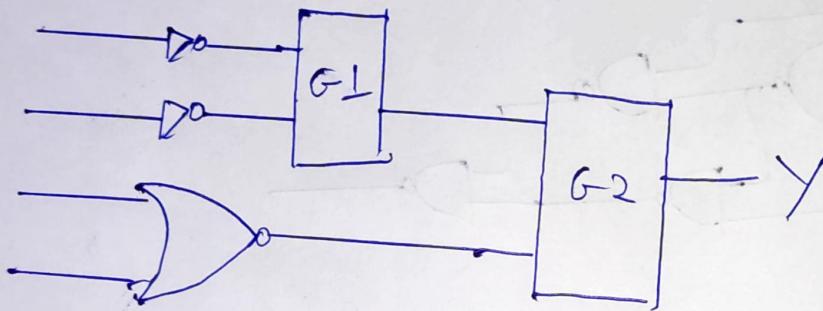
Q7 For the circuit given below the output  $F$  is given by



$X$	$\bar{X}$	$X \oplus X$	$\bar{X} \oplus (X \oplus X)$	$\bar{X} \oplus (\bar{X} \oplus (X \oplus X))$	$F$
0	1	0	1	0	1
1	0	0	0	0	1

∴ Output of  $F = \underline{\underline{1}}$

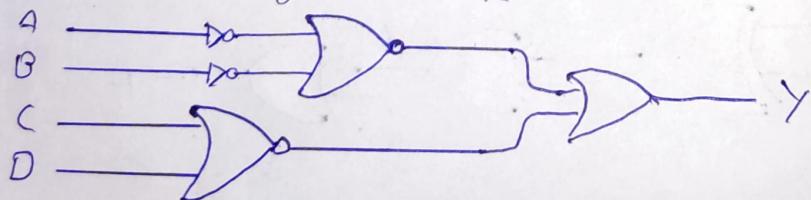
Q8 In the figure shown, the output  $Y$  is required to be  $Y = AB + \bar{C}\bar{D}$ , the gate  $G_1$  and  $G_2$  must be, respectively



$$Y = AB + \bar{C}\bar{D}$$

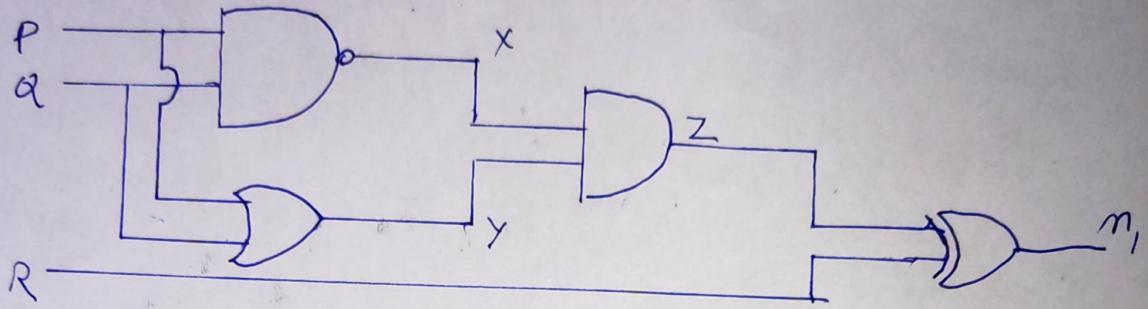
$$Y = \overline{\overline{AB}} + \overline{\bar{C}\bar{D}} = \underline{\underline{(\bar{A} + \bar{B}) + (C + D)}} \quad \text{(De Morgan's law)}$$

∴ The diagram is



(a) NOR, OR

Q9 Which of the following boolean expression correctly represents the relation between  $P, Q, R$  and  $M_1$ ?



$$M_1 = [(P \bar{Q}) (P + Q)] \oplus R$$

$$M_1 = [(P + \bar{Q}) \cdot (P + Q)] \oplus R$$

$$M_1 = [P\bar{Q} + Q\bar{P}] \oplus R$$

$$M_1 = [P \oplus Q] \oplus R$$

(d)  $M_1 = \underbrace{(P \text{ XOR } Q) \text{ XOR } R}$

Q10 The number of product in the minimized SOP expression obtained through the following k-map is (where 'd' denotes don't care)

$AB$	$CD$	00	01	11	10
00	I	0	0	0	I
01	0	d	0	0	
11	0	0	d	I	
10	I	0	0	I	

Dquad  $\rightarrow$  0000, 1000, 1010, 0010

Pair  $\rightarrow$  1110, 1010

\* Dquad  $\rightarrow \bar{B}\bar{D}$

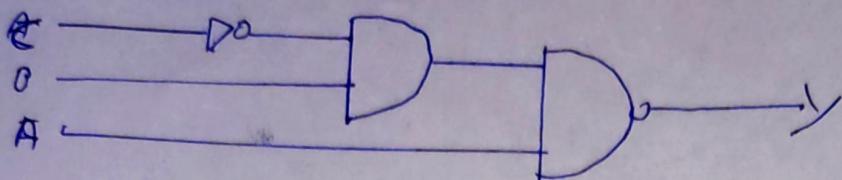
Pair  $\rightarrow A\bar{C}\bar{D}$

$$\therefore F = \bar{B}\bar{D} + A\bar{C}\bar{D}$$

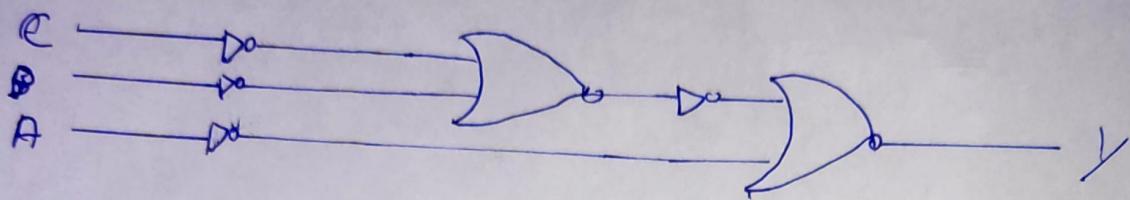
(a) 2

Q11 The truth table for the output  $Y$  in terms of 3 input  $A, B, C$  are given in table. Draw a logic circuit realization only NOR gate.

A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1
Y	1	1	1	0	1	0	0	0



$$Y = \overline{CBA}$$

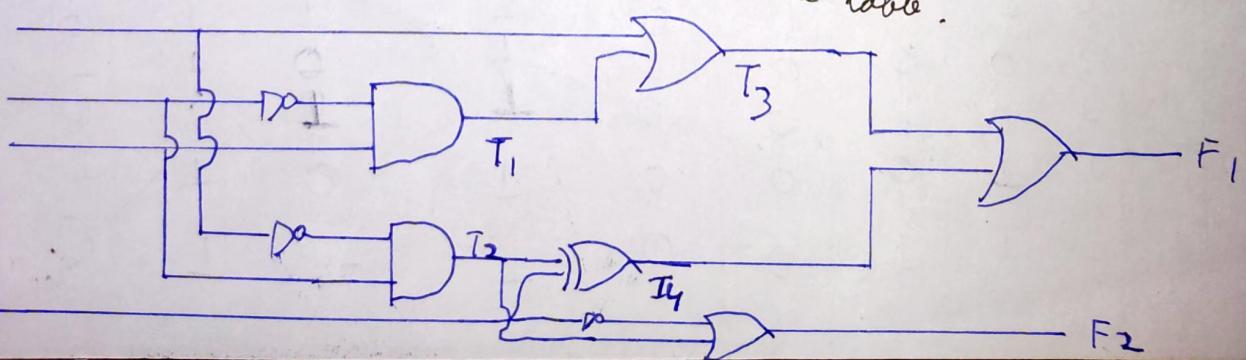


$$Y = /(\overline{C} + \overline{B}) +$$

$$Y = (\overline{\overline{C}} + \overline{\overline{B}}) + \overline{A}$$

$$Y = \overline{\overline{C} + \overline{B}} + \overline{A}$$

- Q12 Consider the combinational circuit shown below
- Derive the Boolean expression of  $T_1$  through  $T_4$ . Evaluate the outputs  $F_1$  and  $F_2$  as a function of four input
  - List the truth table for 16 binary combinations of the four input variables. Then list the binary values of  $T_1$  through  $T_4$  and output  $F_1$  and  $F_2$  in the table.



$$a) T_1 = \underline{\underline{8C}}$$

$$T_2 = \frac{\pi}{\alpha}$$

$$T_3 = \bar{B}C + A$$

$$T_4 = \bar{A}B \oplus D$$

$$F_1 = T_3 + T_4$$

$$F_1 = \bar{Q}C + A + \bar{A}B \oplus D$$

$$F_2 = T_2 + \bar{o}$$

$$F_2 = \bar{A}B + \bar{O}$$

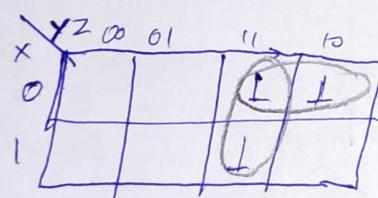
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Q13 Design a combinational circuit with 3 input  $x, y, z$  and 3 output  $A, B, C$ . When the binary input is 0, 1, 2, or 3 the output is two greater than the input. When the input is 4, 5, 6 and 7 the output is 3 less than input.

	$x$	$y$	$z$	$A$	$B$	$C$
0	0	0	0	0	1	0
1	0	0	1	0	1	1
2	0	1	0	1	0	0
3	0	1	1	1	0	1
4	1	0	0	0	0	1
5	1	0	1	0	1	0
6	1	1	0	0	1	1
7	1	1	1	1	0	0

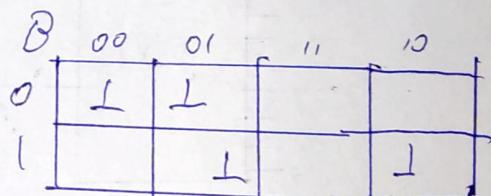
using K-map

for A



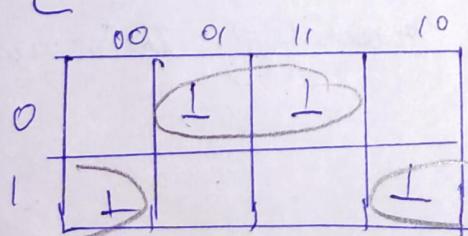
$$A = \bar{x}y + yz$$

for B

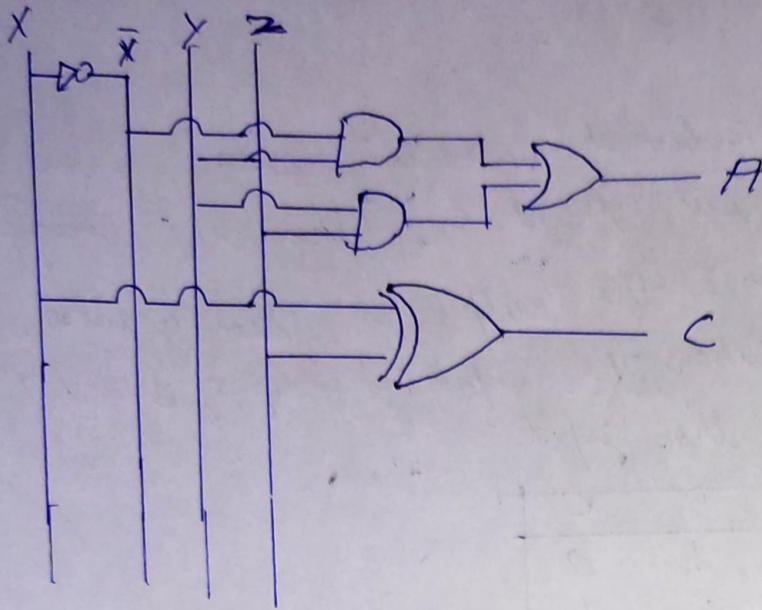


B is not possible

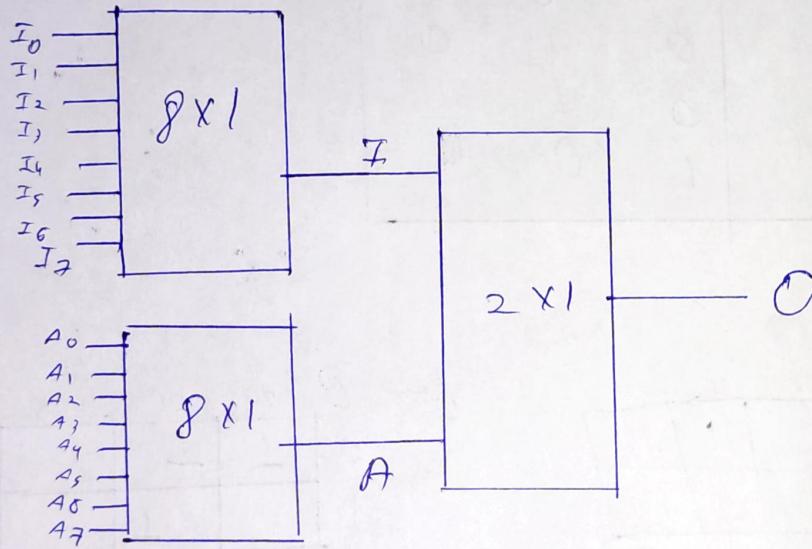
for C



(K/M diagram)  $C = \bar{x}z + x\bar{z} = x \oplus z$



(T4) Construct a  $16 \times 1$  multiplexer with 2  $8 \times 1$  and 1  $2 \times 1$  multiplexers. Use block diagram.



(Q15) Design a combinational circuit that converts a 4-bit gray code to a 4-bit binary number. Write the verilog dataflow model of the circuit.