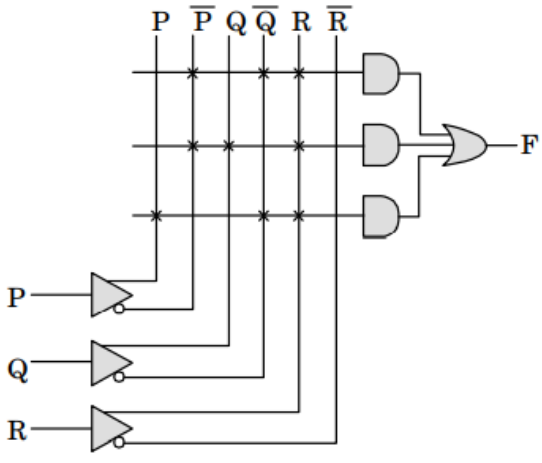
	ITER, SIKSHA 'O' ANUSANDHAN (Deemed to be University)		Assignment
Branch	**Computer Science and Engineering**	Programme	**B.Tech**
Course Name	**Digital Logic Design**	Semester	**III**
Course Code	**EET 1211**	Academic Year	**2022/Odd**
Assignment-4	**Topic- Registers and Counters, Memory and Programmable Logic**	**GP-1**	
Learning Level (LL)	**L1**: Remembering	**L3:** Applying	**L5**: Evaluating
	L2: Understanding	**L4**: Analysing	**L6**: Creating

Q's	Questions	COs	LL
1	Design a MOD 6 counter with T Flip-Flops	**CO4**	**L3**
2	Design a 2-bit synchronous up counter with T Flip-Flops and Write an HDL Behavioural description of the circuit.	**CO4, CO6**	**L3**
3	Design a 3-bit synchronous up counter with JK Flip-Flops.	**CO4**	**L3**
4	Design a 3-bit synchronous down counter with D Flip-Flops	**CO4**	**L3**
5	Design a 3-bit Asynchronous down counter with +ve edge triggered T Flip-Flops	**CO4**	**L3**
6	Design a 2-bit Asynchronous up/down counter with -ve edge triggered T Flip-Flops	**CO4**	**L3**
7	Explain the operation of PISO shift register	**CO4**	**L2**
8	A programmable logic array (PLA) is shown in the figure.  The Boolean function F implemented is **[2017]**	**CO5**	**L2**
09	Draw a PLA circuit to implement the functions $F_1 = A'B + AC + A'BC'$ $F_2 = (AC + AB + BC)'$	**CO5**	**L2**

10	List the PAL programming table for the BCD-to-excess-3-code converter whose Boolean functions are simplified in Fig. 4.3. $z = D'$ $y = CD + C'D' = CD + (C + D)'$ $x = B'C + B'D + BC'D' = B'(C + D) + BC'D'$ $= B'(C + D) + B(C + D)'$ $w = A + BC + BD = A + B(C + D)$	**CO5**	**L2**

Assignment 4	**Topic: Registers and Counters, Memory and Programmable Logic**	**Date of Assignment4: 17.01.2023**	**Date of Submission: 24.01.2023**

Note:

1. assignment carries weightage of **20 marks out of 100**
2. Course outcome CO4 to CO6 was covered.

Course Outcomes	CO1	Able to State and explain different number systems, binary codes
	CO2	Able to apply the principles of Boolean algebra and Karnaugh map to simplify logic expressions and implement it using gates
	CO3	Able to Analyse and design various combinational circuits
	CO4	Able to Analyse and design different synchronous and asynchronous sequential circuits
	CO5	Able to Analyse and design various Memory, Programmable Logic circuits and register transfer level
	CO6	Able to implement various digital circuits using HDL and Standard ICs.