

Programme: B. Tech

Semester: 3RD

Full Marks: 60 Time: 3 Hours

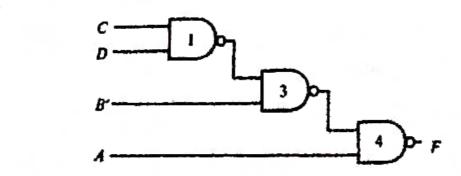
Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1, 2	10
Apply concepts of Boolean Algebra.	L3, L4	2, 3	8
Apply Theorems and functions along with logic gates to solve logic operations.	L4	4	6
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12

^{*}Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

- Translate the binary number (110101)₂ to its ² equivalent decimal number.
 - Using 1's complement method subtract the following binary numbers (101)2-(1110)2 s
 - Obtain the hexadecimal & octal number for the binary number (101110)₂
- 2. (a) Using 10's complement method subtract the 2 following binary numbers (26)10-(538)10
 - Obtain the gray code and 2421 code for (1001)₂. 2
 - (c) Simplify the given expression using Boolean algebra $F = a^{!} + ab'c + bc$

- Simplify the given expression using Boolean algebra F = x'yz + xy'z' + xyz + xyz'
 - Solve the given expression using k-map 2 (b) $F(a,b,c) = \Sigma m(0,1,4,6) + d(2,3)$
 - Construct the following function using NAND gates 2 (c) only

 $F(a,b,c) = \Sigma m(0,1,2,6)$



- Identify the number of input and output variables (a) used in the following logic diagram and obtain the Boolean function of the circuit
- Represent the Boolean Function obtained in 3(a) 2 (b) using K-Map and determine the simplified expression.
- Design a logic circuit to implement the function 2 obtained in 3(b).

A logic circuit accepts 3-bit binary as input and gives even parity as output

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- Draw the truth table. (a)
- (b) Obtain the simplified expressions. 2 Sketch the circuit using minimum number of logic (c)
- gates.
- 6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

4.

	(a)	Draw the truth table.	2
	(b)	Obtain the simplified expressions.	2
	(c)	Sketch the circuit using minimum number of logic	2
7.	(1)	gates. What is a priority encoder?	2
	(45)	Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only.	2
/	(c)	Design a half adder circuit with a decoder and one	2
8.	(a)	OR gates. What is a MULTIPLEXER?	2
,	(b)	Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER	2
	/O) /	Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer.	2
9.	(a)	Explain the working of a gated D-latch with circuit diagram.	2
•	(b)	Design a 2-bit down counter using D Flip Flops.	2
	(c)	How many clock pulse(s) is/are required to transfer the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift register?	2
10/		Design a synchronous MOD 6 down counter using T Flip Flops.	
	(a)	Write the state table	2
	(b)	Obtain the simplified expressions for FF inputs.	2
	(c)	Draw the circuit using T FFs	2
		End of Questions	



Programme: B. Tech Full Marks: 60 Semester: 3RD

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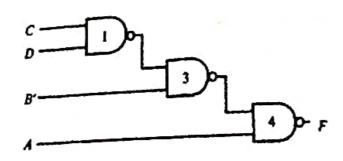
Time: 3 Hours

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks	
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1, 2	10	
Apply concepts of Boolean Algebra.	L3, L4	2, 3	8	
Apply Theorems and functions along with logic gates to solve logic operations.	LA	4	6	
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24	
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12	

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

- (a) Translate the binary number (110101)₂ to its ² equivalent decimal number.
 - (b) Using 1's complement method subtract the following binary numbers (101)₂-(1110)₂ s
 - (c) Obtain the hexadecimal & octal number for the binary number (101110)₂
- (a) Using 10's complement method subtract the 2 following binary numbers (26)₁₀-(538)₁₀
 - (b) Obtain the gray code and 2421 code for (1001)₂. 2
 - (c) Simplify the given expression using Boolean algebra 2 f = a' + ab'c + bc

- 3. (a) Simplify the given expression using Boolean algebra F = x'yz + xy'z' + xyz + xyz'
 - (b) Solve the given expression using k-map $F(a,b,c) = \sum m(0,1,4,6) + d(2,3)$
 - (c) Construct the following function using NAND gates only $F(a,b,c) = \Sigma m(0,1,2,6)$



- (a) Identify the number of input and output variables 2 used in the following logic diagram and obtain the Boolean function of the circuit
- (b) Represent the Boolean Function obtained in 3(a)
 using K-Map and determine the simplified expression.
- (c) Design a logic circuit to implement the function 2 obtained in 3(b).
- 5. A logic circuit accepts 3-bit binary as input and gives even parity as output
 - (a) Draw the truth table.
 - (b) Obtain the simplified expressions. 2
 - (c) Sketch the circuit using minimum number of logic ² gates.
- 6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

4.

	(a)	Draw the truth table.	2
	(b)	Obtain the simplified expressions.	2
	(c)	the state of logic	2
		gates.	2
7.	(a)	What is a priority encoder?	2
	(b)	Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only.	2
	(c)	Design a half adder circuit with a decoder and one	2
	(N	OR gates.	2
8.	(a)	What is a MULTIPLEXER?	
	(b)	Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER	2
	(c)	Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer.	2
9.	(a)		2
	(b)	Design a 2-bit down counter using D Flip Flops.	2
	(c)	How many clock pulse(s) is/are required to transfer the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift register?	2
10.		Design a synchronous MOD 6 down counter using T Flip Flops.	
	(a)	Write the state table	2
	(b)	Obtain the simplified expressions for FF inputs.	2
	(c)	Draw the circuit using T FFs	2
		End of Questions	
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Programme: B. Tech

Semester: 3RD

Time: 3 Hours

	Time:	3 Hours
*Taxonomy Level	Ques. Nos.	Marks
L3	1, 2	10
L3, L4	2, 3	8
L4	4	6
L1, L3, L6	5,6, 7,8	24
L1, L2, L3, L6	9,10	12
	Level L3 L3, L4 L4 L1, L3, L6 L1, L2, L3, L6	*Taxonomy Ques. Level Nos. L3 1, 2 L3, L4 2, 3 L4 4 L1, L3, L6 5,6, 7,8 L1, L2, L3, 9,10

^{*}Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

(a) Translate the binary number (110101)₂ to its a equivalent decimal number.
 (b) Using 1's complement method subtract the following

binary numbers (101)₂-(1110)₂_s
(c) Obtain the hexadecimal & octal number for the binary number (101110)₂

2. (a) Using 10's complement method subtract the following binary numbers (26)10-(538)10

(b) Obtain the gray code and 2421 code for (1001)₂.

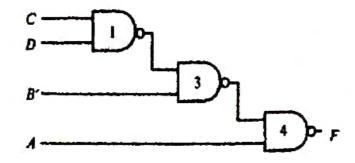
(c) Simplify the given expression using Boolean algebra F = a' + ab'c + bc

page 1 of 4

- 3. (a) Simplify the given expression using Boolean algebra F = x'yz + xy'z' + xyz + xyz'
 - (b) Solve the given expression using k-map $F(a, b, c) = \Sigma m(0, 1, 4, 6) + d(2, 3)$
 - (c) Construct the following function using NAND gates 2 only

$$F(a, b, c) = \Sigma m(0, 1, 2, 6)$$

4.



- (a) Identify the number of input and output variables 2 used in the following logic diagram and obtain the Boolean function of the circuit
- (b) Represent the Boolean Function obtained in 3(a)
 using K-Map and determine the simplified
 expression.
- (c) Design a logic circuit to implement the function 2 obtained in 3(b).
- A logic circuit accepts 3-bit binary as input and gives even parity as output
 - (a) Draw the truth table.
 - (b) Obtain the simplified expressions. 2
 - (c) Sketch the circuit using minimum number of logic ² gates.
- A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

2

	(a)	Draw the truth table.	2
	(b)	Obtain the simplified expressions.	2
	(c)	Sketch the circuit using minimum number of logic	2
7.	(a)	gates. What is a priority encoder?	2
	(b)	Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only.	2
	(c)	Design a half adder circuit with a decoder and one OR gates.	2
8.	(a)	What is a MULTIPLEXER?	2
	(b)	Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER	2
	(c)	Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer.	2
9.	(a)	Explain the working of a gated D-latch with circuit	2
	(b)	diagram. Design a 2-bit down counter using D Flip Flops.	2
	(c)	How many clock pulse(s) is/are required to transfer the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift register?	
10.		Design a synchronous MOD 6 down counter using T Flip Flops.	
	(a)	•	2
	(b)	Obtain the simplified expressions for FF inputs.	2
	(c)		2
		End of Questions	



Programme: B. Tech Full Marks: 60 Semester: 3RD Time: 3 Hours

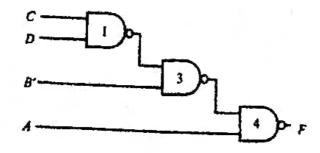
Time. 5 Hours			
*Taxonomy Level	Ques. Nos.	Marks	
L3	1, 2	10	
1.3, L4	2,3	8	
LA	4	6	
L1, L3, L6	5,6, 7,8	24	
L1, L2, L3, L6	9,10	12	
	Level 1.3 1.3, 1.4 1.4 1.1, 1.3, 1.6 1.1, 1.2, 1.3,	*Taxonomy Ques. Level Nos. 1.3 1, 2 1.3, L4 2, 3 L4 4 L1, L3, L6 5,6, 7,8 L1, L2, L3, 9,10	

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

- (a) Translate the binary number (110101)₂ to its ² equivalent decimal number.
 - (b) Using 1's complement method subtract the following 2 binary numbers (101)2-(1110)2s
 - (c) Obtain the hexadecimal & octal number for the binary number (101110)₂
- 2. (a) Using 10's complement method subtract the 2 following binary numbers (26)10-(538)10
 - (b) Obtain the gray code and 2421 code for (1001)2.
 - (c) Simplify the given expression using Boolean algebra F = a' + ab'c + bc

- 3. (a) Simplify the given expression using Boolean algebra 2 F = x'yz + xy'z' + xyz + xyz'
 - (b) Solve the given expression using k-map $F(a, b, c) = \sum m(0, 1, 4, 6) + d(2, 3)$
 - (c) Construct the following function using NAND gates 2 only

$$F(a,b,c) = \Sigma m(0,1,2,6)$$



- (a) Identify the number of input and output variables used in the following logic diagram and obtain the Boolean function of the circuit
- (b) Represent the Boolean Function obtained in 3(a) 2 using K-Map and determine the simplified expression.
- (c) Design a logic circuit to implement the function 2 obtained in 3(b).
- A logic circuit accepts 3-bit binary as input and gives even parity as output
 - (a) Draw the truth table.
 - (b) Obtain the simplified expressions. 2
 - (c) Sketch the circuit using minimum number of logic ² gates.
- 6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

4.

	(a)	Draw the truth table.	2
	(b)		2
			1
	(c)	Sketch the circuit using minimum number of logic	2
7.	(a)	gates. What is a priority encoder?	2
	(b)	Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only.	2
	(c)	Design a half adder circuit with a decoder and one OR gates.	2
8.	(a)	What is a MULTIPLEXER?	2
	(b)	Design a combinational circuit for a 2-bit XOR gate using 4:1 MULTIPLEXER	2
	(c)	Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using Multiplexer.	2
9.	(a)	Explain the working of a gated D-latch with circuit diagram.	2
	(b)	Design a 2-bit down counter using D Flip Flops.	2
	(c)	How many clock pulse(s) is/are required to transfer the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift register?	2
10.		Design a synchronous MOD 6 down counter using T Flip Flops.	
	(a)	Write the state table	2
	(b)	Obtain the simplified expressions for FF inputs.	2
	(c)	Draw the circuit using T FFs	2
		End of Questions	



MID SEMESTER EXAMINATION, OCTOBER-2018 DIGITAL LOGIC (CSE 1011)

Programme: B.Tech

Full Marks: 30

Semester:3RD

Time: 2 Hours

Subject/Course Learning Outcome	*Taxo nomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to	L3	1	6
represent information in digital components.		4	
Apply concepts of Boolean Algebra	L3	2(a)	2
Apply Theorems and functions along with logic gates to solve logic operations.	L6	2(b,c)	4
Design and analyze combinational circuits using logic gates and K-map.	L6	3,4	12
Design and analyze clocked sequential circuits using latches and flip-flops.	L6	5	6

^{*}Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer an questions. Each question carries equal mark.	
1. (a) Construct EX-OR gate using minimum numbers of NAND gates only.	2
Construct EX-OR gate using minimum numbers of NAND gates only. Translate the following binary number to corresponding decimal, octal & hexadecimal number: (110111.1011) Obtain the BCD & excess-3 code for 456.	2
Obtain the BCD & excess-3 code for 456.	प्
Determine the simplified expression of the following Boolean algebra rules $(A + B')(A' + B' + D)(B' + C + D') \qquad B' + ACD$	2
Minimize the given expression using k-map $F(a,b,c) = \sum m(0,5,7) + d(1,4) b + kC$	2
Find the complement of the Boolean function and reduce them to a minimum number of literals. [(AB)'A][(AB)'B] AB+B'+A'=	2
Design a combinational circuit that converts a decimal digit from the 8,4,-2,-1 code to BCD.	
Ma) A Obtain the truth table for the above circuit.	2
and the simplified function in sum of products.	2
2 Draw the logic diagram of the simplified function using	2
NAND gate only. Construct a 3-to-8 line decoder circuit using 2-to-4 line decoder only.	2
(b) Construct a FULL SUBTRACTOR using 8 to 1 line multiplexers.	2
A combinational circuit has three inputs x, y & z and two outputs f1 & F2. The Boolean expression for two outputs is as given below:	2
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Implement the combinational circuit using the decoder and external NAND gates.

5. (a)

What is the difference between a latch and a flip flop?

Compare the behavior of SR Flip Flop with JK Flip Flop...

Convert JK Flip Flop to T Flip Flop and derive its 2 characteristic table.

End of Questions This = ap



MID SEMESTER EXAMINATION, SEPTEMBER-2019 DIGITAL LOGIC (CSE 1011)

Programme : B.Tech (CSE & CSIT)

Semester:3RD

Full Marks: 30

Time: 2 Hours

nomy Level	Nos.	
L3	1,2	12
L3	3	6
L6	4,5	12
-	L3 L3 L6	L3 1,2 L3 3

^{*}Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

- Implement the given function by using only NAND gates. 2 (a) 1.
 - Find (a) the diminished radix and (b) the radix 2 (b) complement of (235)10. 76 81
 - Represent (542)10 in BCD and excess-3 code. 2 (c) 0101
- 2 1000 Find the value of X if

(a) 2. (789) 16+(473) 8=(X) 4 $7 \times 16^{2} + 8 \times 16^{4} + 9 \times 16^{6} + 4 \times 8^{2} + 3 \times 8^{4} + 3 \times 8^{6} = 20$ $(929 + 315 = (2244))_{4} = (x)_{4} = (2030 10)_{4}$

Given X = 10010 and Y = 10011 (a) find X-Y and (b) 2 find Y-X using 2's complement form. 00001 What is the even parity and odd parity of A =0101100 2 (c) Prove X.X = X and (X')' = X using postulates 2 (a) 3. Find the dual of the expression : XY' + (Y+Z)(X+Z')2 (b) Simplify the following expressions using Boolean ABC+D (C+BC) theorems and Postulates (c) AB'C'+CD'+BC'D'ABC + D(C+B) Obtain the Boolean expression that compares two 2 bit 2 numbers A and B to check if A is greater than B. (a) 4. $F = \sum (4, 8, 9, 12, 12/9)$ certain Combinational circuit converts a four bits binary number to a four bits gray code. Design the above circuit by finding the circuit truth table. 2 (b) Determine the Boolean equations required to design the 2

above circui'

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- Construct a 3-to-8 line decoder circuit using 2-to-4 line 2 (a) 5. decoder only.
 - Construct a FULL SUBTRACTOR using 8 to 1 line 2 (b) multiplexers.
 - A combinational circuit has three inputs x, y & z and two 2 (c) outputs F1 & F2. The Boolean expression for two outputs is as given below:

$$F_1 = \Sigma(2,4,7)$$

 $F_2 = \Sigma(0,2,3,4,7)$

Implement the combinational circuit using the decoder and external NAND gates.



MID SEMESTER EXAMINATION, OCTOBER-2018 DIGITAL LOGIC (CSE 1011)

Programme: B.Tech

Full Marks: 30

Semester:3RD

Time: 2 Hours

Subject/Course Learning Outcome	*Taxo nomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1	6
Apply concepts of Boolean Algebra	L3	2(a)	2
Apply Theorems and functions along with logic gates to solve logic operations.	L6	2(b,c)	4
Design and analyze combinational circuits using logic gates and K-	L6	3,4	12
map. Design and analyze clocked sequential circuits using latches and flip-flops.	L6	5	6

^{*}Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

	1	Construct EX-OR gate using minimum numbers of NAND	2
1.	(a)	gates only.	
	(b)	Translate the following binary number to corresponding decimal, octal & hexadecimal number: (110111.1011)	2
	10	Obtain the BCD & excess-3 code for 456.	2
		Determine the simplified expression of the following Boolean function using Boolean algebra rules $(A + B')(A' + B' + D)(B' + C + D')$	2
~	US	Minimize the given expression using k-map $F(a,b,c) = \sum m(0,5,7) + d(1,4)$	2
,	JEY	Find the complement of the Boolean function and reduce them to a minimum number of literals. [(AB)'A][(AB)'B]	2
3.		Design a combinational circuit that converts a decimal digit from the 8,4,-2,-1 code to BCD.	
~	(10)	Obtain the truth table for the above circuit.	2
-	401	Express the simplified function in sum of products.	2
V	40	Draw the logic diagram of the simplified function using	2
4.	las	NAND gate only. Construct a 3-to-8 line decoder circuit using 2-to-4 line decoder only.	2
~	(المار) مر	Construct a FULL SUBTRACTOR using 8 to 1 line multiplexers.	2
`	Jel 1	A combinational circuit has three inputs x, y & z and two outputs F1 & F2. The Boolean expression for two outputs is as given below:	2

F1= XZ + X' Y' Z' F2= X' Y + X Y' Z'

Implement the combinational circuit using the decoder and external NAND gates.



What is the difference between a latch and a flip flop? 2

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Compare the behavior of SR Flip Flop with JK Flip Flop.. 2

Convert JK Flip Flop to T Flip Flop and derive its 2 characteristic table.

End of Questions



Programme: B. Tech Full Marks: 60 Semester: 3RD Time: 3 Hours

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Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	1.3	1,2	10
Apply concepts of Boolean Algebra.	13, L4	2,3	8
Apply Theorems and functions along with logic gates to solve logic operations.	L4	4	6
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

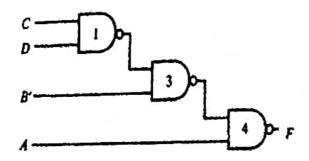
- (a) Translate the binary number (110101)₂ to its ² equivalent decimal number.
 - (b) Using 1's complement method subtract the following binary numbers (101)₂-(1110)₂ s
 - (c) Obtain the hexadecimal & octal number for the binary number (101110)₂
- (a) Using 10's complement method subtract the ² following binary numbers (26)₁₀-(538)₁₀
 - (b) Obtain the gray code and 2421 code for (1001)₂.
 - (c) Simplify the given expression using Boolean algebra F = a' + ab'c + bc

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- 3. (a) Simplify the given expression using Boolean algebra F = x'yz + xy'z' + xyz + xyz'
 - (b) Solve the given expression using k-map $F(a, b, c) = \Sigma m(0, 1, 4, 6) + d(2, 3)$
 - (c) Construct the following function using NAND gates 2 only

 $F(a, b, c) = \Sigma m(0, 1, 2, 6)$

4.



- (a) Identify the number of input and output variables ² used in the following logic diagram and obtain the Boolean function of the circuit
- (b) Represent the Boolean Function obtained in 3(a) 2 using K-Map and determine the simplified expression.
- (c) Design a logic circuit to implement the function obtained in 3(b).
- 5. A logic circuit accepts 3-bit binary as input and gives even parity as output
 - (a) Draw the truth table.

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- (b) Obtain the simplified expressions.
- (c) Sketch the circuit using minimum number of logic ² gates.
- 6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

	(a)	Draw the truth table.	2
	(b)	Obtain the simplified expressions.	2
	(c)	Sketch the circuit using minimum number of logic gates.	2
7.	(a)		2
	(b)	Construct a 3-to-8 line decoder circuit using 2-to-4 line decoders only.	2
	(c)	Design a half adder circuit with a decoder and one OR gates.	2
8.	(a)	What is a MULTIPLEXER?	2
0,	(b)	Design a combinational circuit for a 2-bit XOR gate	2
	()	using 4:1 MULTIPLEXER	
	(c)	Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using	2
9.	(a)	Multiplexer. Explain the working of a gated D-latch with circuit	2
		diagram	2
	(b)	Design a 2-bit down counter using D Flip Flops.	2
	(c)	How many clock pulse(s) is/are required to transfer the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift	
		register? Design a synchronous MOD 6 down counter using T	•
10.		Design a synchronous wie by	
	20.5	Flip Flops.	2
	(a)	Write the state table	2
	(b)	Obtain the simplified expressions for FF inputs.	2
	(c)	Draw the circuit using T FFs	
		End of Questions	

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SUMMER QUARTER EXAMINATION, JUNE - 2018 DIGITAL LOGIC (CSE 1011)

Programme: B. Tech Full Marks: 60 Semester: 3RD

Time: 3 Hours

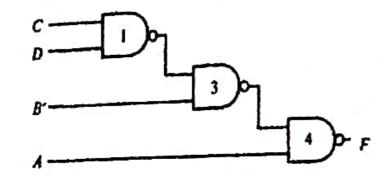
Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Apply concepts of number systems, binary codes to represent information in digital components.	L3	1, 2	10
Apply concepts of Boolean Algebra.	L3, L4	2, 3	8
Apply Theorems and functions along with logic gates to solve logic operations.	L4	4	6
Design and analyze combinational circuits using logic gates and K-Map.	L1, L3, L6	5,6, 7,8	24
Design and analyze sequential circuits	L1, L2, L3, L6	9,10	12

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

- (a) Translate the binary number (110101)₂ to its equivalent decimal number.
 - (b) Using 1's complement method subtract the following binary numbers (101)₂-(1110)₂ s
 - (c) Obtain the hexadecimal & octal number for the binary number (101110)₂
- 2. (a) Using 10's complement method subtract the 2 following binary numbers (26)10-(538)10
 - (b) Obtain the gray code and 2421 code for (1001)₂.
 - (c) Simplify the given expression using Boolean algebra F = a' + ab'c + bc

- 3. (a) Simplify the given expression using Boolean algebra F = x'yz + xy'z' + xyz + xyz'
 - (b) Solve the given expression using k-map $F(a,b,c) = \Sigma m(0,1,4,6) + d(2,3)$
 - (c) Construct the following function using NAND gates 2 only

 $F(a,b,c) = \Sigma m(0,1,2,6)$



- (a) Identify the number of input and output variables used in the following logic diagram and obtain the Boolean function of the circuit
- (b) Represent the Boolean Function obtained in 3(a) 2 using K-Map and determine the simplified expression.
- (c) Design a logic circuit to implement the function ² obtained in 3(b).
- A logic circuit accepts 3-bit binary as input and gives even parity as output
 - (a) Draw the truth table.
 - (b) Obtain the simplified expressions. 2
 - (c) Sketch the circuit using minimum number of logic ² gates.
- 6. A logic circuit accepts 4-binary as input and gives output as 1 if and only if the input binary is not a BCD number.

4.

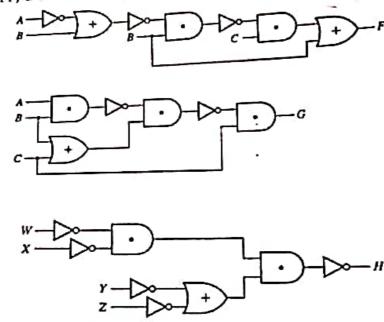
			_
			2
		Draw the truth table.	2
	(b)	Obtain the simplified expressions.	2
	(1)	Sketch the circuit using minimum number of logic	-
	(c)	skeith the chesses	2
7.	(a)	gates. What is a priority encoder?	2
	(b)	Construct a 3-to-8 line decoder circuit using 2-to-4	***
	(b)	line decoders only.	2
	(c)	line decoders only. Design a half adder circuit with a decoder and one	_
		OR gates.	2
8.	(a)	ATTI TIDI EXEK!	2
	(b)	Design a combinational circuit for a	
		using 4:1 MULTIPLEXER - The (0.1.2.6.8.9.11,13,14,15) using	2
	(c)	using 4:1 MULTIPLEXER Implement $F = \sum m(0,1,2,6,8,9,11,13,14,15)$ using	2
		Multiplexer. Explain the working of a gated D-latch with circuit	
9.	(a)	Explain the works o	2
	(h)	diagram. Design a 2-bit down counter using D Flip Flops. Design a 2-bit down counter using D Flip Flops.	2
	(b)		-
	(c)	How many clock pulse(s) is/are required to the data (1001) ₂ through a 4-bit (i) SISO (ii) PIPO shift	
		register?	<u>.</u>
10).	register? Design a synchronous MOD 6 down counter using T	
		Flip Flops.	2
	(a	the state table	2
	(b	Obtain the simplified expressions for FF inputs.	2
	(0	Draw the circuit using T FFs	
	•	*End of Questions*	9

DIGITAL LOGIC Assignment - 1

Course Code: CSE 1011 Branch: CSE, CSIT Grading Pattern: 1
Semester: 3rd

- Convert to hexadecimal, octal and binary
 - a. (123)10
 - b. (356)10
 - c. (1063)10
 - d. (725.25)10
- 2. Add and Subtract in binary
 - a. (1111)₂ and (1001)₂
 - b. $(1101001)_2$ and $(110110)_2$
 - c. $(100010)_2$ and $(11101)_2$
- Perform the subtraction with the following decimal numbers using 9's complement.
 - a. 5250 321
 - b. 753 864
- 4. Perform the subtraction using 2's complement method
 - a. 11010 1101
 - b. 10010 10011
 - c. 11010 -10000
- 5. The solution of the quadratic equation $X^2-11X+22=0$ are X=3 and X=6. What is the base of the number
- 6 Represent (542)₁₀ in BCD and 8421 BCD code
- 7 Prove Excess 3 Code is a self complementing code
- 8 Prove X+X= X and X+1=1 using postulates
- 9 $(16)_{10} = (100)_y$, Find y
- 10 Find the value of X
 - a) $(432)_5 = (X)_7$
 - b) $(789)_{16} + (473)_{8} = (X)_{4}$
- 11 Find the 16's complement of (BABA)₁₆

11. Find F, G & H and simplify.



12 Minimize the following expression

$$f = A[B + \bar{C}(\overline{A.B + A.\bar{C}})]$$

$$f = A + B[AC + (B + \bar{C})D]$$

$$f = (\overline{A + BC})(AB + A\bar{B}C)$$

$$f = (B + BC)(B + B\bar{C})(B + D)$$

- 13 Simplify each of the following expressions using Boolean theorems and Postulates.
 - a) ABCD' + A'B'CD + CD'
 - b) AB'C'+CD'+BC'D'
 - c) (A+B')(A'+B'+D)(B'+C+D')
 - d) xy' + z + (x' + y)z'
 - e) w'x' + x'y' + yz + w'z'
- Plot the following functions on a K-map F(A,B,C,D)=BD'+B'CD+ABC+ABC'D+B'D'
 - a) Find the minimum SOP.
 - b) Find the minimum POS
- 15 Find the minimized expression for each function
 - a) $f(a,b,c,d) = \Sigma m(0,2,3,4,7,8,14)$
 - b) $f(a,b,c,d) = \sum m(1,2,4,15) + d(0,3,14)$
 - c) $f(a,b,c,d) = \Pi M(1,2,3,4,9,15)$
 - d) $f(a,b,c,d) = \Pi M(0,2,4,6,8) \cdot D(1,9,12,15)$

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For given table, express F1 and F2 in product of maxterms

1	A	В	C	F1	F2
	0	0	0	1	<u>r</u> 2
	0	0	1	0	0
	0	1	0	•	1
	0	1	1	0	1
\vdash	1	0	1	0	1
\vdash	1		U	0	0
-	1	0	1	1	1
\vdash	1	_1	0	1	0
	1	1	1	1	1
					-

Obtain the simplified function in SOP and POS

17 Find Min term and Max term of the function

$$F_1=x'y'+yz+xz'$$

- Simplify the following functions and implement with NAND gates F=(B'+D')(A'+C'+D)(A+B'+C'+D)(A'+B+C'+D')
- 19 Implement the function F=X'Y +XY' + Z with NOR gates
- 20 Implement EX-OR gate using minimum number of NAND and NOR gate