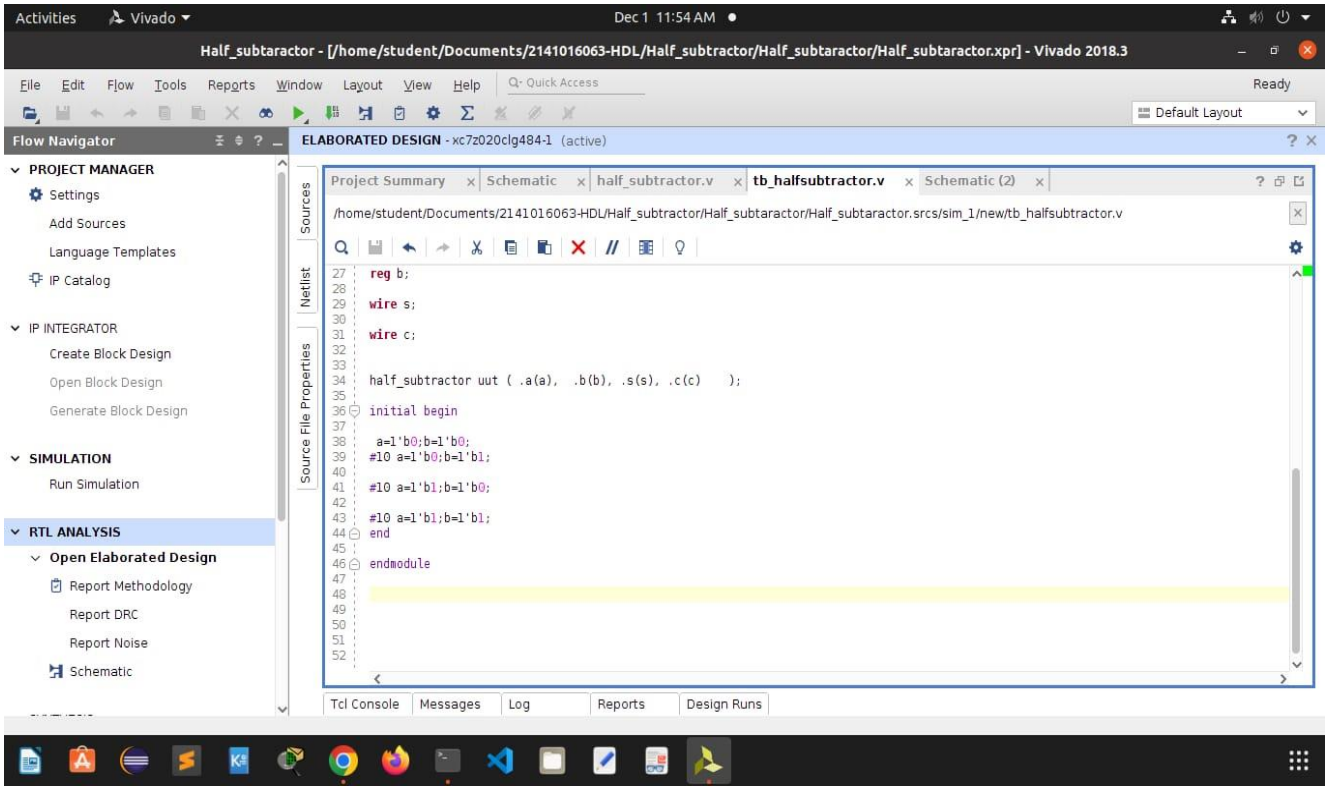
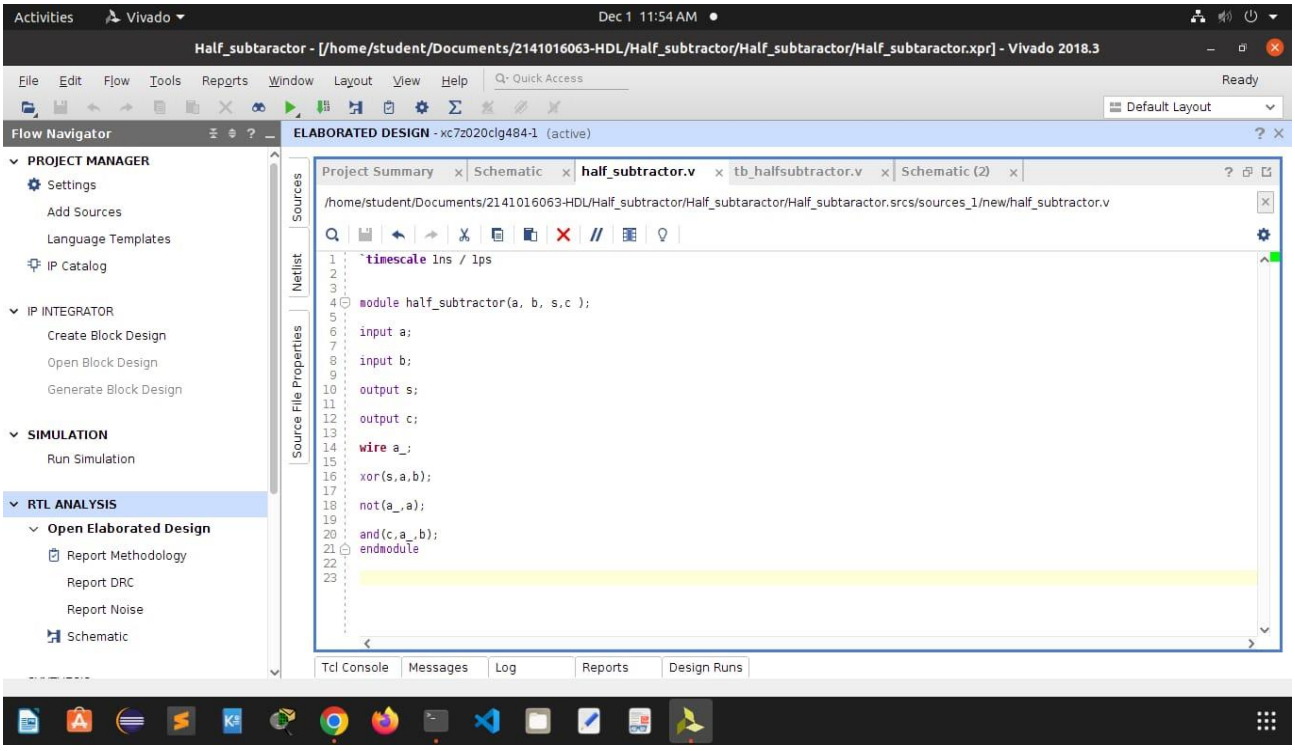
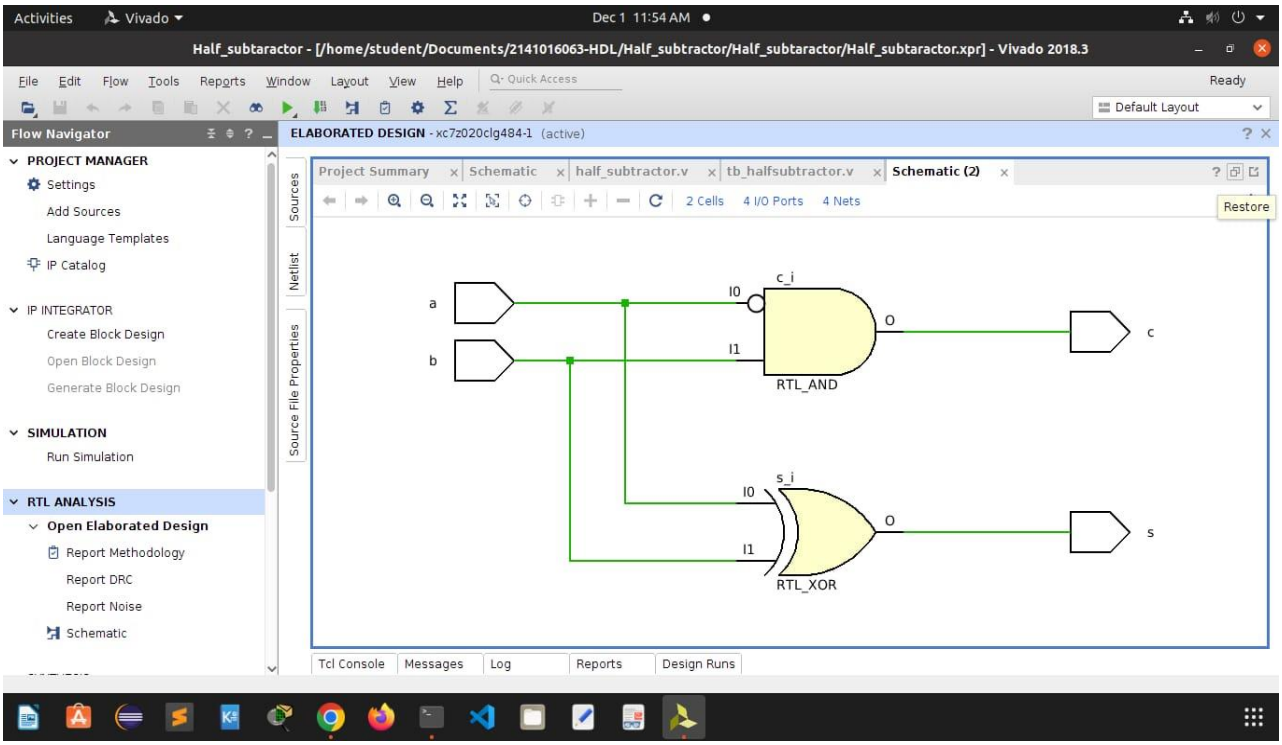
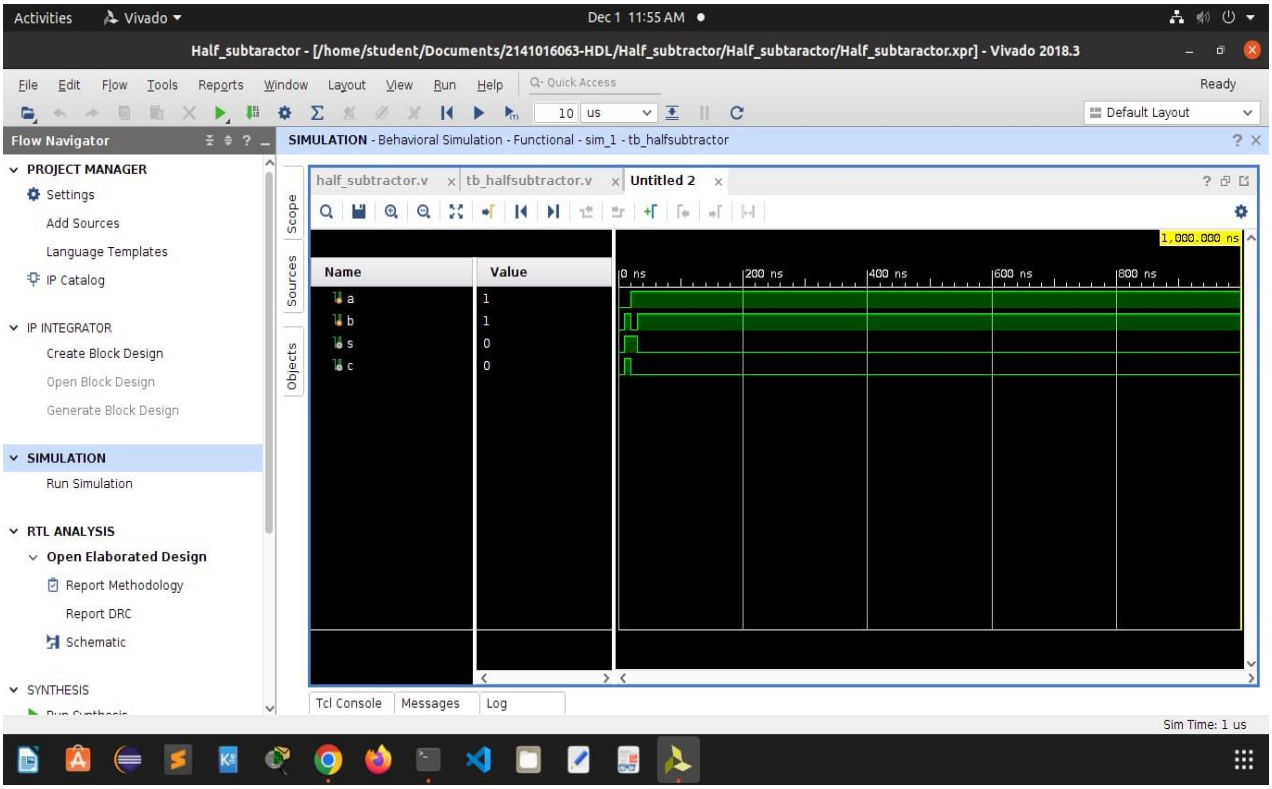
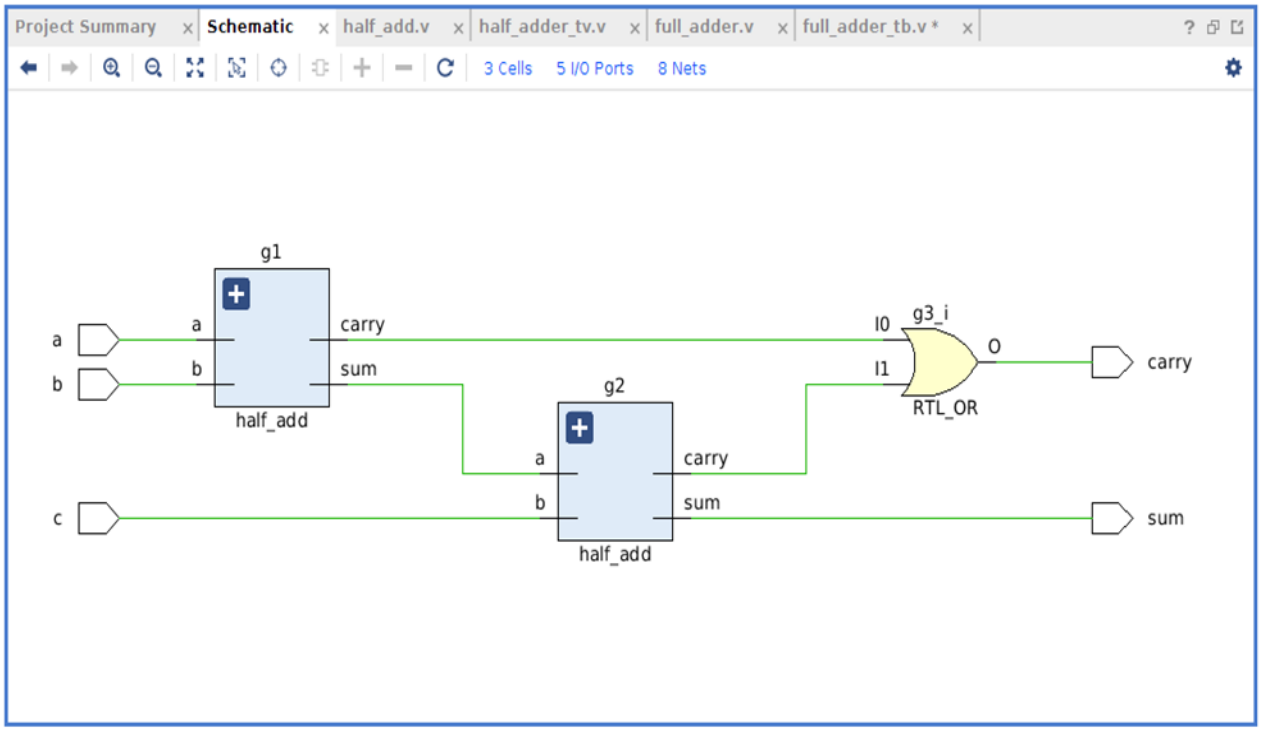
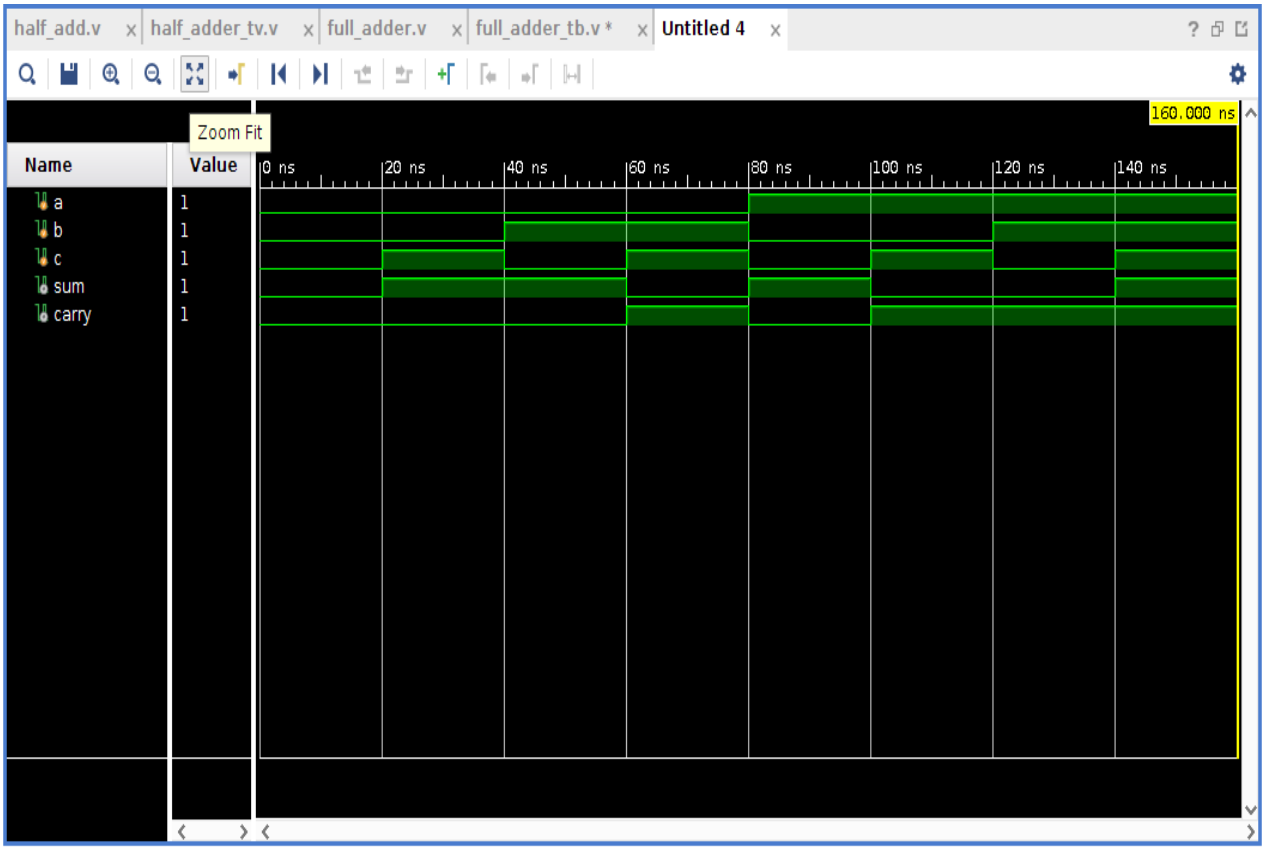

Activities
Vivado
Dec 1 11:54 AM
Half_subtaractor - [/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7z020clg484-1 (active)
Project Summary
Schematic
half_subtractor.v
tb_halfsubtractor.v
Schematic (2)
/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.srcs/sim_1/new/tb_halfsubtractor.v
reg b;
wire s;
wire c;
half_subtractor uut (.a(a), .b(b), .s(s), .c(c));
initial begin
a=1'b0;b=1'b0;
#10 a=1'b0;b=1'b1;
#10 a=1'b1;b=1'b0;
#10 a=1'b1;b=1'b1;
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Sources
Netlist
Source File Properties


Activities
Vivado
Dec 1 11:54 AM
Half_subtaractor - [/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7z020clg484-1 (active)
Project Summary
Schematic
half_subtractor.v
tb_halfsubtractor.v
Schematic (2)
/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.srcs/sources_1/new/half_subtractor.v
`timescale 1ns / 1ps
module half_subtractor(a, b, s,c);
input a;
input b;
output s;
output c;
wire a_;
xor(s,a,b);
not(a_,a);
and(c,a_,b);
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Sources
Netlist
Source File Properties


Activities
Vivado
Dec 1 11:54 AM
Half_subtaractor - [/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7z020clg484-1 (active)
Project Summary
Schematic
half_subtractor.v
tb_halfsubtractor.v
Schematic (2)
2 Cells
4 I/O Ports
4 Nets
Restore
Sources
Netlist
Source File Properties
a
b
c_i
I0
I1
O
RTL_AND
c
s_i
I0
I1
O
RTL_XOR
s
Tcl Console
Messages
Log
Reports
Design Runs


Activities
Vivado
Dec 1 11:55 AM
Half_subtaractor - [/home/student/Documents/2141016063-HDL/Half_subtractor/Half_subtaractor/Half_subtaractor.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
10 us
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_halfsubtractor
half_subtractor.v
tb_halfsubtractor.v
Untitled 2
Scope
Sources
Objects
Name
Value
a
1
b
1
s
0
c
0
1,000.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
Tcl Console
Messages
Log
Sim Time: 1 us


Project Summary
Schematic
half_add.v
half_adder_tv.v
full_adder.v
full_adder_tb.v *
3 Cells
5 I/O Ports
8 Nets
g1
a
b
carry
sum
half_add
g2
a
b
carry
sum
half_add
c
g3_i
I0
I1
O
RTL_OR
carry
sum


half_add.v
half_adder_tv.v
full_adder.v
full_adder_tb.v *
Untitled 4
Zoom Fit
160.000 ns
Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
a
b
c
sum
carry
1
1
1
1
1

half_add.v | half_adder_tv.v | full_adder.v | full_adder_tb.v | Untitled 4

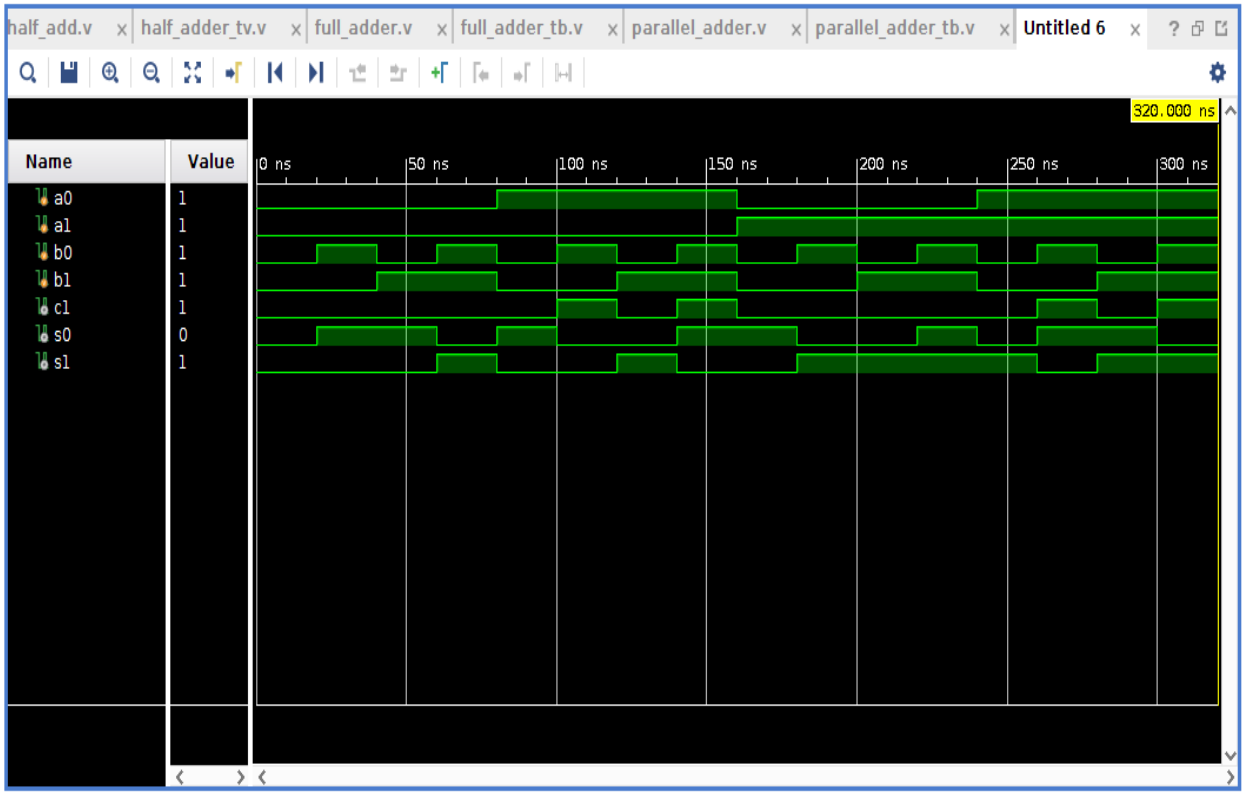
/home/student/Laxmidhar_2141019147/full_adder.srcs/sourses_1/new/full_adder.v

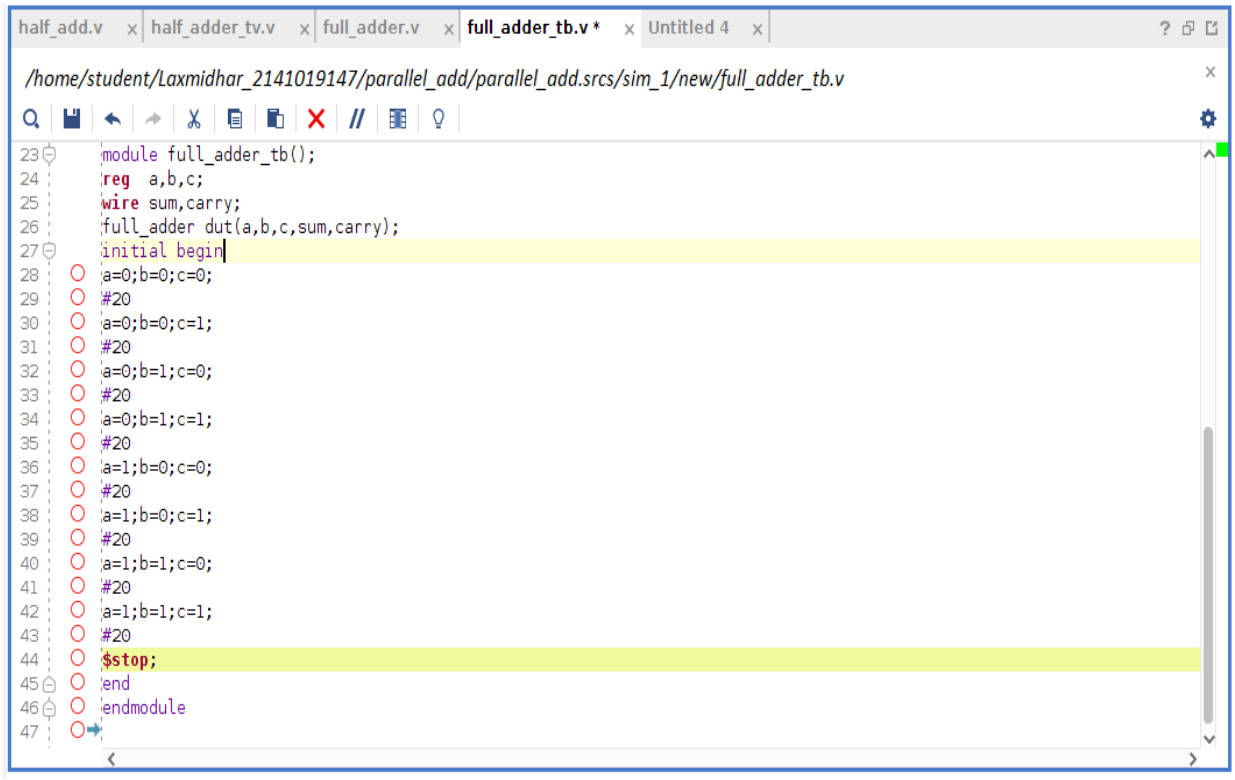
```
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25  module full_adder(
26      input a,
27      input b,
28      input c,
29      output sum,
30      output carry
31      );
32
33    wire w1,w2,w3; //intermediate o/ps
34    half_add g1(a,b,w1,w2);
35    half_add g2(w1,c,sum,w3);
36    or g3(carry,w2,w3);
37  endmodule
38
```

half_add.v | half_adder_tv.v | full_adder.v | full_adder_tb.v * | Untitled 4

/home/student/Laxmidhar_2141019147/full_adder/full_adder.srcs/sim_1/new/full_adder_tb.v

```
23  module full_adder_tb();
24  reg  a,b,c;
25  wire sum,carry;
26  full_adder dut(a,b,c,sum,carry);
27  initial begin
28  a=0;b=0;c=0;
29  #20
30  a=0;b=0;c=1;
31  #20
32  a=0;b=1;c=0;
33  #20
34  a=0;b=1;c=1;
35  #20
36  a=1;b=0;c=0;
37  #20
38  a=1;b=0;c=1;
39  #20
40  a=1;b=1;c=0;
41  #20
42  a=1;b=1;c=1;
43  #20
44  $stop;
45  end
46  endmodule
47
```


half_add.v
half_adder_tv.v
full_adder.v
full_adder_tb.v
parallel_adder.v
parallel_adder_tb.v
Untitled 6
320.000 ns
Name
Value
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
a0 1
a1 1
b0 1
b1 1
c1 1
s0 0
s1 1


half_add.v
half_adder_tv.v
full_adder.v
full_adder_tb.v *
Untitled 4
/home/student/Laxmidhar_2141019147/parallel_add/parallel_add.srcs/sim_1/new/full_adder_tb.v
module full_adder_tb();
reg a,b,c;
wire sum,carry;
full_adder dut(a,b,c,sum,carry);
initial begin
a=0;b=0;c=0;
#20
a=0;b=0;c=1;
#20
a=0;b=1;c=0;
#20
a=0;b=1;c=1;
#20
a=1;b=0;c=0;
#20
a=1;b=0;c=1;
#20
a=1;b=1;c=0;
#20
a=1;b=1;c=1;
#20
$stop;
end
endmodule

half_add.v | half_adder_tv.v | full_adder.v | full_adder_tb.v | parallel_adder.v * | parallel_adder_tb.v | Schema

/home/student/Laxmidhar_2141019147/parallel_adder/parallel_adder.srcs/sim_1/new/parallel_adder_tb.v

```
22
23  module parallel_adder_tb();
24  reg a0,a1,b0,b1;
25  wire c1,s0,s1;
26  parallel_adder dut(a0,a1,b0,b1,c1,s0,s1);
27  initial begin
28  a1=0;a0=0;b1=0;b0=0;
29  #20
30  a1=0;a0=0;b1=0;b0=1;
31  #20
32  a1=0;a0=0;b1=1;b0=0;
33  #20
34  a1=0;a0=0;b1=1;b0=1;
35  #20
36  a1=0;a0=1;b1=0;b0=0;
37  #20
38  a1=0;a0=1;b1=0;b0=1;
39  #20
40  a1=0;a0=1;b1=1;b0=0;
41  #20
42  a1=0;a0=1;b1=1;b0=1;
43  #20
```