

LOGIC DESIGN

EET-1021

CHAPTER 04

Lecture 24



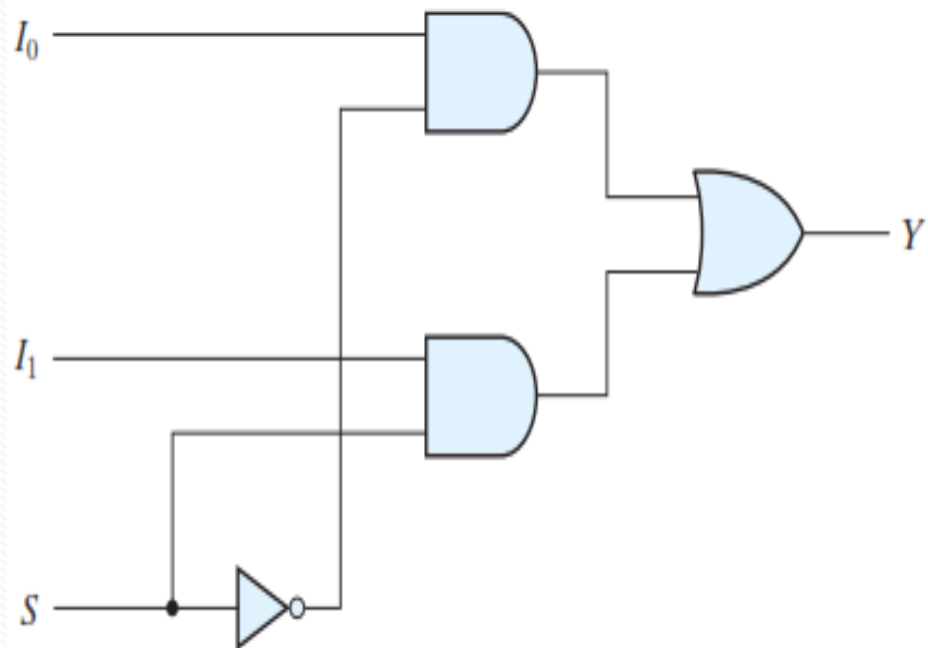
Combinational Logic

Overview of previous lecture

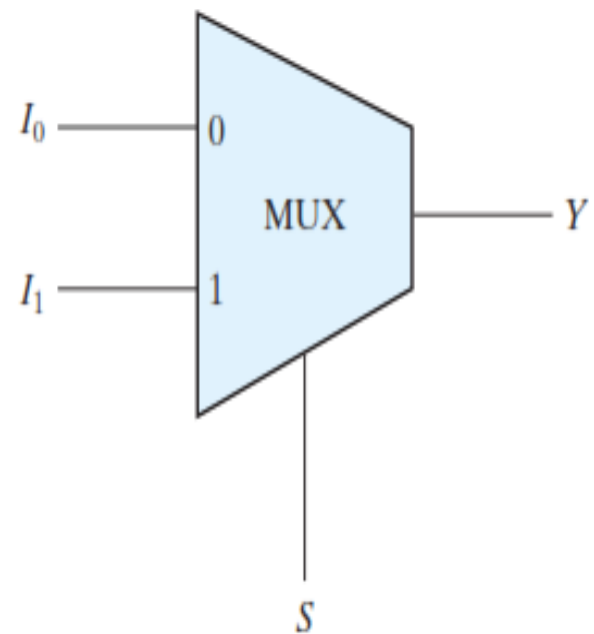
➤ **What is a Multiplexer**

Multiplexers

- A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n *selection* lines whose bit combinations determine which input is selected.
- In general, a 2^n -to-1-line multiplexer is constructed from an n -to- 2^n decoder by adding 2^n input lines to it, one to each AND gate. The outputs of the AND gates are applied to a single OR gate.



(a) Logic diagram



(b) Block diagram

Two-to-one-line multiplexer

HDL for Two-to-One Multiplexer

// Dataflow description of two-to-one-line multiplexer

```
module mux_2x1_df(Y, Io, I1, s);
```

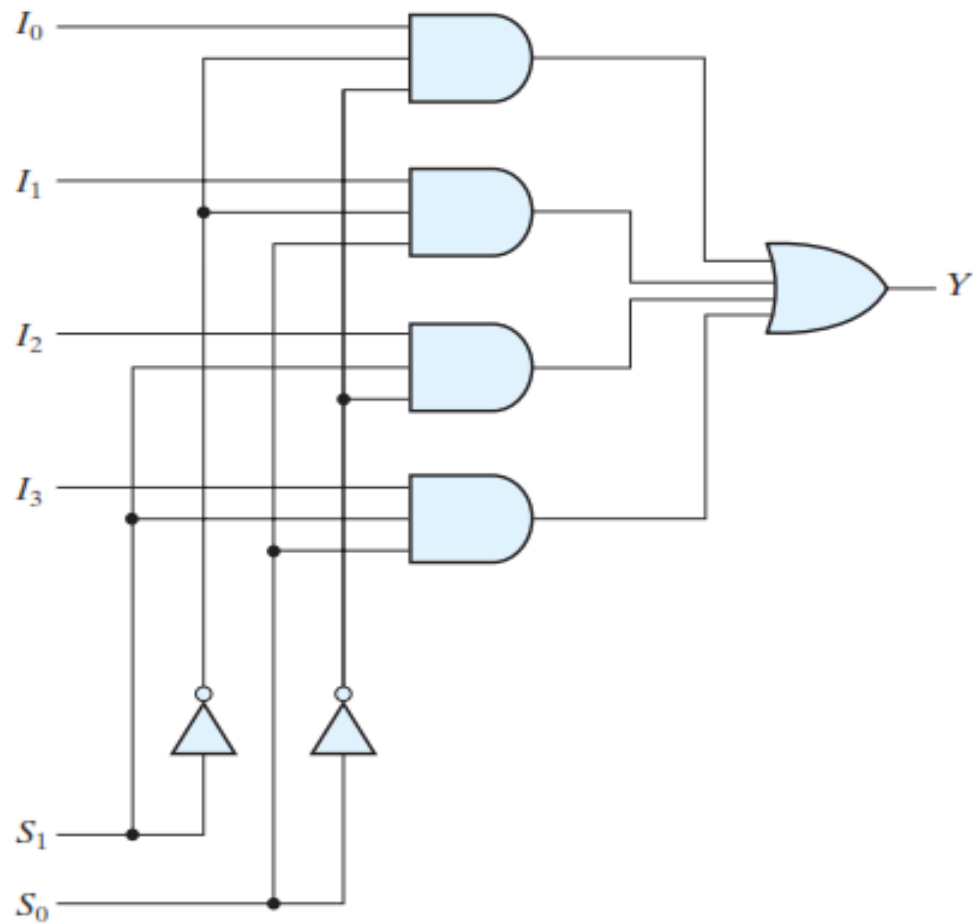
```
  output Y;
```

```
  input Io, I1;
```

```
  input s;
```

```
  assign Y = (s)? Io : I1;
```

```
endmodule
```



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

Four-to-one-line multiplexer

- **HDL for Four-to-One Multiplexer**

// Behavioral description of four-to-one-line multiplexer

```
module mux_4x1_beh (Y, I0, I1, I2, I3, s);
```

```
output Y;
```

```
input I0, I1, I2, I3;
```

```
input [1:0]s;
```

```
reg Y;
```

```
always @ (I0 or I1 or I2 or I3 or s)
```

```
begin
```

```
Case (s)
```

```
2' b00: Y<= I0;
```

```
2' b01: Y<= I1;
```

```
2' b10: Y<= I2;
```

```
2' b11: Y<= I3;
```

```
endcase
```

```
end
```

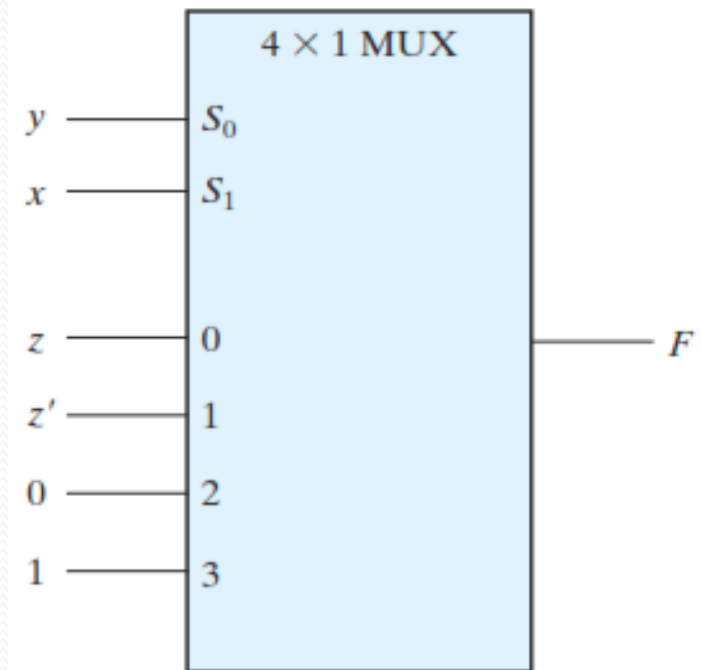
```
endmodule
```


Boolean Function Implementation

$$F(x, y, z) = \Sigma(1, 2, 6, 7)$$

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

(a) Truth table



(b) Multiplexer implementation

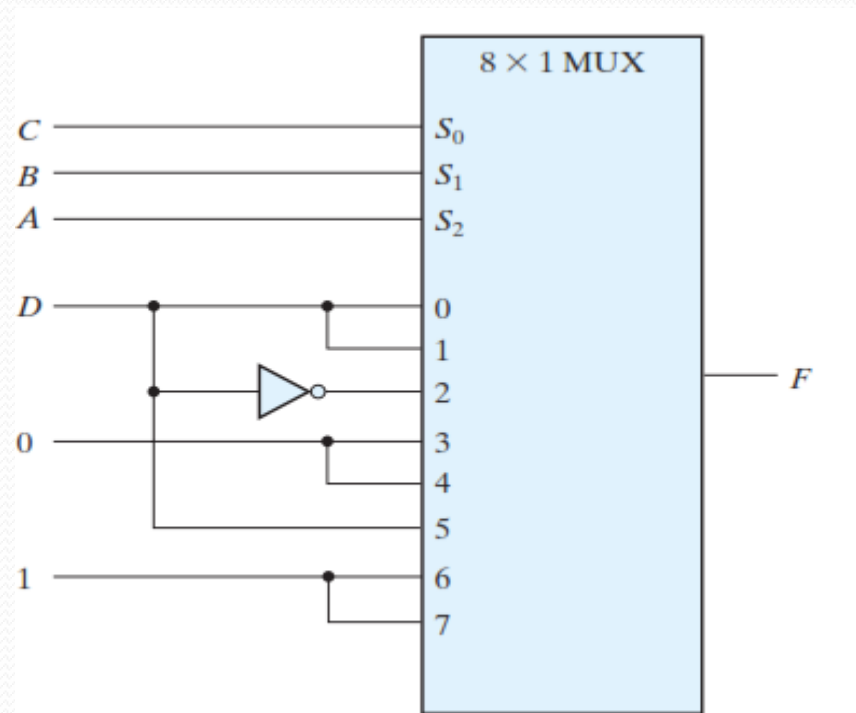
HDL for implementing a Boolean Function using Multiplexer :

```
module booleanfunction (F, z, s);  
input z;  
input [1:0]s;  
output F;  
wire z';  
not (z', z);  
mux_4x1_beh (F, z, z', 0, 1, s);  
endmodule
```

As a second example, consider the implementation of the Boolean function

$$F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>F</i>	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	



Implementing a four-input function with a multiplexer



THANK YOU