

: DL ASSIGNMENT - 4 :

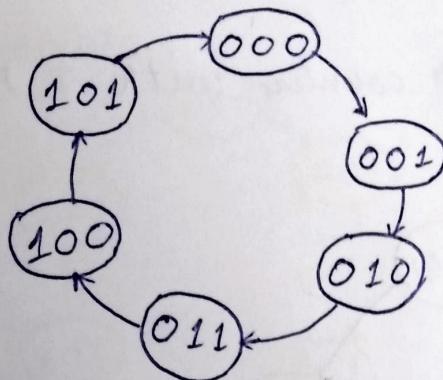
Name:- Vivek Kumar Mohanta  
Regd. No:- 2141013166

Section:- CSE - 'B'

1. MOD-6 counter using T- flipflops:-

MOD-6 can count 6 states.

State Diagram :-



State Table :-

PRESENT State			NEXT State			FLIP FLOP Inputs		
$Q_A$	$Q_B$	$Q_C$	$Q_{A+1}$	$Q_{B+1}$	$Q_{C+1}$	$T_A$	$T_B$	$T_C$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	1	0	1

$T_A$	00	01	11	$Q_B Q_C$
$Q_A$	0		1	
1		1	X	X

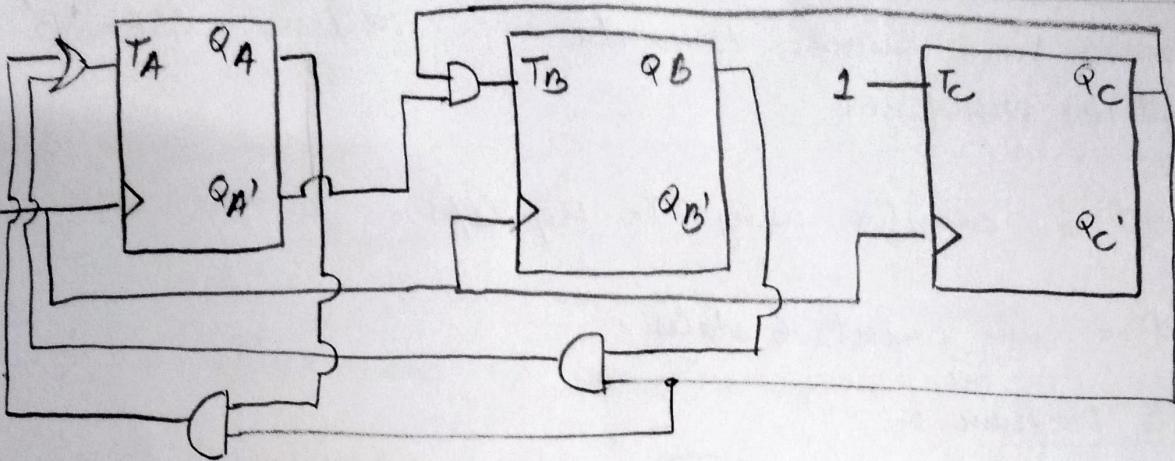
$$T_A = Q_A Q_C + Q_B Q_C$$

$$Q_A Q_C$$

$$T_C = 1$$

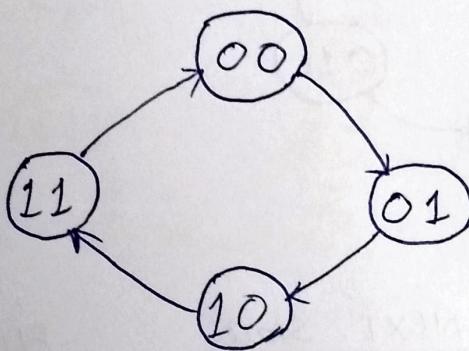
$T_B$	00	01	11	$Q_A' Q_C$
$Q_A$	0		1	
1		1	X	X

$$T_B = Q_A' Q_C$$



2. 2-bit synchronous up counter with T Flip-Flops:-

State Diagram :-

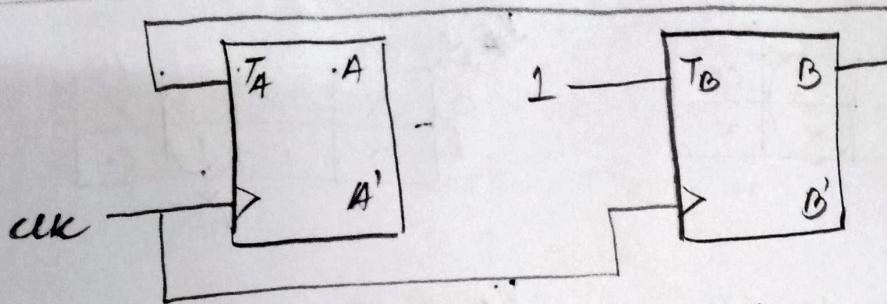


State Table :-

Present State		Next State		Flip Flop Inputs	
A	B	$A_{n+1}^{+1}$	$B_{n+1}^{+1}$	TA	TB
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

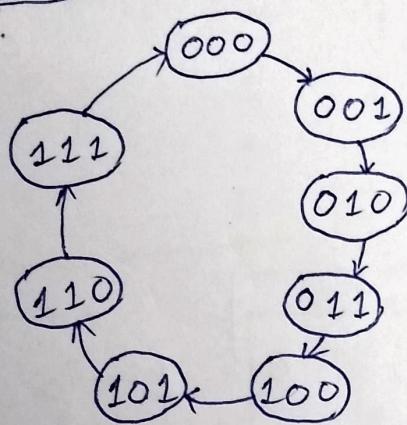
$$T_A = B$$

$$T_B = 1$$



3. 3-bit synchronous up counter with JK flip flop:-

State Diagram :-



State Table :-

Present State			Next State			Flip Flop Inputs					
A	B	C	A+1	B+1	C+1	J <sub>A</sub>	K <sub>A</sub>	J <sub>B</sub>	K <sub>B</sub>	J <sub>C</sub>	K <sub>C</sub>
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

		BC	
		00	01
		11	10
J <sub>A</sub>	0	0	0
J <sub>A</sub>	1	X	X

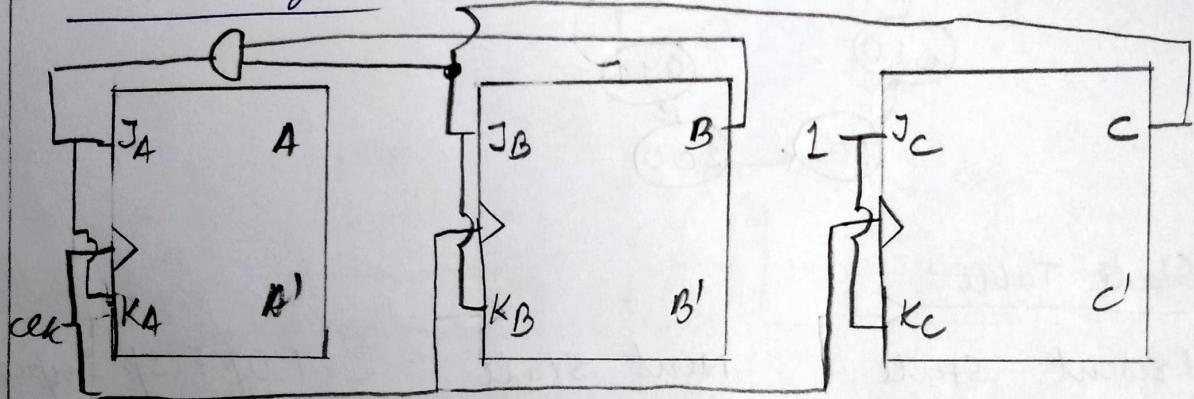
		BC	
		00	01
		11	10
K <sub>C</sub>	0	X	X
K <sub>C</sub>	1	0	0

		BC	
		00	01
		11	10
J <sub>B</sub>	0	0	1
J <sub>B</sub>	1	0	1

		BC	
		00	01
		11	10
K <sub>B</sub>	0	X	X
K <sub>B</sub>	1	X	X

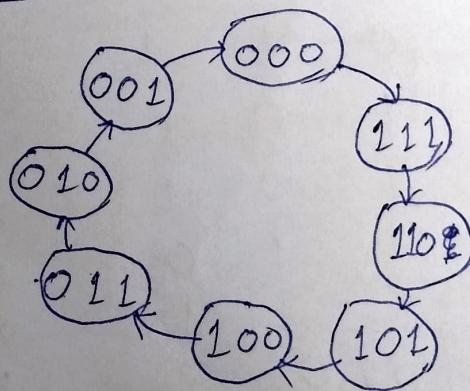
$$J_C = K_C = 1$$

Circuit Diagram :-



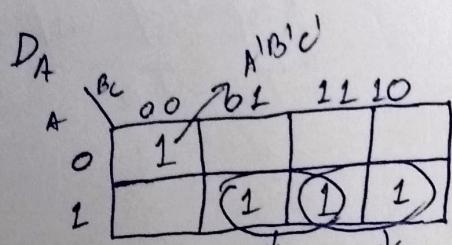
4. 3-bit synchronous down counter using D flip flop :-

State Diagram :-

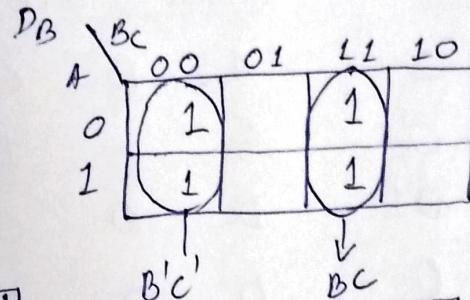


State Table:-

Present State			Next State			Flip Flop Input		
A	B	C	A+1	B+1	C+1	D <sub>A</sub>	D <sub>B</sub>	D <sub>C</sub>
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0

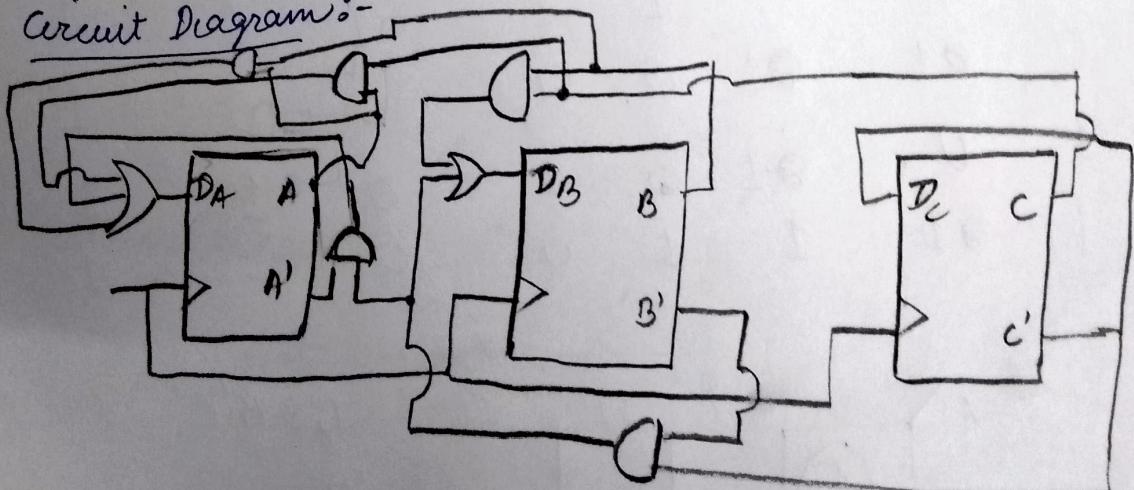


$$D_A = A'B'C' + AC + AB$$



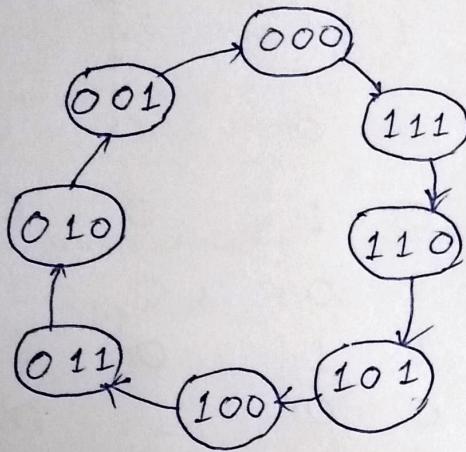
$$D_B = B'C'$$

Circuit Diagram:-



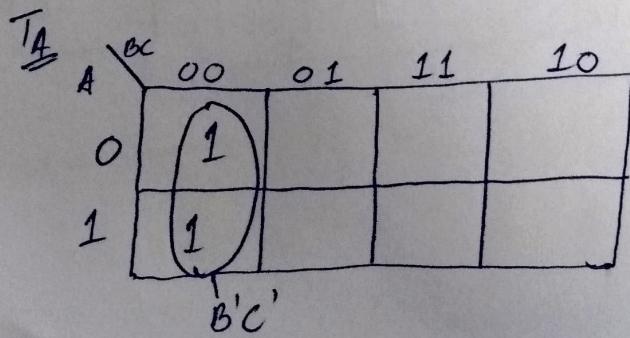
5-3-Bit asynchronous down counter with +ve edge triggered T-Flip Flop:-

State Diagram:-

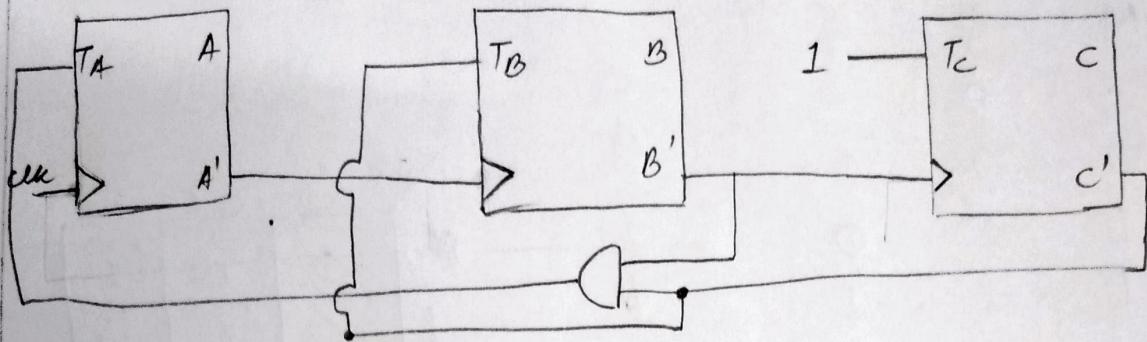


State Table:-

Present State			Next State			Flip-Flop inputs:		
A	B	C	A	B	C	$T_A$	$T_B$	$T_C$
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	0	1	0	0	0	1
1	1	0	0	1	1	0	1	1
1	1	1	1	1	0	0	0	1



$$\begin{aligned}T_A &= B'C' \\ T_B &= C' \\ T_C &= 1\end{aligned}$$

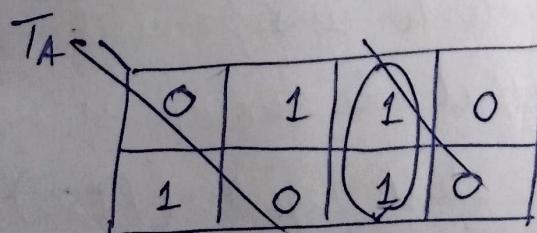


6. 2-Bit Asynchronous up-down counter using -ve edge triggered T F.F.

$$M = 0$$

$$M = 1$$

M	Present State		Next State		F.F. Inputs	
	A	B	A	B	T <sub>A</sub>	T <sub>B</sub>
0	0	0	0	1	0	1
0	0	1	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1



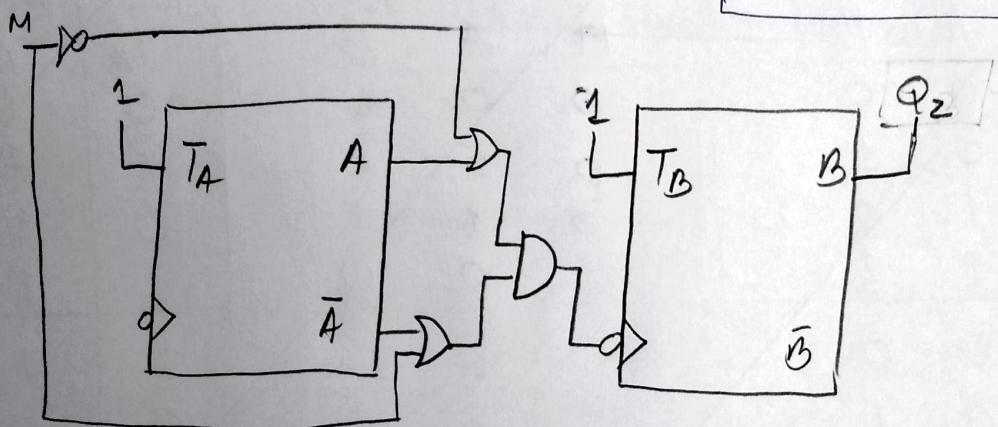
M	Q	$\bar{Q}$	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

QQ		00	01	11	10
M	0	0	0	1	1
1	0	1	1	1	0

$$Y = I + II$$

$$Y = \bar{M}Q + M\bar{Q}$$

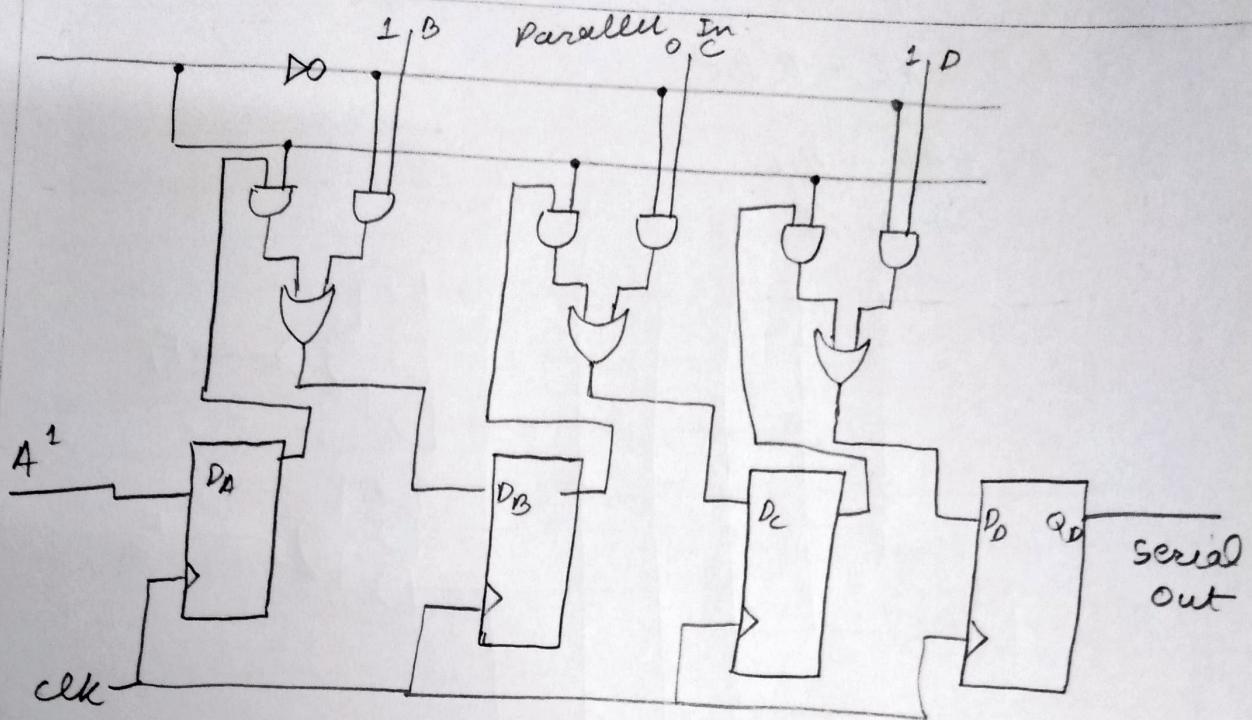
$$Y' = M\bar{Q} \oplus \bar{M}Q$$



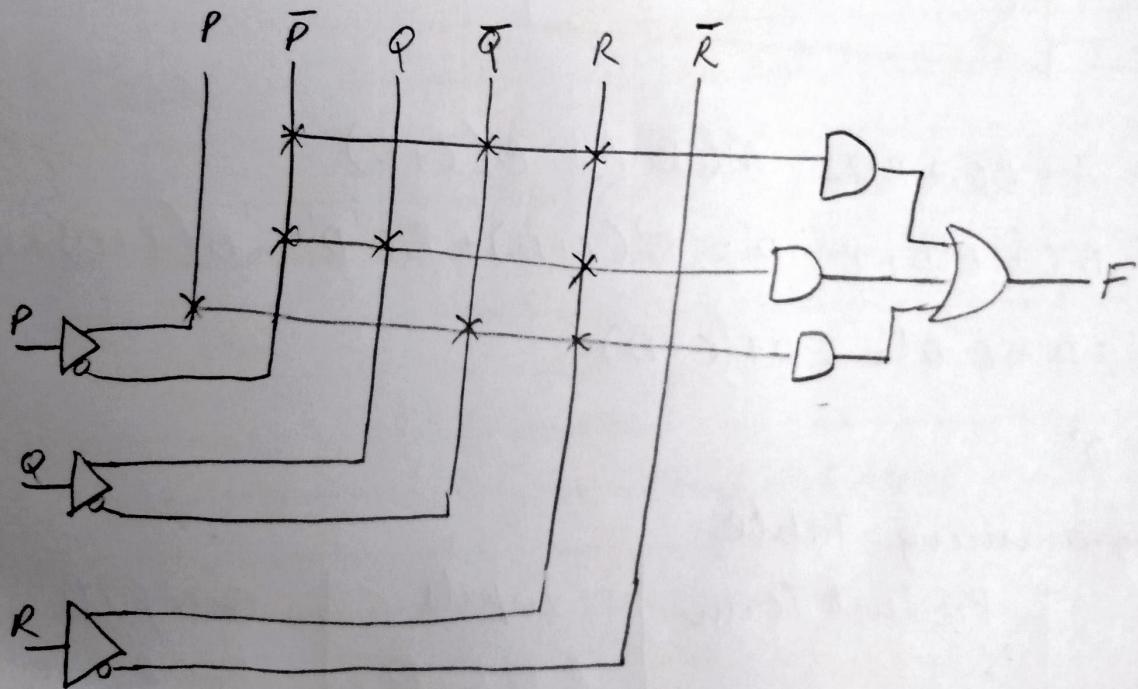
~~AB~~  $M=0 \Rightarrow$  up counter

$M=1 \Rightarrow$  down counter

7. The circuit, <sup>shift</sup>register which uses parallel input & generates serial output is known as the parallel input serial output shift register (PISO). The input of the 2nd Flip Flop is the output of the 1st flip flop.



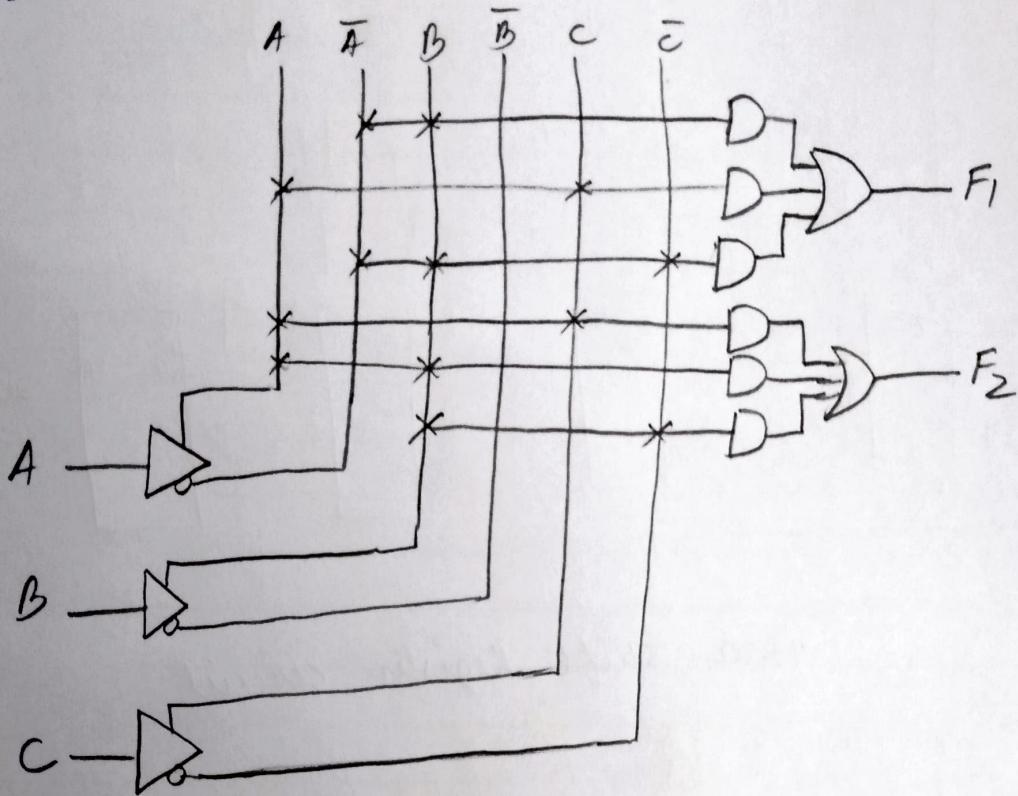
PISO shift Register circuit.



$$F = \bar{P}\bar{Q}R + \bar{P}QR + P\bar{Q}R$$

$$9. F_1 = A'B + AC + A'BC$$

$$F_2 = AC + AB + BC'$$



$$10. W = A + BC + BD = \cancel{A} + \cancel{B} A + B(C+D)$$

$$X = B'C + B'D + BC'D' = B'(C+D) + BC'D' = B'(C+D) + B(C+D)'$$

$$Y = CD + C'D' = CD + (C+D)'$$

$$Z = D'$$

Programming Table

Product Term	Inputs	Outputs					
		A	B	C	D	$F_1$	$F_2$
A	1	1	-	-	-	1	-
BC	2	-	1	1	-	1	1
BD	3	-	1	-	1	1	-
$B'C'D'$	4	-	0	0	0	-	1
CD	5	--	1	1	-	-	1
$C'D'$	6	--	-	0	0	-	-
$D'$	7	--	-	-	0	-	-