DIGITAL LOGIC

CHAPTER 5

Lecture 27

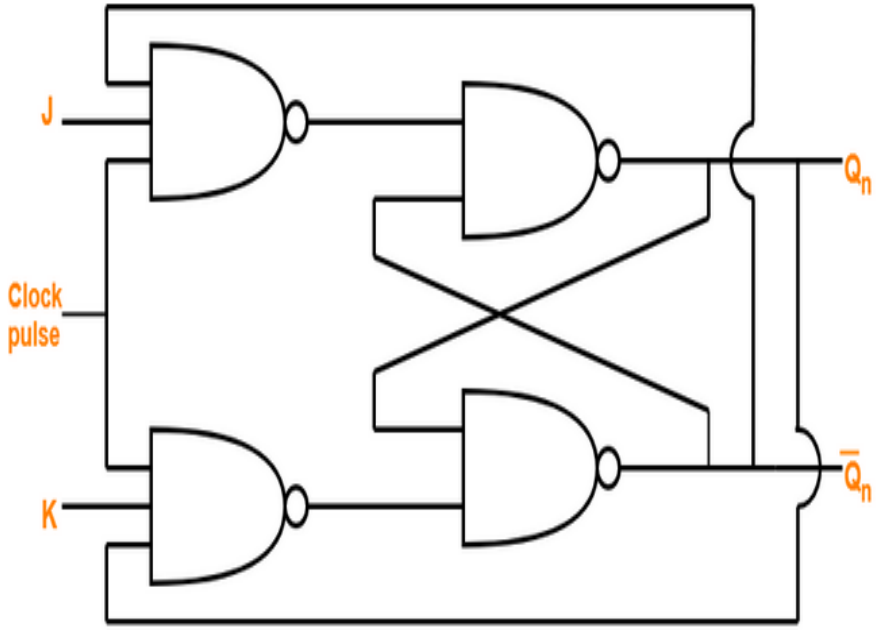
SEQUENTIAL LOGIC CIRCUITS

Clocked JK Flip-Flop

- The JK flip flop is the most versatile flip-flop, and the most commonly used flip flop.
- Like the RS flip-flop,it has two data inputs, J and K, and a clock pulse input (CP).
- In the following circuit diagram NAND gates are used instead of NOR gates.
- It has no undefined states, however.
- The fundamental difference of this device is the feedback paths.
- If the J and K inputs at 1 and the clock pulse is applied ,then the output will change state regardless of the previous condition.

Clocked JK Flip-Flop

Logic Symbol



Logic Circuit For JK Flip Flop Using SR Flip Flop

JK Flip Flop

CLK	J	K	Q
0	X	X	Unchanged
1	0	0	Unchanged
1	0	0	Reset(0)
1	1	0	Set(1)
1	1	1	Toggle(Q?)

FUNCTIONAL TABLE

JK Flip Flop

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

CHARACTERISTIC TABLE

K Map

$$Q_{n+1} = Q'_n J + Q_n K'$$

CHARACTERISTIC EQUATION

JK Flip Flop

$$Q_{n+1} = Q'_n J + Q_n K'$$

CHARACTERISTIC EQUATION

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

EXCITATION TABLE

HDL for JK Flip Flop:

```
module JKFLIPFLOP(input j, input k, input clk, output reg q, output q_not);
assign q_not =!q;
always@(posedge clk)
begin
if(clk==1) q <= (q_not&&j) || (q&&(!k));
end;
endmodule;
```

THANK YOU