DIGITAL LOGIC

CHAPTER 5

Lecture 26

SEQUENTIAL LOGIC CIRCUITS

STORAGE ELEMENTS: FLIP-FLOPS

- Latches and flip-flops are the basic elements for storing information.
- One latch or flip-flop can store one bit of information.

- The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted.

- In other words, when they are enabled, their content changes immediately when their inputs change.

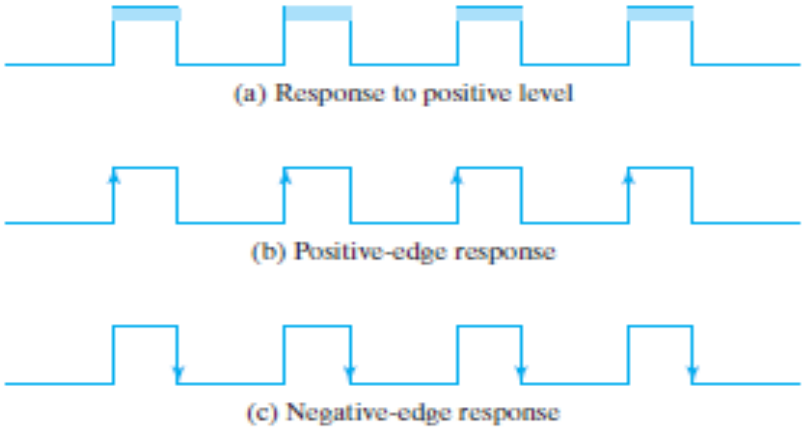
- Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal.

- This enable signal is usually the controlling clock signal.

- There are basically four main types of latches and flip-flops: **SR, D, JK,** and **T**.

- The major differences in these flip-flop types are the number of inputs they have and how they change state.

Clock response in latch and flip-flop



- The latch responds to a change in the ***level*** *of a clock pulse.*
- The key to the proper operation of a flip-flop is to trigger it only during a signal *transition .*
- *This can be accomplished* by eliminating the feedback path that is inherent in the operation of the sequential circuit using latches.
- A clock pulse goes through two transitions: from 0 to 1 and the return from 1 to 0.
- As shown in Figure , the positive transition is defined as the positive edge and the negative transition as the negative edge.

SR FLIP FLOP

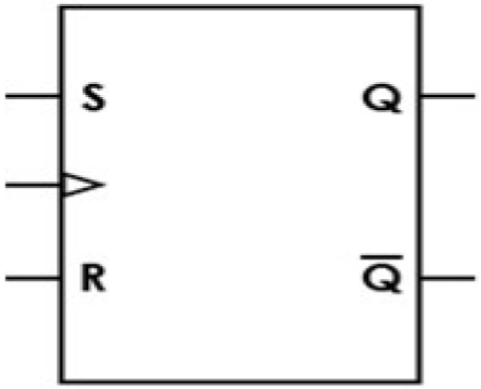
- The **SR flip-flop** can be considered as one of the most basic sequential logic circuit possible.

- This simple flip-flop is basically a one-bit memory bi-stable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled **S** and one which will “RESET” the device (meaning the output = “0”), labelled **R**.

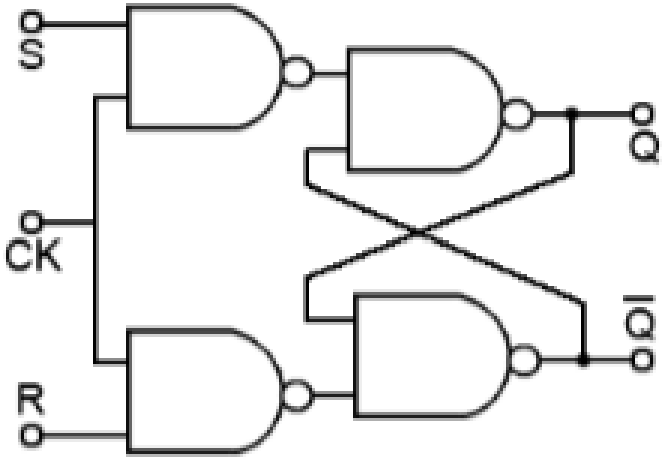
- Then the SR description stands for “Set-Reset”.

- The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level “1” or logic “0” depending upon this set/reset condition.

SR Flip Flop



FLIP-FLOP SYMBOL



LOGIC DIAGRAM

CLK	S	R	Q
0	X	X	Unchanged
1	0	0	Unchanged
1	0	0	Reset(0)
1	1	0	Set(1)
1	1	1	Indetermined

FUNCTIONAL TABLE

SR Flip Flop

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

CHARACTERISTIC TABLE

$$Q_{n+1} = S + Q_n R'$$

CHARACTERISTIC EQUATION

SR Flip Flop

$$Q_{n+1} = S + Q_n R'$$

CHARACTERISTIC EQUATION

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

EXCITATION TABLE

HDL for SR Flip Flop:

```
module sr_ff (input s, input r, input clk, output reg q, output q_not);
assign q_not =!q;
always @ (posedge clk)
begin
if(clk==1)
q <= s||(!r&&q);
end;
endmodule;
```

THANK YOU