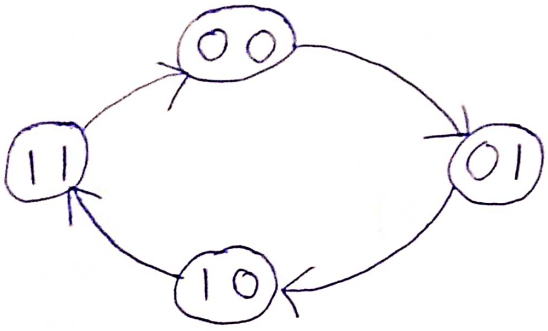
OBJECTIVE I : I

a) 2-bit synchronous up counter using D-flip-flop.



Exatiation table :-

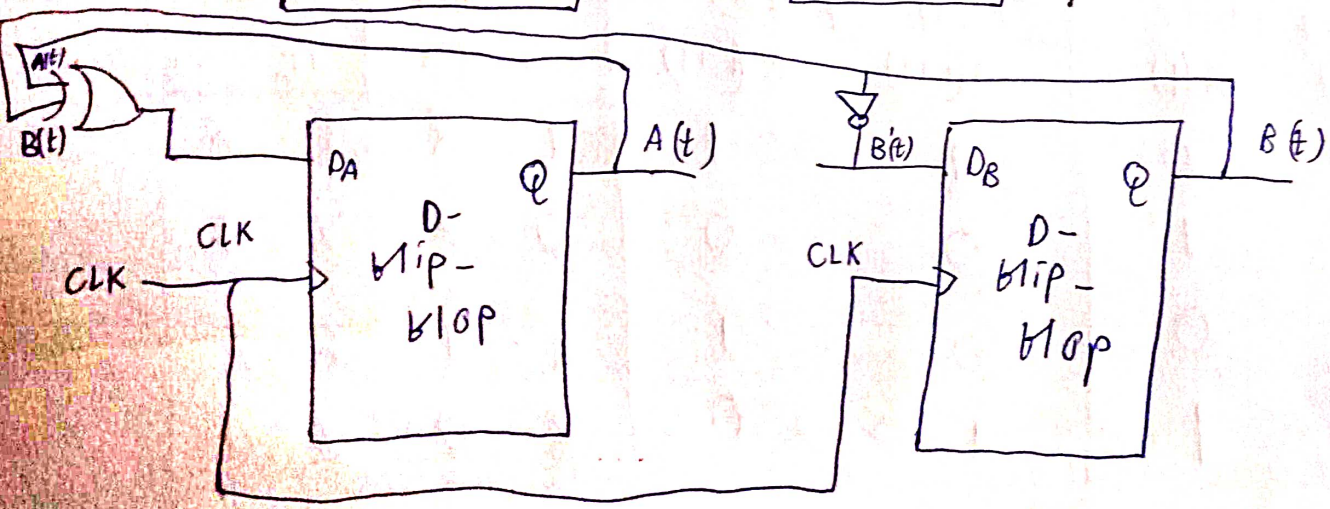
Present state		Next state		flip flop	
A(t)	B(t)	A(t+1)	B(t+1)	D_A	D_B
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

$D_A = AB' + A'B$

$D_A = A \oplus B$

$D_B = A'B' + AB'$

$D_B = B'$



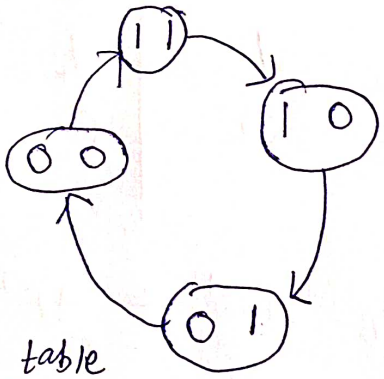
b) HDL code

```
Module 2-bit_up (QA, QB, CLK, DA, DB)
    input DA, DB, CLK,
    output QA, QB
    reg QA, QB
    always @ (posedge CLK)

assign DA = QA ^ QB
assign DB = ~QB
end module
```

OBJECTIVE-II

a) 2-bit down counter using JK flip-flop

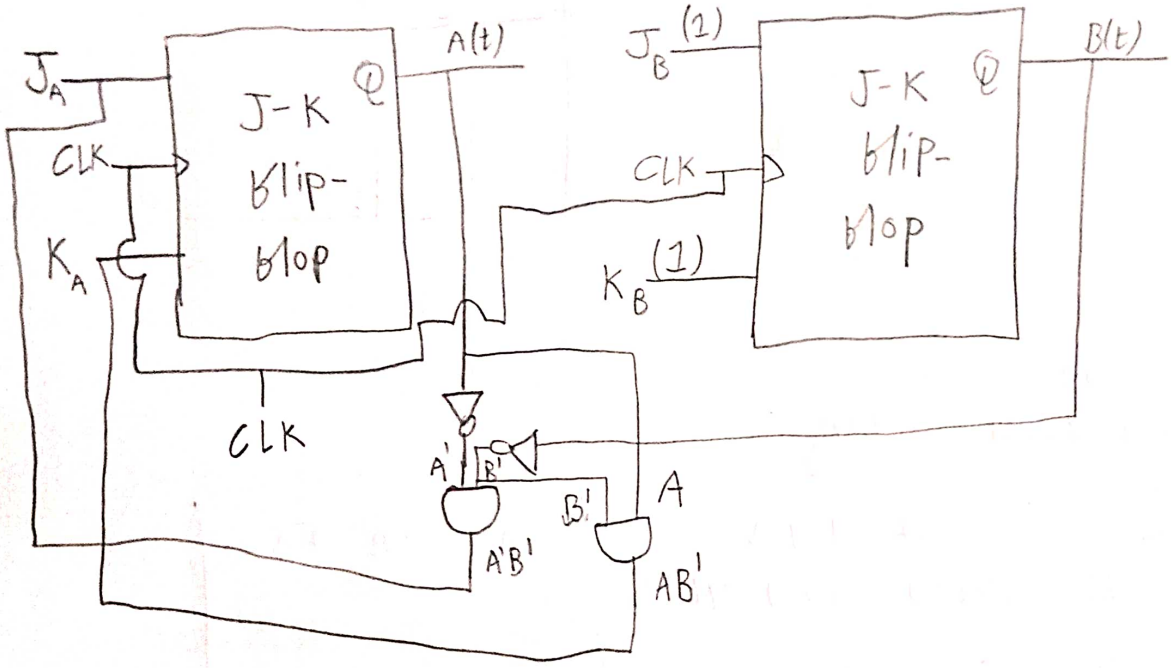


Excitation table

present state		Next state		flip-flop			
A(t)	B(t)	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	1	1	1	X	1	X
0	1	0	0	0	X	X	1
1	0	0	1	X	1	1	X
1	1	1	0	X	0	X	1

~~K-Map for J_A~~

$J_A = A'B'$ $K_A = AB'$ $J_B = 1$ $K_B = 1$

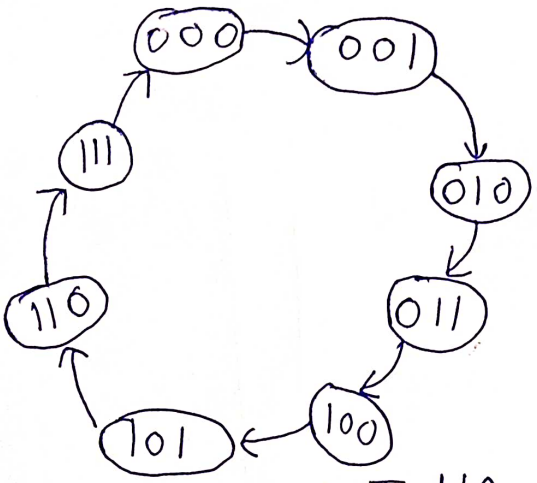


b) HDL code

```
module 2_bit_down (QA, QB, CLK, JA, KA, JB, KB)
    Output QA, QB
    Input CLK, JA, KA, JB, KB
    reg QA, QB
    always @ (Posedge CLK)
    assign JB = 1
    assign KB = 1
    assign JA = (~QA) & (~QB)
    assign KA = QA & (~QB)
endmodule
```

OBJECTIVE - III

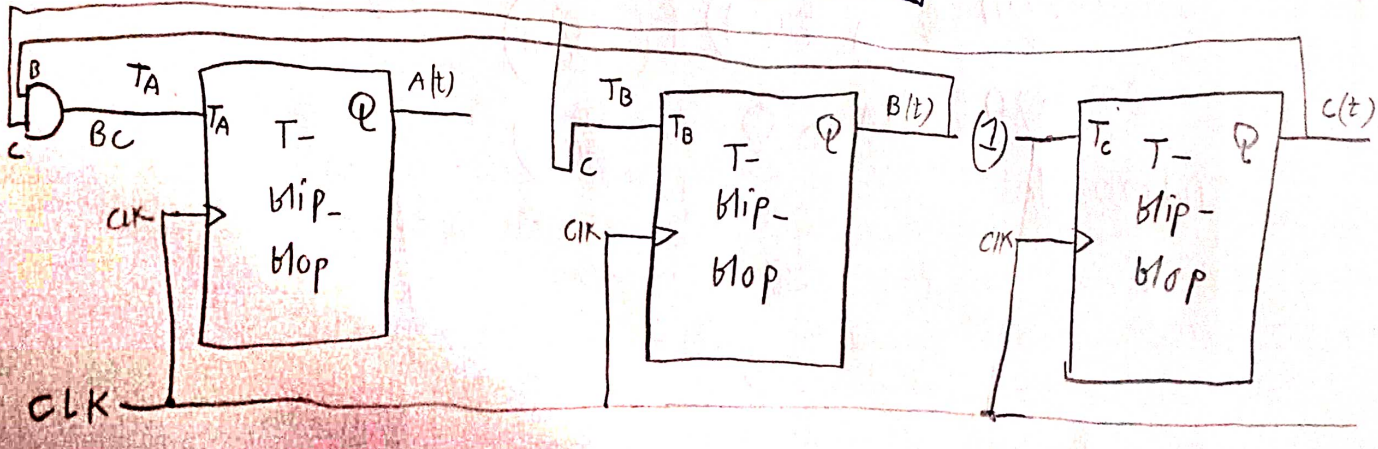
a) 3-bit up counter using T-flip-flop



Exitation Table

Present State A(t)	B(t)	C(t)	Next State A(t+1)	B(t+1)	C(t+1)	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

$T_A = BC$ $\quad$ $T_B = C$ $\quad$ $T_C = 1$



b) HDL code:-

```
module 3-bit-up(QA,QB,QC, TA, TB, TC, CLK)
    input TA, TB, TC
    output QA, QB, QC
    wire DTA, DTB, TTC
    always @ (posedge CLK)
    assign DTA = QB & QC;
    assign DTB = QC;
    assign DTC = 1;
endmodule
```

III. LAB:

S.NO	Name of component	Specification	Quantity
1	D-flip-flop	7474	1
2	XOR	7486	1
3	Inverter	7404	1
4	J-K-flip-flop	7476	1
5	AND	7408	1
6	T-flip-flop	7476	2

Conclusion

1) The ~~output of the~~ 3-bit up counter ~~can be used~~ is a digital circuit that counts up from 0 to 3 and then resets back to 0.

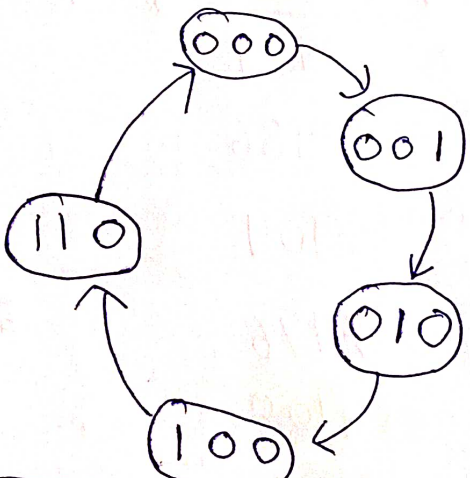
2) A 2-bit synchronous down counter using JK-flip-flop is a digital circuit that counts down from 3 to 0 and then resets back to 3.

3) A 3-bit synchronous up counter using T-flip-flops is a digital circuit that counts up from 0 to 7 and then resets back to 0.

IV. POST LAB:

1) 3 flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following count 1001100111.

2) $0 \rightarrow 1 \rightarrow 2 \rightarrow 4 \rightarrow 6$

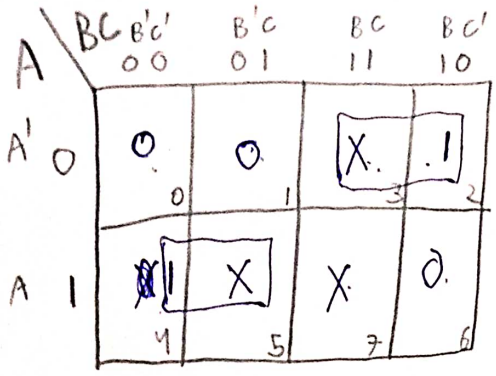


0 - 0 0 0
1 - 0 0 1
2 - 0 1 0
3 - 0 1 1
4 - 1 0 0
5 - 1 0 1
6 - 1 1 0
7 - 1 1 1

Present state			Next state			flip flop		
A(t)	B(t)	C(t)	A(t+1)	B(t+1)	C(t+1)	D_A	D_B	D_C
0	0	0	0	0	1	0	0	0
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

$D_A = A'BC'$ D_B

K-map for D_A



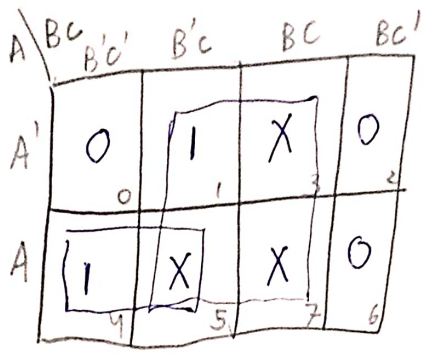
$I = \begin{cases} A'BC \\ A'BC' \end{cases} = A'B$

$II = \begin{cases} AB'C' \\ AB'C \end{cases} = AB'$

$D_A = A'B + AB'$

$D_A = A \oplus B$

K-map for D_B



$I = \begin{cases} A'B'C \\ A'BC \\ AB'C \\ ABC \end{cases} = C$

$II = \begin{cases} AB'C' \\ AB'C \end{cases} = AB'$

$D_B = C + AB'$

K-map for D_C

$D_C = 0$