DIGITAL LOGIC DESIGN LAB (EET1211)

LAB IV: Construct and Test various Binary Adder and Subtractor circuits

Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar

Branch:			**Section:**
S. No.	**Name**	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE:

1. Design, construct and test a Full Adder circuit using two ICs, 7486(XOR) and 7400(NAND).

2. Design, construct, and test a Half Subtractor circuit using two ICs, 7486(XOR) and 7400(NAND).

3. Design, construct, and test a 2 bit Parallel Adder circuit.

II. PRE-LAB

For Obj. 1:

a) Write the truth table for full-adder.
b) Derive the Boolean expression for sum and carry using XOR and NAND operation respectively.
c) Draw the logic diagram for sum and carry as output of the full-adder circuit.
d) Write HDL code.

For Obj. 2:

a) Write the truth table for Half Subtractor logic.
b) Derive the Boolean expression for difference and borrow using XOR and NAND operation respectively.
c) Draw the logic diagram for difference and borrow as output of the half-subtractor circuit.
d) Write HDL code.

For Obj. 3:

a) Write the truth table for 2-bit parallel adder.
b) Derive the Boolean expression for sum bit and carry bit using XOR and NAND operation respectively.
c) Draw the logic diagram based on Boolean expression.
d) Write HDL code.

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

HDL Program:

Observation:

Conclusion:

IV. POST LAB:

1. A Half-adder is characterized by

   a. Two inputs and two outputs
   b. Three inputs and two outputs
   c. Two inputs and three outputs
   d. Two inputs and one outputs

2. A 4-bit parallel adder can add

   a. Two 4-bit binary numbers
   b. Two 2-bit binary number
   c. Four bits at a time
   d. Four bits at a time

3. Two four bit numbers can be added using two full adders. Yes or No? Justify answer.