DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VII: CONSTRUCT, TEST AND INVESTIGATE THE OPERATION OF VARIOUS FLIP-FLOP CIRCUITS

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Branch:		**Section:**	
S. No.	**Name**	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE

1. Design and test of SR latch using universal logic gates.

2. Design and test of SR flip-flop using universal logic gates.

3. Design and test of JK flip-flop using universal logic gates.

4. Investigation of the logic behavior of various flip flop ICs:
   7474 D flip-flop IC
   7476 JK flip-flop IC

5. Realize the function of T flip flop using the JK flip-flop IC.

II. PRE-LAB

For Obj. 1:

a. Obtain the characteristic table for the SR latch.
b. Draw the logic diagram for SR latch using NAND gates.
c. Write HDL code for SR latch.

For Obj. 2:

a. Obtain the characteristic table for the SR flip flop.
b. Draw the logic diagram for SR flip flop using two cross coupled NAND gates.
c. Write HDL code for SR flip flop.

For Obj. 3:

a. Obtain the characteristic table for the JK flip flop.
b. Draw the logic diagram for JK flip flop using two cross coupled NAND gates.
c. Write HDL code for JK flip flop.

For Obj. 4:

a. Write the characteristic table for D flip-flop.
b. Write the characteristic table of JK flip-flop.
c. Write the characteristic table of T flip-flop.

For Obj. 5:

a. Draw the logic diagram for T Flip flop using JK flip-flop.
b. Write HDL code for T flip flop.

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

HDL Program:

Observation:

Conclusion:

IV. POST LAB

1. Differentiate between a latch and a flip-flop.

2. If both inputs of a SR NOR Latch are low, what will happen to the output?
   a) The output will reset.
   b) The output will toggle.
   c) The output will become unpredictable.
   d) The output will not be changed

3. If both inputs of a SR NAND Latch are low, what will happen to the output?
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4. Which of the following describes the operation of a positive edge-triggered D-type flip-flop?
   a) If both inputs are high, the output will toggle.
   b) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.
   c) When both inputs are LOW, an invalid state exists.
   d) The output will follow the input on the leading edge of the clock.