DIGITAL LOGIC DESIGN LAB (EET1211)

LAB IX: CONSTRUCT, TEST AND INVESTIGATE THE OPERATION OF VARIOUS COUNTER CIRCUITS

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Branch:		**Section:**	
S. No.	**Name**	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE

1. Design and Test of 2-bit synchronous up counter with D Flip-Flops

2. Design and Test of 2-bit synchronous down counter with JK Flip-Flops

3. Design and Test of 3-bit synchronous up counter with T Flip-Flops

II. PRE-LAB

For Obj. 1:

a. Draw the logic diagram for 2-bit synchronous up counter with D Flip-Flops

b. Write HDL code for 2-bit synchronous up counter

For Obj. 2:

a. Draw the logic diagram for 2-bit synchronous down counter with JK Flip-Flops

b. Write HDL code for 2-bit synchronous down counter

For Obj. 3:

a. Draw the logic diagram for 3-bit synchronous up counter with T Flip-Flops

b. Write HDL code for 3-bit synchronous up counter

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

HDL Program:

Observation:

Conclusion:

IV. POST LAB

1. How many Flip-Flops will be complemented in a 10-bit binary ripple counter to reach the next count after the following count?
   1001100111

2. Using D Flip-Flops design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6.