DIGITAL LOGIC DESIGN LAB (EET1211)

LAB VI: DESIGN OF MAGNITUDE COMPARATOR, DECODER, ENCODER AND MULTIPLEXER CIRCUIT

Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar

Branch:			**Section:**
S. No.	**Name**	**Registration No.**	**Signature**

Marks: _____/10

Remarks:

Teacher's Signature

I. OBJECTIVE:

1. Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

2. Design a 2 X 1 Multiplexer that will select the binary information from one of the two input lines and direct it to a single output line based on the value of a selection line.

3. Design a 4 bit priority encoder with inputs D_3 (MSB), D_2, D_1 and D_0 (LSB) and outputs X, Y and V. The priority assigned to inputs is $D_3 > D_2 > D_1 > D_0$.The output V shows a value 1 when one or more inputs are equal to one. If all inputs are 0, V is equal to 0. When V=0, then other two outputs are not inspected and are specified as don't care conditions.

4. Design a full adder using 3 to 8 line decoder and external OR gates.

II. PRE-LAB

For Obj. 1:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for the output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 2:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for the output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 3:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 4:

a. Write the truth table for the circuit.
b. Derive the Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

HDL Program:

Observation:

Conclusion:

IV. POST LAB:

1. Logically derive the Boolean expressions for the output variables of a 4 bit magnitude comparator.
2. Why is a multiplexer known as data selector?
3. Implement a Full Adder using two 4 X 1 multiplexers.