Project Summary | Schematic | obj1.v * | obj1_tb.v

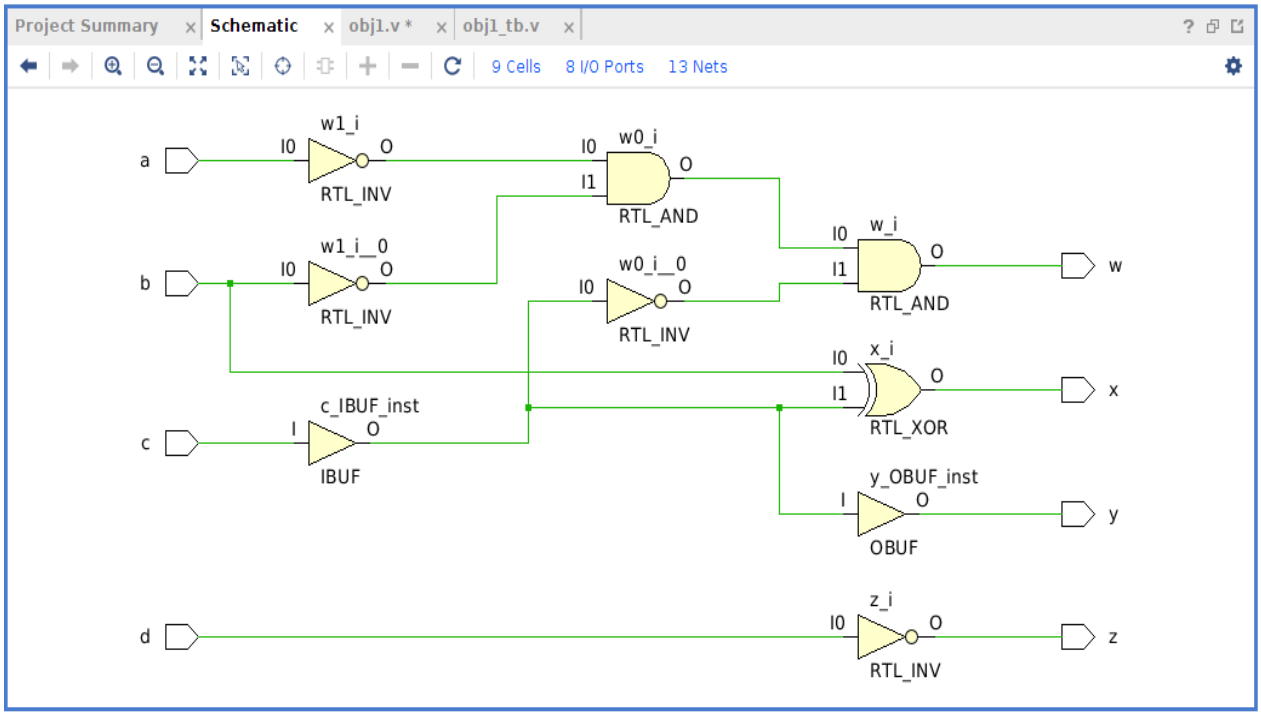
/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sources_1/new/obj.v

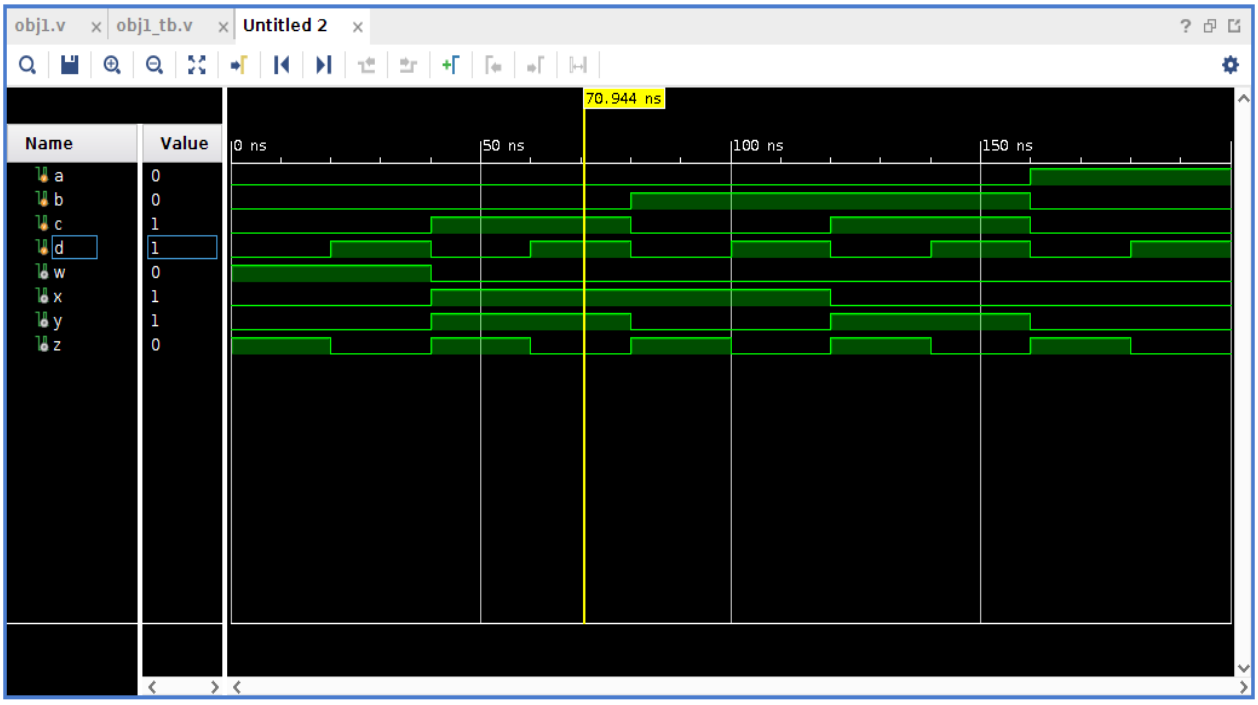
```
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  //Sec: CSE-M
24  //Name: Laxmidhar Sahu
25  //Regd No: 2141019147
26  module obj1(
27      input a,
28      input b,
29      input c,
30      input d,
31      output w,
32      output x,
33      output y,
34      output z
35      );
36
37      assign w=(!a)&&(!b)&&(!c);
38      assign x=b^c;
39      assign y=c;
40      assign z=!d;
41  endmodule
42
```

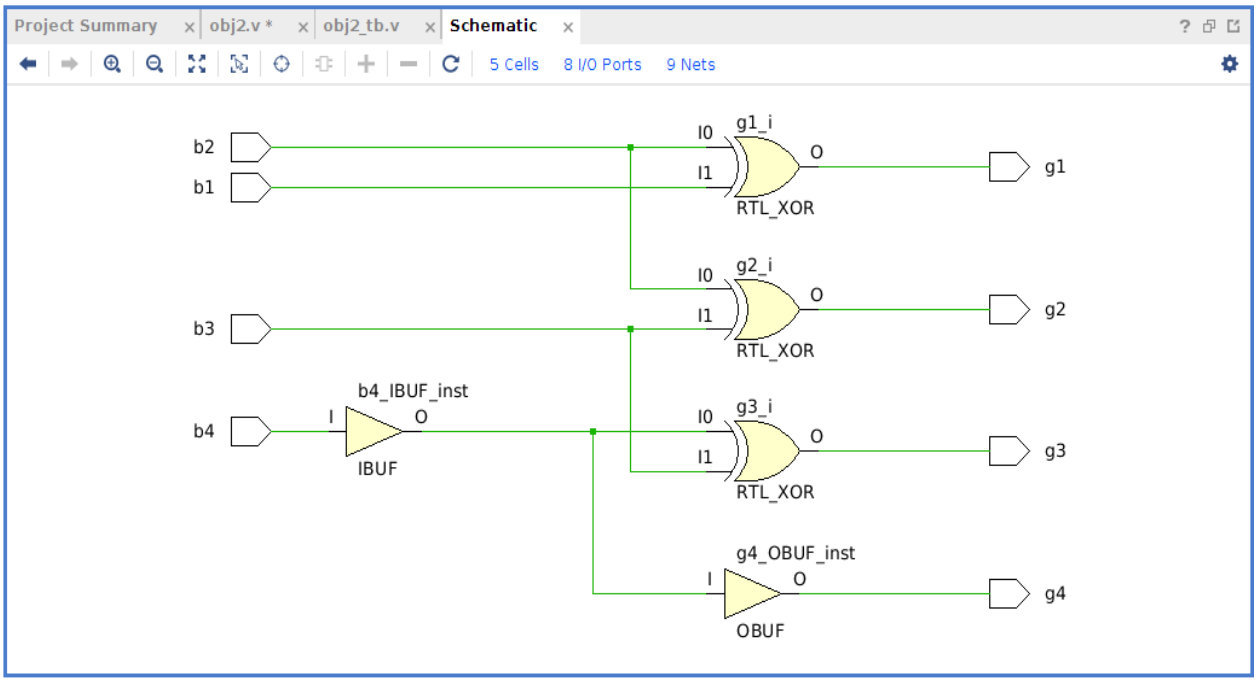
Project Summary | Schematic | obj1.v * | obj1_tb.v

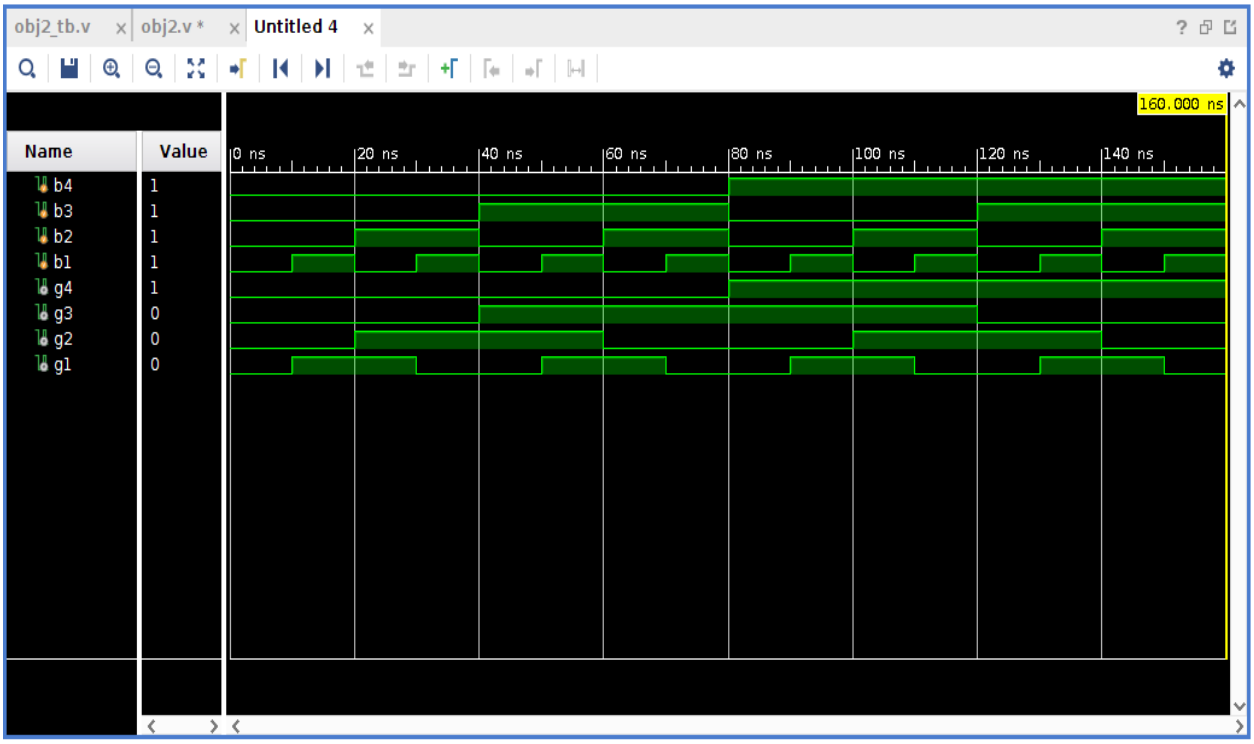
/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sim_1/new/obj1_tb.v

```
22
23  module obj1_tb();
24  reg a,b,c,d;
25  wire w,x,y,z;
26  obj1 dut(a,b,c,d,w,x,y,z);
27  initial begin
28
29
30  a=0;b=0;c=0;d=0;
31  #20
32  a=0;b=0;c=0;d=1;
33  #20
34  a=0;b=0;c=1;d=0;
35  #20
36  a=0;b=0;c=1;d=1;
37  #20
38  a=0;b=1;c=0;d=0;
39  #20
40  a=0;b=1;c=0;d=1;
41  #20
42  a=0;b=1;c=1;d=0;
43  #20
44  a=0;b=1;c=1;d=1;
45  #20
```


Project Summary
Schematic
obj1.v *
obj1_tb.v
9 Cells
8 I/O Ports
13 Nets
a
b
c
d
w1_i
RTL_INV
w1_i__0
RTL_INV
c_IBUF_inst
IBUF
w0_i
RTL_AND
w0_i__0
RTL_INV
w_i
RTL_AND
x_i
RTL_XOR
y_OBUF_inst
OBUF
z_i
RTL_INV
w
x
y
z


obj1.v
obj1_tb.v
Untitled 2
Name
Value
a 0
b 0
c 1
d 1
w 0
x 1
y 1
z 0
70.944 ns
0 ns
50 ns
100 ns
150 ns


Project Summary
obj2.v *
obj2_tb.v
Schematic
5 Cells
8 I/O Ports
9 Nets
b2
b1
b3
b4
I0
I1
g1_i
O
RTL_XOR
g1
g2_i
g2
g3_i
g3
b4_IBUF_inst
I
IBUF
g4_OBUF_inst
OBUF
g4


obj2_tb.v
obj2.v *
Untitled 4
160.000 ns
Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
b4 1
b3 1
b2 1
b1 1
g4 1
g3 0
g2 0
g1 0

obj2_tb.v | obj2.v * | Untitled 4

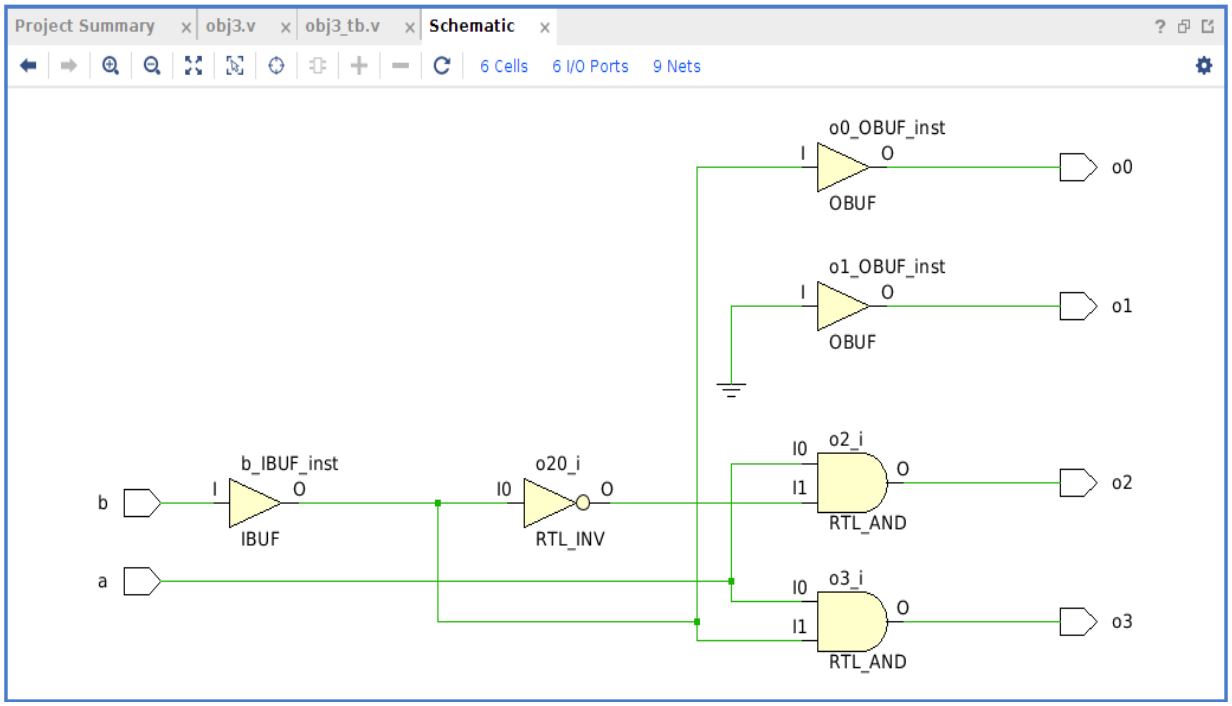
/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sources_1/new/obj2.v

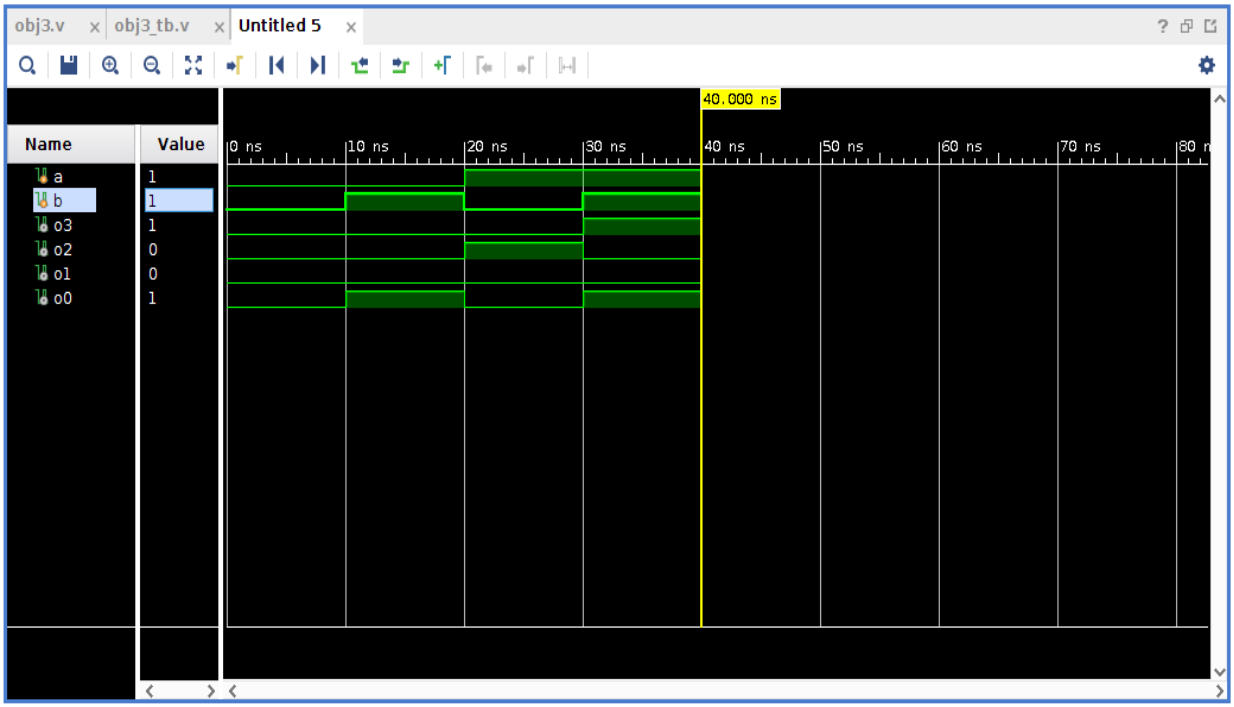
```
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25  module obj2(
26      input b4,
27      input b3,
28      input b2,
29      input b1,
30      output g4,
31      output g3,
32      output g2,
33      output g1
34      );
35
36      assign g4 = b4;
37      assign g3 = b4^b3;
38      assign g2 = b2^b3;
39      assign g1 = b2^b1;
40  endmodule
41
```

obj2_tb.v | obj2.v * | Untitled 4

/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sim_1/new/obj2_tb.v

```
22
23  module obj2_tb();
24  reg b4,b3,b2,b1;
25  wire g4,g3,g2,g1;
26  obj2 dut(b4,b3,b2,b1,g4,g3,g2,g1);
27  initial begin
28
29
30  b4=0;b3=0;b2=0;b1=0;
31  #10
32  b4=0;b3=0;b2=0;b1=1;
33  #10
34  b4=0;b3=0;b2=1;b1=0;
35  #10
36  b4=0;b3=0;b2=1;b1=1;
37  #10
38  b4=0;b3=1;b2=0;b1=0;
39  #10
40  b4=0;b3=1;b2=0;b1=1;
41  #10
42  b4=0;b3=1;b2=1;b1=0;
43  #10
44  b4=0;b3=1;b2=1;b1=1;
45  #10
```


Project Summary
obj3.v
obj3_tb.v
Schematic
6 Cells
6 I/O Ports
9 Nets
o0_OBUF_inst
I
O
OBUF
o0
o1_OBUF_inst
I
O
OBUF
o1
b
b_IBUF_inst
I
O
IBUF
o20_i
I0
O
RTL_INV
o2_i
I0
I1
O
RTL_AND
o2
a
o3_i
I0
I1
O
RTL_AND
o3


obj3.v
obj3_tb.v
Untitled 5
40.000 ns
Name
Value
a
1
b
1
o3
1
o2
0
o1
0
o0
1
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns

obj3.v | obj3_tb.v | Untitled 5

/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sources_1/new/obj3.v

```
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25  module obj3(
26      input a,
27      input b,
28      output o3,
29      output o2,
30      output o1,
31      output o0
32      );
33
34      assign o3 = a && b;
35      assign o2 = a && (!b);
36      assign o1 = 0;
37      assign o0 = b;
38  endmodule
39
```

obj3.v | obj3_tb.v | Untitled 5

/home/student/Laxmidhar_2141019147/Lab5/Lab5.srcs/sim_1/new/obj3_tb.v

```
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module obj3_tb();
24  reg a,b;
25  wire o3,o2,o1,o0;
26  obj3 dut(a,b,o3,o2,o1,o0);
27  initial begin
28
29  a=0;b=0;
30  #10
31  a=0;b=1;
32  #10
33  a=1;b=0;
34  #10
35  a=1;b=1;
36  #10
37
38  $stop;
39  end
40  endmodule
41
42
```