COUNTERS :→

⇒ A counter by function, is a sequential ckt consisting a set of flip-flops connected in a suitable manner to count the ~~no of states~~ sequence of the input pulses presented to in digital form.

⇒ counter can be broadly classified under 3-heads as follows.

1. Asynchronous and Synchronous counter.
2. Single and multimode counter.
3. Modulus counter.

Asynchronous (up / down) **Synchronous** (up / down) **Singlemode**

⇒ O/p of each flipflop is not synchronised with CLK. The O/p of one FF is used as a CLK to the next FF. So delay is more.

⇒ It is also known as ripple or serial counter

⇒ Each FF in the ckt are implemented with same CLK. i.e O/p of all the FFs are synchronized with CLK.

⇒ Propagation delay is less.

⇒ It is also known as parallel counter.

⇒ A counter maybe synchronous or asynchronous is used as singlemode operation i.e as an upcounter or downcounter

Multimode :

* A synchronous or asynchronous counter maybe used as multimode operation i.e UP/down counter.

Modulus Counter : are defined based on the member of states they are capable of counting

eg MOD-10, counter :- it counts 10 states

MOD-N : It has 'N' states i.e it counts from '0' to "N-1" numbers.

Note : always the MOD of the counter is defined by the no of FFs used to design the counter ckt.

If 'n' = no of flipflops.

then: $2^n \geq N$

Note : The counters are also named as n-Bit Counter, where 'n' is the no of FFs present in the counter ckt. and it will count from $(0 \text{ to } 2^n - 1)$ i.e 2^n no of states

~~Asynchronous~~

Asynchronous (Serial OR RIPPLE) COUNTER

⇒ Asynchronous counter is easy to design & requires less hardware. But here the propagation delay is more, because here each FF is triggered by the previous one.

⇒ For design of any counter always the state diagram is required.

State diagram:- represents the pulse sequence on states which are counted by the counter ckt.

* always the counting operation is started from state 0 and at last again it comes to state (0).

⇒ For the design of counter always JK and T flipflops are required. Because these two FF has toggle operations.

⇒ Timing diagram of counter is important.

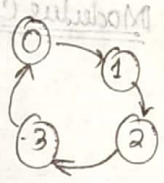
⇒ For asynchronous counter design, the J&K inputs or the T input is always connected to logic-1, so that each FF is operated in toggle mode. and the $\overline{Pr}$ and $\overline{Clr}$ of each FF is are connected to logic-1 for normal operation.

⇒ 2-Bit Asynchronous ~~Ripple counter~~ (UP counter)

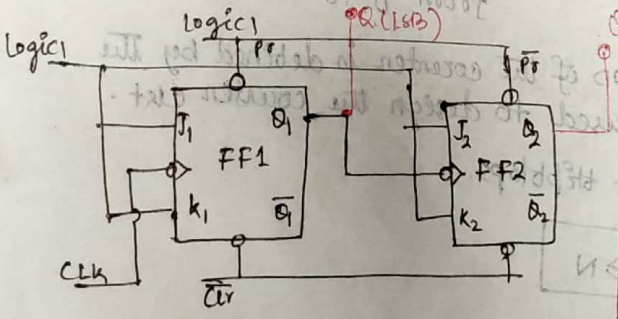
$n = 2$ (FFs)

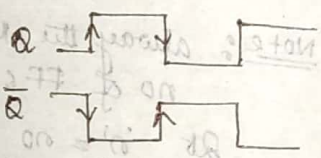
$N = 2^n = 4$ states

Count from 0 to $(N-1)$ i.e 0 to 3



Clk	$\overline{Pr}$	$\overline{Clr}$	Q_1
X	0	0	~~Q~~
X	0	1	1
↓	1	0	0
X	1	1	Next state





+ve edge of $\overline{Q}$ ≡ −ve edge of Q
−ve edge of Q ≡ +ve edge of $\overline{Q}$

NOTE FOR UP counting :→

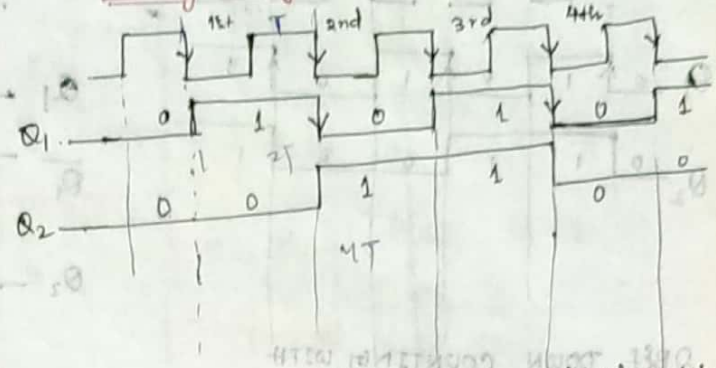
Q is used as −ve Edge Triggering of next FF

Or $\overline{Q}$ is " " +ve Edge Triggering of next FF

Truth table

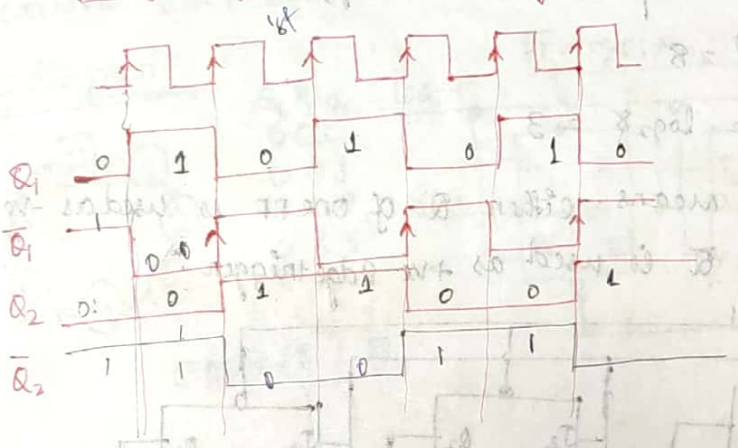
CLK	Q_2	Q_1	State
	0	0	0
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	0

Timing Diagram ($Q \rightarrow$ -ve edge triggered)



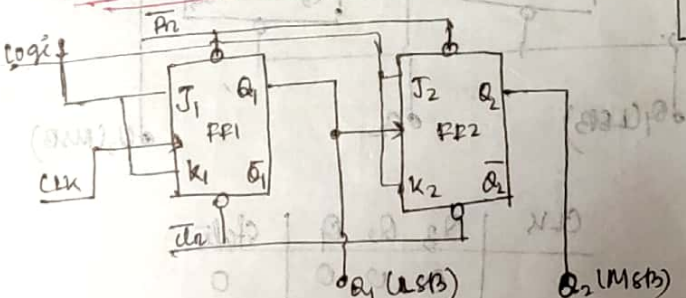
Note:
- 1st FF O/P gives O/P whose Freq is half of clk freq.
- 2nd FF O/P gives O/P whose Freq is 1/4 of CLK freq
- the nth FF O/P gives O/P whose freq is $\frac{1}{2^n}$ of CLK freq.

Timing Diagram ($\bar{Q} \Rightarrow$ +ve edge triggering.) up-counting



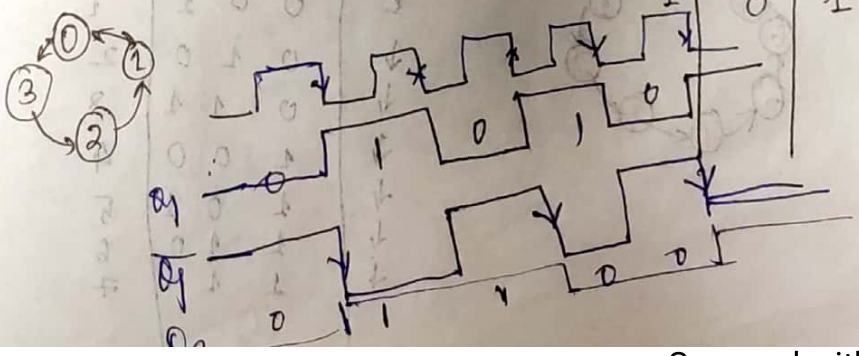
2-Bit Asynchronous Down Counter

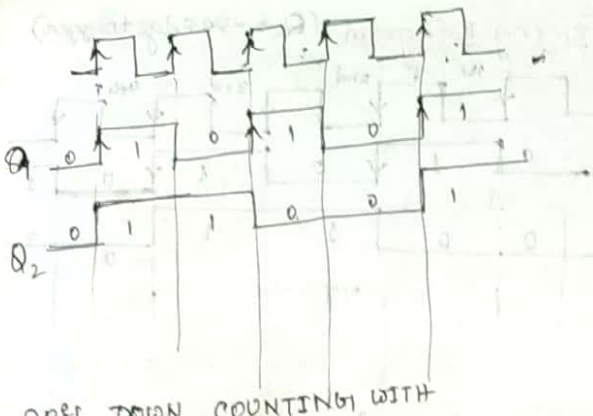
$Q \rightarrow$ is used as +ve edge.
$\bar{Q} \rightarrow$ is used as -ve edge.



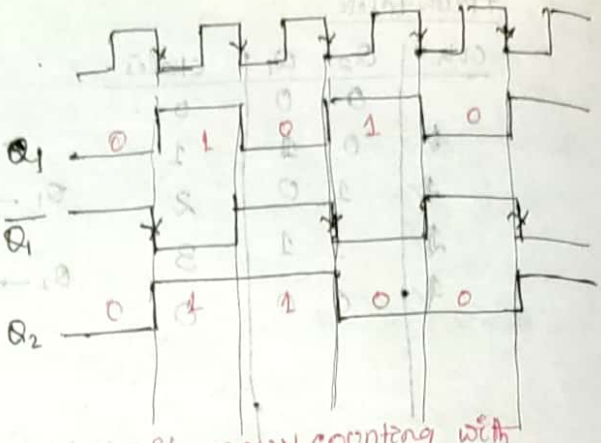
Truth table

State	Q_2	Q_1
0	0	0
3	1	1
2	1	0
1	0	1





2 BIT DOWN COUNTING WITH +ve edge



2 BIT DOWN COUNTING WITH -ve Edge

Q. Design an asynchronous Mod 8 UP counter. & Draw the timing diagram?

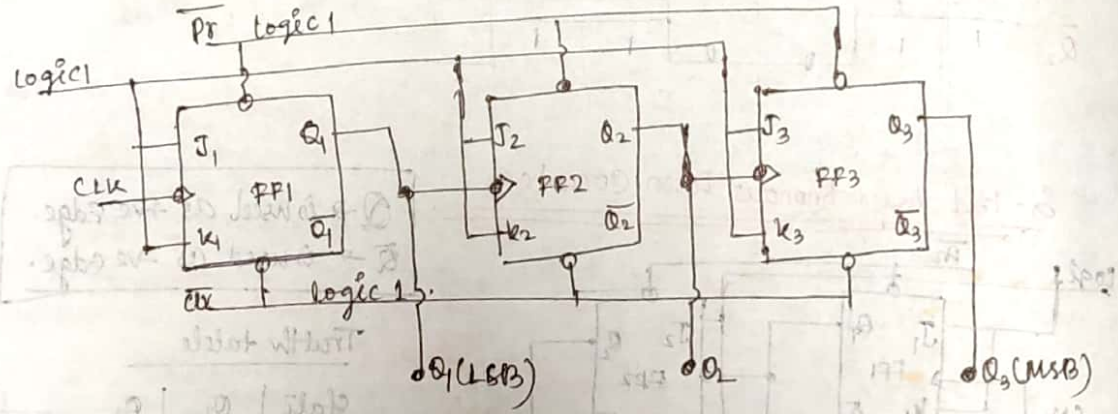
MOD-8 means it counts 8 states (N) → counts from 0 to N-1
i-e 0 to 7

⇒ no of FFs required is n (say)

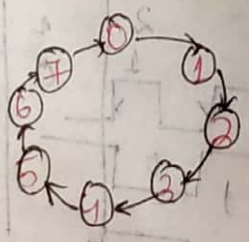
⇒ $2^n = 8$

⇒ $n = \log_2 8 = 3$

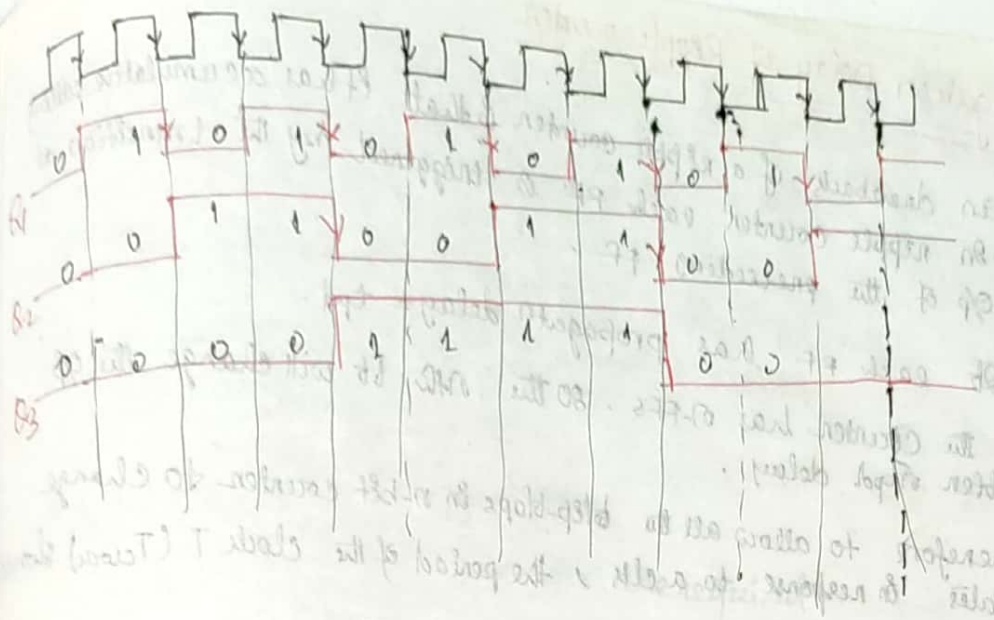
⇒ UP counter means either Q of one FF is used as -ve edge trigger to next or $\bar{Q}$ is used as +ve edge trigger.



State diagram :-



CLK	Q_3	Q_2	Q_1	State
	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	1	1	0	6
↓	1	1	1	7

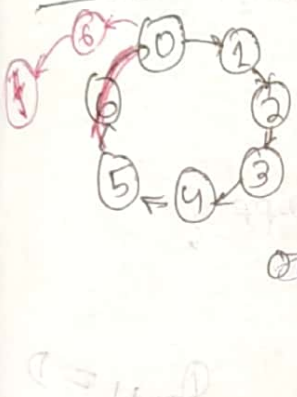


Q Design an asynchronous MOD-6 up counter?

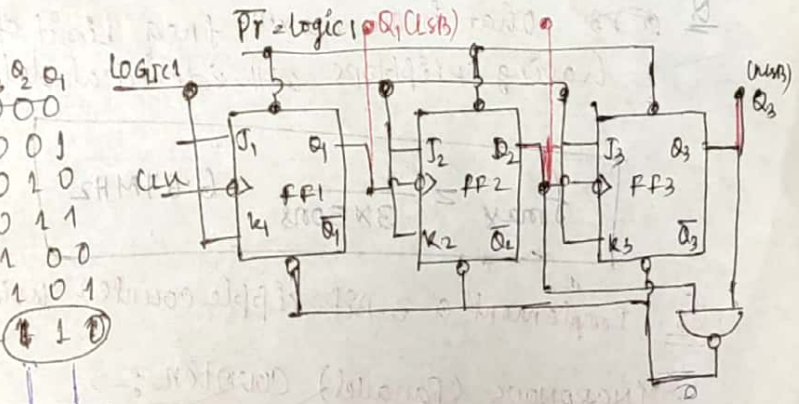
Mod-6 → 6 states → count from 0 to 5 → at least 3 FFs are required.
000 101.

But by using 3-Bit counter, we counts upto 111, so for MOD-6 counter 6,7 states are invalid.

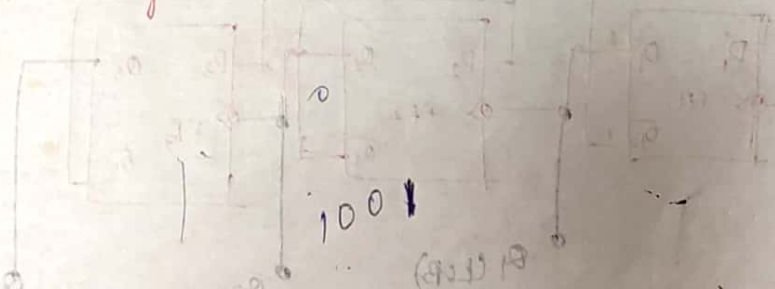
State diagram.

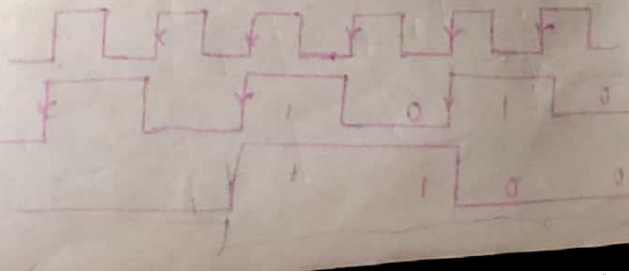


Q_3	Q_2	Q_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0



Q Design an asynchronous Decade counter?





Propagation Delay of Ripple counter

The main drawback of a ripple counter is that it has a cumulative settling time. In ripple counter each FF is triggered by the transition at the O/p of the preceeding FF.

⇒ If each FF has propagation delay = t_{pd}.

If the counter has n-FFs. So the nth FF will change the O/p after nt_{pd} delay.

⇒ Therefore to allow all the flip-flops in n-bit counter to change states in response to a clk, the period of the clock T (T_{clock}) should be

$$T_{clock} \geq n\,t_{pd}.$$

$$\frac{1}{f_{clock}} \geq nt_{pd}$$

$$\frac{1}{n \times t_{pd}} \geq f_{clock}.$$

Q What is the max? freq limit of a 3-bit counter having flipflops with identical delay 50ns.

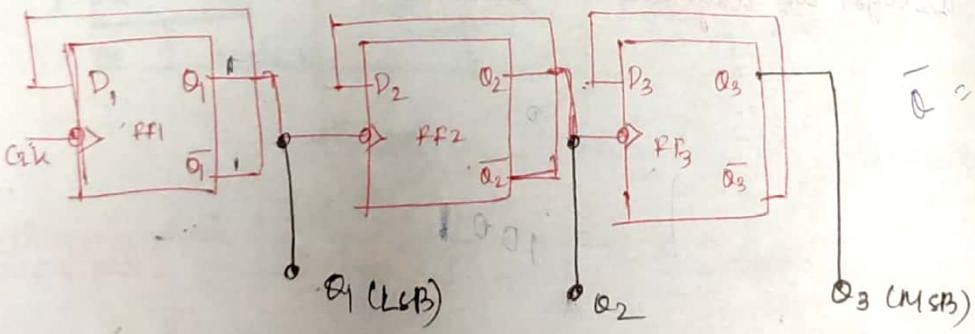
$$f_{max} \leq \frac{1}{3 \times 50ns} \approx 6.67MHz$$

Q Implement a 3-bit ripple counter using D-FF?

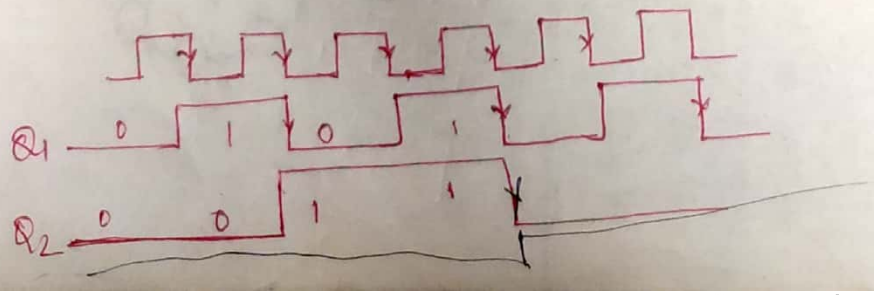
SYNCHRONOUS (Parallel) Counter :→

$Q_{n+1} = D$

$\bar{Q} = 1$



D-FF can be used as toggle mode. If $\bar{Q}_D$ is connected to D.



Q. A binary ripple counter is required to count upto 16383_{10}. How many FFs are required? If the clk freq is 8.192 MHz. What is the freq at the O/p of the MSB?

Ans Let the no. of FFs = n. So $2^n \geq N$.

N = no of states = 16383 + 1 = 16384

$\Rightarrow 2^n = 16384$

$\Rightarrow n = \log_2 16384$

$\Rightarrow \boxed{n = 14}$ → FFs are required.

$\Rightarrow$ Freq at the O/P of MSB $(f) = \frac{f_{clock}}{2^n} = \frac{8.192\,MHz}{2^{14}} = 500\,Hz$

Ans

Q. For what minm value of propagation delay in each FF will a 10 bit ripple counter skip a count when it is clocked at 10MHz.

Ans For a state change to ripple through all n-stages.

$T_c = n\,t_{pd}$

$f_c = \frac{1}{T_c} = \frac{1}{n\,t_{pd}}$

$\frac{1}{f_{ci}} > n\,t_{pd}$

$\Rightarrow \boxed{t_{pd} = \frac{1}{n f_c} = \frac{1}{10 \times 10\,MHz} = 10\,ns.}$

SYNCHRONOUS COUNTER

Design of Synchronous Counter:→

Step-1 Based on the description of the problem determine the required number 'n' of the FFs - the smallest value of 'n' is such that number of states $\boxed{N' \leq 2^n}$.

Step-2 Draw the state diagram showing all the possible states. A state diagram which can also be called as transition diagram, is a graphical means of describing the sequence of states through which the counter progresses. In each case the counter goes to a particular

state counter goes to a particular state from the invalid state on the next clock pulse, the same can also be included in the state diagram.

Step-3 Write the excitation table that lists the present state (PS), the next state (NS) and the required excitation.

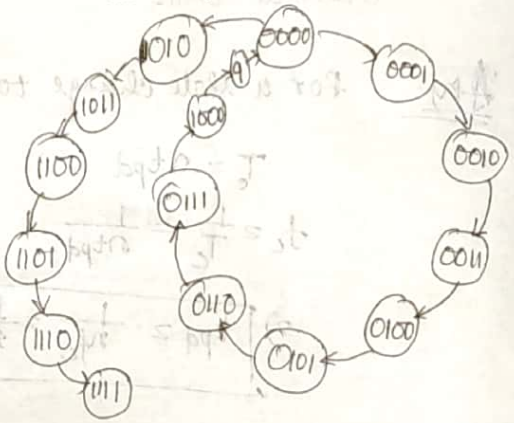
Step 4 Obtain the minimal expression for the excitations of the FFs using K-maps.

Step-5 Implement the minimal expressions to get the logic ckt.

Q Design a ① Synchronous Decade counter using T-Flipflop and also draw its timing diagram?

Ans N=10 (0 to 9)
n=4

State diagram

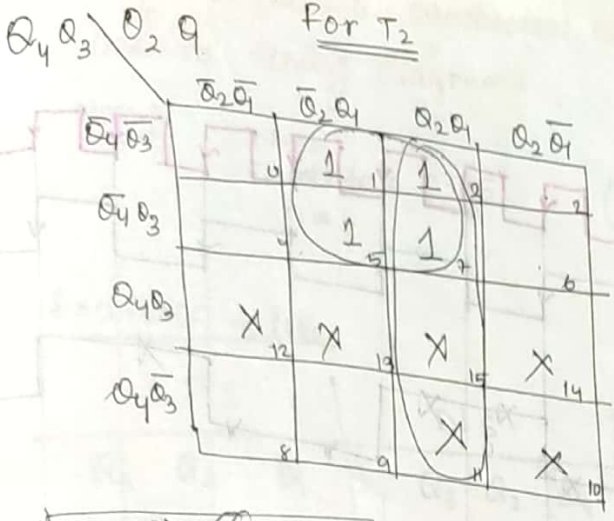


Excitation table

PS				NS							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	T_4	T_3	T_2	T_1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

$T_1 = 1$

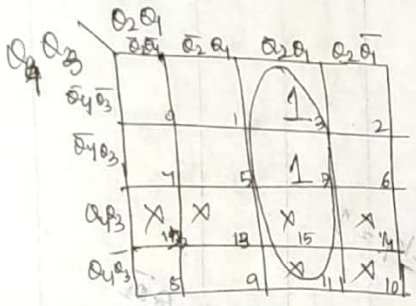
For T_2



$T_2 = Q_2\bar{Q}_1 + \bar{Q}_4Q_1$

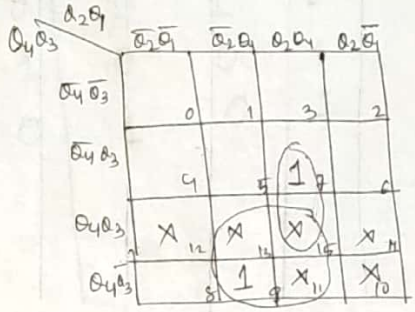
$T_2 = \bar{Q}_4Q_1$

For T_3

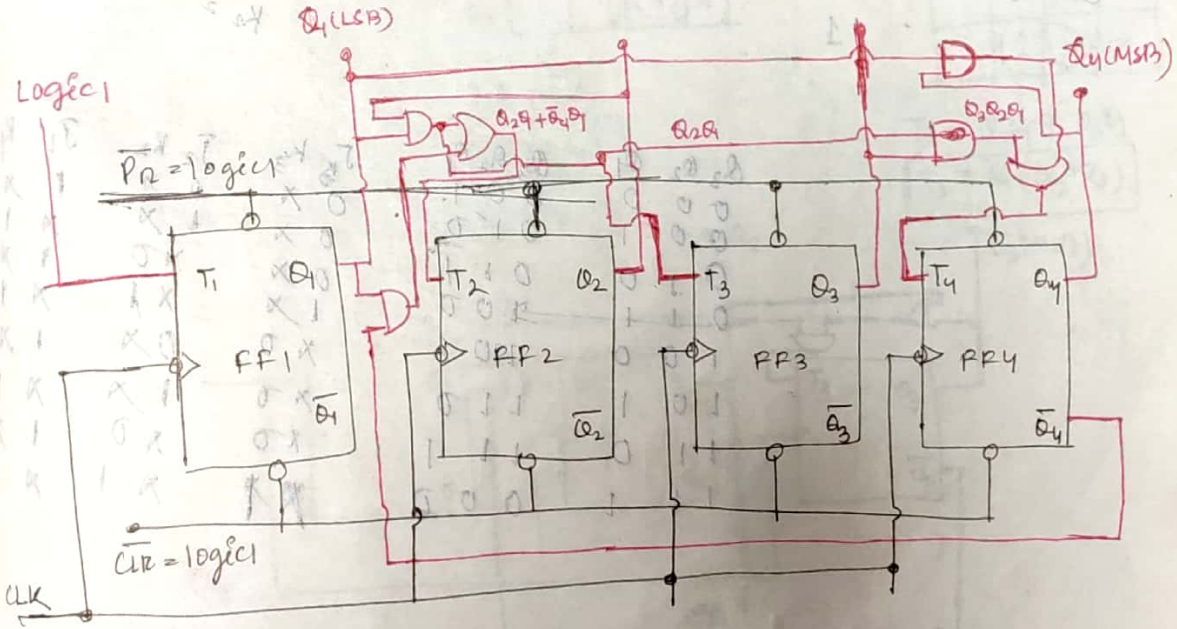


$T_3 = Q_2Q_1$

For T_4

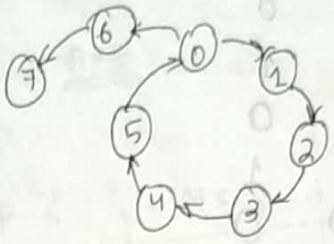


$T_4 = Q_4Q_1 + Q_3Q_2Q_1$



8 Design a MOD-6 synchronous counter using T-FF and Draw its timing diagram?

MOD-6 N = 6
counts from 0 to 5
n = 3

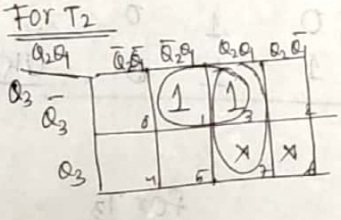


Excitation table

PS			NS			FF inputs		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	0	0						

$T_1 = 1$

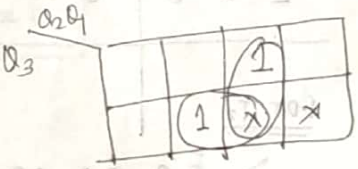
For T_2



$T_2 = Q_2Q_1 + \bar{Q}_3Q_1$

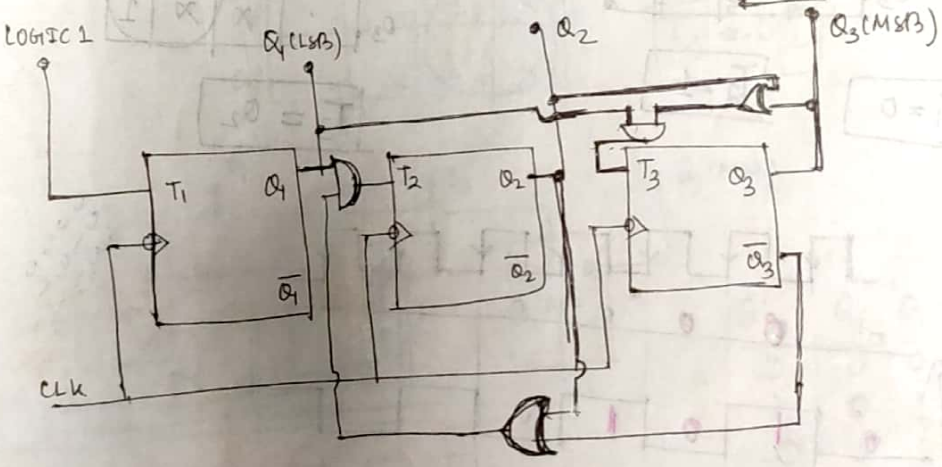
$T_2 = Q_1(Q_2 + \bar{Q}_3)$

For T_3



$T_3 = Q_2Q_1 + Q_3Q_1$

$T_3 = Q_1(Q_2 + Q_3)$

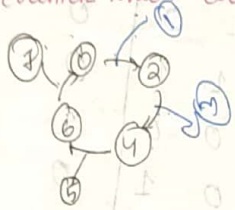


$T_3 = Q_1(Q_2 + Q_3)$ $T_2 = Q_1(Q_3 + \bar{Q}_2)$ 1

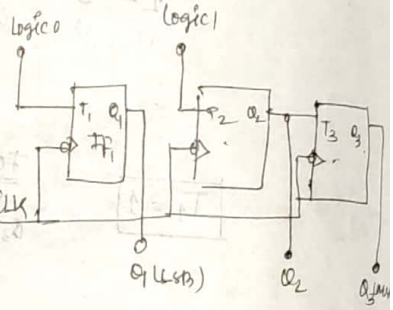
Q_3	Q_2	Q_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
0	0	0

8 Design a skip counter which counts the states 0, 2, 4, 6, 0 . . . .

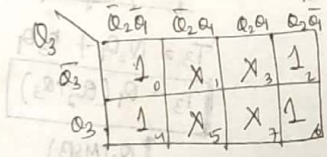
n = 3



PS			NS			FF Excitation		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	1	0	0	1	0
0	1	0	1	0	0	1	1	0
1	0	0	1	1	0	0	1	0
1	1	0	0	0	0	1	1	0



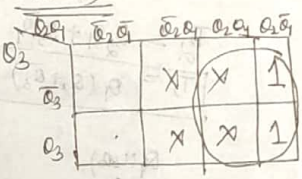
for T_2



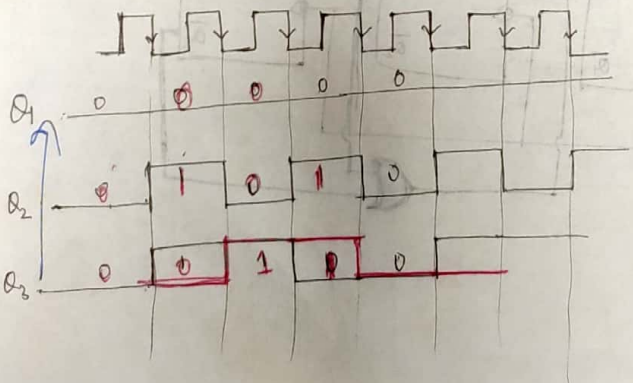
$T_1 = 0$

$T_2 = 1$

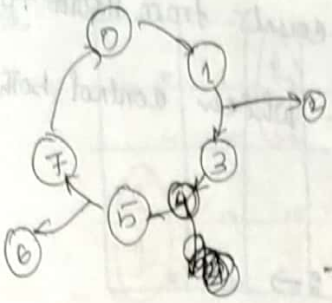
for T_3



$T_3 = Q_2$



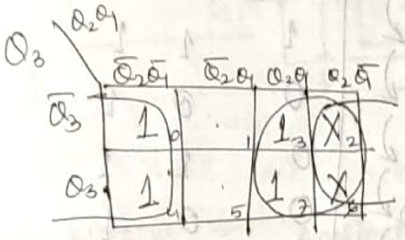
Q. Design an synchronous skip counter which counts 0, 1, 3, 4, 5, 7, 0.



n = 3

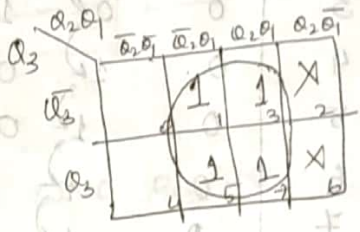
PS			NS			FF Inputs		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1	0
1	1	1	0	0	0	1	1	1

For T_1



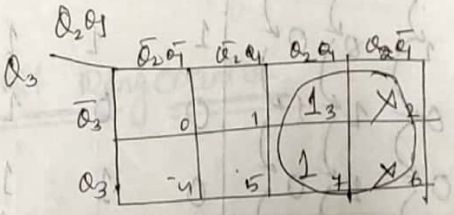
$T_1 = Q_2 + \bar{Q}_1$

For T_2

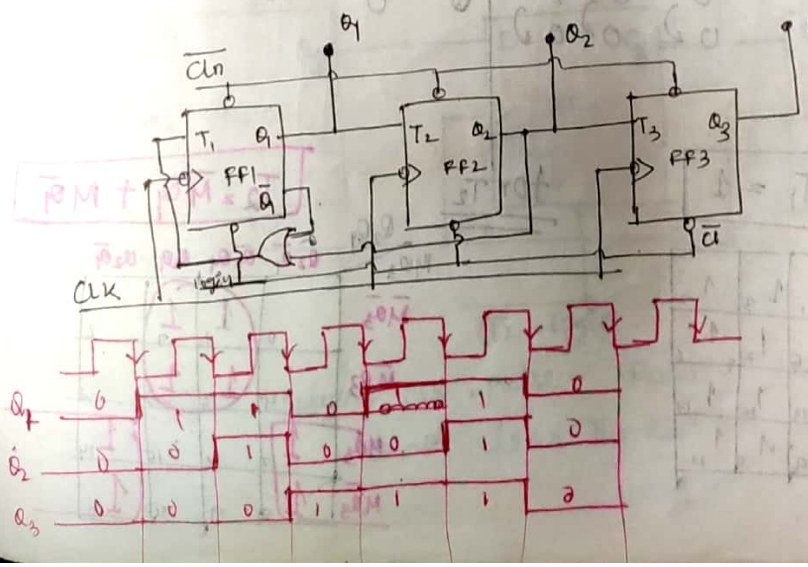


$T_2 = Q_1$

For T_3



$T_3 = Q_2$



Q_3	Q_2	Q_1
0	0	0
0	0	1
0	1	1
1	0	0
1	0	1
1	1	1
0	0	0

Q Design a synchronous 3-bit UP/DOWN counter

⇒ UP counter → up counter counts from LOW to HIGH 000 to 111,

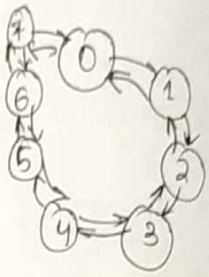
⇒ Down counter → down counter counts from HIGH to LOW 111 to 000

⇒ There must be a control bit which control both the up & down count operation separately.

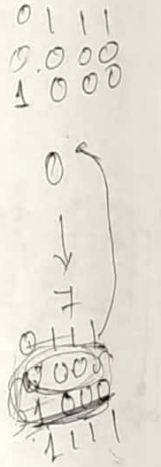
⇒ Let M is the control bit :→

M=0 → is used for UP operation.

M=1 → is used for down operation.

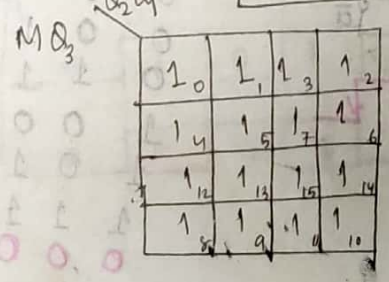


CLK	M	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	0	0	1
1	0	0	0	1	0	1	1
2	0	0	1	0	0	0	1
3	0	0	1	1	1	1	1
4	0	1	0	0	0	0	1
5	0	1	0	1	0	1	1
6	0	1	1	0	0	0	1
7	0	1	1	1	1	1	1
8	1	0	0	0	1	1	1
9	1	1	1	1	0	0	1
10	1	1	1	0	0	1	1
11	1	1	0	1	0	0	1
12	1	1	0	0	1	1	1
13	1	0	1	1	0	0	1
14	1	0	1	0	0	1	1
15	1	0	0	1	0	0	1
16	1	0	0	0			



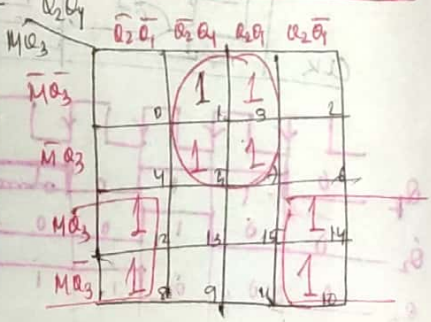
for T_1

$T_1 = 1$

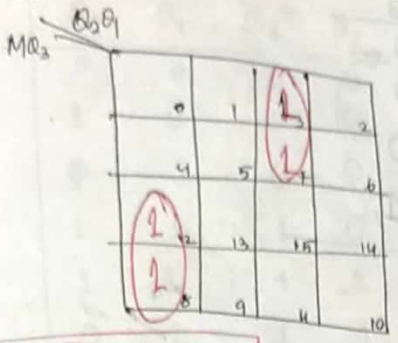


for T_2

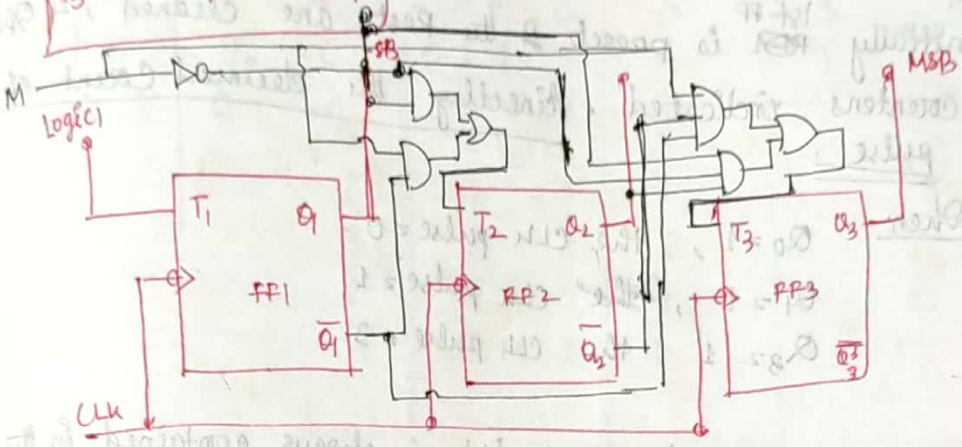
$T_2 = \bar{M}Q_1 + M\bar{Q}_1$



FOR T_3



$T_3 = M\bar{Q}_2\bar{Q}_1 + \bar{M}Q_2Q_1$



RING COUNTER: ⇒ Application of SISO Register.

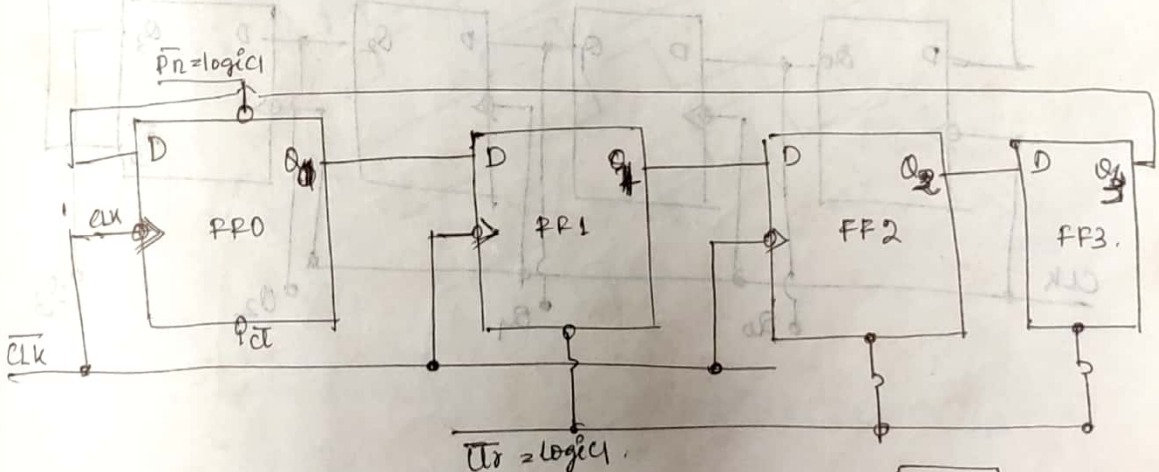
⇒ It is used as a Decoder ckt.

⇒ This a type of synchronous counter.

⇒ The ring counter utilizes, 1 FF for each state in its sequence and it is therefore wasteful of FFs.

⇒

4-Bit Ring counter



⇒ Before applying CLK, pulse Preset FF1 i.e $Q_1 = 1$ and clear the rest FFs i.e $Q_2 = Q_3 = Q_4 = 0$

⇒

CLK	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

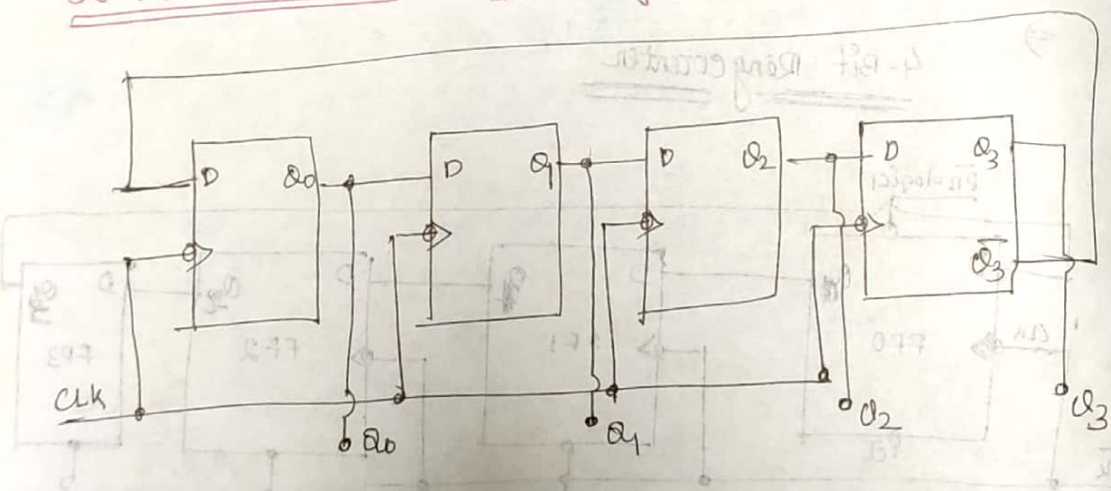
Initially 1st FF is preset & the Rest are cleared, 4 O/ps of the counters indicated directly the decimal count of the CLK pulse.

When $Q_0 = 1$, the CLK pulse = 0,
$Q_1 = 1$, the CLK pulse = 1
$Q_3 = 1$ the CLK pulse = 3.

Hence we concludes that '1' is always contained in the counter and simply shifted around the counter ckt with the application of a CLK, so it produces a Ring Structure.

⇒ Ring counter is a decimal counter, it is a divided by-N counter, where 'N' is the no of stages

Johnson Counter :→ Twisted Ring Counter:



CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

2+ has 8 states