obj1.v | obj1_tb.v | Untitled 7

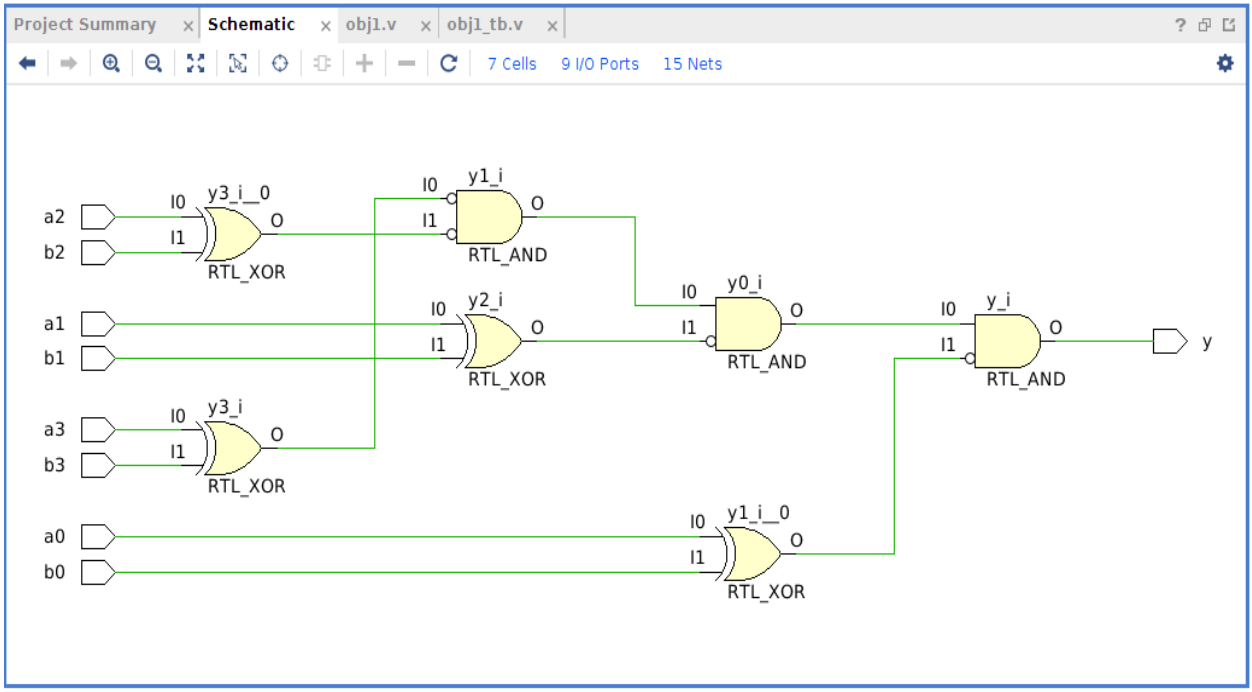
/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sources_1/new/obj1.v

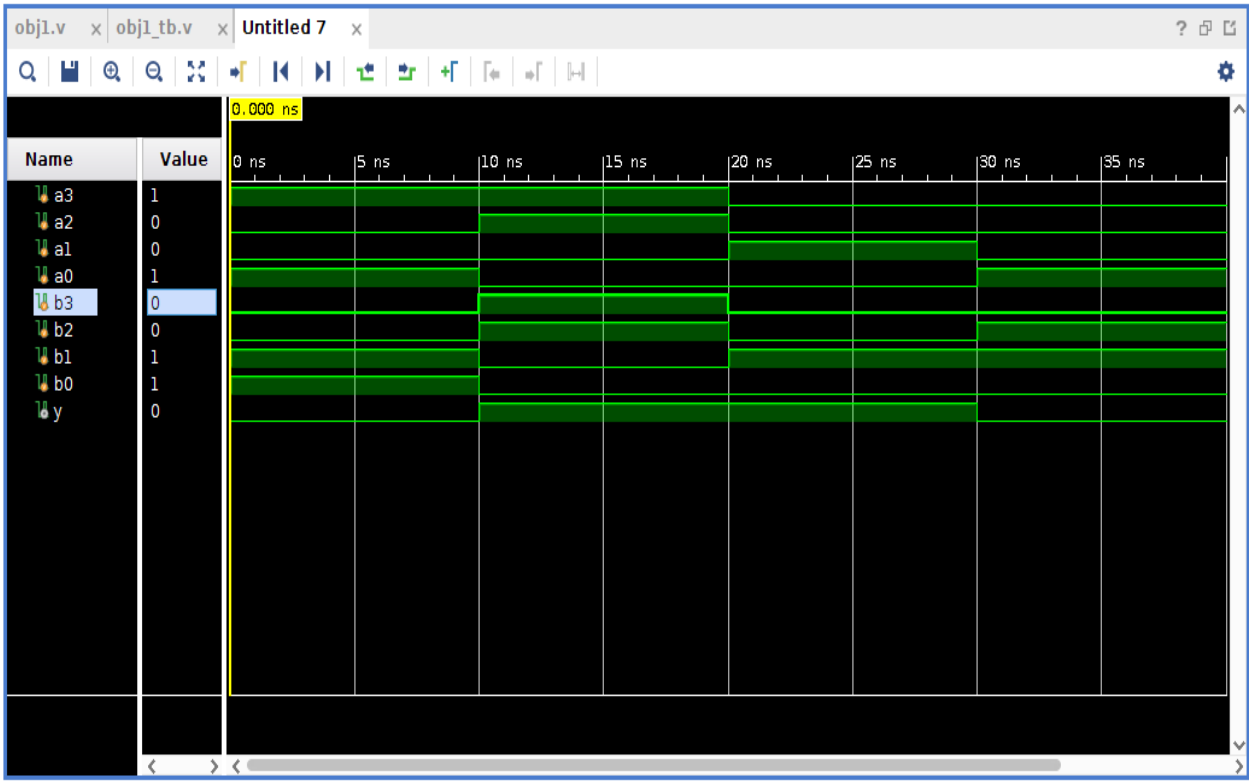
```
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25  module obj1(
26      input a3,
27      input a2,
28      input a1,
29      input a0,
30      input b3,
31      input b2,
32      input b1,
33      input b0,
34      output y
35
36      );
37
38      assign y =(~(a3^b3))&(~(a2^b2))&(~(a1^b1))&(~(a0^b0));
39  endmodule
40
```

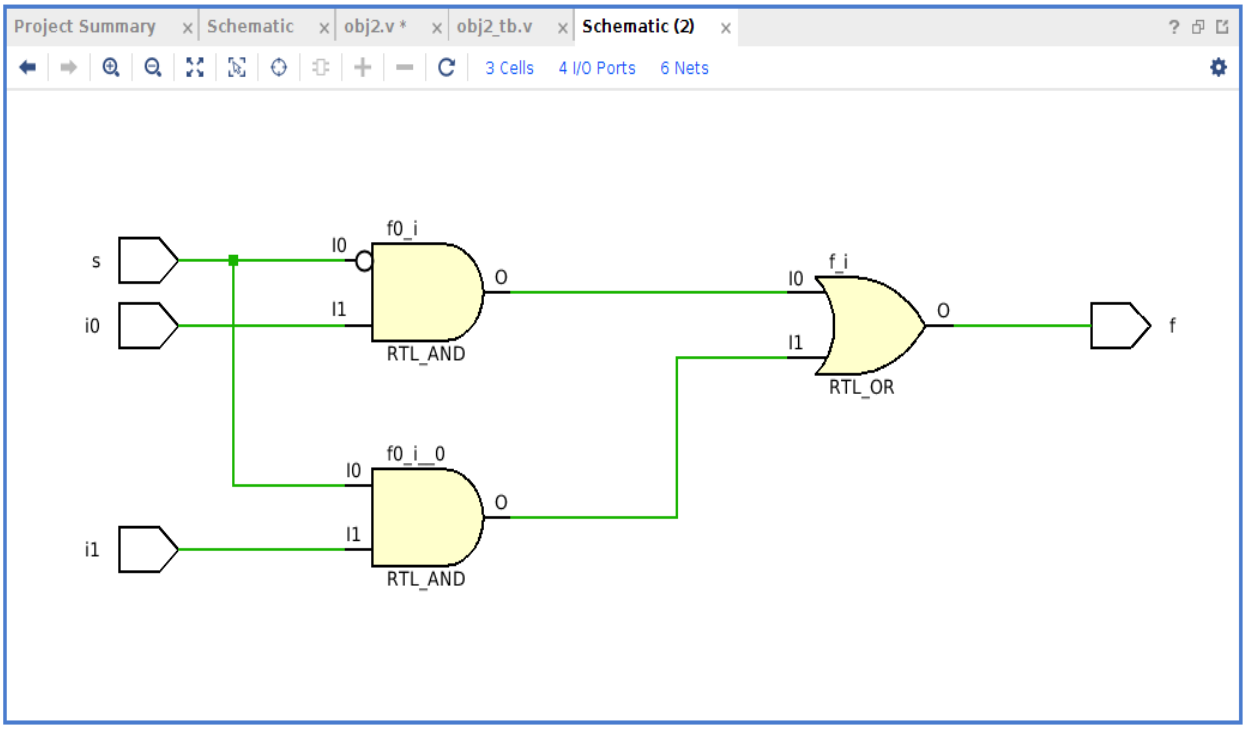
obj1.v | obj1_tb.v | Untitled 7

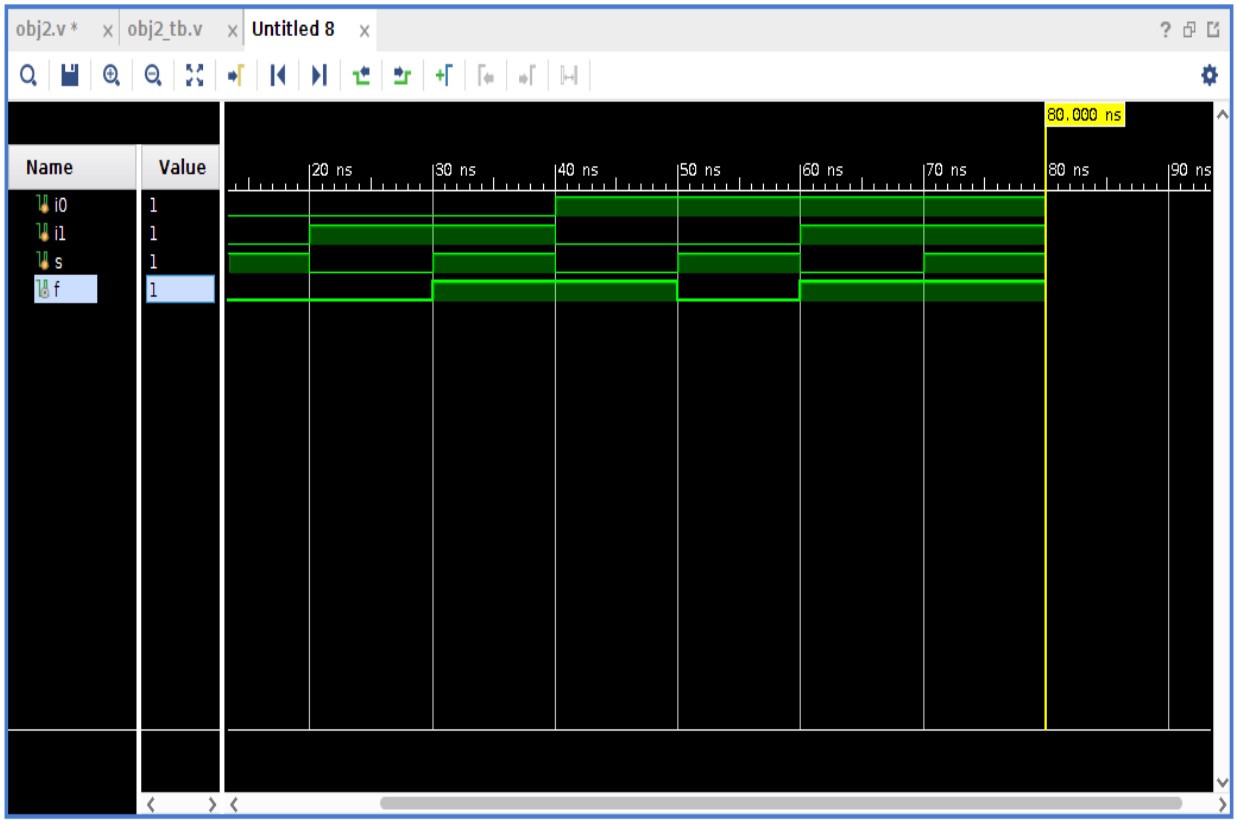
/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sim_1/new/obj1_tb.v

```
22
23  module obj1_tb();
24  reg a3,a2,a1,a0,b3,b2,b1,b0;
25  wire y;
26  obj1 dut(a3,a2,a1,a0,b3,b2,b1,b0,y);
27  initial begin
28  a3=1;a2=0;a1=0;a0=1;
29  b3=0;b2=0;b1=1;b0=1;
30  #10
31  a3=1;a2=1;a1=0;a0=0;
32  b3=1;b2=1;b1=0;b0=0;
33  #10
34  a3=0;a2=0;a1=1;a0=0;
35  b3=0;b2=0;b1=1;b0=0;
36  #10
37  a3=0;a2=0;a1=0;a0=1;
38  b3=0;b2=1;b1=1;b0=0;
39  #10
40
41  $stop;
42  end
43  endmodule
44
```


Project Summary
Schematic
obj1.v
obj1_tb.v
7 Cells
9 I/O Ports
15 Nets
a2
b2
a1
b1
a3
b3
a0
b0
I0
I1
O
y3_i_0
y3_i
y1_i
y2_i
y0_i
y1_i_0
y_i
RTL_XOR
RTL_AND
y


obj1.v
obj1_tb.v
Untitled 7
0.000 ns
Name
Value
a3
a2
a1
a0
b3
b2
b1
b0
y
1
0
0
1
0
0
1
1
0
0 ns
5 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns


Project Summary
Schematic
obj2.v *
obj2_tb.v
Schematic (2)
3 Cells
4 I/O Ports
6 Nets
s
i0
i1
f0_i
I0
I1
O
RTL_AND
f0_i_0
I0
I1
O
RTL_AND
f_i
I0
I1
O
RTL_OR
f


obj2.v *
obj2_tb.v
Untitled 8
Name
Value
i0
i1
s
f
1
1
1
1
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
80.000 ns

obj2.v * | obj2_tb.v | Untitled 8

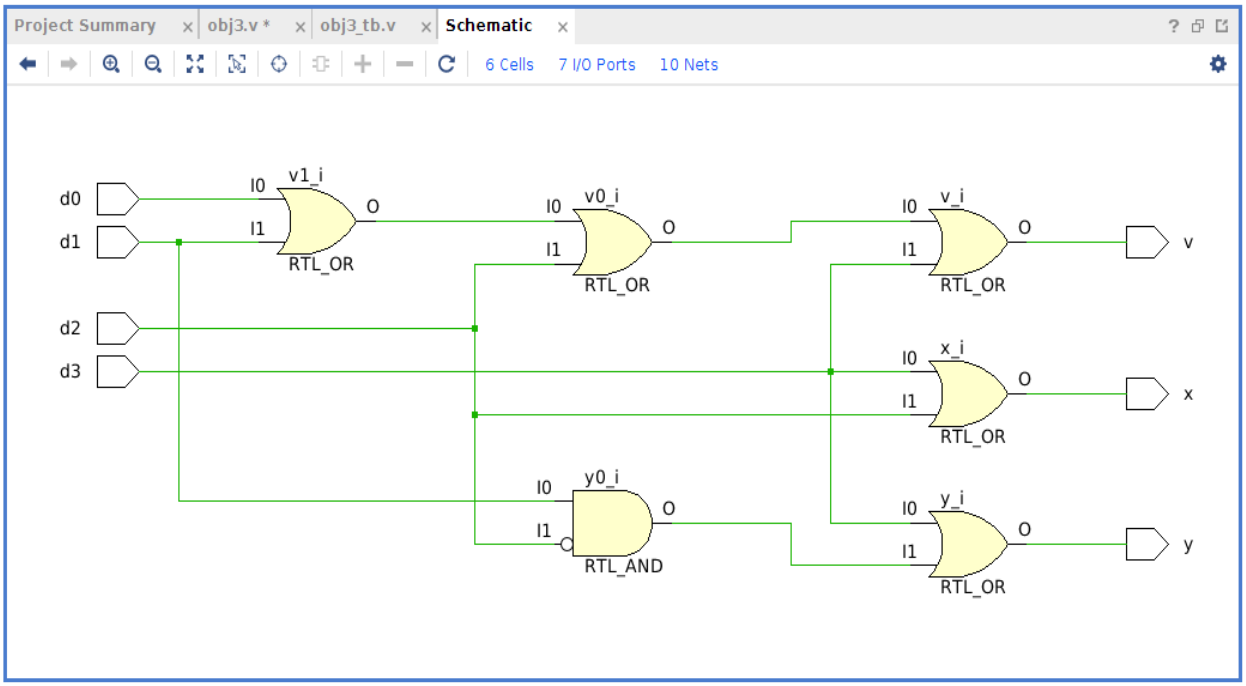
/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sources_1/new/obj2.v

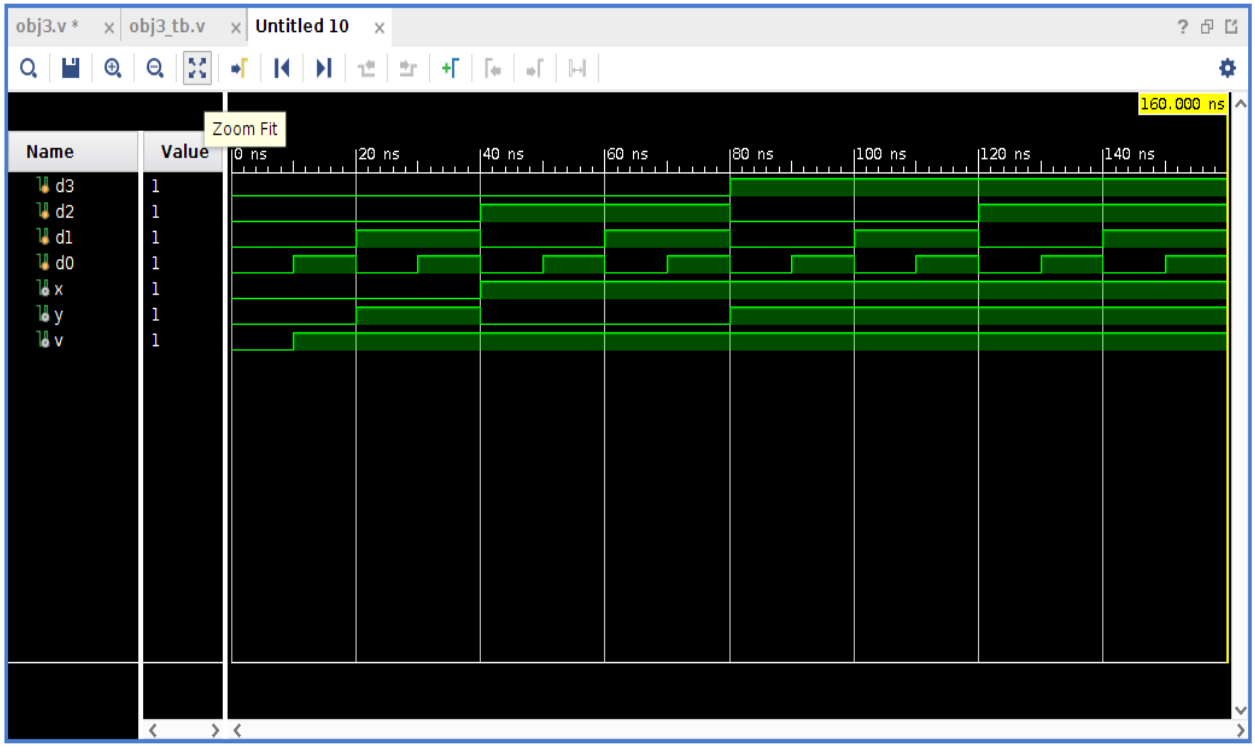
```
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25  module obj2(
26
27      input i0,
28      input i1,
29      input s,
30      output f
31      );
32      assign f =(~s&i0)|(s&i1);
33  endmodule
34
```

obj2.v * | obj2_tb.v | Untitled 8

/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sim_1/new/obj2_tb.v

```
22
23  module obj2_tb();
24  reg i0,i1,s;
25  wire f;
26  obj2 dut(i0,i1,s,f);
27  initial begin
28  i0=0;i1=0;s=0;
29  #10;
30  i0=0;i1=0;s=1;
31  #10;
32  i0=0;i1=1;s=0;
33  #10;
34  i0=0;i1=1;s=1;
35  #10;
36  i0=1;i1=0;s=0;
37  #10;
38  i0=1;i1=0;s=1;
39  #10;
40  i0=1;i1=1;s=0;
41  #10;
42  i0=1;i1=1;s=1;
43  #10;
44
45  $stop;
```


Project Summary
obj3.v *
obj3_tb.v
Schematic
6 Cells
7 I/O Ports
10 Nets
d0
d1
d2
d3
I0
I1
v1_i
O
RTL_OR
v0_i
v_i
v
x_i
x
y0_i
RTL_AND
y_i
y


obj3.v *
obj3_tb.v
Untitled 10
Zoom Fit
160.000 ns
Name
Value
d3
d2
d1
d0
x
y
v
1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns

obj3.v * | obj3_tb.v | Untitled 10

/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sources_1/new/obj3.v

```
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
//Name: Laxmidhar Sahu
//Regd No: 2141019147
//Sec: CSE-M


module obj3(
    input d3,
    input d2,
    input d1,
    input d0,
    output x,
    output y,
    output v
    );
    assign x = d3 | d2;
    assign y = d3 | (d1 & (~d2));
    assign v = d0|d1|d2|d3;
endmodule

```

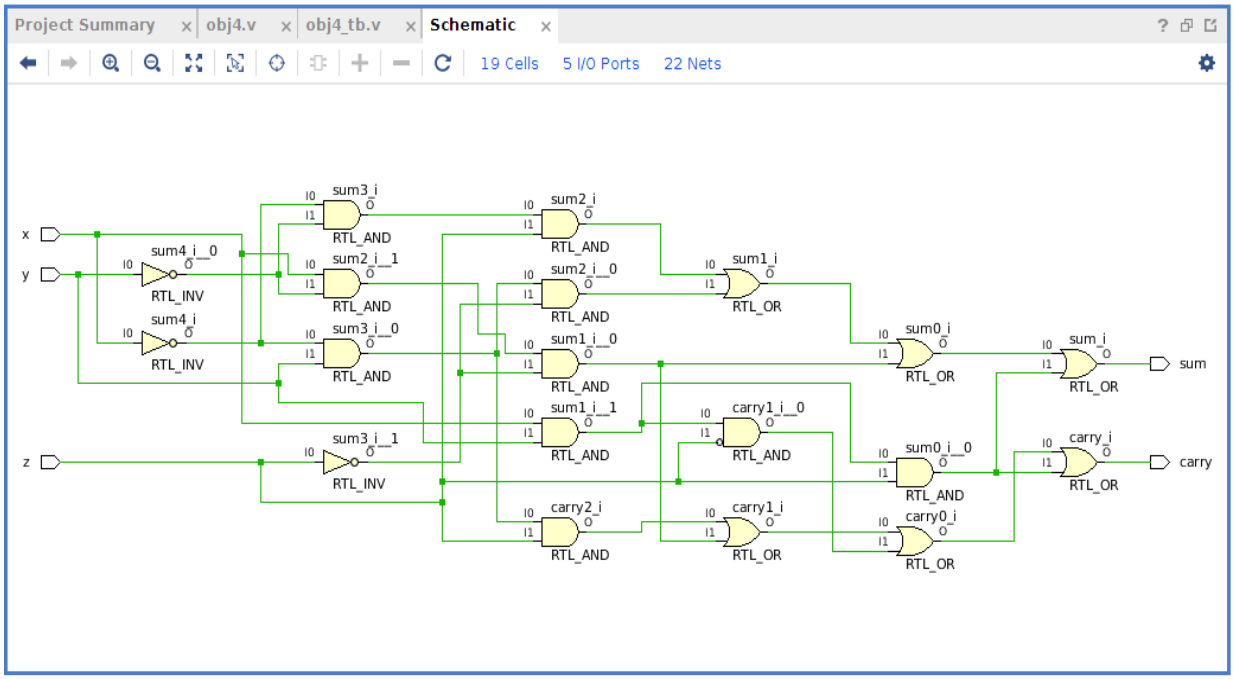
obj3.v * | obj3_tb.v | Untitled 10

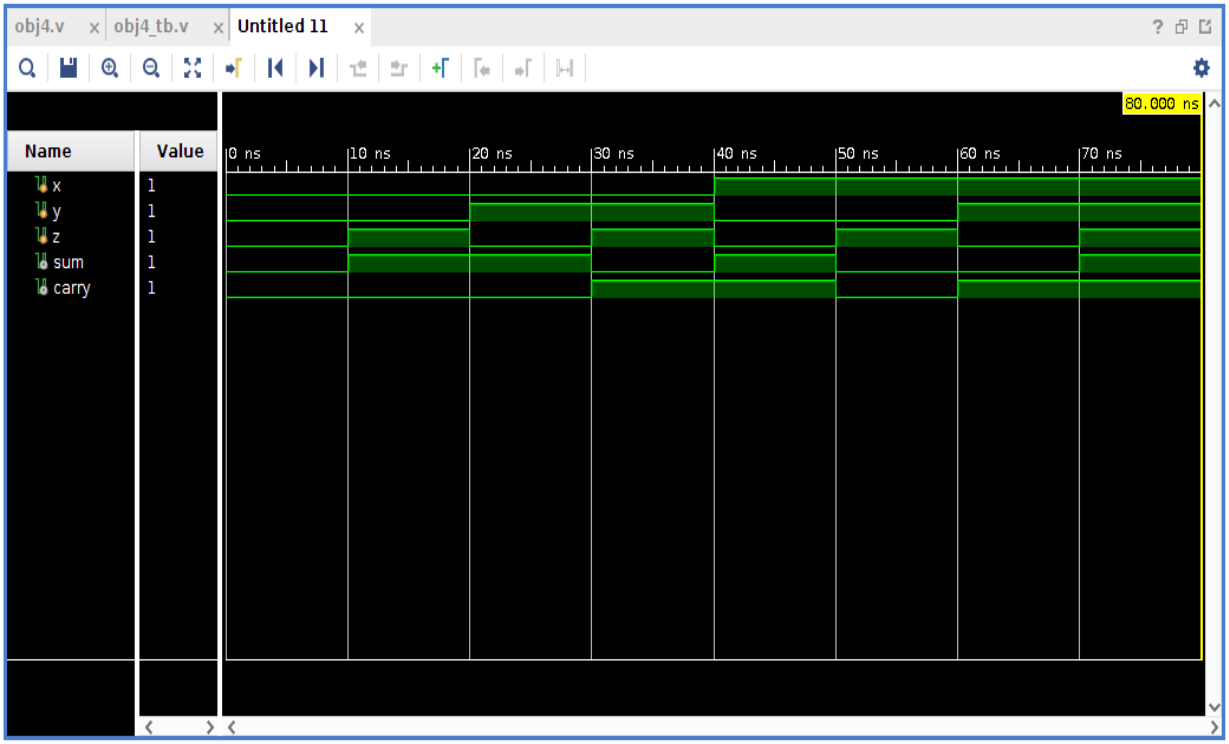
/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sim_1/new/obj3_tb.v

```

module obj3_tb();
reg d3,d2,d1,d0;
wire x,y,v;
obj3 dut(d3,d2,d1,d0,x,y,v);
initial begin


d3=0;d2=0;d1=0;d0=0;
#10;
d3=0;d2=0;d1=0;d0=1;
#10;
d3=0;d2=0;d1=1;d0=0;
#10;
d3=0;d2=0;d1=1;d0=1;
#10;
d3=0;d2=1;d1=0;d0=0;
#10;
d3=0;d2=1;d1=0;d0=1;
#10;
d3=0;d2=1;d1=1;d0=0;
#10;
d3=0;d2=1;d1=1;d0=1;
#10;
```


Project Summary
obj4.v
obj4_tb.v
Schematic
19 Cells
5 I/O Ports
22 Nets
x
y
z
sum
carry
sum4_i_0
sum4_i
sum3_i
sum2_i_1
sum3_i_0
sum3_i_1
sum2_i
sum2_i_0
sum1_i_0
sum1_i_1
carry2_i
sum1_i
carry1_i_0
carry1_i
sum0_i
sum0_i_0
carry0_i
sum_i
carry_i
RTL_INV
RTL_AND
RTL_OR


obj4.v
obj4_tb.v
Untitled 11
80.000 ns
Name
Value
x
y
z
sum
carry
1
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns

obj4.v | obj3_tb.v | obj4_tb.v | Untitled 11

/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sources_1/new/obj4.v

```
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  //Name: Laxmidhar Sahu
22  //Regd No: 2141019147
23  //Sec: CSE-M
24
25
26  module obj4(
27      input x,
28      input y,
29      input z,
30      output sum,
31      output carry
32      );
33
34      assign sum = (~x&~y&z)|(~x&y&~z)|(x&~y&~z)|(x&y&z);
35      assign carry= (~x&y&z)|(x&~y&~z)|(x&y&~z)|(x&y&z);
36  endmodule
37
```

obj4.v | obj4_tb.v | Untitled 11

/home/student/Laxmidhar_2141019147/Lab 6/Lab 6.srcs/sim_1/new/obj4_tb.v

```
27  initial begin
28
29  x=0;y=0;z=0;
30  #10
31  x=0;y=0;z=1;
32  #10
33  x=0;y=1;z=0;
34  #10
35  x=0;y=1;z=1;
36  #10
37  x=1;y=0;z=0;
38  #10
39  x=1;y=0;z=1;
40  #10
41  x=1;y=1;z=0;
42  #10
43  x=1;y=1;z=1;
44  #10
45
46
47  $stop;
48  end
49  endmodule
50
```