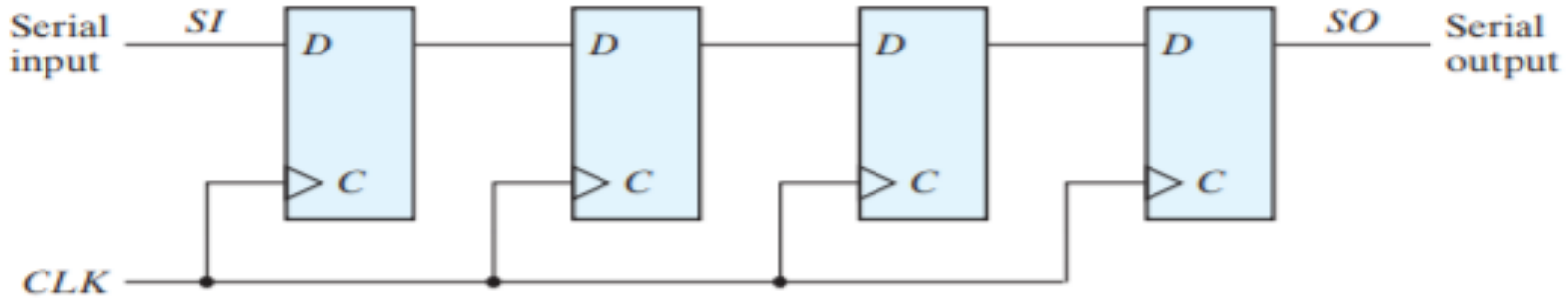
Shift Registers

(Lecture-32)

Shift Registers

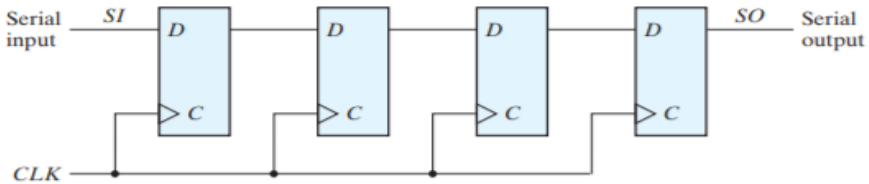
- A register capable of shifting the binary information held in each cell to its neighbouring cell, in a selected direction, is called a shift register.
- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next.
- The simplest possible shift register is one that uses only flip-flops, as shown in Fig.



4 bit shift register

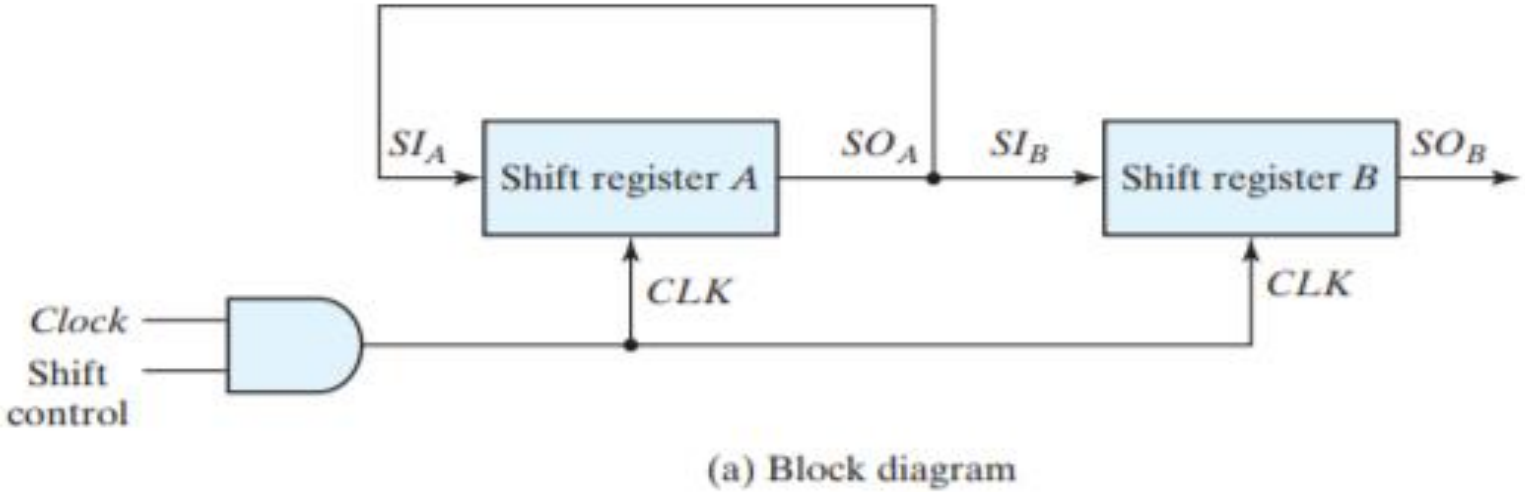
Shift Registers

- The output of a given flip-flop is connected to the D input of the flip-flop at its right.
- This shift register is unidirectional (left-to-right).
- Each clock pulse shifts the contents of the register one bit position to the right.
- The configuration does not support a left shift.
- The serial input determines what goes into the leftmost flip-flop during the shift.
- The serial output is taken from the output of the rightmost flip-flop.
- Sometimes it is necessary to control the shift so that it occurs only with certain pulses, but not with others.

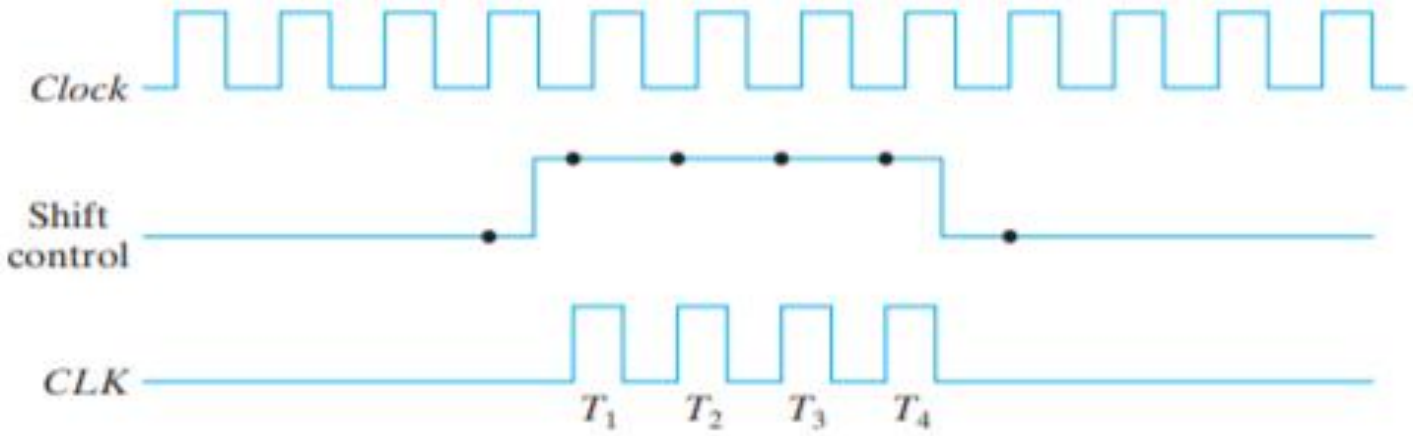


4 bit shift register

Serial transfer from register A to register B



(a) Block diagram



(b) Timing diagram

Shift Registers

- Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops.
- N flip flops are to be connected in an order to store n bits of data.
- A **Register** is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data . The information stored within these registers can be transferred with the help of **shift registers**.

Shift Registers

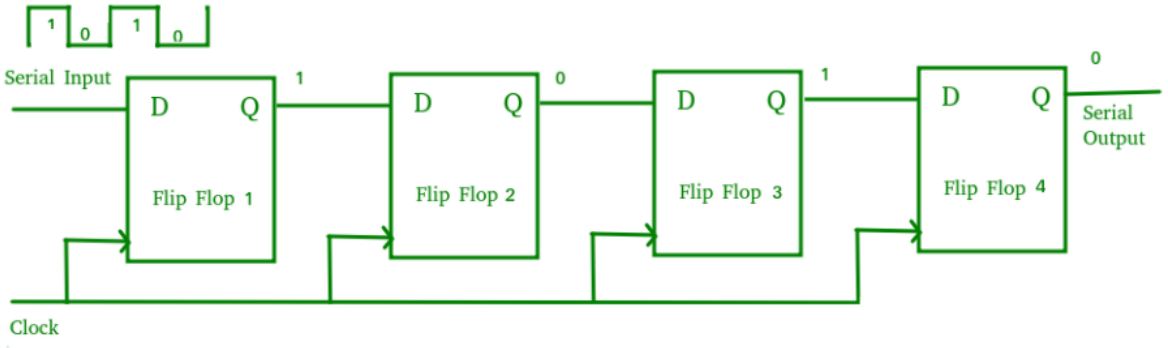
- Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.
- An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. The registers which will shift the bits to left are called “Shift left registers”.
- The registers which will shift the bits to right are called “Shift right registers”.

Shift Registers Types

- Serial In Serial Out shift register
- Serial In parallel Out shift register
- Parallel In Serial Out shift register
- Parallel In parallel Out shift register

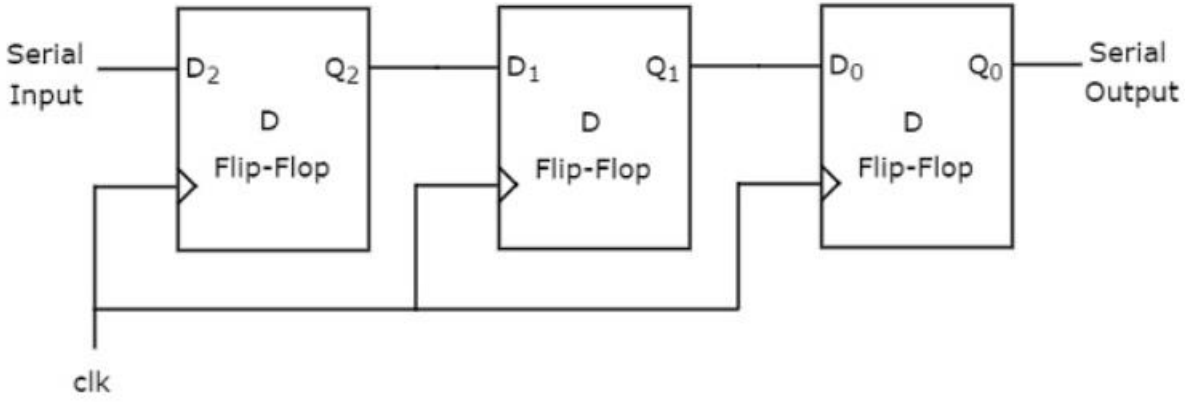
SISO Shift Registers

- The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register.
- Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.
- The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.



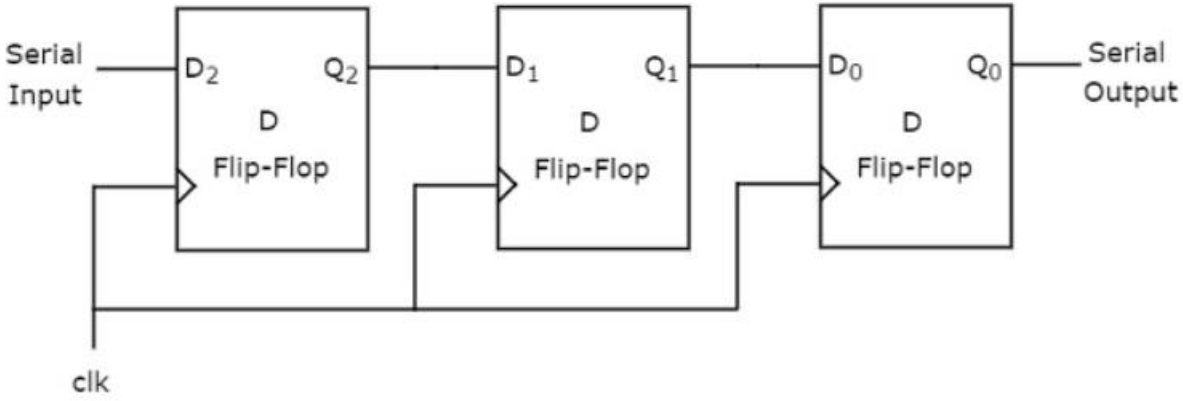
SISO Shift Registers

- The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop.
- The main use of a SISO is to act as a delay element.
- The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out SISO shift register.
- The **block diagram** of 3-bit SISO shift register is shown in the following figure.



SISO Shift Registers

- This block diagram consists of three D flip-flops, which are **cascaded**. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
- In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as **serial output**.



Example

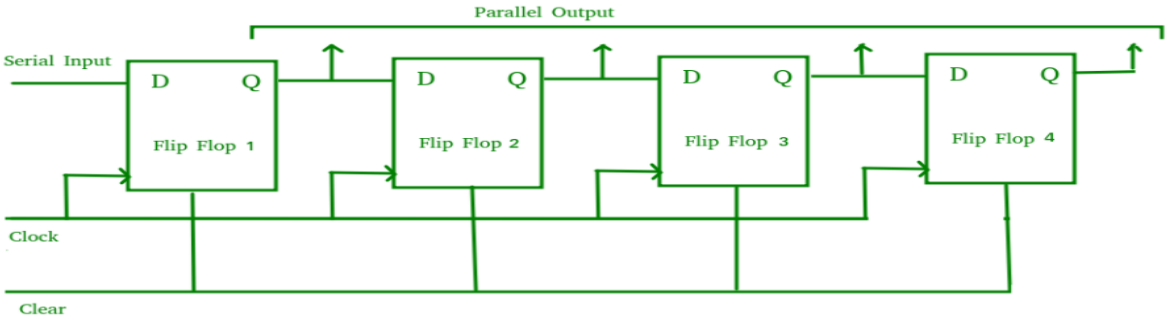
- Let us see the working of 3-bit SISO shift register by sending the binary information **“011”** from LSB to MSB serially at the input.
- Assume, initial status of the D flip-flops from leftmost to rightmost is Q2Q1Q0=000 Q2Q1Q0=000. We can understand the **working of 3-bit SISO shift register** from the following table.
- The initial status of the D flip-flops in the absence of clock signal is Q2Q1Q0=000Q2Q1Q0=000. Here, the serial output is coming from Q0Q0. So, the LSB 11 is received at 3^{rd} positive edge of clock and the MSB 00 is received at 5^{th} positive edge of clock.
- Therefore, the 3-bit SISO shift register requires five clock pulses in order to produce the valid output. Similarly, the **N-bit SISO shift register** requires **2N-1** clock pulses in order to shift ‘N’ bit information.

Example

No of positive edge of Clock	Serial Input	Q_2	Q_1	Q_0
0	-	0	0	0
1	1 LSB	1	0	0
2	1	1	1	0
3	0 MSB	0	1	1 LSB
4	-	-	0	1
5	-	-	-	0 MSB

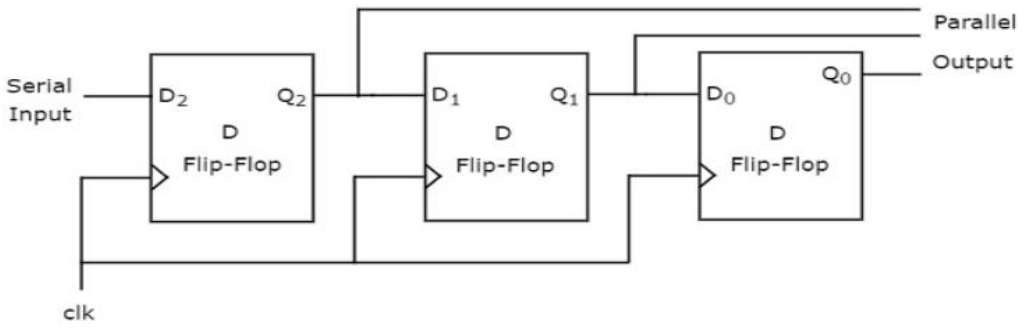
SIPO Shift Registers

- The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.
- The logic circuit given below shows a serial-in-parallel-out shift register.
- The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them.
- The output of the first flip flop is connected to the input of the next flip flop and so on.
- All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.



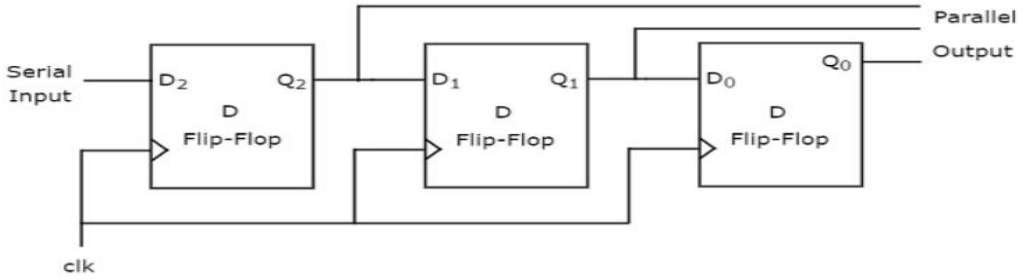
SIPO Shift Registers

- The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop and producing a parallel output.
- They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of the SIPO register is to convert serial data into parallel data.
- The shift register, which allows serial input and produces parallel output is known as Serial In – Parallel Out SIPOSIPO shift register.
- The **block diagram** of 3-bit SIPO shift register is shown in the following figure.



SIPO Shift Registers

- This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop.
- All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
- In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**.
- For every positive edge triggering of clock signal, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel. So, we will get **parallel outputs** from this shift register.



Example

- Let us see the working of 3-bit SIPO shift register by sending the binary information **“011”** from LSB to MSB serially at the input.
- Assume, initial status of the D flip-flops from leftmost to rightmost is Q2Q1Q0=000 Q2Q1Q0=000. Here, Q2Q2 & Q0Q0 are MSB & LSB respectively. We can understand the **working of 3-bit SIPO shift register** from the following table.
- The initial status of the D flip-flops in the absence of clock signal is Q2Q1Q0=000 Q2Q1Q0=000. The binary information **“011”** is obtained in parallel at the outputs of D flip-flops for third positive edge of clock.
- So, the 3-bit SIPO shift register requires three clock pulses in order to produce the valid output. Similarly, the **N-bit SIPO shift register** requires **N** clock pulses in order to shift ‘N’ bit information.

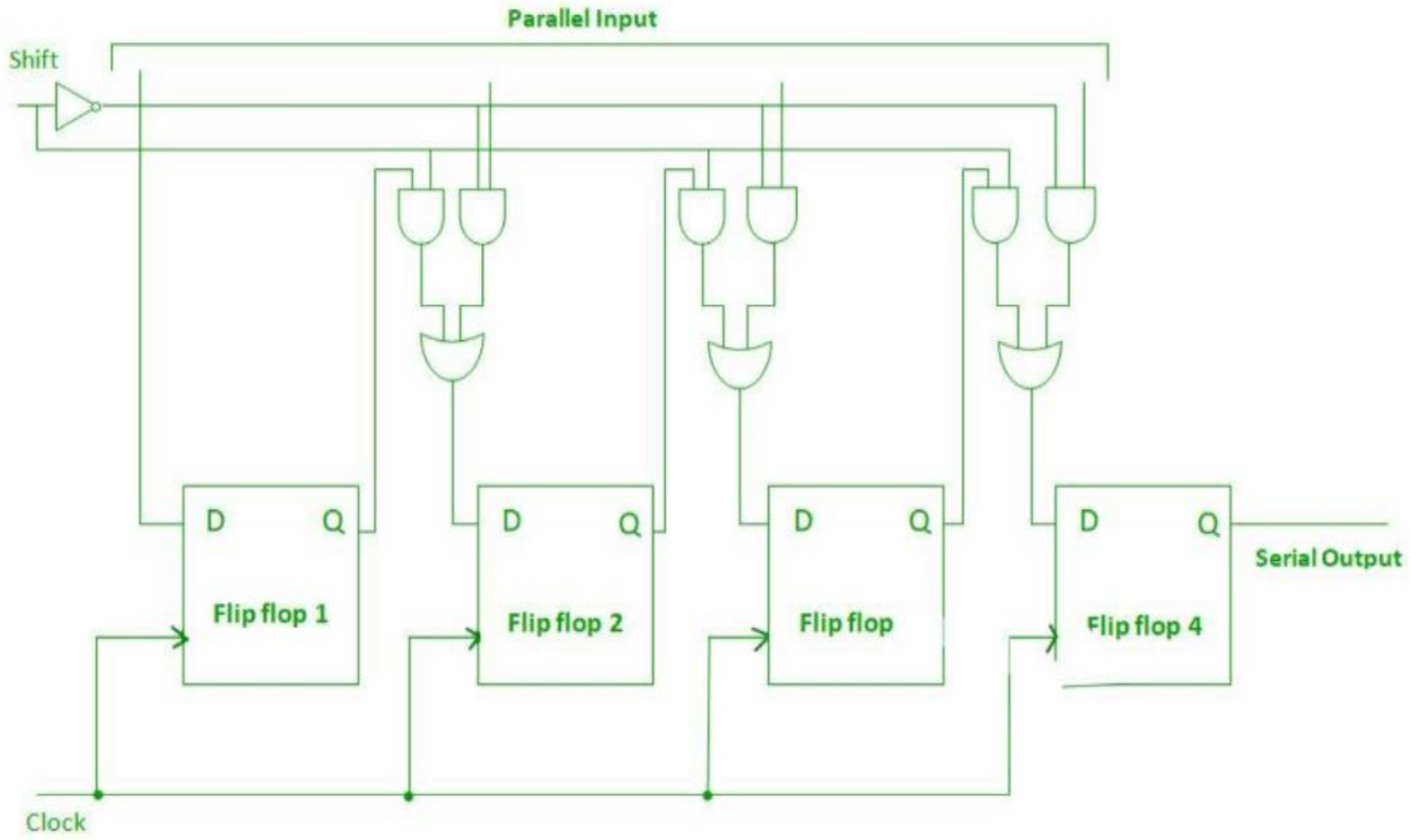
Example

No of positive edge of Clock	Serial Input	Q_2 MSB	Q_1	Q_0 LSB
0	-	0	0	0
1	1 LSB	1	0	0
2	1	1	1	0
3	0 MSB	0	1	1

PISO Shift Registers

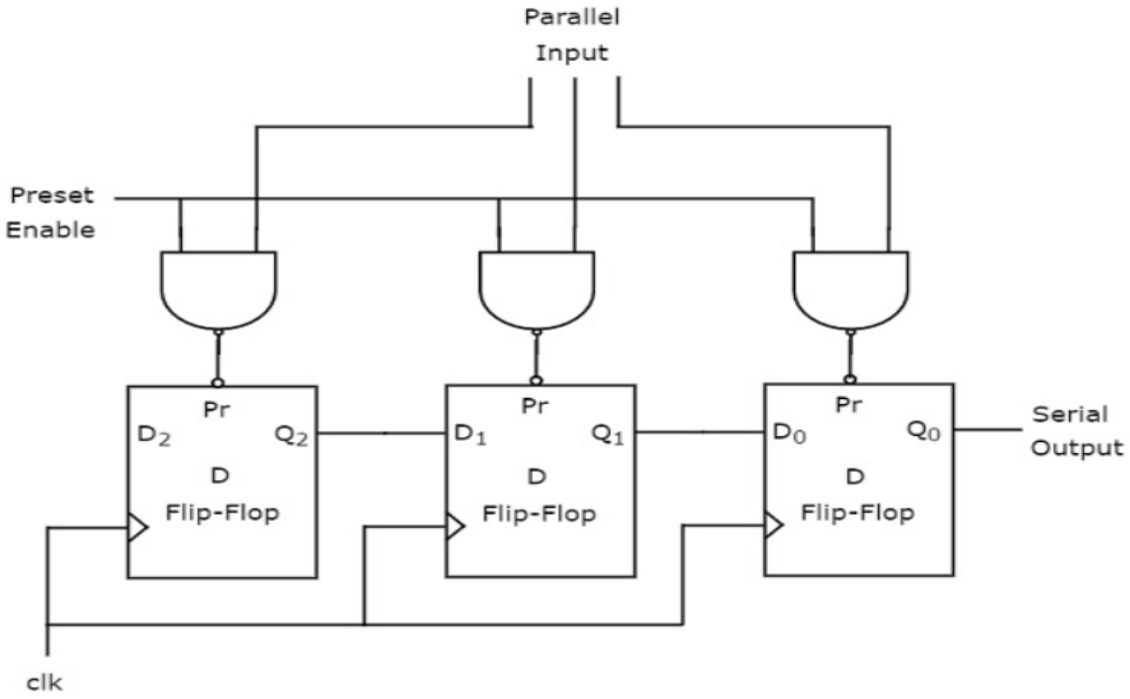
- The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register.
- The logic circuit given below shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected.
- The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a multiplexer at the input of every flip flop.
- The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop.
- All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

PISO Shift Registers



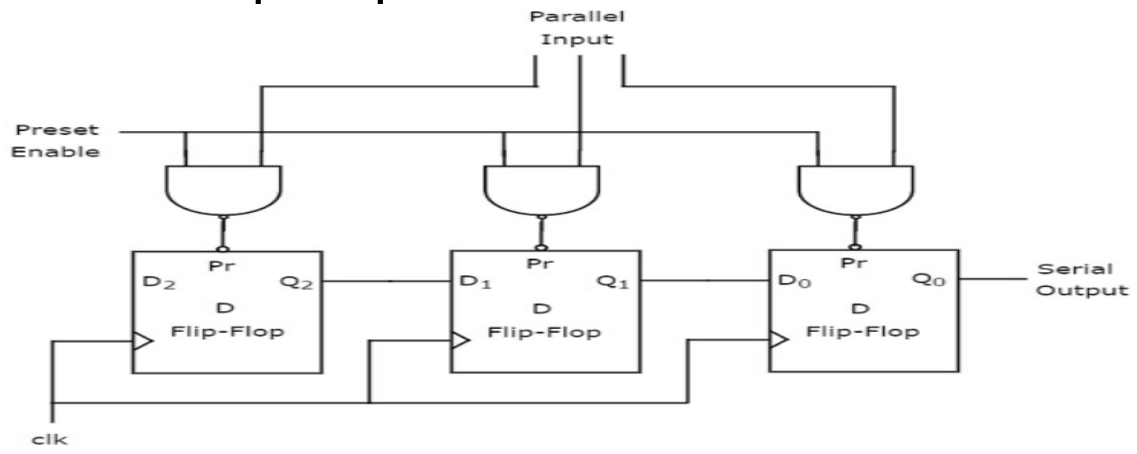
PISO Shift Registers

- A Parallel in Serial out (PISO) shift register us used to convert parallel data to serial data.
- The shift register, which allows parallel input and produces serial output is known as Parallel In – Serial Out PISO shift register.
- The **block diagram** of 3-bit PISO shift register is shown in the following figure



PISO Shift Registers

- This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop.
- All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
- In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1.
- For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we will get the **serial output** from the right most D flip-flop.



Example

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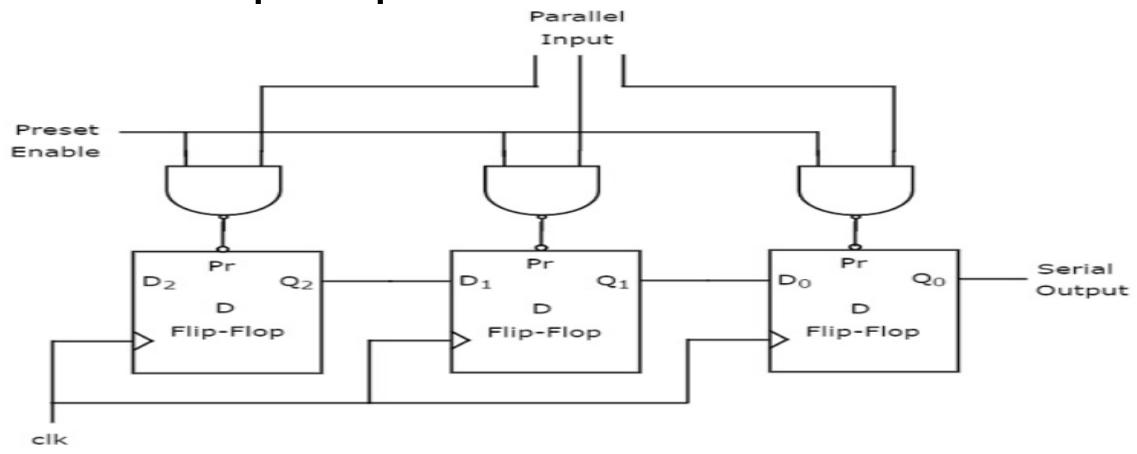


Example

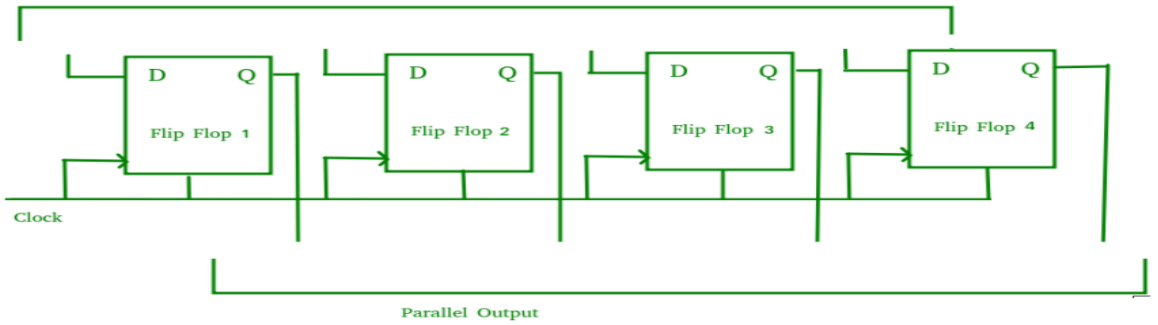
- Let us see the working of 3-bit PISO shift register by applying the binary information **“011”** in parallel through preset inputs.
- Since the preset inputs are applied before positive edge of Clock, the initial status of the D flip-flops from leftmost to rightmost will be Q2Q1Q0=011Q2Q1Q0=011. We can understand the **working of 3-bit PISO shift register** from the following table.
- Here, the serial output is coming from Q0Q0. So, the LSB 11 is received before applying positive edge of clock and the MSB 00 is received at 2^{nd} positive edge of clock.
- Therefore, the 3-bit PISO shift register requires two clock pulses in order to produce the valid output. Similarly, the **N-bit PISO shift register** requires **N-1** clock pulses in order to shift ‘N’ bit information.

Example

No of positive edge of Clock	Q_2	Q_1	Q_0
0	0	1	1 LSB
1	-	0	1
2	-	-	0 LSB

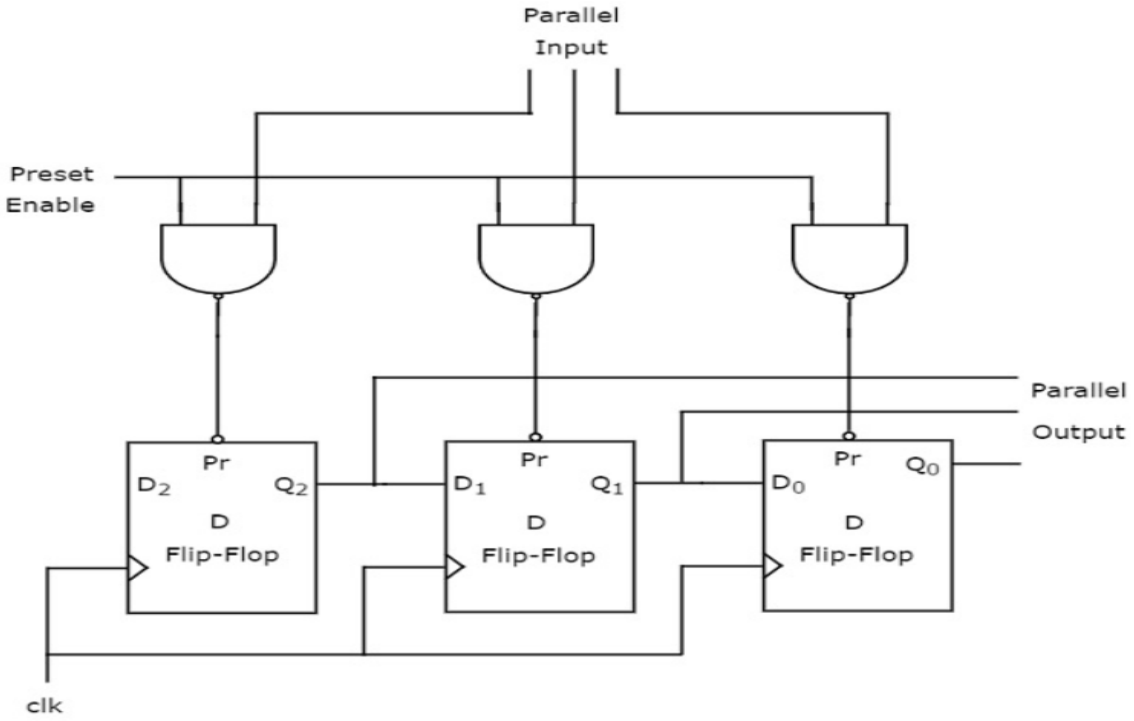
PIPO Shift Registers

- The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register.
- The logic circuit given below shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all the 4 flip flops.
- In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.



PIPO Shift Registers

- A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device and like SISO Shift register it acts as a delay element.
- The shift register, which allows parallel input and produces parallel output is known as Parallel In – Parallel Out PIPOPIPO shift register. The **block diagram** of 3-bit PIPO shift register is shown in the following figure



PIPO Shift Registers

- This circuit consists of three D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop.
- All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
- In this shift register, we can apply the **parallel inputs** to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs. That means, the flip-flops produce the corresponding outputs, based on the values of asynchronous inputs.
- In this case, the effect of outputs is independent of clock transition. So, we will get the **parallel outputs** from each D flip-flop.

Example

- Let us see the working of 3-bit PIPO shift register by applying the binary information **“011”** in parallel through preset inputs.
- Since the preset inputs are applied before positive edge of Clock, the initial status of the D flip-flops from leftmost to rightmost will be Q2Q1Q0=011Q2Q1Q0=011. So, the binary information **“011”** is obtained in parallel at the outputs of D flip-flops before applying positive edge of clock.
- Therefore, the 3-bit PIPO shift register requires zero clock pulses in order to produce the valid output. Similarly, the **N-bit PIPO shift register** doesn’t require any clock pulse in order to shift ‘N’ bit information.

Example

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- Therefore, the 3-bit PIPO shift register requires zero clock pulses in order to produce the valid output. Similarly, the **N-bit PIPO shift register** doesn’t require any clock pulse in order to shift ‘N’ bit information.

Assignment

1. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains Answer: c

   a) 01110
   b) 00001
   c) 00101
   d) 00110

   Explanation: LSB bit is inverted and feed back to MSB:
   01110->initial
   10111->first clock pulse
   01011->second
   00101->third.

2. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

   a) 1100Answer: c
   b) 0011
   c) 0000
   d) 1111

   Explanation: In Serial-In/Serial-Out shift register, data will be shifted one at a time with every clock pulse. Therefore,
   Wait | Store
   1100 | 0000
   110 | 0000 1st clock
   11 | 0000 2nd clock.

Assignment

1. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____

   a) 0000
   b) 1111
   c) 0111
   d) 1000

   Answer: c
   Explanation: In Serial-In/Parallel-Out shift register, data will be shifted all at a time with every clock pulse. Therefore,
   Wait | Store
   0111 | 0000
   011 | 1000 1st clk
   01 | 1100 2nd clk
   0 | 1110 3rd clk
   X | 1111 4th clk.

2. 1. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.

   a) 2
   b) 3
   c) 4
   d) 5

   Answer:c