DIGITAL LOGIC DESIGN LAB (EET1211)

LAB V: DESIGN AND TEST VARIOUS CODE CONVERTER CIRCUITS

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Marks: _____/10

Remarks:

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I. OBJECTIVE:

1. Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.

2. Design a combinational circuit with four inputs and four outputs that converts a 4bit binary number into the equivalent 4bit Gray code.

3. Design a combinational circuit that accepts a 2-bit number and generate output binary number equal to the square of the input number.

II. PRE-LAB

For Obj. 1:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 2:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

For Obj. 3:

a. Write the truth table for the circuit.
b. Derive the Minimized Boolean expression for each output of the circuit.
c. Draw the logic diagram for the circuit.
d. Write HDL code.

OBJECTIVE - 1

a)

	A	B	C	D	W	X	Y	Z
0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0
2	0	0	1	0	0	1	1	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	0

[10-15 are unused bit. They are considered as don't care condition]

b)

$W = \Sigma m(0,1)$

AB \ CD	00	01	11	10
00	1	1		
01				
11	×	×	×	×
10			×	×

$W = A'B'C'$

$X = \Sigma(2,3,4,5)$

AB \ CD	00	01	11	10
00			1	1
01	1	1		
11	×	×	×	×
10			×	×

$X = B \oplus C$

$Y = \Sigma m(2,3,6,7)$

AB \ CD	00	01	11	10
00			1	1
01			1	1
11	×	×	×	×
10			×	×

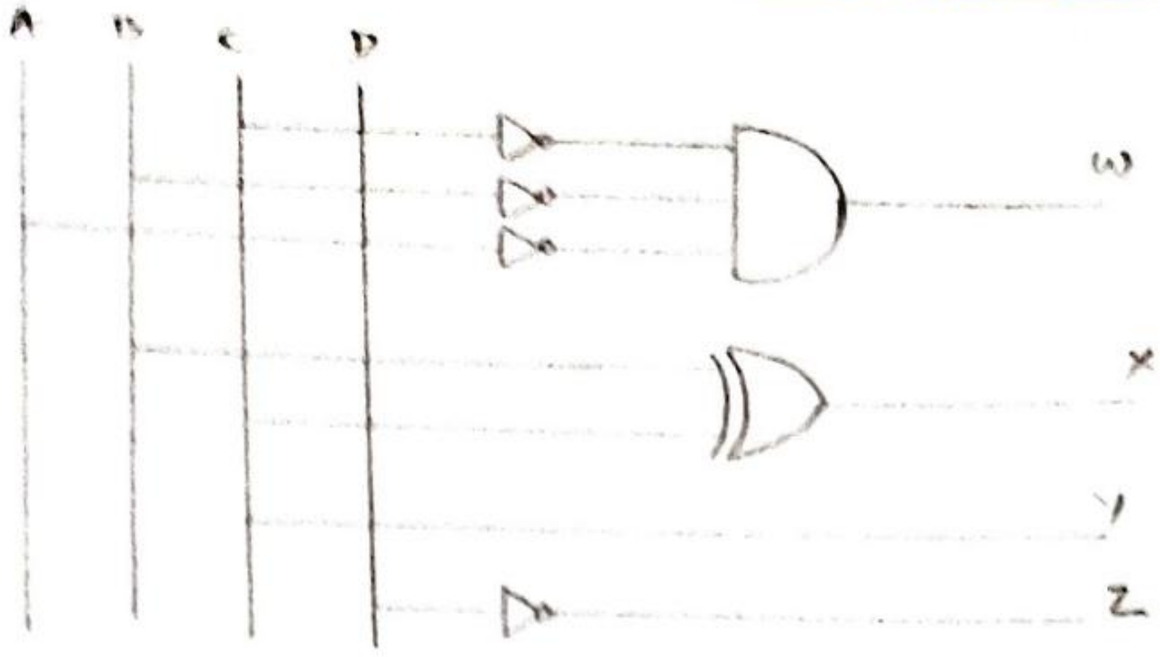
$Y = C$

$Z = \Sigma(0,2,4,6,8)$

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	×	×	×	×
10	1		×	×

$Z = D'$

c)

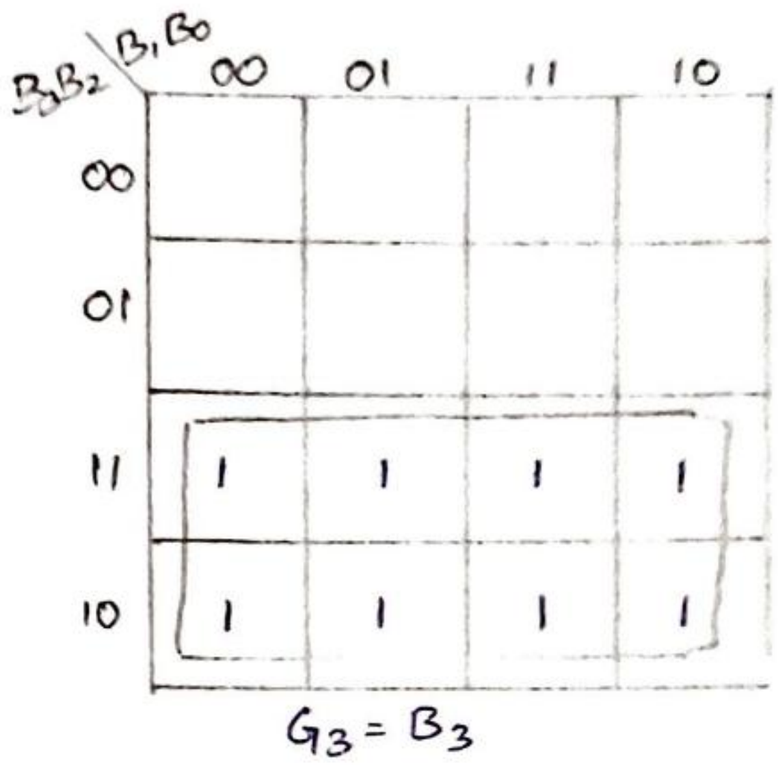


OBJECTIVE - 2

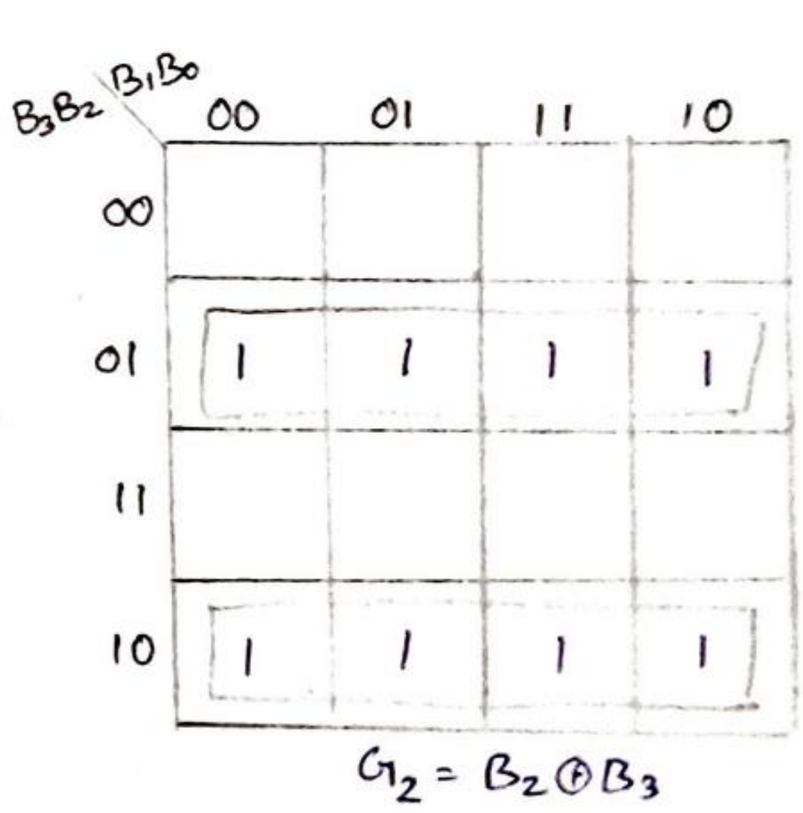
a)

B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

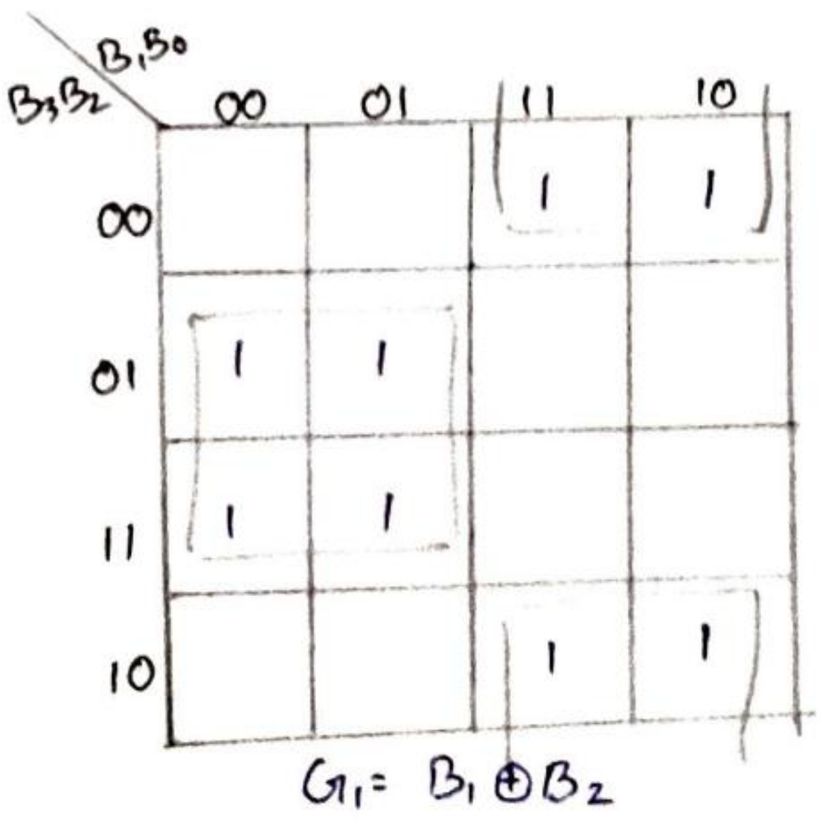
b)



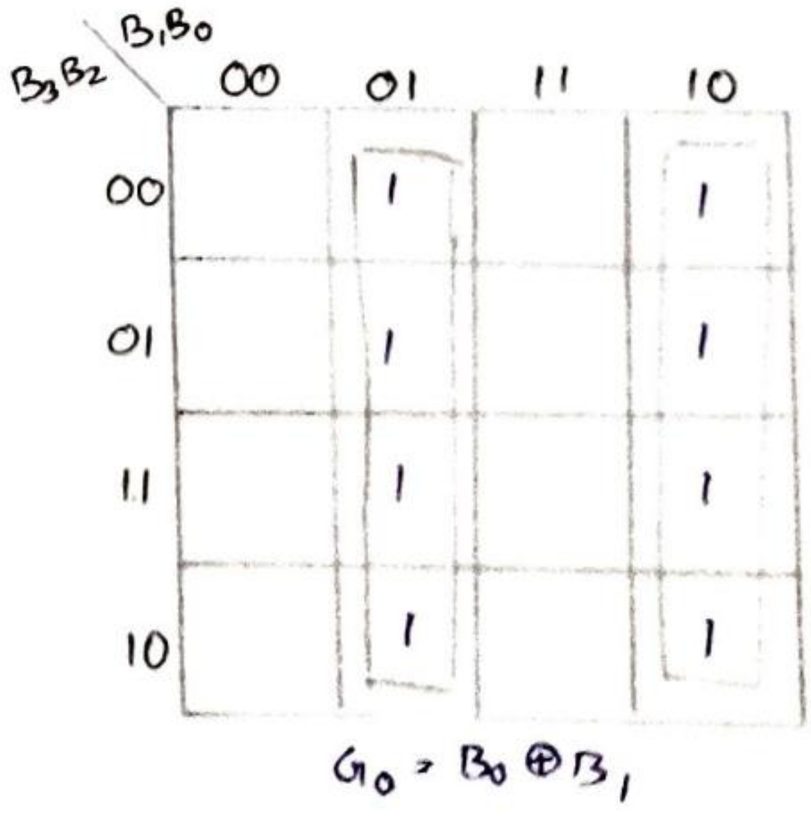
$G_3 = B_3$



$G_2 = B_2 \oplus B_3$

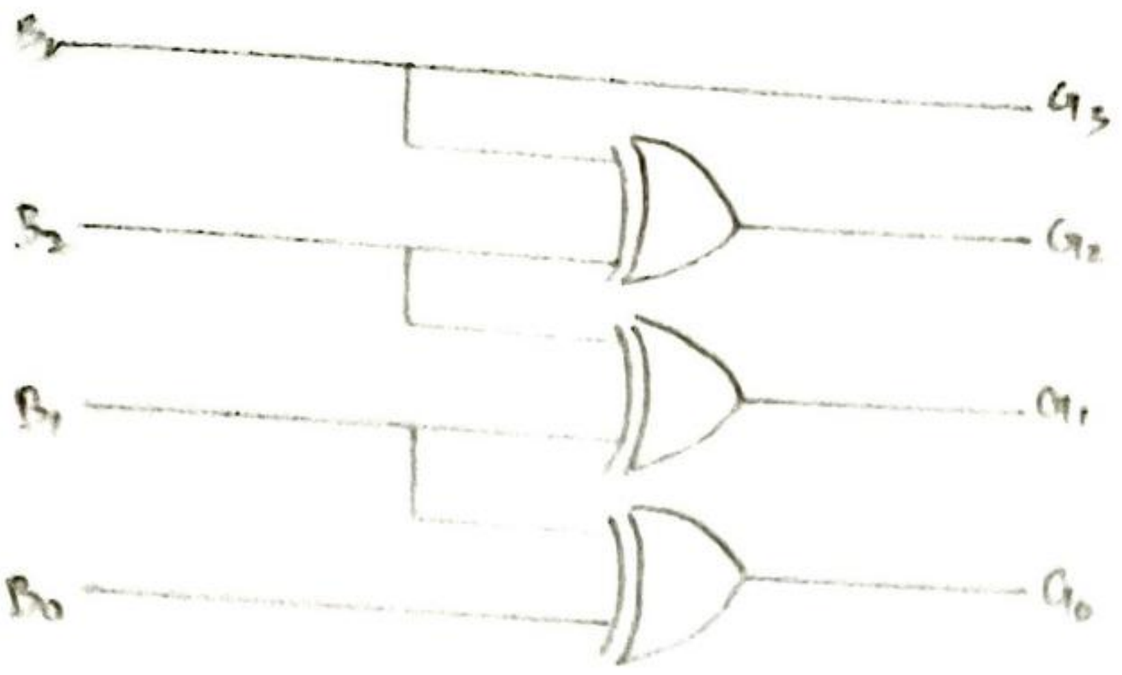


$G_1 = B_1 \oplus B_2$



$G_0 = B_0 \oplus B_1$

e)



c) HDL Code

```
module obj2(B3, B2, B1, B0, G3, G2, G1, G0);
output G3, G2, G1, G0;
input  B3, B2, B1, B0;
assign G3 = B3;
assign G2 = B2 ^ B3;
assign G1 = B1 ^ B2;
assign G0 = B0 ^ B1;
endmodule.
```

d) HDL Code

```
module obj1(A, B, C, D, W, X, Y, Z);
output W, X, Y, Z;
input  A, B, C, D;
wire   w1, w2, w3;
assign w = ((!A) && (!B) && (!C));
assign X = B^C;
assign Y = C;
assign Z = (!D);
endmodule
```

OBJECTIVE - 3

a)

A	B	W	X	Y	Z
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	0	0
1	1	1	0	0	1

b) $W = AB$

$X = A\bar{B}$

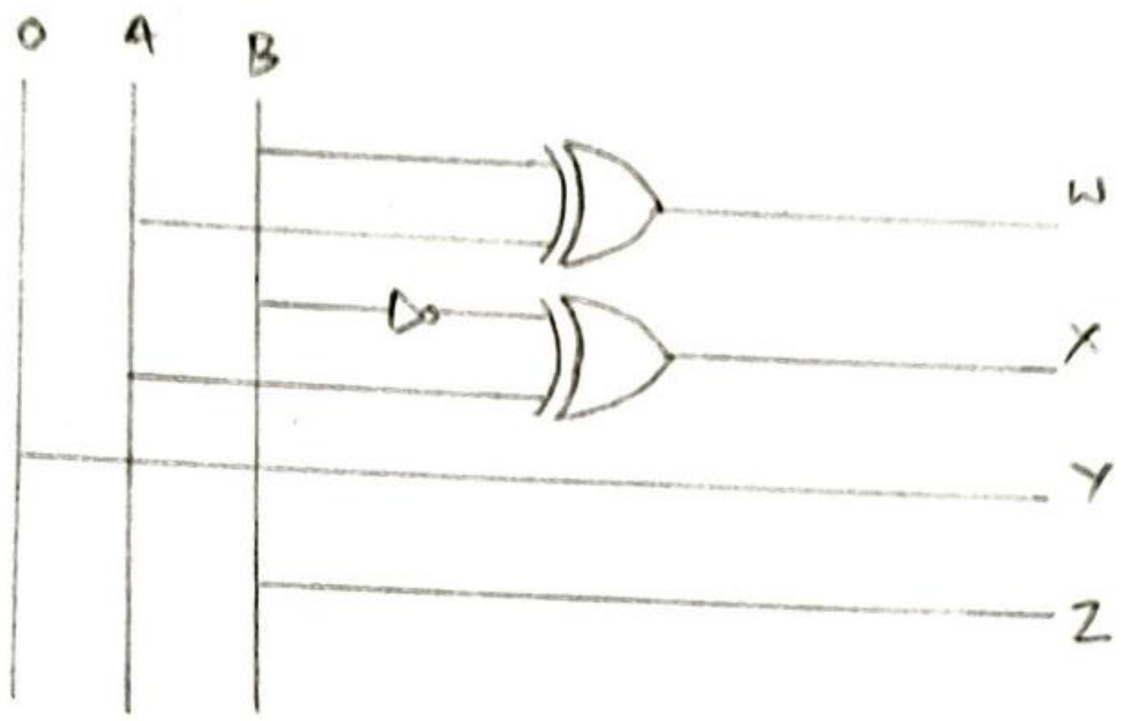
$Y = 0$

$Z = \bar{A}B + AB$

$= B(\bar{A} + A)$

$= B$

c)



d) HDL Code

```
module obj3(A, B, W, X, Y, Z);
input A, B;
output W, X, Y, Z;
assign W = A && B;
assign X = A && !B;
assign Y = 0;
assign Z = B;
endmodule
```