PRODUCT DESIGN GUIDE

NVIDIA Jetson Nano

(Preliminary – Subject to Change)

Abstract

This document contains recommendations and guidelines for Engineers to follow to create a product that is optimized to achieve the best performance from the common interfaces supported by the NVIDIA® Jetson Nano™ System-on-Module (SoM).

This document provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

Notes: Most of the interface usage noted in this document is based on the NVIDIA Developer Kit carrier board design.

Document Change History

Date	Description
JUN 7, 2019	Initial Release

NVIDIA.

Table of Contents

1.0 INTRODUCTION

1.1 References

Refer to the documents or models listed in Table 1 for more information. Use the latest revision of all documents at all times.

Table 1. List of Related Documents

Document
Jetson Nano Module Data Sheet
Tegra X1 (SoC) Technical Reference Manual
Jetson Nano Developer Kit Carrier Board Specification
Jetson Nano Module Pinmux
Jetson Nano Thermal Design Guide
Jetson Nano Developer Kit Carrier Board Design Files
Jetson Nano Developer Kit Carrier Board BOM
Jetson Nano SCL (Supported Component List)

1.2 Abbreviations and Definitions

Table 2 lists abbreviations that may be used throughout this document and their definitions.

Table 2. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
DP	Display Port
DSI	Display Serial Interface
eDP	Embedded Display Port
ESD	Electrostatic Discharge
eMMC	Embedded MMC
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LPDDR4	Low Power Double Data Rate DRAM, Fourth-generation
MDI	Medium-Dependent Interface
MIL	$1/1000^{th}$ of an inch
MIPI	Mobile Industry Processor Interface
mm	Millimeter
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
ps	Pico-Seconds
PMU	Power Management Unit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock
SD Card	Secure Digital Card
SDIO	Secure Digital I/O Interface
SE	Single-Ended
SPI	Serial Peripheral Interface
TMDS	Transition-minimized differential signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

2.0 JETSON NANO

2.1 Overview

The Jetson Nano resides at the center of the embedded system solution and includes:

- Power (PMIC/Regulators, etc.)
- DRAM (LPDDR4)
- eMMC
- Gigabit Ethernet Controller
- Power Monitor

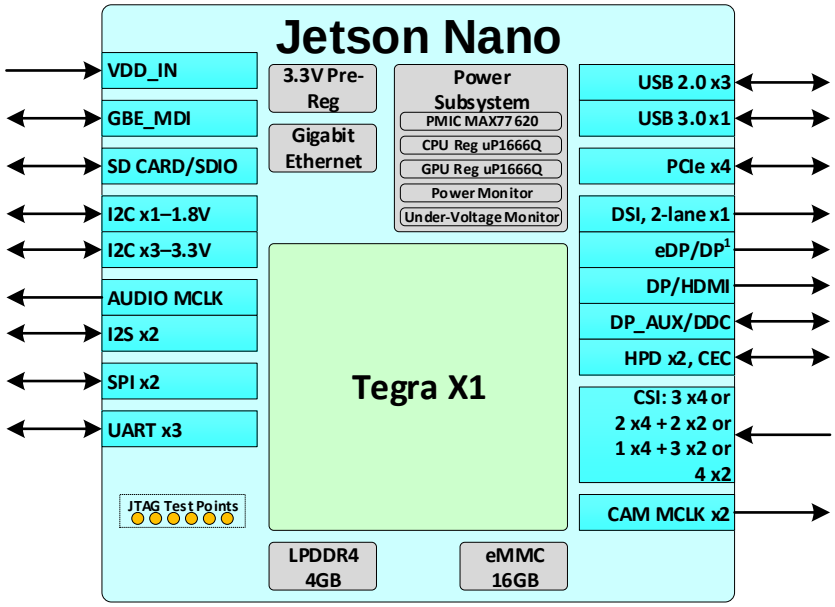
In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown below.

Table 3. Jetson Nano Interfaces

Category	Function		Category	Function
USB	USB 2.0 Interface (3x)		**LAN**	Gigabit Ethernet
	USB 3.0 (1x)		**I2C**	4x
PCIe	PCIe (x1/2/4)		**UART**	3x
Camera	CSI (3 x4 or 2 x4 + 2 x2 or 1 x4 + 3 x2), Control, Clock		**SPI**	2x
Display	eDP/DP (see note 1)		**Wi-Fi/BT/Modem**	PCIe/UART/I2S, Control/handshake
	HDMI/DP Interface (w/CEC)		**Fan**	FAN PWM and Tach Input
	DSI (1 x2), Display/Backlight Control		**Debug**	JTAG test points on module and UART
Audio	I2S Interface (2x) and Clock		**System**	Power Control, Reset, alerts
SD Card/SDIO	SD Card or SDIO Interface (1x)		**Power**	Main Input and battery back-up for RTC

Notes: 1. DP on eDP interface does not support HDCP or Audio.

Figure 1. Jetson Nano Block Diagram



Notes: 1. DP on eDP interface does not support HDCP or Audio.

Table 4. Jetson Nano Connector (260-Pin SO-DIMM) Pin Out Matrix

Module Signal Name	Pin #		Pin #	Module Signal Name
GND	1		2	GND
CSI1_D0_N	3		4	CSI0_D0_N
CSI1_D0_P	5		6	CSI0_D0_P
GND	7		8	GND
RSVD	9		10	CSI0_CLK_N
RSVD	11		12	CSI0_CLK_P
GND	13		14	GND
CSI1_D1_N	15		16	CSI0_D1_N
CSI1_D1_P	17		18	CSI0_D1_P
GND	19		20	GND
CSI3_D0_N	21		22	CSI2_D0_N
CSI3_D0_P	23		24	CSI2_D0_P
GND	25		26	GND
CSI3_CLK_N	27		28	CSI2_CLK_N
CSI3_CLK_P	29		30	CSI2_CLK_P
GND	31		32	GND
CSI3_D1_N	33		34	CSI2_D1_N
CSI3_D1_P	35		36	CSI2_D1_P
GND	37		38	GND
DP0_TXD0_N	39		40	CSI4_D2_N
DP0_TXD0_P	41		42	CSI4_D2_P
GND	43		44	GND
DP0_TXD1_N	45		46	CSI4_D0_N
DP0_TXD1_P	47		48	CSI4_D0_P
GND	49		50	GND
DP0_TXD2_N	51		52	CSI4_CLK_N
DP0_TXD2_P	53		54	CSI4_CLK_P
GND	55		56	GND
DP0_TXD3_N	57		58	CSI4_D1_N
DP0_TXD3_P	59		60	CSI4_D1_P
GND	61		62	GND
DP1_TXD0_N	63		64	CSI4_D3_N
DP1_TXD0_P	65		66	CSI4_D3_P
GND	67		68	GND
DP1_TXD1_N	69		70	DSI_D0_N
DP1_TXD1_P	71		72	DSI_D0_P
GND	73		74	GND
DP1_TXD2_N	75		76	DSI_CLK_N
DP1_TXD2_P	77		78	DSI_CLK_P
GND	79		80	GND
DP1_TXD3_N	81		82	DSI_D1_N
DP1_TXD3_P	83		84	DSI_D1_P
GND	85		86	GND
GPIO00	87		88	DP0_HPD
SPI0_MOSI	89		90	DP0_AUX_N
SPI0_SCK	91		92	DP0_AUX_P
SPI0_MISO	93		94	HDMI_CEC
SPI0_CS0*	95		96	DP1_HPD
SPI0_CS1*	97		98	DP1_AUX_N
UART0_TXD	99		100	DP1_AUX_P
UART0_RXD	101		102	GND
UART0_RTS*	103		104	SPI1_MOSI
UART0_CTS*	105		106	SPI1_SCK
GND	107		108	SPI1_MISO
USB0_D_N	109		110	SPI1_CS0*
USB0_D_P	111		112	SPI1_CS1*
GND	113		114	CAM0_PWDN
USB1_D_N	115		116	CAM0_MCLK
USB1_D_P	117		118	GPIO01
GND	119		120	CAM1_PWDN
USB2_D_N	121		122	CAM1_MCLK
USB2_D_P	123		124	GPIO02
GND	125		126	GPIO03
GPIO04	127		128	GPIO05
GND	129		130	GPIO06
PCIE0_RX0_N	131		132	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
PCIE0_RX0_P	133		134	PCIE0_TX0_N
GND	135		136	PCIE0_TX0_P
PCIE0_RX1_N	137		138	GND
PCIE0_RX1_P	139		140	PCIE0_TX1_N
GND	141		142	PCIE0_TX1_P
RSVD	143		144	GND
KEY	KEY		KEY	KEY
RSVD	145		146	GND
GND	147		148	PCIE0_TX2_N
PCIE0_RX2_N	149		150	PCIE0_TX2_P
PCIE0_RX2_P	151		152	GND
GND	153		154	PCIE0_TX3_N
PCIE0_RX3_N	155		156	PCIE0_TX3_P
PCIE0_RX3_P	157		158	GND
GND	159		160	PCIE0_CLK_N
USBSS_RX_N	161		162	PCIE0_CLK_P
USBSS_RX_P	163		164	GND
GND	165		166	USBSS_TX_N
RSVD	167		168	USBSS_TX_P
RSVD	169		170	GND
GND	171		172	RSVD
RSVD	173		174	RSVD
RSVD	175		176	GND
GND	177		178	MOD_SLEEP*
PCIE_WAKE*	179		180	PCIE0_CLKREQ*
PCIE0_RST*	181		182	RSVD
RSVD	183		184	GBE_MDI0_N
I2C0_SCL	185		186	GBE_MDI0_P
I2C0_SDA	187		188	GBE_LED_LINK
I2C1_SCL	189		190	GBE_MDI1_N
I2C1_SDA	191		192	GBE_MDI1_P
I2S0_DOUT	193		194	GBE_LED_ACT
I2S0_DIN	195		196	GBE_MDI2_N
I2S0_FS	197		198	GBE_MDI2_P
I2S0_SCLK	199		200	GND
GND	201		202	GBE_MDI3_N
UART1_TXD	203		204	GBE_MDI3_P
UART1_RXD	205		206	GPIO07
UART1_RTS*	207		208	GPIO08
UART1_CTS*	209		210	CLK_32K_OUT
GPIO09	211		212	GPIO10
CAM_I2C_SCL	213		214	FORCE_RECOVERY*
CAM_I2C_SDA	215		216	GPIO11
GND	217		218	GPIO12
SDMMC_DAT0	219		220	I2S1_DOUT
SDMMC_DAT1	221		222	I2S1_DIN
SDMMC_DAT2	223		224	I2S1_FS
SDMMC_DAT3	225		226	I2S1_SCLK
SDMMC_CMD	227		228	GPIO13
SDMMC_CLK	229		230	GPIO14
GND	231		232	I2C2_SCL
SHUTDOWN_REQ*	233		234	I2C2_SDA
PMIC_BBAT	235		236	UART2_TXD
POWER_EN	237		238	UART2_RXD
SYS_RESET*	239		240	SLEEP/WAKE*
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VDD_IN	251		252	VDD_IN
VDD_IN	253		254	VDD_IN
VDD_IN	255		256	VDD_IN
VDD_IN	257		258	VDD_IN
VDD_IN	259		260	VDD_IN

Legend

Ground	Power	Reserved - must be left unconnected

3.0 POWER

Caution *Jetson Nano is not hot-pluggable. Before installing or removing the module, the main power supply (to VDD_IN pins) must be disconnected and adequate time (recommended > 1 minute) allowed for the various power rails to fully discharge.*

Power for the module is supplied on the VDD_IN pins and is nominally 5.0V (see the Jetson Nano Data Sheet for supply tolerance and maximum current).

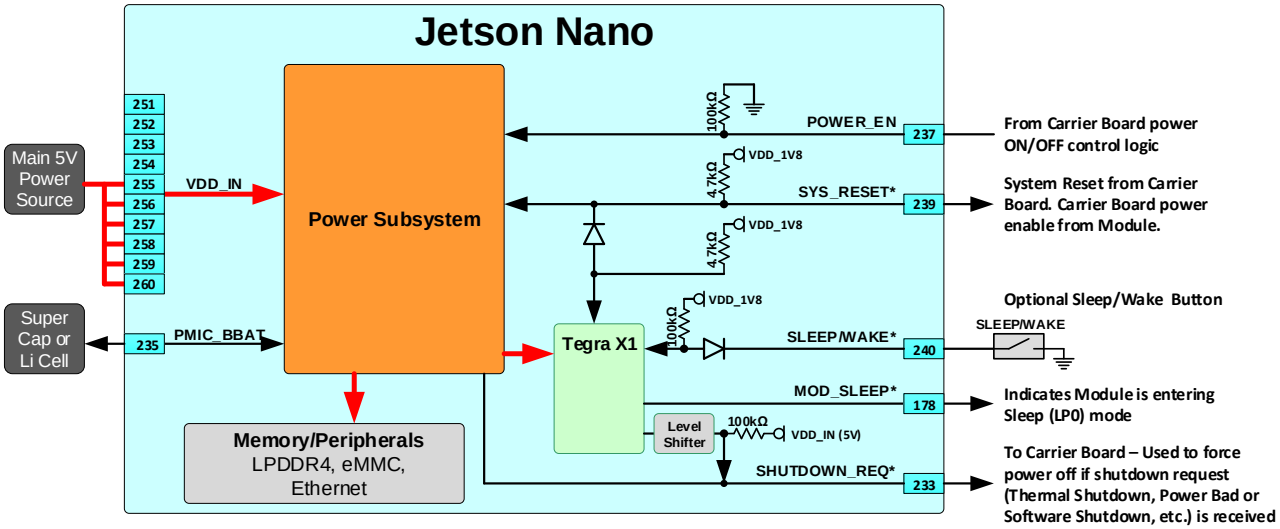
Table 5. Jetson Nano Power and System Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
251 ↓ 260	VDD_IN	–	Main power – Supplies PMIC and other regulators	Main DC input	Input	5.0V
235	PMIC_BBAT	–	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is source when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Battery Back-up using Super-capacitor	Bidir	1.65V-5.5V
214	FORCE_RECOVERY*	BUTTON_VOL_UP	Force Recovery strap pin	System	Input	CMOS – 1.8V
240	SLEEP/WAKE*	BUTTON_PWR_ON	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V
233	SHUTDOWN_REQ*	–	Used by the module to request the carrier board to shut down. ~5kΩ pull-up to VDD_IN (5V) on the module.	System	Output	Open Drain, 5.0V
237	POWER_EN	(PMIC EN0 through converter logic)	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. 100kΩ pulldown on the module.	System	Input	Analog 5.0V
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 4.7kΩ pull-up to 1.8V on the module.	System	Bidir	Open Drain, 1.8V
178	MOD_SLEEP*	GPIO_PA6	Indicates the module sleep status. Low is in sleep mode, high is normal operation. This pin is controlled by system software and should not be modified.	HDMI termination pull-down FET control disable	Output	CMOS – 1.8V

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 2. Jetson Nano Power and Control Block Diagram



3.1 Power Supply and Sequencing

The carrier board receives the main power source and uses this to generate the enable to Jetson Nano (POWER_EN) after the carrier board has ensured the main supply is stable and the associated decoupling capacitors have charged. The carrier board supplies are not enabled at this time. Once POWER_EN is driven active (high), Jetson Nano begins to Power-ON. When the module Power-ON sequence has completed, the SYS_RESET* signal is driven inactive (high) and this is used by the carrier board to enable its various supplies. SYS_RESET* is bidirectional and can be driven by the carrier board to reset Jetson Nano, which results in a full system power cycle. The SHUTDOWN_REQ* signal from Jetson Nano can be driven active (low) if the system must be shut down, due to a critical thermal issue, etc. The power control logic on the carrier board should drive POWER_EN inactive (low) if SHUTDOWN_REQ* is asserted.

Figure 3. System Power and Control Block Diagram

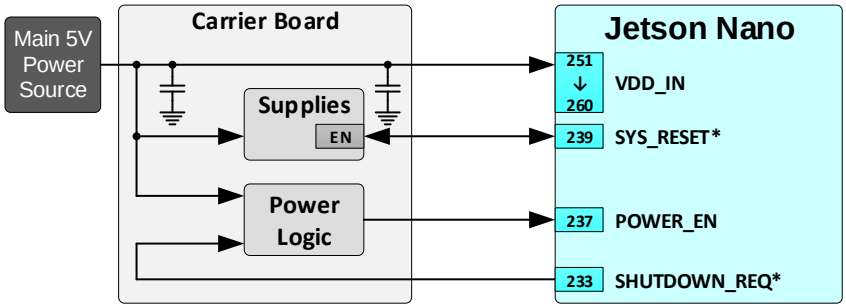


Figure 4. Power Up Sequence

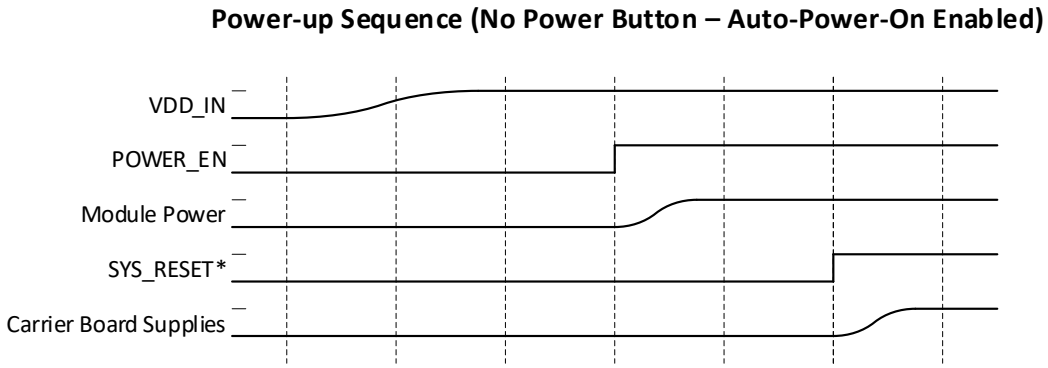


Figure 5. Power Down (Initiated by SHUTDOWN_REQ* Assertion)

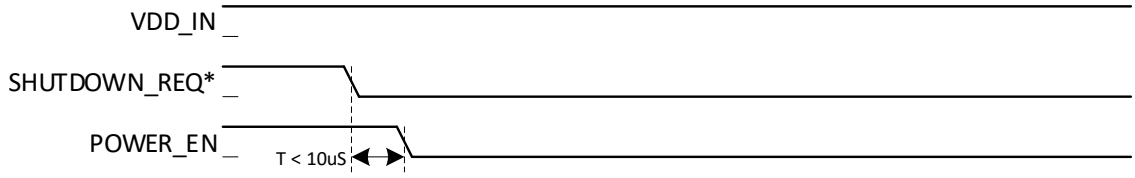
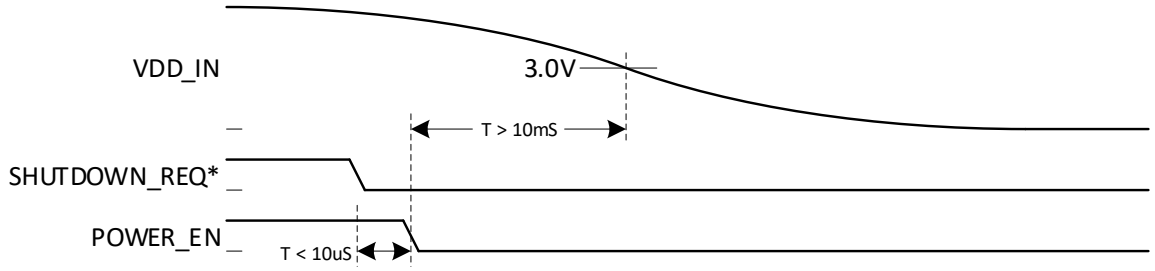


Figure 6. Power Down (Sudden Power Loss)



Note: - SHUTDOWN_REQ* must always be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss.

4.0 USB AND PCIE

Jetson Nano allows multiple USB 2.0, USB 3.0 and PCIe interfaces to be brought out of the module.

Table 6. Jetson Nano USB 2.0 Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
87	GPIO00	USB_VBUS_EN0	GPIO #0 (USB 0 VBUS Detect)	USB 2.0 Micro B	Input	Open Drain, 1.8V
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB 2.0 Micro B	Bidir	USB PHY
111	USB0_D_P	USB0_DP				
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB Hub	Bidir	USB PHY
117	USB1_D_P	USB1_DP				
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	M.2 Key E	Bidir	USB PHY
123	USB2_D_P	USB2_DP				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Table 7. Jetson Nano USB 3.0 and PCIe Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
131	PCIE0_RX0_N	PEX_RX4N	PCIe #0 Receive 1 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Input	PCIe PHY, AC-Coupled on carrier board only if direct connect to device
133	PCIE0_RX0_P	PEX_RX4P				
137	PCIE0_RX1_N	PEX_RX3N	PCIe #0 Receive 1 (PCIe Ctrl #0 Lane 1)	Not Assigned		
139	PCIE0_RX1_P	PEX_RX3P				
149	PCIE0_RX2_N	PEX_RX2N	PCIe #0 Receive 2 (PCIe Ctrl #0 Lane 2)			
151	PCIE0_RX2_P	PEX_RX2P				
155	PCIE0_RX3_N	PEX_RX1N	PCIe #0 Receive 3 (PCIe Ctrl #0 Lane 3)			
157	PCIE0_RX3_P	PEX_RX1P				
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	M.2 Key E	Input	Open Drain 3.3V, Pull-up on the module
181	PCIE0_RST*	PEX_L0_RST_N	PCIe #0 Reset (PCIe Ctrl #0). 4.7kΩ pull-up to 3.3V on the module.	Not Assigned	Output	Open Drain 3.3V, Pull-up on the module
134	PCIE0_TX0_N	PEX_TX4N	PCIe #0 Transmit 0 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Output	PCIe PHY, AC-Coupled on carrier board
136	PCIE0_TX0_P	PEX_TX4P				
140	PCIE0_TX1_N	PEX_TX3N	PCIe #0 Transmit 1PCIe Ctrl #0 Lane 1)	Not Assigned		
142	PCIE0_TX1_P	PEX_TX3P				
148	PCIE0_TX2_N	PEX_TX2N	PCIe #0 Transmit 2 (PCIe Ctrl #0 Lane 2)			
150	PCIE0_TX2_P	PEX_TX2P				
154	PCIE0_TX3_N	PEX_TX1N	PCIe #0 Transmit 3 (PCIe Ctrl #0 Lane 3)			
156	PCIE0_TX3_P	PEX_TX1P				
160	PCIE0_CLK_N	PEX_CLK1N	PCIe #0 Reference Clock (PCIe Ctrl #0)	M.2 Key E	Output	PCIe PHY
162	PCIE0_CLK_P	PEX_CLK1P				
180	PCIE0_CLKREQ*	PEX_L0_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module.	Not Assigned	Bidir	Open Drain 3.3V, Pull-up on the module
161	USBSS_RX_N	PEX_RX6N	USB SS Receive (USB 3.0 Ctrl #0)	USB 3.0 Type A	Input	USB SS PHY, AC-Coupled only if direct connect to device
163	USBSS_RX_P	PEX_RX6P				
166	USBSS_TX_N	PEX_TX6N	USB SS Transmit (USB 3.0 Ctrl #0)		Output	USB SS PHY, AC-Coupled on carrier board
168	USBSS_TX_P	PEX_TX6P				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

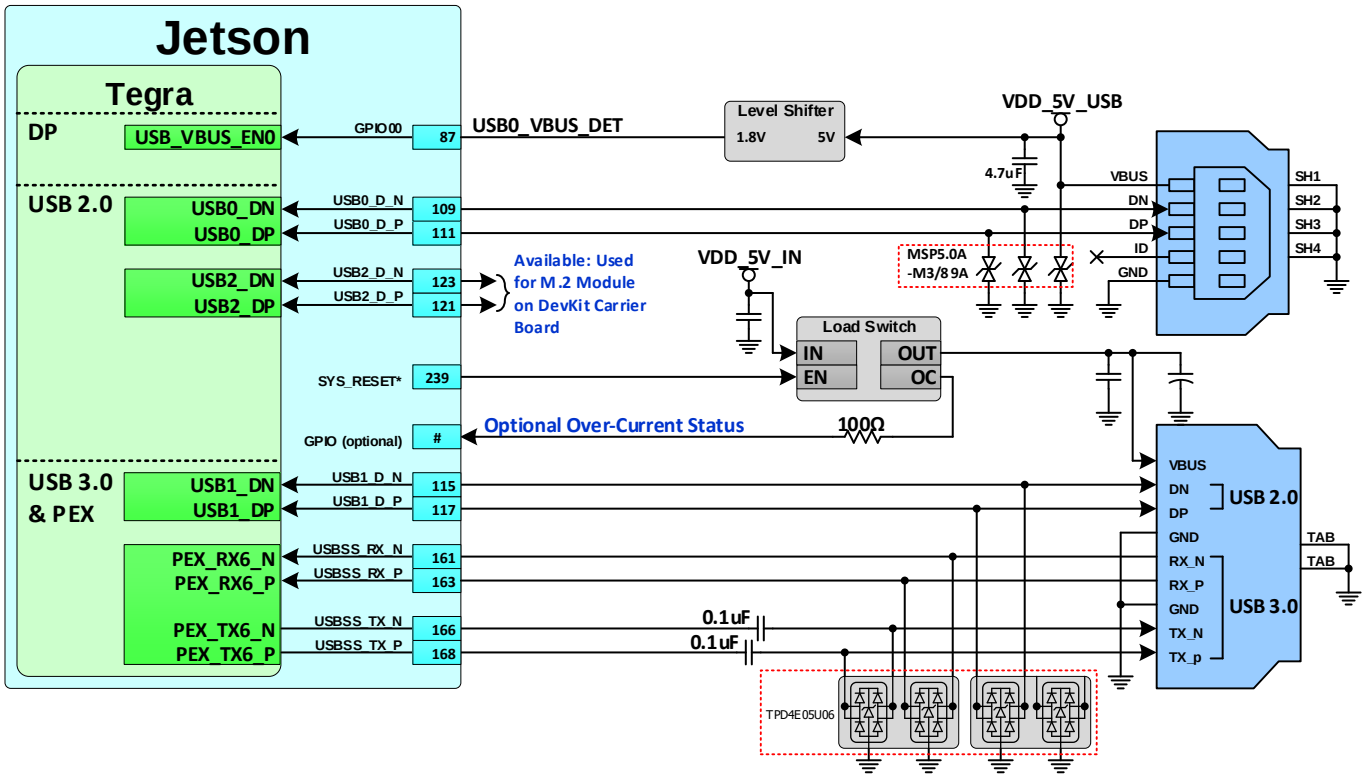
The table below the mapping options for Jetson Nano.

Table 8. Jetson Nano USB 3.0 and PCIe Lane Mapping Configurations

Module Pin Names		na	PCIe3	PCIe 2	PCIe 1	PCIe 0	USBSS
Tegra X1 Lanes		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 6
USB 3.0	PCIe						
1	1x4	PCIe#1_0 - Used for Ethernet on Module	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#0
Usage on NVIDIA DevKit Carrier Board		N/A	Unused			M.2 Key E	USB Type A

4.1 USB

Figure 7 USB Connection Example



Note:
1. AC capacitors should be located close to either the USB connector, or the Jetson Nano pins.
2. For USB 3.0 IF shown above (**USBSS_TX/RX**), AC caps are required on the TX lines. If routed directly to a peripheral, AC caps are needed on the peripheral TX lines as well. The AC caps are recommended to be located near the Jetson Nano connector pins, although locating the caps near the peripheral RX pins is acceptable.
3. USB0 must be available to use as USB Device for USB Recovery Mode.
4. Load switch can be enabled by SYS_RESET* or an available GPIO.
5. Connector used must be USB Implementers Forum certified if USB 3.0 implemented.

USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[2:0]_D_N/P**

Table 9. USB 2.0 Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency (high speed)	Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max loading	High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane		**GND**		
Trace impedance	Diff pair / SE	90 / 50	Ω	±15%
Via proximity (signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay	Microstrip / Stripline	6 (960)	In (ps)	
Max intra-pair skew between **USBx_D_P** and **USBx_D_N**		7.5	ps	

Note:
1. Up to four signal vias can share a single **GND** return via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

USB 3.0 Design Guidelines

The requirements following apply to the USB 3.0 port #0 PHY interface: USBSS_TX_N/P, USBSS_RX_N/P.

Table 10. USB 3.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data rate / UI period	5.0 / 200	Gbps / ps	
Max number of loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX
Electrical Specification			
Insertion loss @ 2.5GHz Type-C Type A Resonance dip frequency	<=2 <=7 >8	dB dB GHz	Only PCB with add-on components (connector excluded) is considered
TDR dip	>= 75	Ω	Using TDR pulse with Tr (10%-90%) = 200ps
Near-end crosstalk (NEXT) @ DC to 5GHz	<=-45	dB	For each TX-RX NEXT
IL/NEXT plot	See USB 3.0 Guideline Figure 1		
Impedance			
Reference plane	**GND**		
Trace impedance Diff pair / SE	85-90 / 45-55	Ω	±15%
Trace Spacing – for TX/RX non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If it is necessary to have interleaved routing in breakout, all the inter-pair spacing should follow the rule of inter-SNEXT			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
See USB 3.0 Guideline Figure 2			
Min inter-S_{NEXT} Breakout (between TX/RX) Main-route	4.85x 3x	Dielectric height	- This is the recommended dimension for meeting NEXT requirement - Stripline structure in a GSSG structure is assumed; it holds in broadside-coupled stripline structure - All values are in terms of minimum dielectric height
Min inter-S_{FEXT} Breakout (between TX/TX or RX/RX) Main-route	1x 1x	Inter-pair spacing	
Max length Breakout Main-route	11 Max trace length - LBRK	mm	
Trace Spacing			
Pair-Pair (inter-pair) Microstrip / Stripline To plane and capacitor pad Microstrip / Stripline To unrelated high-speed signals Microstrip / Stripline	4x / 3x 4x / 3x 4x / 3x	dielectric	
Trace Length/Skew			
Trace loss characteristic @ 2.5GHz	< 0.7	dB/in	The following max length is derived based on this characteristic. See Note 1.
Breakout region Max trace delay	11	mm	Minimum width and spacing
Max trace length/delay	152.3 (1014)	mm (ps)	
Max PCB via distance/delay from pin	6.29 (41.9)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Differential pair uncoupled length/delay	6.29 (41.9)	mm (ps)	
AC Cap			
Value	0.1	uF	Smallest size preferred (i.e. 0201). See note under USB Connection Diagrams for details on when AC capacitors are required
Location (max distance to adjacent discontinuities)	8 (53.22)	mm (ps)	The AC cap location should be located as close as possible to nearby discontinuities
Via			
via structure	Y-pattern is strongly recommended (keep symmetry)		Xtalk suppression is best when using Y-pattern. Can also reduce the limit of pair-pair distance. See figure 3.
GND via	- Place **GND** via as symmetrically as possible to the data pair vias. - Up to 4 signal vias (2 diff pairs) can share a single **GND** return via"		**GND** via is used to maintain return path, while its Xtalk suppression is limited.

AC cap pad voiding	GND (or PWR) void under / above the cap is preferred		Voiding is required if cap size is 0603 or large.
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check).
ESD			
Preferred device			Type: Texas Instruments TPD4I05U06. Optional. Place ESD component near connector
Max junction capacitance (IO to GND)	0.8	pF	
Location (max distance to connector)	8 (53)	mm (ps)	
Layout recommendations			See USB 3.0 Guideline Figure 4
Common-mode choke (not recommended – only used if absolutely required for EMI issues) See Appendix A for details on CMC if implemented.			
Component Order			
Component order			Chip – AC capacitor (TX only) – common mode choke – ESD – Connector: See USB 3.0 Guideline Figure 5.
General: See Appendix A for guidelines related to serpentine routing, routing over voids and noise coupling			

Note:
1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. Recommend trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
3. Place **GND** vias as symmetrically as possible to data pair vias.

Table 11. USB 3.0 Interface Signal Routing Requirements Figures

Figure 1: IL/NEXT plot

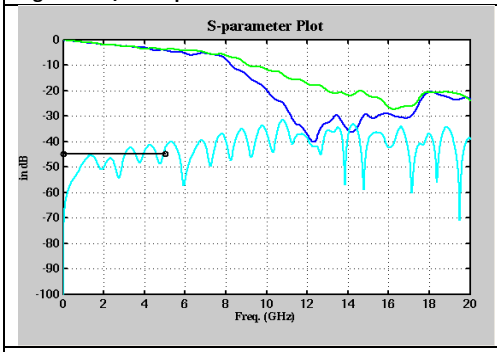


Figure 3: Via structure

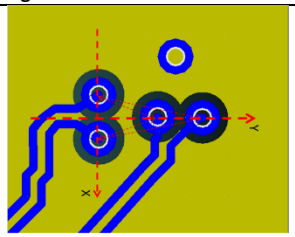


Figure 2: Trace spacing – for TX/RX non-interleaving

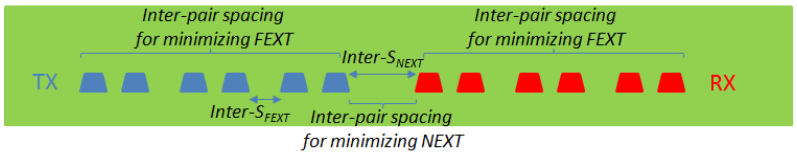


Figure 4: ESD Layout recommendations

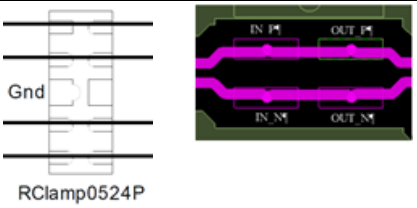
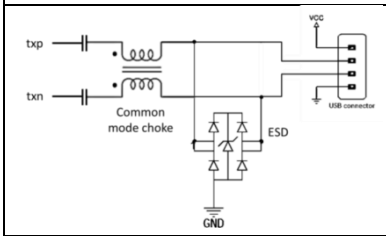


Figure 5: Component order



Common USB Routing Guidelines

Guideline
If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs/flexes must be used for the max trace and skew calculations.
Keep critical USB related traces away from other signal traces or unrelated power traces/areas or power supply components

Table 12. Tegra USB 2.0 Signal Connections

Jetson Nano Ball Name	Type	Termination	Description
USB[2:0]_D_P **USB[2:0]_D_N**	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	**USB Differential Data Pair:** Connect to USB connector, Mini-Card socket, hub or another device on the PCB.

Table 13. Miscellaneous USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
GPIO00	A	5V to 1.8V level shifter	**USB0 VBUS Enable:** Connect to VBUS pin of USB connector receiving USB0_+/– interface through level shifter. Also connects to VBUS power supply if host mode supported.

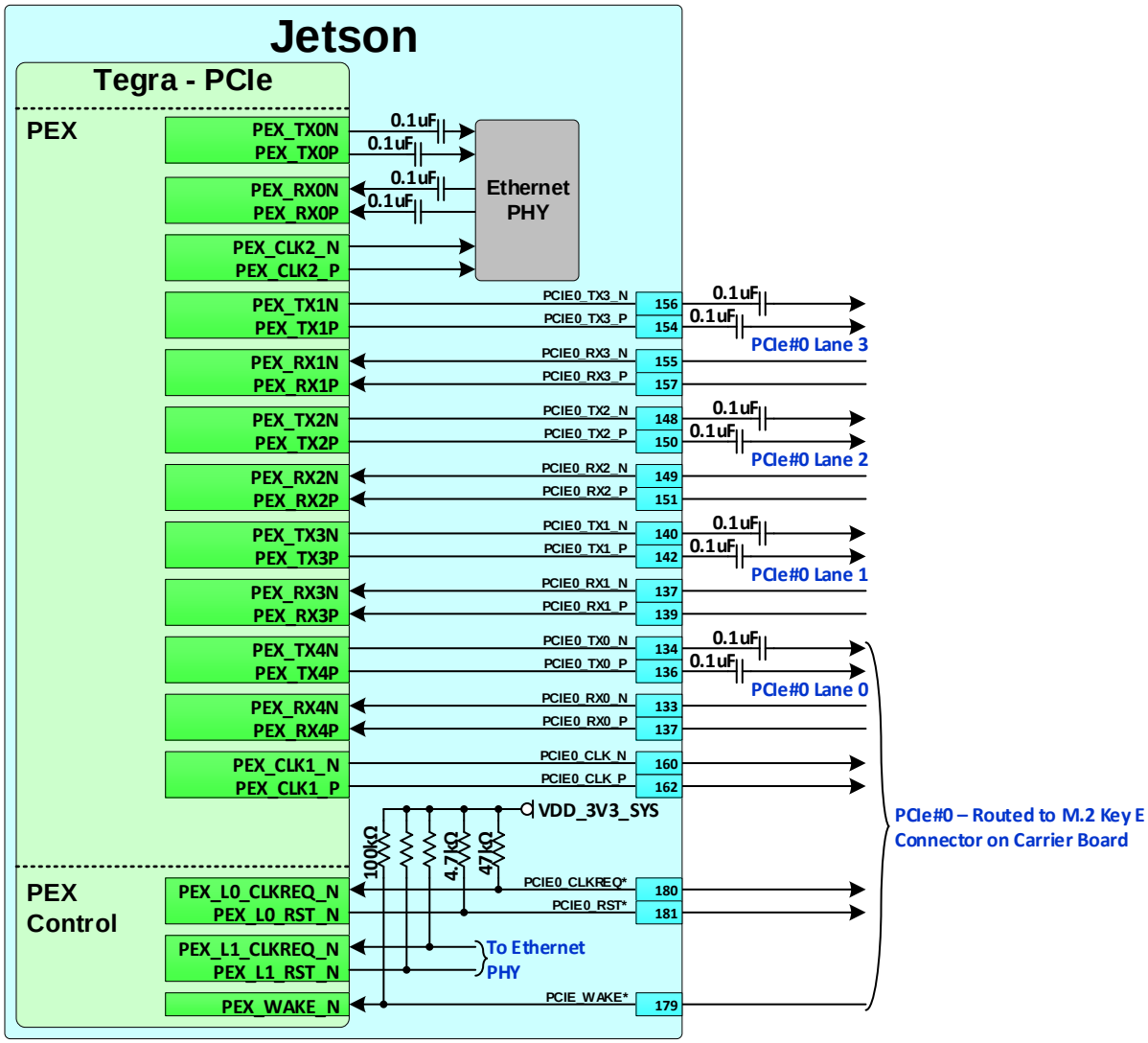
Table 14. Tegra USB 3.0 Signal Connections

Module Pin Name		Type	Termination	Description
USBSS_TX_N/P	**(USB 3.0 Port #0)**	DIFF Out	Series 0.1uF caps. ESD Protection near connector if required.	**USB 3.0 Differential Transmit Data Pairs:** Connect to USB 3.0 connectors, hubs or other devices on the PCB.
USBSS_RX_N/P	**(USB 3.0 Port #0)**	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. ESD protection near connector if required.	**USB 3.0 Differential Receive Data Pairs:** Connect to USB 3.0 connectors, hubs or other devices on the PCB.

4.2 PCIe

Tegra contains a PCIe controller that brings one interface up to four lanes to the module pins for use on the carrier board. A second single-lane PCIe interface is used on-module for Ethernet.

Figure 8. Example PCIe Connections



PCIE Design Guidelines

Table 15. PCIe Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data rate / UI period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Configuration / device organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance diff / SE	85 / 50	Ω	±15%. See note 1
Reference plane	**GND**		
Spacing			
Trace Spacing (Stripline/Microstrip) pair – pair To plane and capacitor pad To unrelated high-speed signals	3x / 4x 3x / 4x 3x / 4x	Dielectric	
Length/Skew			
Trace loss characteristic @ 2.5GHz	< 0.7	dB/in	The following max length is derived based on this characteristic. See note 3
Breakout region (max length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length/delay	5.5 (880)	in (ps)	
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of vias PTH vias Micro-vias	2 for TX traces and 2 for RX trace No requirement		
Max via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		
AC Cap			
Value Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		See PCIe Guideline Figure 3
General: See Appendix A for guidelines related to serpentine routing, routing over voids and noise coupling			

Note:
1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
4. Do length matching before via transitions to different layers or any discontinuity to minimize common mode conversion.

Table 16. PCIe Interface Signal Routing Requirements Figure

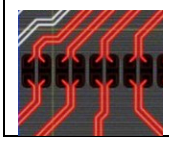
Figure 1: AC Cap Voiding


Table 17. PCIe Signal Connections

Module Pin Name	Type	Termination	Description
PCIe Interface #0 (x4)			
PCIE0_TX3_N/P (Lane 3) **PCIE0_TX2_N/P (Lane 2)** **PCIE0_TX1_N/P (Lane 1)** **PCIE0_TX0_N/P (Lane 0)**	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_N/P** pins of PCIe connector or **RX_N/P** pin of PCIe device through AC cap according to supported configuration.
PCIE0_RX3_N/P (Lane 3) **PCIE0_RX2_N/P (Lane 2)** **PCIE0_RX1_N/P (Lane 1)** **PCIE0_RX0_N/P (Lane 0)**	DIFF IN	Series 0.1uF capacitors near Jetson Nano pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_N/P** pins of PCIe connector or **TX_N/P** pin of PCIe device through AC cap according to supported configuration.
PCIE0_CLK_N/P	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_N/P** pins of PCIe device/connector
PCIE0_CLKREQ*	I/O	47kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Clock Request for PCIE0_CLK:** Connect to **CLKREQ** pins on device/connector(s)
PCIE0_RST*	O	4.7kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Reset:** Connect to **PERST** pins on device/connector(s)
PCIE_WAKE*	I	100kΩ pull-up to **VDD_3V3_SYS** on module	**PCIe Wake:** Connect to **WAKE** pins on device or connector

4.3 Gigabit Ethernet

Jetson Nano integrates a Realtek RTL9119I Gigabit Ethernet controller. The magnetics and RJ45 connector would be implemented on the carrier board. Contact Realtek for carrier board placement/routing guidelines.

Table 18. Jetson Nano Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)	LAN	Output	
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output	
184	GBE_MDI0_N	–	GbE Transformer Data 0		Bidir	MDI
186	GBE_MDI0_P	–				
190	GBE_MDI1_N	–	GbE Transformer Data 1			
192	GBE_MDI1_P	–				
196	GBE_MDI2_N	–	GbE Transformer Data 2			
198	GBE_MDI2_P	–				
202	GBE_MDI3_N	–	GbE Transformer Data 3			
204	GBE_MDI3_P	–				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 9. Jetson Nano Ethernet Connections

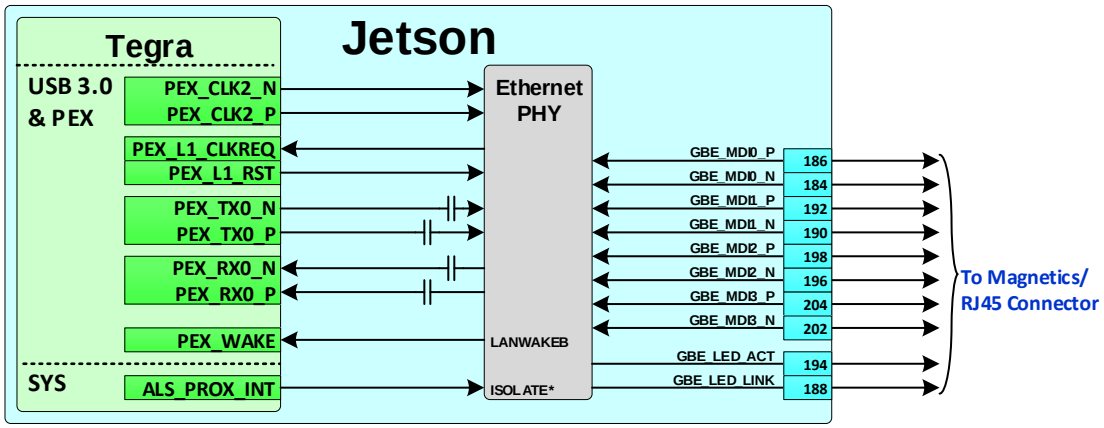


Figure 10. Gigabit Ethernet Magnetics and RJ45 Connections

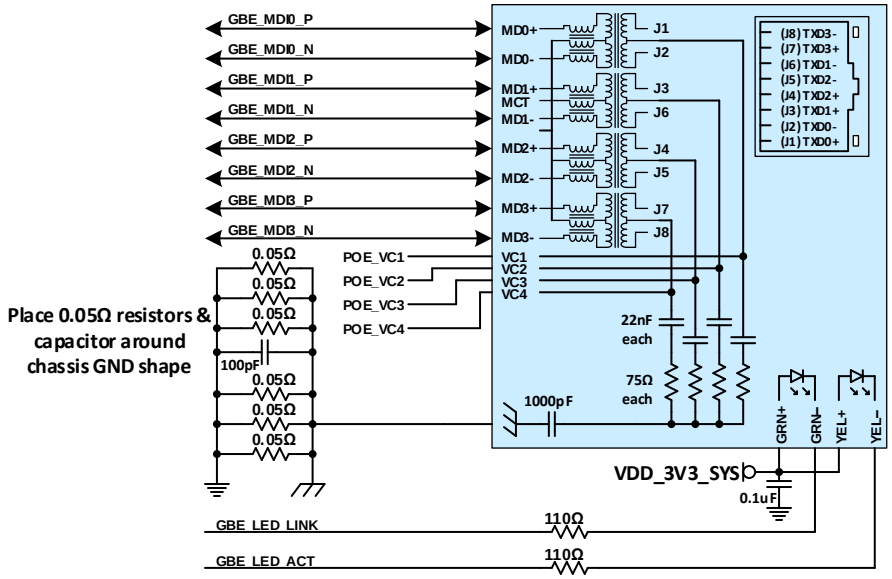


Table 19. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	**GND**		
Trace impedance Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)	0.763	mm	
Max trace length/delay	109 (690)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Number of vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Table 20. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
GBE_MDI[3:0]_N/P	DIFF I/O		**Gigabit Ethernet MDI IF Pairs:** Connect to Magnetics -/+ pins
GBE_LED_LINK	O	110Ω series resistor	**Gigabit Ethernet Link LED:** Connect to green LED on RJ45 connector
GBE_LED_ACT	O	110Ω series resistor	**Gigabit Ethernet Activity LED:** Connect to yellow LED on RJ45 connector

5.0 DISPLAY

Tegra X1 Embedded designs can select from several display options including MIPI DSI and eDP for embedded displays, and HDMI or DP for external displays. The maximum number of simultaneous displays supported by Jetson Nano is two.

Table 21. Jetson Nano Display General Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
206	GPIO07	LCD_BL_PWM	GPIO or Pulse Width Modulation signal	Expansion header	Output	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

5.1 MIPI DSI

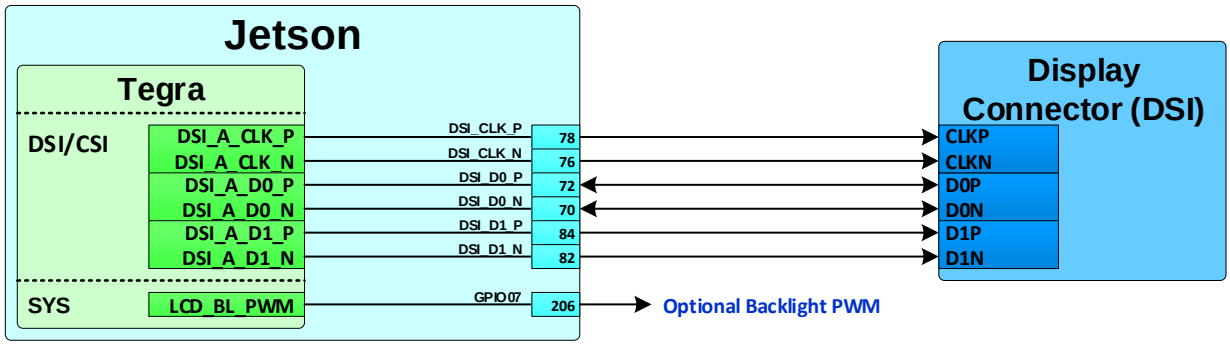
Tegra supports two total MIPI DSI data lanes and a single clock lane. Each data lane has a peak bandwidth up to 1.5Gbps.

Table 22. Jetson Nano DSI Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
76	DSI_CLK_N	DSI_A_CLK_N	Display, DSI clock	Not assigned	Output	MIPI D-PHY
78	DSI_CLK_P	DSI_A_CLK_P				
70	DSI_D0_N	DSI_A_D0_N	Display, DSI data lane 0		Bidir	
72	DSI_D0_P	DSI_A_D0_P				
82	DSI_D1_N	DSI_A_D1_N	Display, DSI data lane 1		Output	
84	DSI_D1_P	DSI_A_D1_P				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 11: DSI 1 x 2-Lane Connection Example



Note: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

MIPI DSI / CSI Design Guidelines

Table 23. MIPI DSI and CSI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency/data rate (per data lane)		750 / 1500	MHz/Mbps	
Number of loads		1	load	
Reference plane		**GND**		
Trace impedance	Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)		< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing		0.15mm	mm	Can be adjusted to meet Differential Impedance. Loosely Coupled Diff. Pair recommended by Spec.
Inter-pair trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Max PCB breakout length		5	mm	
Max trace delay	1 Gbps 1.5 Gbps	1100 800	ps	
Max intra-pair skew		1	ps	
Max trace delay skew between **DQ** and **CLK**		5	ps	**DQ** includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components				

MIPI DSI / CSI Connection Guidelines

Table 24. MIPI DSI Signal Connections

Module Pin Name	Type	Termination	Description
DSI_CLK_N/P	DIFF OUT		**DSI Differential Clock:** Connect to **CLKn and CLKp** pins of the primary DSI display
DSI_D[1:0]_N/P	DIFF OUT		**DSI Differential Data Lanes 1:0:** Connect to corresponding data lanes of DSI display.
GPIO07	O		**Optional LCD Backlight Pulse Width Modulation:** Connect to LCD backlight solution PWM input if supported

5.2 eDP / DP

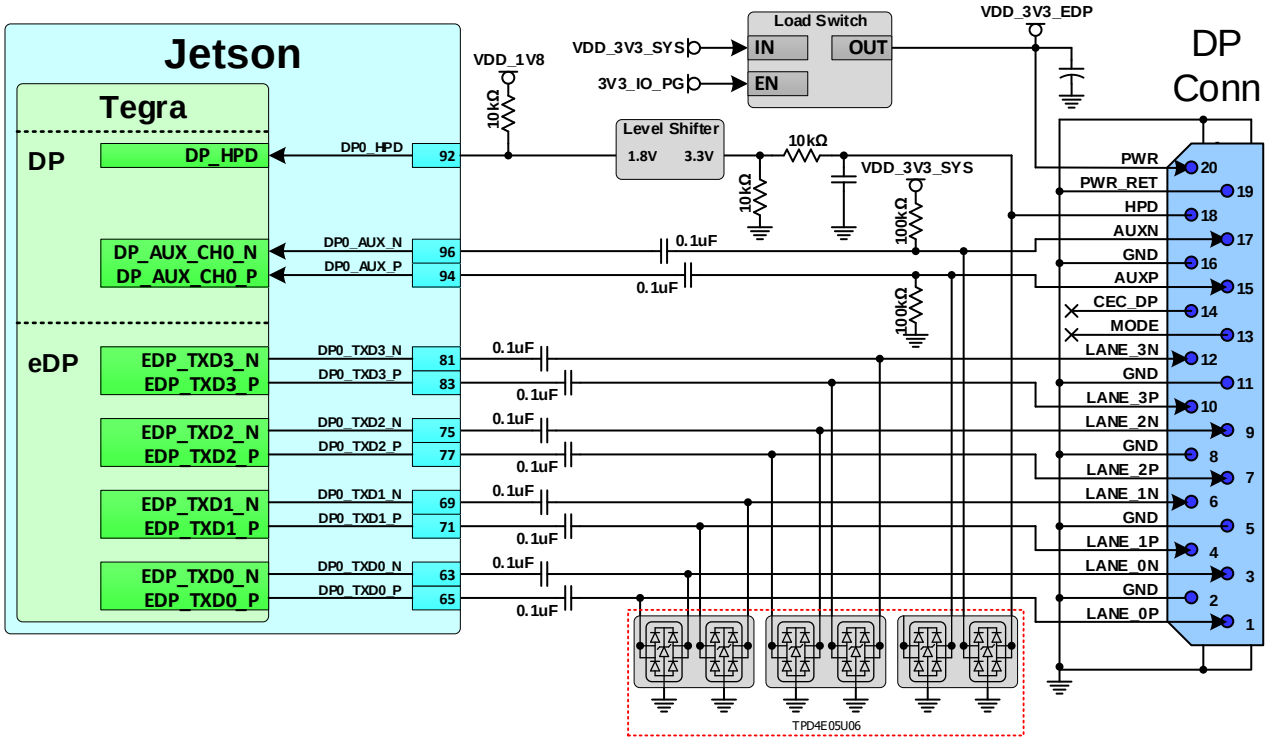
Table 25. Jetson Nano eDP / DP Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
90	DP0_AUX_N	DP_AUX_CH0_N	Display Port 0 auxiliary channel	DP connector	Bidir	AC-Coupled on Carrier Board (eDP/DP)
92	DP0_AUX_P	DP_AUX_CH0_P				
39	DP0_TXD0_N	EDP_TXDN0	Display port 0 data lane 0		Output	AC-Coupled on carrier board
41	DP0_TXD0_P	EDP_TXDP0				
45	DP0_TXD1_N	EDP_TXDN1	Display port 0 data lane 1			
47	DP0_TXD1_P	EDP_TXDP1				
51	DP0_TXD2_N	EDP_TXDN2	Display port 0 data lane 2			
53	DP0_TXD2_P	EDP_TXDP2				
57	DP0_TXD3_N	EDP_TXDN3	Display port 0 data lane 3			
59	DP0_TXD3_P	EDP_TXDP3				
88	DP0_HPD	DP_HPD0	Display port 0 hot-plug detect		Input	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Tegra supports an eDP interface. The eDP interface can also be used for DP. DP support on these pins does not include HDCP or Audio.

Figure 12: DP/eDP Connection Example (on DP0 pins)



Note:
- Level shifter required on DP0_HPD to avoid the pin from being driven when Jetson Nano is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
- Load Switch enable is from powergood pin of main 3.3V supply.
- If eDP interface used for DP, note that HDCP is not supported.

eDP Routing Guidelines

Figure 13: eDP (Differential Main Link) Topology

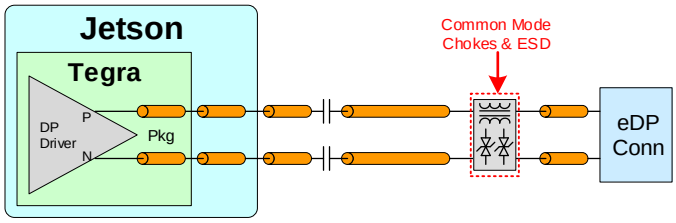


Table 26. eDP/DP Main Link Signal Routing Requirements (Including DP_AUX)

Parameter		Requirement	Units	Notes
Specification				
Max data rate / Min UI	**RBR**	1.62 / 617	Gbps / ps	Per data lane
	HBR	2.7 / 370		
	HBR2	5.4 / 185		
Number of loads / topology		1	load	Point-Point, differential, unidirectional
Termination		100	Ω	On die at TX/RX
Electrical Spec				
IL	**RBR**	0.7	dB @ 0.81GHz	
	HBR	1.2	dB @ 1.35GHz	
	HBR2	2.4	dB @ 2.7GHz	
Resonance dip frequency		>8	GHz	
TDR dip		>85	Ω	@ Tr-200ps (10%-90%)
FEXT		<= -40dB @ DC	See eDP/DP Guideline Figure 1	

Parameter		Requirement	Units	Notes
		<= -30dB @ 2.7GHz		
Impedance				
Trace impedance	Diff pair	90-100 85	Ω (±15%)	- 90Ω–100Ω is the spec. target. 85Ω is an implementation option (Zdiff does not account for trace coupling) - 85Ω is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference plane		**GND**		
Trace Length, Spacing and Skew				
Trace loss characteristic:		< 0.81	dB/in	@ 2.7GHz. The following max length is derived based on this characteristic. See note 2.
Max PCB via dist. from connector	**RBR/HBR** **HBR2**	No requirement 7.63 (0.3)	mm (in)	
Max trace length/delay from Jetson Nano TX to connector **RBR/HBR** (Stripline / Microstrip) **HBR2** (Stripline) **HBR2** (Microstrip, 5x / 7x)		 215 (1138)/215 (975) 102 (700) 89 (525) / 102 (600)	 mm (ps)	175ps/inch assumption for stripline, 150ps/inch for microstrip.
Trace spacing (pair-pair)	Stripline Microstrip (**HBR/RBR**) Microstrip (**HBR2**)	3x 4x 5x to 7x	dielectric	
Trace spacing (Main link to AUX)	Stripline/Microstrip	3x / 5x	dielectric	
Max intra-pair (within pair) skew		0.15 (1)	mm (ps)	See note 2
Maxinter-pair (pair-pair) skew		150	ps	See note 3
Via				
Max **GND** transition via distance		< 1x	diff pair pitch	For signals switching reference layers, add symmetrical **GND** stitching via near signal vias.
Via Structure				
Impedance dip Recommended via dimension for impedance control	Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	The via dimension is required for HDMI-DP co-layout.
Topology		- Y-pattern is recommended - keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See eDP/DP guideline figure 2
		For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2mm center-center.		See eDP/DP guideline figure 3
GND via		Place **GND** via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain a return path, while its Xtalk suppression is limited.
Max # of vias	PTH vias Micro vias	2 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max via stub length		0.4	mm	
AC Cap				
Value		0.1	uF	Discrete 0402
Max distance from AC cap to connector	**RBR/HBR** **HBR2**	No requirement 0.5	 in	
Voiding	**RBR/HBR** **HBR2**	No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
Connector				
Voiding	**RBR/HBR** **HBR2**	No requirement Voiding required		**HBR2:** Standard DP connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad.
General: See Appendix A for guidelines related to Serpentine routing, routing over voids and noise coupling				

Notes:
1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
4. The average of the differential signals is used for length matching.

Table 27. eDP/DP Interface Signal Routing Requirements Figures

Figure 1: S-parameter

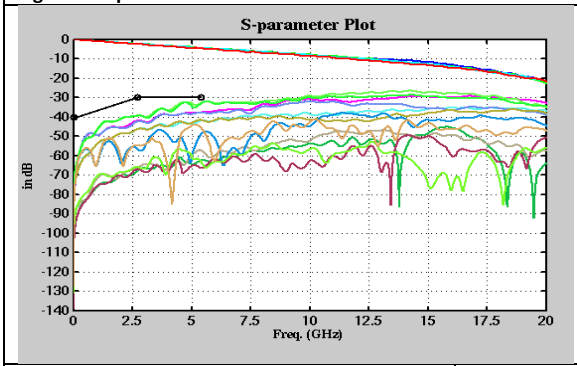


Figure 2: Via Topology #1

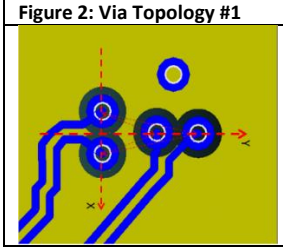


Figure 3: Via Topology #2

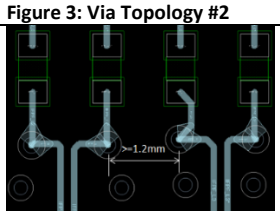


Table 28. eDP Signal Connections

Module Pin Name	Type	Termination	Description
DP0_TXD[3:0]_N/P	O	Series 0.1uF capacitors and ESD to **GND** on all.	**eDP/DP Differential CLK/Data Lanes:** Connect to matching pins on display connector.
DP0_AUX_N/P	I/OD	Series 0.1uF capacitors. 100kΩ pulldown on DP0_AUX_P and 100kΩ pull-up to VDD_3V3_SYS on DP0_AUX_N. ESD to **GND** on both.	**eDP/DP: Auxiliary Channels**: Connect to **AUX_CH**-/+ on display connector.
DP0_HPD	I	From module pin: 10kΩ pull-up to 1.8V, level shifter and 100kΩ pulldown on connector side of shifter and ESD to **GND**.	**eDP/DP: Hot Plug Detect**: Connect to **HPD** pin on display connector through level shifter.

5.3 HDMI / DP

A standard DP 1.2a or HDMI V2.0 interface is supported. These share the same set of interface pins, so either Display Port or HDMI can be supported natively.

Table 29. Jetson Nano HDMI / DP Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
98	DP1_AUX_N	DP_AUX_CH1_N	DisplayPort 1 Aux– or HDMI DDC SDA	HDMI Conn.	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
100	DP1_AUX_P	DP_AUX_CH1_P	DisplayPort 1 Aux+ or HDMI DDC SCL			
63	DP1_TXD0_N	HDMI_DP_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2		Output	AC-Coupled on carrier board
65	DP1_TXD0_P	HDMI_DP_TXDP0				
69	DP1_TXD1_N	HDMI_DP_TXDN1	DisplayPort or HDMI Lane 1			
71	DP1_TXD1_P	HDMI_DP_TXDP1				
75	DP1_TXD2_N	HDMI_DP_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0			
77	DP1_TXD2_P	HDMI_DP_TXDP2				
81	DP1_TXD3_N	HDMI_DP_TXDN3	DisplayPort 1 Lane 3– or HDMI Clk Lane			
83	DP1_TXD3_P	HDMI_DP_TXDP3				
96	DP1_TXD0_N	HDMI_INT_DP_HPD	HDMI or Display Port Hot Plug Detect		Input	CMOS – 1.8V
94	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 1.8V (3.3V tolerant)

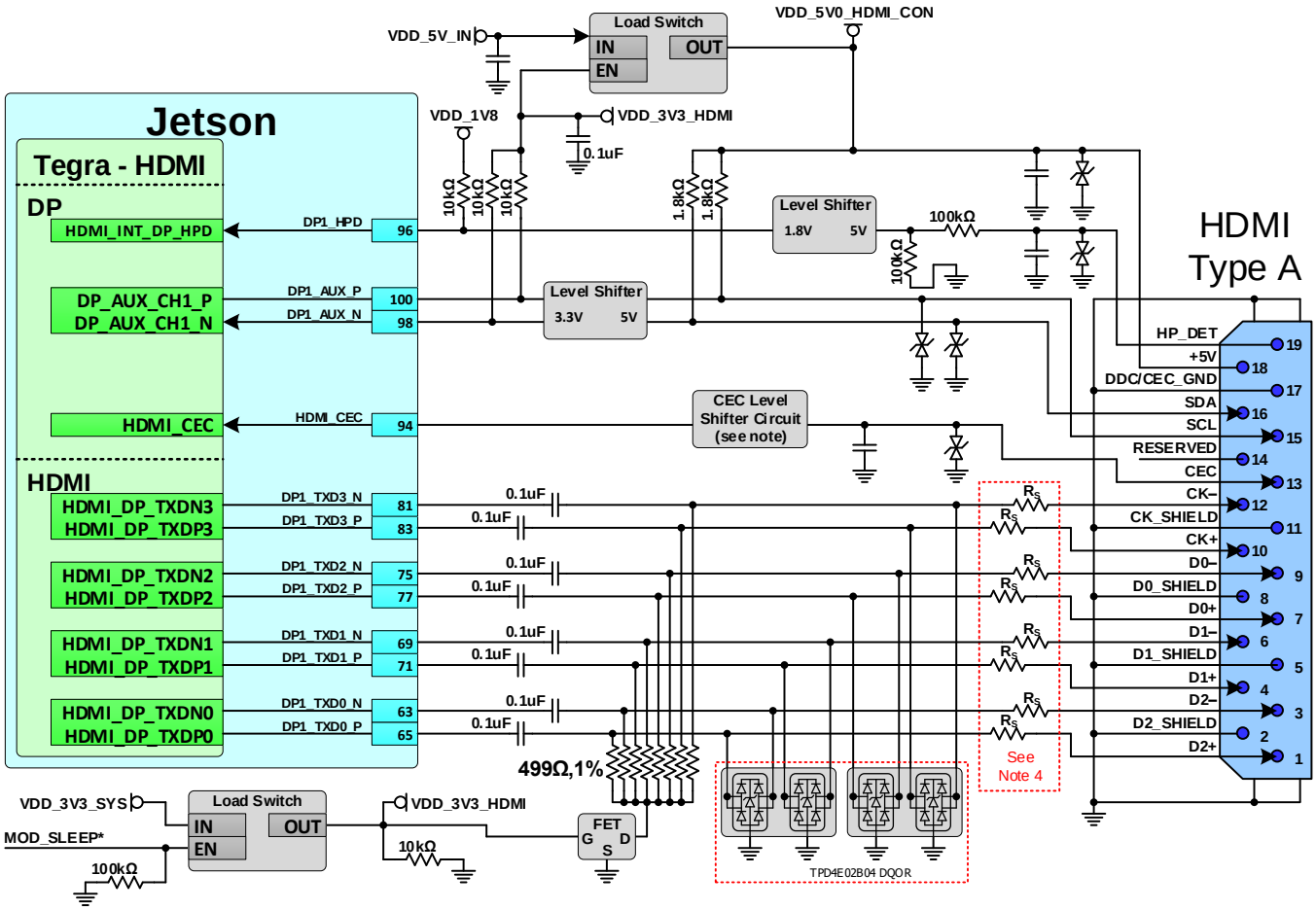
Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Table 30. DP/HDMI Pin Mapping

Module Pin Name	Module Pin #s	HDMI	DP
DP1_TXD3_P	**83**	**TXC+**	**TX3+**
DP1_TXD3_N	**81**	**TXC –**	**TX3–**
DP1_TXD2_P	**77**	**TX0+**	**TX2+**
DP1_TXD2_N	**75**	**TX0–**	**TX2–**
DP1_TXD1_P	**71**	**TX1+**	**TX1+**
DP1_TXD1_N	**69**	**TX1–**	**TX1–**
DP1_TXD0_P	**65**	**TX2+**	**TX0+**
DP1_TXD0_N	**63**	**TX2–**	**TX0–**

5.3.1 HDMI

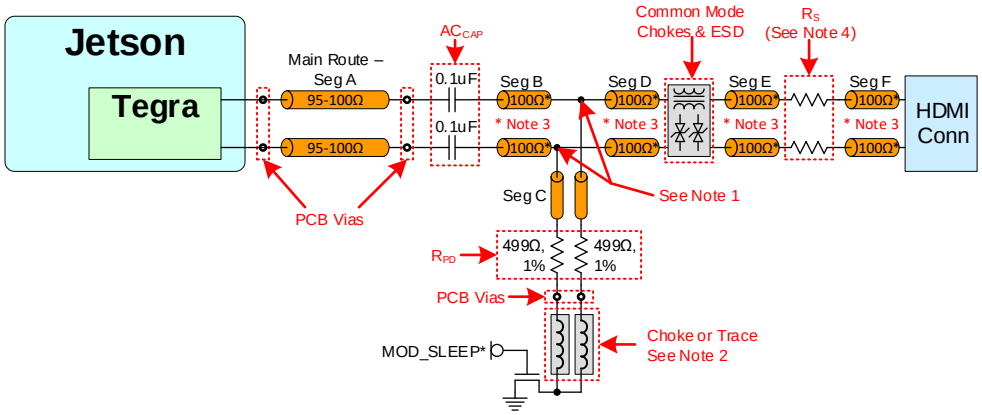
Figure 14: HDMI Connection Example



Note:

1. Level shifters required on DDC/HPD. Tegra pads are not 5V tolerant and cannot directly meet HDMI V_{IL}/V_{IH} requirements. HPD level shifter can be non-inverting or inverting. HPD level shifter on the Jetson Nano Developer Kit is inverting.
2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of the HDMI Interface Signal Routing Requirements table.
3. The DP1_TXx pads are native DP pads and require series AC capacitors (AC_{CAP}) and pull-downs (R_{PD}) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when Jetson Nano is off or in sleep mode to meet the HDMI V_{OFF} requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
4. Series resistors R_S are required. See the R_S section of the HDMI Interface Signal Routing Requirements table for details.
5. See reference design for CEC level shifting/blocking circuit.

Figure 15: HDMI Clk/Data Topology



Note:
1. R_{PD} pad must be on the main trace. R_{PD} and AC_{CAP} must be on same layer.
2. Chokes (600Ω@100MHz) or narrow traces (1uH@DC-100MHz) between pull-downs and FET are chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
3. The trace after the main-route via should be routed on the top or bottom layer of the PCB, and either with 100ohm differential impedance, or as uncoupled 50ohm SE traces.
4. R_S series resistor is required. See the R_S section of the HDMI Interface Signal Routing Requirements table for details.

Table 31. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, differential
Termination At receiver On-board	100 500	Ω	Differential To **3.3V** at receiver To **GND** near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs
	IL/FEXT plot: See HDMI Guideline Figure 1		TDR plot: See HDMI Guideline Figure 2
Impedance			
Trace impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	**GND**		
Trace spacing/Length/Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. See note 1.
Trace spacing (pair-pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	 3x 4x 5x to 7x	 dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing Stripline (Main link to DDC) Microstrip	3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max total length/delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	 mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).

Parameter	Requirement	Units	Notes
Max Total Length/Delay (Pre-1.4b) (up to 165Mhz) Microstrip Stripline	 254/10 (1500) 225/8.5 (1500)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max **GND** transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	- Y-pattern is recommended - keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See HDMI Guideline Figure 3
Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	 uM	
GND via	Place **GND** via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Max # of vias PTH via u-via	4 if all vias are PTH via Not limited as long as total channel loss meets IL spec.		
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main-route via dimensions should comply with the via structure rules (See via section)			See topology figure above this table
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main-route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top: See HDMI Guideline Figure 4		Bottom: See HDMI Guideline Figure 5
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-via design	Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		See HDMI Guideline Figure 6
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		Placement: See HDMI Guideline Figure 7
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between R_{PD} and FET choke Max trace Rdc Max trace length	600 or 1 ≤20 4	Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	**GND**/**PWR** void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) **See Appendix A for details on CMC if implemented.**			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR

Parameter	Requirement	Units	Notes
(IO to **GND**)			
Footprint	Pad right on the net instead of trace stub		See HDMI Guideline Figure 8
Location	After pull-down resistor/CMC and before R_S		
Void	**GND**/**PWR** void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		See HDMI Guideline Figure 9
Series Resistor (R_S) – Series resistor on N/P path for HDMI 2.0 (mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	**GND**/**PWR** void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		See HDMI Guideline Figure 10
Trace between components	Uncoupled structure		See HDMI Guideline Figure 11
HDMI connector			
Connector voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		See HDMI Guideline Figure 12
General: See Appendix A for guidelines related to Serpentine routing, routing over voids and noise coupling			

Note:
1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

Table 32. HDMI Interface Signal Routing Requirements Figures

Figure 1: IL/FEXT plot

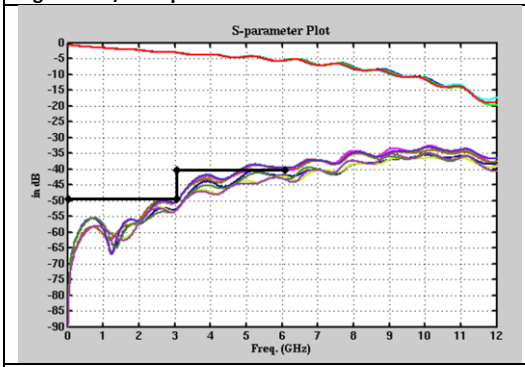


Figure 3: Via Topology

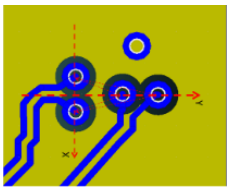


Figure 2: TDR plot

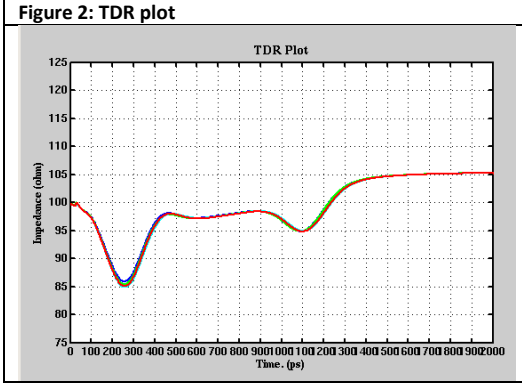


Figure 4: Add-on Components (Top)

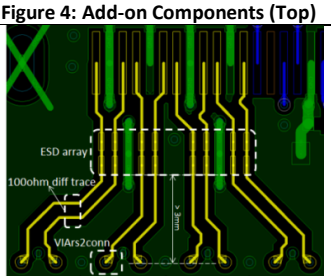


Figure 5: Add-on Components (Bottom)

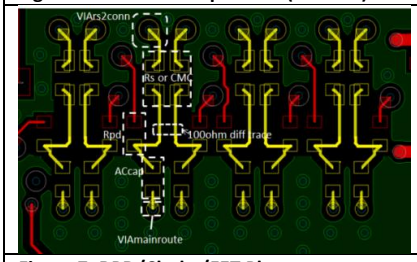
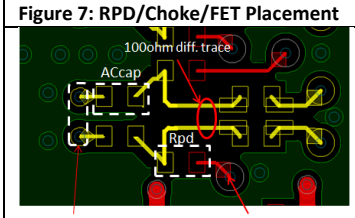


Figure 6: AC Cap Void

Figure 7: RPD/Choke/FET Placement



Main-route Via with short stub

PTH via to connect FET (and optional choke) on opposite side

Figure 8: ESD Footprint

Figure 9: ESD Void

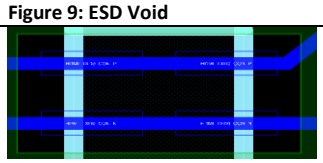


Figure 10: SMT Pad: Trace Entering

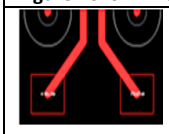


Figure 11: SMT Pad: Trace Between

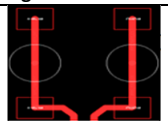


Figure 12: Connector Voiding

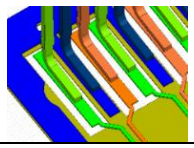


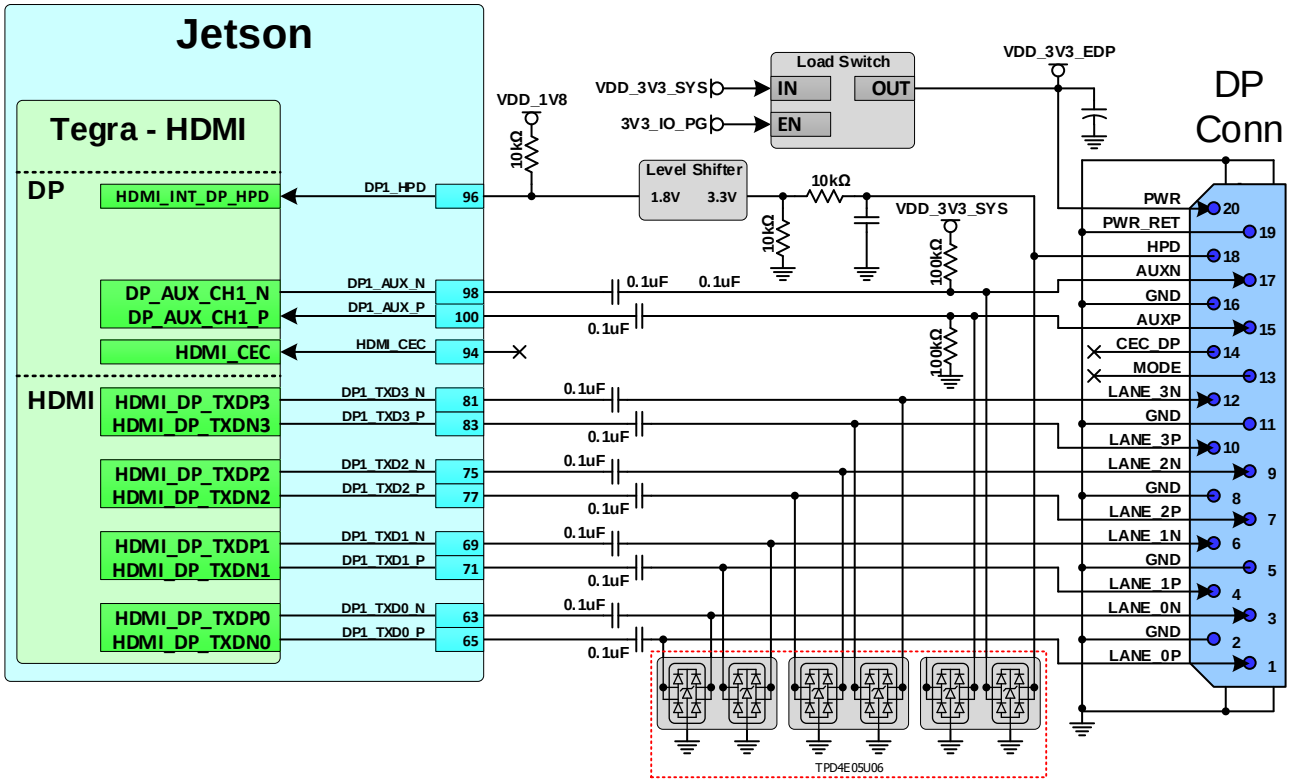
Table 33. HDMI Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DP1_TXD3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → ESD to **GND** →.≤6Ω R_S (series resistor)	**HDMI Differential Clock:** Connect to **C–/C+** and pins on HDMI connector
DP1_TXD[2:0]_N/P	DIFF OUT		**HDMI Differential Data:** Connect to HDMI Data pins (See DP/HDMI pin mapping table)
DP1_HPD	I	From module pin: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side → 100pF/12pF caps to **GND** → ESD to **GND**.	**HDMI Hot Plug Detect:** Connect to **HPD** pin on HDMI connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure for details.	**HDMI Consumer Electronics Control:** Connect to **CEC** on HDMI connector through circuitry.
DP1_AUX_N/P	I/OD	From module pins: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → ESD to **GND**	**HDMI: DDC Interface – Clock and Data**: Connect **DP1_AUX_N** to **SDA** and **DP1_AUX_P** to **SCL** on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector and ESD to **GND**.	**HDMI 5V supply to connector:** Connect to **+5V** on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

5.3.2 DP (on DP1 pins)

Figure 16: DP Connection Example



Note:
1. Level shifter required on DP1_HPD to avoid the pin from being driven when Jetson Nano is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
2. Any EMI/ESD included on the HDMI_DP pins must be suitable for the highest frequency modes supported (<1pf capacitive load recommended).

DP Interface Signal Routing Requirements

See eDP/DP Signal Routing Requirements.

Table 34. DP Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DP1_TXD3_N/P **DP1_TXD[2:0]_N/P**	O	Series 0.1uF capacitors → ESD on all.	**DP Differential Lanes:** Connect to **D[3:0] –/+.** See DP/HDMI pin mapping table for correct connections of data pins.
DP1_HPD	I	From Module pin: 10kΩ pull-up to 1.8V → level shifter and 100kΩ pulldown on connector side of shifter → ESD to **GND**.	**DP Interrupt (Hot Plug Detect):** Connect to **HPD** pin on DP connector w/termination described.
DP1_AUX_N/P	I/OD	From module pins: series 0.1uF caps → then 100KΩ PD on **AUX_P** and 100KΩ PU to 3.3V on **AUX_N** → ESD.	**DP: Auxiliary Channels**: Connect to **AUX_CH–/+** on DP connector
DP 3.3V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector.	**DP supply to connector:** Connect 3.3V supply pin on DP connector to **VDD_3V3_SYS**.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

6.0 MIPI CSI (VIDEO INPUT)

Jetson Nano brings twelve MIPI CSI lanes to the connector. Three quad-lane camera streams or two quad-lane plus two dual-lane camera streams or one quad-lane plus three dual-lane camera streams are supported. Each data lane has a peak bandwidth of up to 1.5Gbps.

Table 35. Jetson Nano CSI Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	Camera Connector	Input	MIPI D-PHY
12	CSI0_CLK_P	CSI_A_CLK_P				
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0			
6	CSI0_D0_P	CSI_A_D0_P				
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1			
18	CSI0_D1_P	CSI_A_D1_P				
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0	Not Assigned		
5	CSI1_D0_P	CSI_B_D0_P				
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1			
17	CSI1_D1_P	CSI_B_D1_P				
28	CSI2_CLK_N	CSI_E_CLK_N	Camera, CSI 2 Clock			
30	CSI2_CLK_P	CSI_E_CLK_P				
22	CSI2_D0_N	CSI_E_D0_N	Camera, CSI 2 Data 0			
24	CSI2_D0_P	CSI_E_D0_P				
34	CSI2_D1_N	CSI_E_D1_N	Camera, CSI 2 Data 1			
36	CSI2_D1_P	CSI_E_D1_P				
27	CSI3_CLK_N	CSI_F_CLK_N	Camera, CSI 3 Clock	Not Assigned		
29	CSI3_CLK_P	CSI_F_CLK_P				
21	CSI3_D0_N	CSI_F_D0_N	Camera, CSI 3 Data 0			
23	CSI3_D0_P	CSI_F_D0_P				
33	CSI3_D1_N	CSI_F_D1_N	Camera, CSI 3 Data 1			
35	CSI3_D1_P	CSI_F_D1_P				
52	CSI4_CLK_N	CSI_C_CLK_N	Camera, CSI 4 Clock			
54	CSI4_CLK_P	CSI_C_CLK_P				
46	CSI4_D0_N	CSI_C_D0_N	Camera, CSI 4 Data 0			
48	CSI4_D0_P	CSI_C_D0_P				
58	CSI4_D1_N	CSI_C_D1_N	Camera, CSI 4 Data 1			
60	CSI4_D1_P	CSI_C_D1_P				
40	CSI4_D2_N	CSI_D_D0_N	Camera, CSI 4 Data 2			
42	CSI4_D2_P	CSI_D_D0_P				
64	CSI4_D3_N	CSI_D_D1_N	Camera, CSI 4 Data 3			
66	CSI4_D3_P	CSI_D_D1_P				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Table 36. Jetson Nano Camera Miscellaneous Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Camera Connector	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.			
114	CAM0_PWDN	CAM1_PWDN	Camera 0 Powerdown or GPIO	Camera Connector	Output	CMOS – 1.8V
116	CAM0_MCLK	CAM1_MCLK	Camera 0 Reference Clock			
120	CAM1_PWDN	CAM2_PWDN	Camera 1 Powerdown or GPIO			
122	CAM1_MCLK	CAM2_MCLK	Camera 1 Reference Clock			

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 17: 4-Lane CSI Camera Connection Example

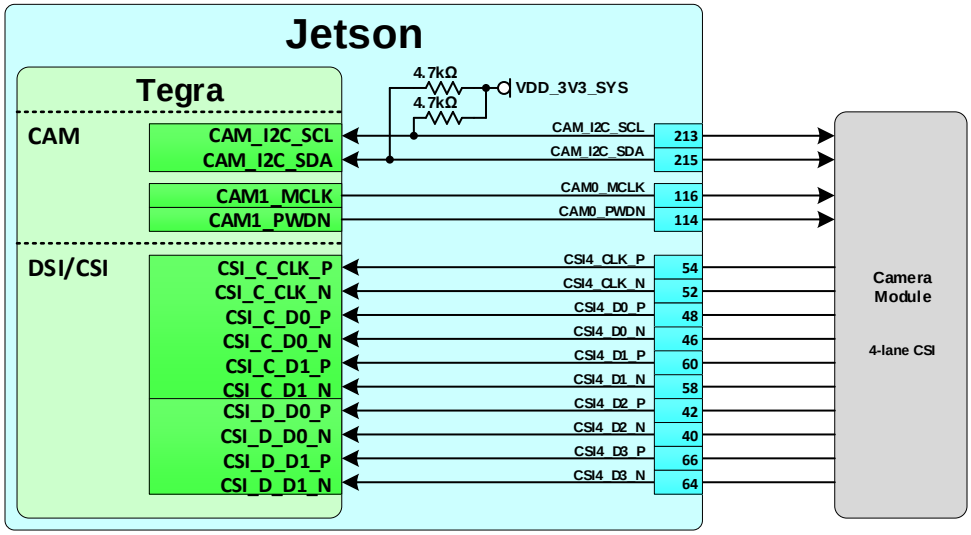
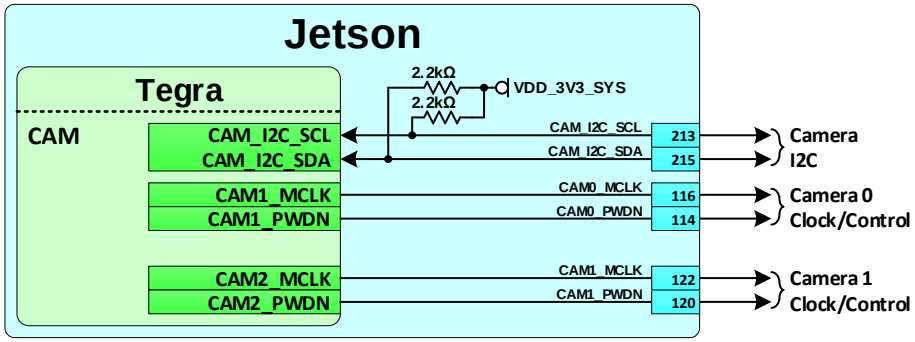


Table 37. CSI Configurations

Cameras	CSI_0 CLK/Data[1:0]	CSI_1 Data[1:0]	CSI_2 CLK/Data[1:0]	CSI_3 CLK	CSI_3 Data[1:0]	CSI_4 CLK/Data[1:0]
2-Lanes Each						
1 of 4 cameras	√					
2 of 4 cameras			√			
3 of 4 cameras				√	√	
4 of 4 cameras						√
4-Lanes Each						
1 of 3 cameras	√	√				
2 of 3 cameras			√		√	
3 of 3 cameras						√

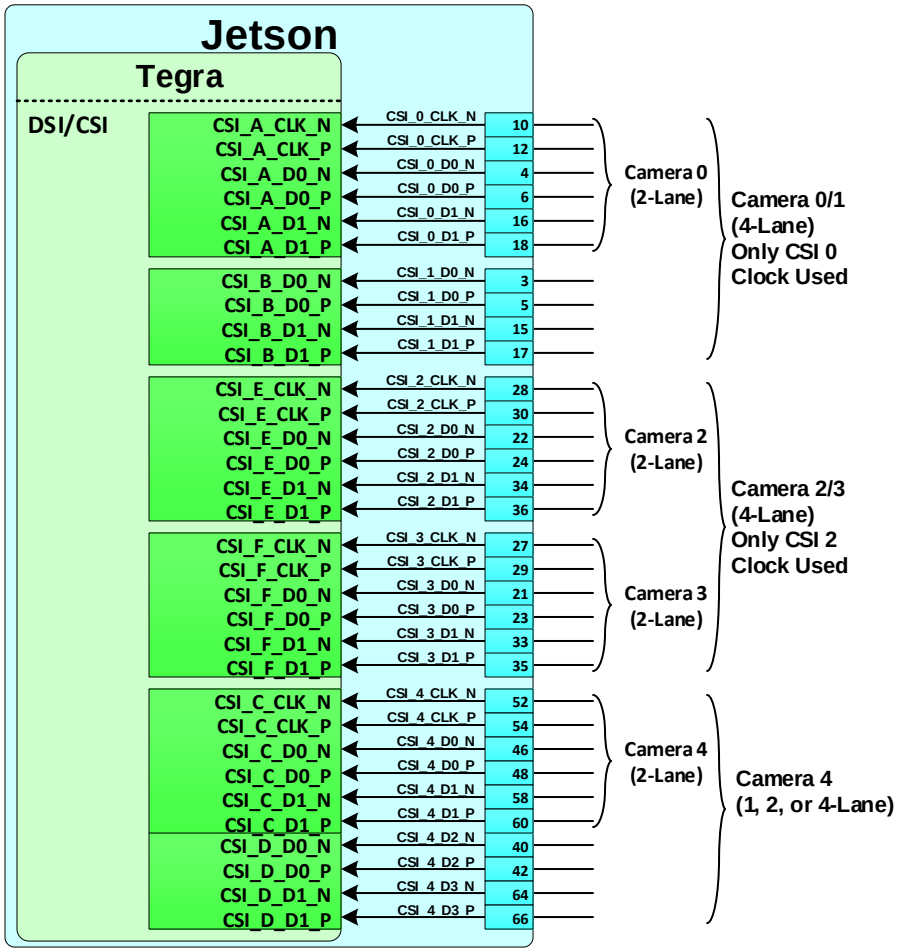
Note:
1. CSI 4 can be used as as a x1, x2, or x4 CSI interface.
2. If CSI 0/1 and CSI 4 are used for 4-lane interfaces each, CSI 2 and CSI 2 can be used for two 1 or 2-lane interfaces.
3. Each 2-lane options shown above can also be used for one single lane camera.

Figure 18: Available Camera Control Pins



Note: The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Figure 19: CSI Connection Options



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

CSI Design Guidelines

CSI and DSI use the MIPI D-PHY for the physical interface. The routing and connection requirements are found in the DSI section.

Table 38. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[4:2,0]_CLK_N/P	I	See note	**CSI Differential Clocks:** Connect to clock pins of camera. See the CSI Configurations table for details
CSI[3:0]_D[1:0]_N/P **CSI4_D[3:0]_N/P**	I/O	See note	**CSI Differential Data Lanes:** Connect to data pins of camera. See the CSI Configurations table for details

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.

Table 39. Miscellaneous Camera Connections

Module Pin Name	Type	Termination	Description
CAM_I2C_CLK **CAM_I2C_DAT**	O I/O	2.2kΩ pull-ups **VDD_3V3_SYS** (on Jetson Nano). See note related to EMI/ESD under MIPI CSI Signal Connections table.	**Camera I2C Interface:** Connect to I2C **SCL and SDA** pins of imager. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.
CAM[1:0]_MCLK	O	120Ω bead in series (on Jetson Nano) See note related to EMI/ESD under MIPI CSI Signal Connections table.	**Camera Master Clocks:** Connect to camera reference clock inputs.
CAM[1:0]_PWDN	O		**Camera Power Control signals (or GPIOs [1:0])**: Connect to power down pins on camera(s).

7.0 SD CARD / SDIO

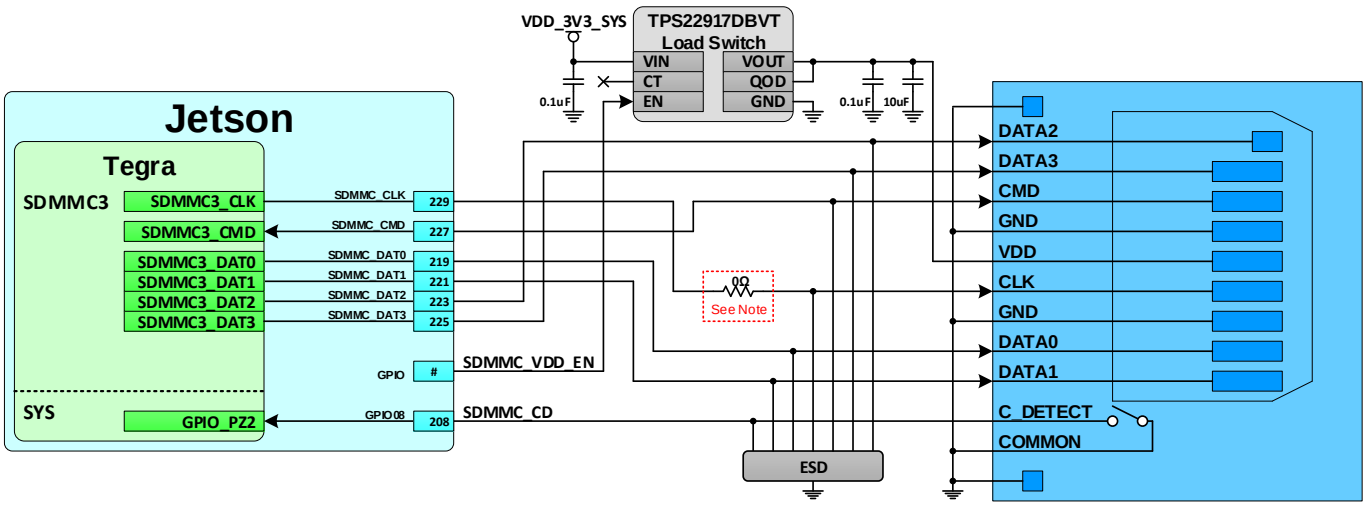
Jetson Nano uses one SDMMC interface for on-module eMMC (SDMMC4 on Tegra) and brings one to the connector pins for SD Card or SDIO use.

Table 40. Jetson Nano SDIO Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock	Not Assigned	Output	CMOS – 1.8V
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command		Bidir	
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0			
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1			
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2			
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3			
208	GPIO08	GPIO_PZ2	GPIO #8 or SD Card Detect	Fan	Input	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 20: SD Card Connection Example



Notes: Having 0Ω, 0402 resistor is recommended in case of issues with EMI where it can be replaced with an appropriate device.

Table 41. SD Card / SDIO Interface Signal Routing Requirements

Parameter			Requirement	Units	Notes
Max frequency	3.3V Signaling	DS	25 (12.5)	MHz (MB/s)	See note 1
		HS	50 (25)		
	1.8V Signaling	SDR12	25 (12.5)		
		SDR25	50 (25)		
		SDR50	100 (50)		
		SDR104	208 (104)		
		DDR50	50 (50)		
Topology			Point to point		
Reference plane			**GND** or **PWR**		See note 2
Trace impedance			50	Ω	±15%. 45Ω optional depending on stack-up
Max via count		PTH	4		Independent of stack-up layers.
		HDI	10		Depends on stack-up layers.
Via proximity (Signal to reference)			< 3.8 (24)	mm (ps)	Up to four signal vias can share 1 **GND** return via
Trace spacing		Microstrip / Stripline	4x / 3x	dielectric	
Trace length					

SDR50 / SDR25 / SDR12 / HS / DS	Min	16 (100)	mm (ps)	
	Max	139 (876)		
SDR104 / DDR50	Min	16 (100)		
	Max	83 (521)		
Max trace length/delay skew in/between **CLK** and **CMD**/**DAT**				See note 3
SDR50 / SDR25 / SDR12 / HS / DS		14 (87.5)	mm (ps)	
SDR104 / DDR50		2 (12.5)		
Keep CLK, CMD and DATA traces away from other signal traces or unrelated power traces/areas or power supply components				

Note:
1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current

Table 42. SD Card / SDIO Signal Connections

Function Signal Name	Type	Termination	Description
SDMMC_CLK	O		**SD Card / SDIO Clock:** Connect to **CLK** pin of device.
SDMMC_CMD	I/O		**SD Card / SDIO Command:** Connect to **CMD** pin of device
SDMMC_D[3:0]	I/O		**SD Card / SDIO Data:** Connect to **Data** pins of device
GPIO08	I		**SD Card Detect (Optional):** Connect to **CD** pin of SD Card socket.

8.0 AUDIO

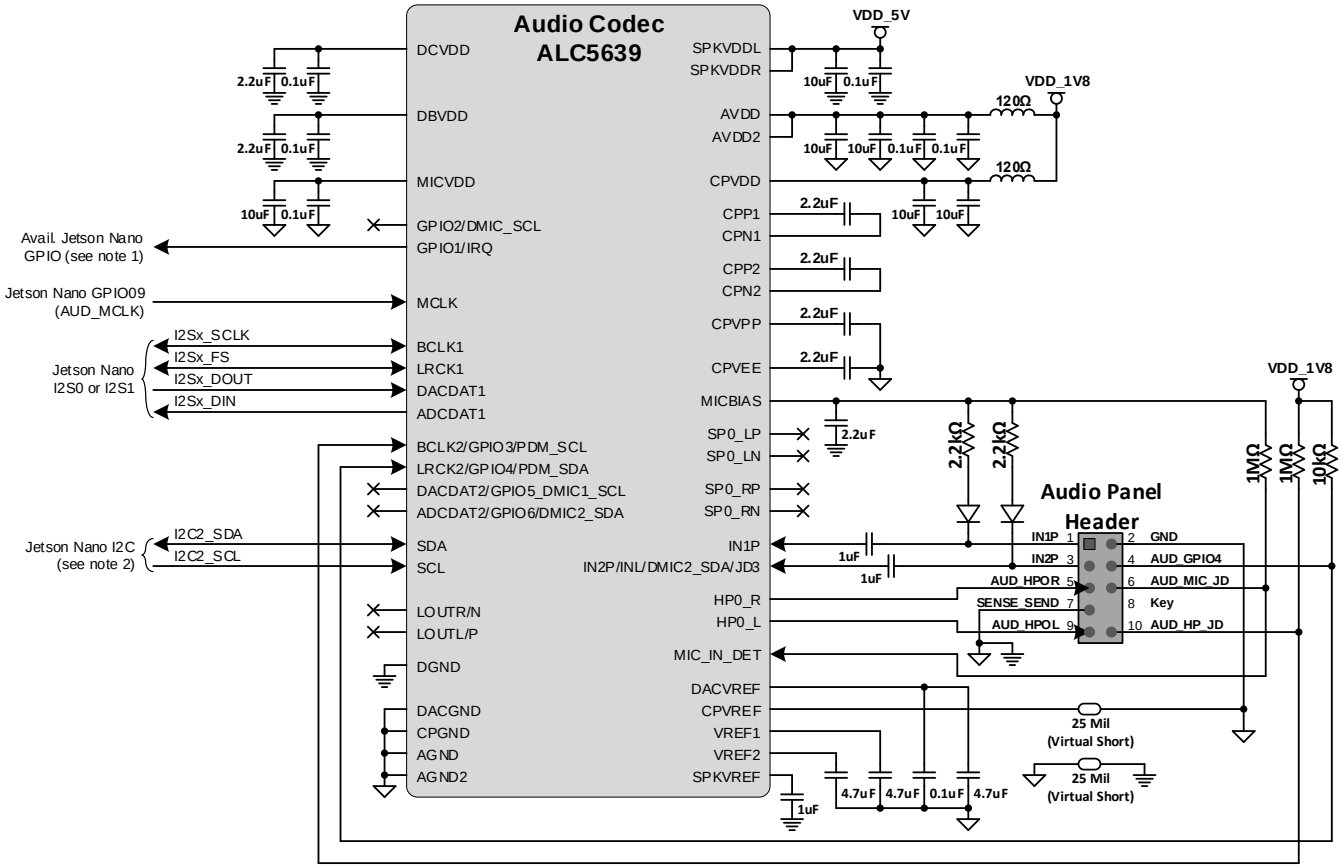
Tegra supports multiple PCM/I2S audio interfaces and includes a flexible audio-port switching architecture.

Table 43. Jetson Nano Audio Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
193	I2S0_DOUT	DAP4_DOUT	I2S Audio Port 0 Data Out	Expansion Header	Output	CMOS – 1.8V
195	I2S0_DIN	DAP4_DIN	I2S Audio Port 0 Data In		Input	CMOS – 1.8V
197	I2S0_FS	DAP4_FS	I2S Audio Port 0 Left/Right Clock		Bidir	CMOS – 1.8V
199	I2S0_SCLK	DAP4_SCLK	I2S Audio Port 0 Clock		Bidir	CMOS – 1.8V
220	I2S1_DOUT	DMIC2_CLK	I2S Audio Port 1 Data Out	M.2 Key E	Bidir	CMOS – 1.8V
222	I2S1_DIN	DMIC1_DAT	I2S Audio Port 1 Data In		Input	CMOS – 1.8V
224	I2S1_FS	DMIC1_CLK	I2S Audio Port 1 Left/Right Clock		Bidir	CMOS – 1.8V
226	I2S1_SCLK	DMIC2_DAT	I2S Audio Port 1 Clock		Bidir	CMOS – 1.8V
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Expansion Header	Output	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 21. Audio Codec Connection Example



Note:
1. The Interrupt pin from the audio codec can connect to any available Jetson Nano GPIO. If the pin must be wake-capable, choose one of the GPIOs that supports this function.
2. I2C2 supports 1.8V operation since the interface is pulled to 1.8V through 4.7kΩ resistors on the module. If another I2C interface on Jetson Nano is used, a level shifter will be required as all the others are 3.3V.

Table 44. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / device organization	1	load	
Max loading	8	pF	
Reference plane	**GND**		
Breakout region impedance	Min width/spacing		
Trace impedance	50	Ω	±20%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note 1
Trace spacing Microstrip or Stripline	2x	dielectric	
Max trace length/delay	~22 (3600)	In (ps)	See note 2
Max trace length/delay skew between **SCLK** and **SDATA_OUT/IN**	~1.6 (250)	In (ps)	See note 2

Note: Up to four signal vias can share a single **GND** return via

Table 45. Audio Signal Connections

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		**I2S Serial Clock:** Connect to I2S/PCM **CLK** pin of audio device.
I2S[1:0]_FS	I/O		**I2S Frame Select (Left/Right Clock):** Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		**I2S Data Output:** Connect to data input pin of audio device.
I2S[1:0]_DIN	I		**I2S Data Input:** Connect to data output pin of audio device.
GPIO09	O		**Audio Codec Master Clock:** Connect to clock pin of audio codec.

9.0 MISCELLANEOUS INTERFACES

9.1 I2C

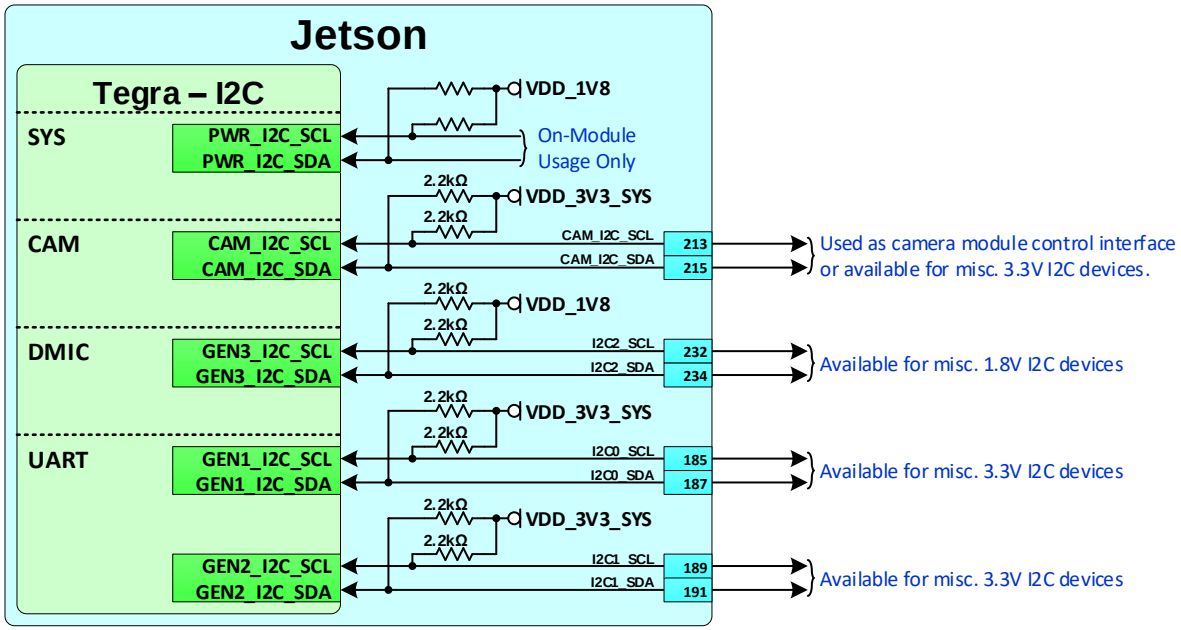
Jetson Nano brings four I2C interfaces to the connector pins. CAM_I2C is included in the camera pin description table earlier in this document. The assignments in the I2C Interface Mapping table should be used where applicable for the I2C interfaces

Table 46. Jetson Nano I2C Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
185	I2C0_SCL	GEN1_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (general)	Bidir	Open Drain – 3.3V
187	I2C0_SDA	GEN1_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
189	I2C1_SCL	GEN2_I2C_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
191	I2C1_SDA	GEN2_I2C_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
232	I2C2_SCL	GEN3_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V
234	I2C2_SDA	GEN3_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 22. I2C Connections



I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson Nano do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format). The I2C2 interface is connected to an EEPROM on the module which uses I2C address 7'h50. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Notes: The Jetson Nano I2C interfaces have 2.2kΩ pull-ups on the module. Pads for additional pull-ups are recommended in case a stronger pull-up is required due to additional loading on the interfaces.

Table 47. I2C Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency	Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology		Single ended, bi-directional, multiple masters/slaves		
Max loading	Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane		**GND** or **PWR**		
Trace impedance		50 – 60	Ω	±15%
Trace spacing		1x	dielectric	
Max trace length/delay	Standard Mode Fm, Fm+ Modes	3400 (~20) 1700 (~10)	ps (in)	

Note:
1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for **PWR** reference

Table 48. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C0_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Nano	**I2C #0 Clock and Data.** Connect to **CLK and Data** pins of any 3.3V devices
I2C1_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Nano	**I2C #1 Clock and Data.** Connect to **CLK and Data** pins of 3.3V devices.
I2C2_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_1V8** on Jetson Nano	**I2C #2 Clock and Data.** Connect to **CLK and Data** pins of any 1.8V devices
CAM_I2C_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Nano	**Camera I2C Clock and Data.** Connect to **CLK and Data** pins of any 3.3V devices

Note:
1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

9.2 SPI

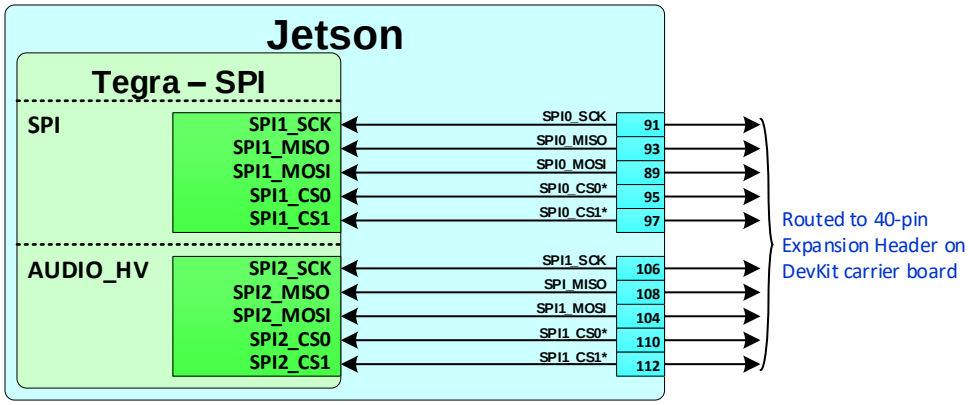
The Jetson Nano brings out two of the Tegra SPI interfaces. See the Figure below the Pin Descriptions table.

Table 49. Jetson Nano SPI Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
89	SPI0_MOSI	SPI1_MOSI	SPI 0 Master Out / Slave In	Expansion header	Bidir	CMOS – 1.8V
91	SPI0_SCK	SPI1_SCK	SPI 0 Clock			
93	SPI0_MISO	SPI1_MISO	SPI 0 Master In / Slave Out			
95	SPI0_CS0*	SPI1_CS0	SPI 0 Chip Select 0			
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1			
104	SPI1_MOSI	SPI2_MOSI	SPI 1 Master Out / Slave In			
106	SPI1_SCK	SPI2_SCK	SPI 1 Clock			
108	SPI1_MISO	SPI2_MISO	SPI 1 Master In / Slave Out			
110	SPI1_CS0*	SPI2_CS0	SPI 1 Chip Select 0			
112	SPI1_CS1*	SPI2_CS1	SPI 1 Chip Select 1			

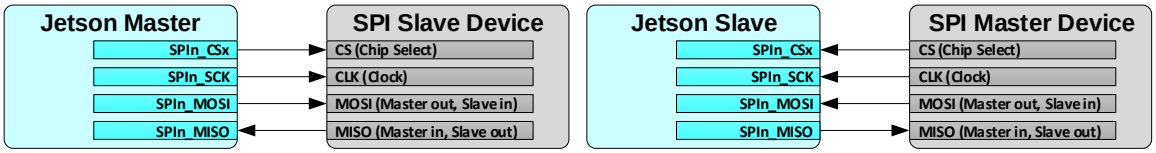
Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 23. SPI Connections



The figure below shows the basic connections used.

Figure 24. Basic SPI Master/Slave Connections



SPI Design Guidelines

Figure 25. SPI Topologies

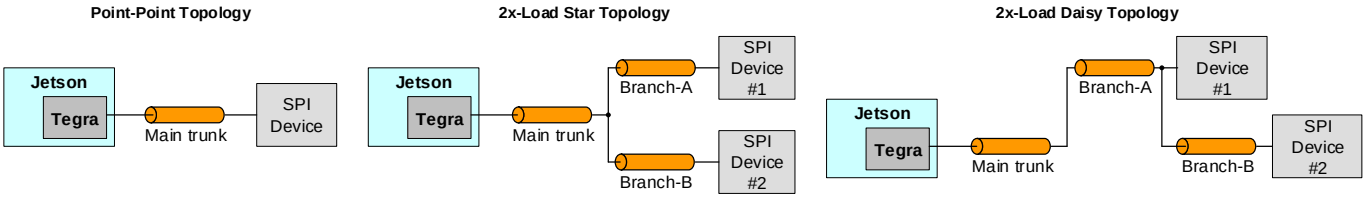


Table 50. SPI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max frequency		65	MHz	
Configuration / device organization		4	load	
Max loading (total of all loads)		15	pF	
Reference plane		**GND**		
Breakout region impedance		Minimum width and spacing		
Max PCB breakout delay		75	ps	
Trace impedance		50 – 60	Ω	±15%
Via proximity (signal to reference)		< 3.8 (24)	mm (ps)	See note 1
Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Max trace length/delay (PCB main trunk) For **MOSI, MISO, SCK** and **CS**	Point-point 2x-load star/daisy	195 (1228) 120 (756)	mm (ps)	
Max trace length/delay (Branch-A) for **MOSI, MISO, SCK** and **CS**	2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from **MOSI, MISO** and **CS** to **SCK**		16 (100)	mm (ps)	At any point

Note: Up to four signal vias can share a single **GND** return via

Table 51. SPI Signal Connections

Module Pin Names	Type	Termination	Description
SPI[1:0]_CLK	I/O		**SPI Clock.:** Connect to peripheral **CLK** pin(s)
SPI[1:0]_MOSI	I/O		**SPI Data Output:** Connect to slave peripheral **MOSI** pin(s)
SPI[1:0]_MISO	I/O		**SPI Data Input:** Connect to slave peripheral **MISO** pin(s)
SPI[1:0]_CS[1:0]*	I/O		**SPI Chip Selects.:** Connect one **CSx*** pin per SPI interface to each slave peripheral **CS** pin on the interface

9.3 UART

The Jetson Nano brings three UARTs out to the main connector. See figure below for typical assignments of the three available UARTs.

Table 52. Jetson Nano UART Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on DevKit Carrier Board	Direction	Pin Type
99	UART0_TXD	UART3_TXD	UART #0 Transmit	M.2 Key E	Output	CMOS – 1.8V
101	UART0_RXD	UART3_RXD	UART #0 Receive	M.2 Key E	Input	
103	UART0_RTS*	UART3_RTS	UART #0 Request to Send	M.2 Key E	Output	
105	UART0_CTS*	UART3_CTS	UART #0 Clear to Send	M.2 Key E	Input	
203	UART1_TXD	UART2_TXD	UART #1 Transmit	Expansion Header	Output	
205	UART1_RXD	UART2_RXD	UART #1 Receive	Expansion Header	Input	
207	UART1_RTS*	UART2_RTS	UART #1 Request to Send	Expansion Header	Output	
209	UART1_CTS*	UART2_CTS	UART #1 Clear to Send	Expansion Header	Input	
236	UART2_TXD	UART1_TXD	UART #2 Transmit.	Serial Port	Output	
238	UART2_RXD	UART1_RXD	UART #2 Receive	Serial Port	Input	

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 26. Jetson Nano UART Connections

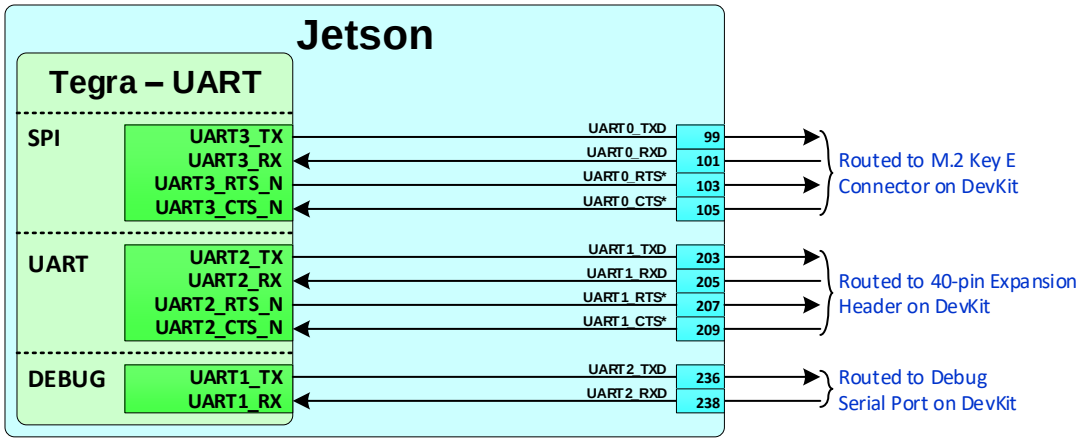


Table 53. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TXD	O		**UART Transmit:** Connect to peripheral **RXD** pin of device
UART[2:0]_RXD	I		**UART Receive:** Connect to peripheral **TXD** pin of device
UART[1:0]_CTS*	I		**UART Clear to Send:** Connect to peripheral **RTS** pin of device
UART[1:0]_RTS*	O		**UART Request to Send:** Connect to peripheral **CTS** pin of device

9.4 Fan

Jetson Nano provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins/functions can be found in the following locations:

Jetson Nano Module Pin Mux:

- This is used to configure GPIO14 (PWM) for FAN_PWM and GPIO08 (SDMMC_CD) for FAN_TACH. The pin used for FAN_PWM is configured as PM3_PWM3. The pin used for FAN_TACH is configured as a GPIO.

Tegra X1 (SoC) Technical Reference Manual (TRM):

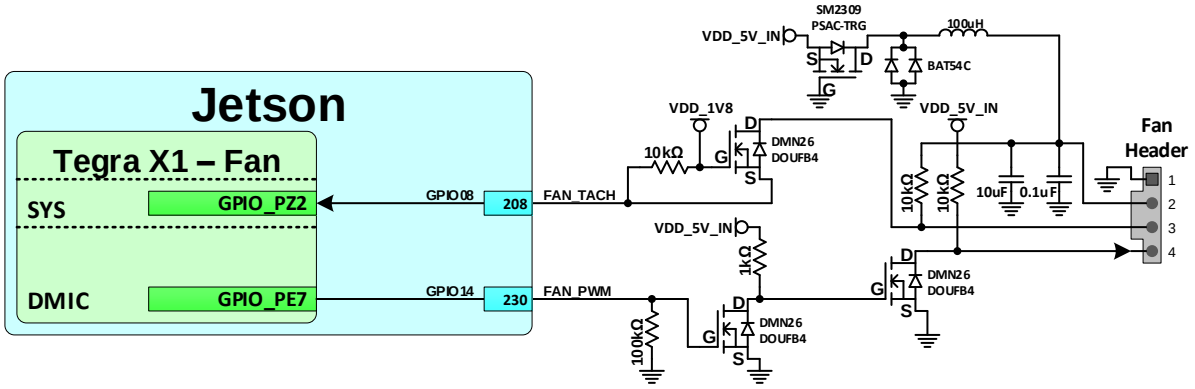
- Functional descriptions and related registers can be found in the TRM for the FAN_PWM (PWM chapter).

Table 54. Jetson Nano Fan Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on the Carrier Board	Direction	Pin Type
230	GPIO14	GPIO_PE7	Fan PWM	Fan	Output	CMOS – 1.8V
208	GPIO08	GPIO_PX2	Fan tachometer	Fan	Input	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 27. Jetson Nano Fan Connections



9.5 Debug

Jetson Nano supports JTAG and a UART for debugging purposes. JTAG is not brought to the module pins, however, but to test points on the module. The UART intended for debug is UART1 with is routed to a level shifter then to a 6-pin UART header on the Developer Kit Carrier Board.

Table 55. Jetson Nano JTAG and Debug UART Pin Descriptions

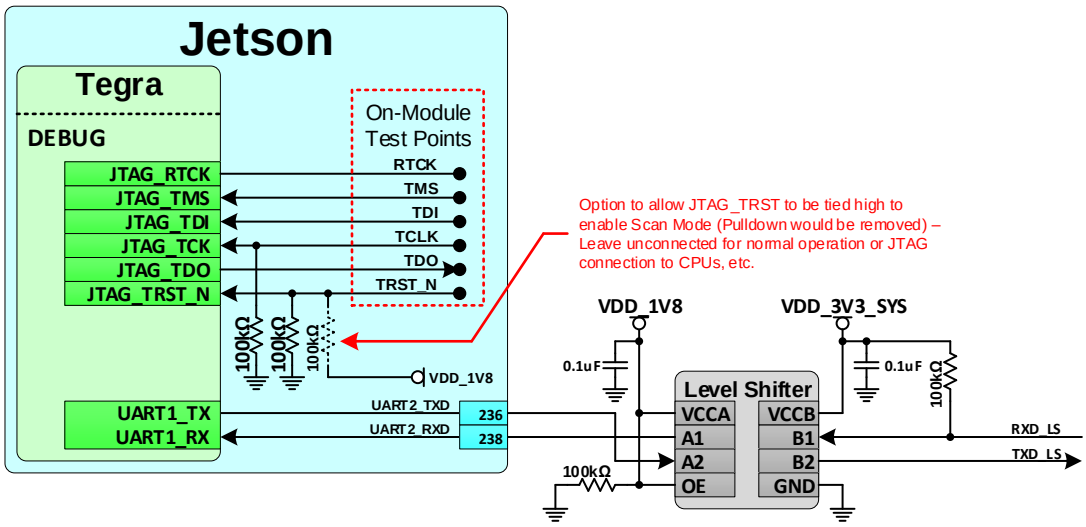
Pin #	Module Pin Name (see note)	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
	JTAG_GP0	JTAG_TRST_N	JTAG test reset	None – JTAG not brought to the module pins on Jetson Nano	Input	CMOS – 1.8V
	JTAG_RTCK	JTAG_RTCK	JTAG return clock		Input	CMOS – 1.8V
	JTAG_TCK	JTAG_TCK	JTAG test clock		Input	CMOS – 1.8V
	JTAG_TDI	JTAG_TDI	JTAG test data In		Input	CMOS – 1.8V
	JTAG_TDO	JTAG_TDO	JTAG test data Out		Output	CMOS – 1.8V
	JTAG_TMS	JTAG_TMS	JTAG test mode select		Input	CMOS – 1.8V
238	UART2_RXD	UART1_RX	UART 1 receive	Serial port	Input	CMOS – 1.8V
236	UART2_TXD	UART1_TX	UART 1 transmit		Output	

Notes:
- In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
- JTAG is brought to on-module test points only

9.5.1 JTAG

Jetson Nano provides access to JTAG via test points on the module.

Figure 28. JTAG and Debug UART Connections (Based on Jetson Nano DevKit Design)



Note:
1. Pull-ups or Pull-downs are present on the UART TX and RTS lines for RAM Code strapping.
2. If level shifter is implemented, pull-up is required on the RXD line on the non-Jetson Nano side of the level shifter. This is required to keep the input from floating and toggling when no device is connected to the debug UART.

Figure 29. JTAG Test Point Detail

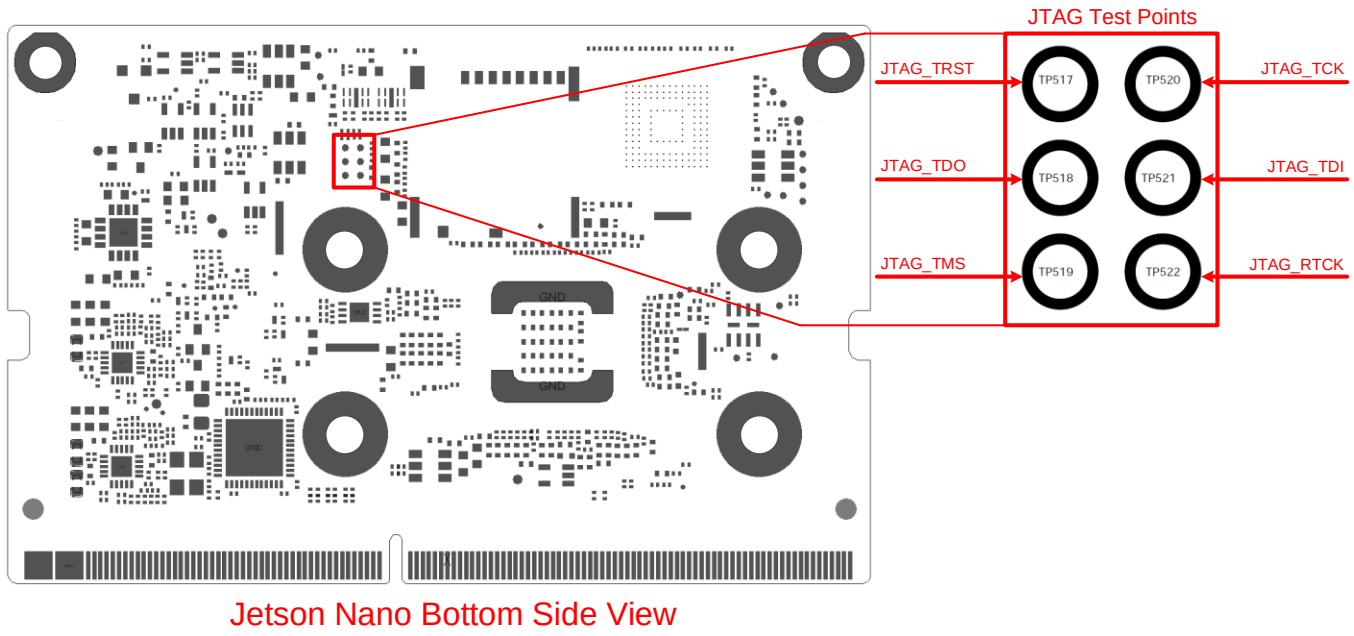


Table 56. JTAG Connections

Jetson Nano Test Point Signal Name (See note)	Type	Termination	Description
JTAG_TMS	I		**JTAG Mode Select:** Connect to **TMS** pin of connector
JTAG_TCK	I	100kΩ to **GND** (on module)	**JTAG Clock:** Connect to **TCK** pin of connector
JTAG_TDO	O		**JTAG Data Out:** Connect to **TDO** pin of connector
JTAG_TDI	I		**JTAG Data In:** Connect to **TDI** pin of connector
JTAG_RTCLK	I		**JTAG Return Clock:** Connect to **RTCK** pin of connector
JTAG_TRST_N	I	100kΩ to **GND** (on module)	**JTAG Test Reset:** This signal is used to select normal operation or scan test mode operation. - Normal operation: Leave pulldown resistor on module installed. - Boundary Scan test mode: Connect **JTAG_TRST_N** to **VDD_1V8** (install 100kΩ resistor to **VDD_1V8** and remove 100kΩ resistor to **GND** (see figure). Or, install strong enough resistor connected to **VDD_1V8** to overcome weak 100kΩ pulldown (1ΩΩ to 4.7kΩ.

9.5.2 Debug UART

The UART2 interface is intended to be used for debug purposes.

Table 57. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART2_TXD	O		**UART #2 Transmit:** Connect to **RX** pin of serial device
UART2_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Nano side of the device.	**UART #2 Receive:** Connect to **TX** pin of serial device

10.0 PADS

Note: Jetson Nano signals that come from Tegra X1 may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

10.1 Internal Pull-ups for Dual-Voltage Block Pins Powered @ 1.8V

Several of the MPIO pads are on blocks designed to be powered at either 1.8V or 3.3V. These blocks are powered at 1.8V on Jetson Nano, and the internal pull-up at initial Power-ON is not effective. The signal may only be pulled up a fraction of the 1.8V rail. Once the system boots, software can configure the pins for 1.8V operation and the internal pull-ups will work correctly. If these signals need the pull-ups during Power-ON, external pull-up resistors should be added. The affected pins are listed below. These are the Jetson Nano pins on the dual-voltage blocks powered at 1.8V with Power-ON reset default of Internal pull-up enabled.

- SDMMC_DAT0
- SDMMC_DAT1
- SDMMC_DAT2
- SDMMC_DAT3
- SDMMC_CMD
- SPI1_CS0*
- SPI1_CS1*

10.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt-trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt-trigger mode provides better noise immunity and can help avoid extra edges from being “seen” by the Tegra inputs. Input clocks include the I2S and SPI clocks (I2Sx_SCLK and SPIx_SCK) when Tegra is in slave mode. The FAN_TACH pin [GPIO8] is another input that could be affected by noise on the signal edges. The SDMMC_CLK pin, while used to output the clock, also sample the clock at the input to help with read timing. Therefore, the SDMMC_CLK pin may benefit from enabling Schmitt-trigger mode. Care should be taken if the Schmitt-trigger mode setting is changed from the default initialization mode as this can influence interface timing.

10.3 Pins Pulled/Driven High During Power-ON

The Jetson Nano is powered up before the carrier board (See Power Sequencing section). The table below lists the pins on Jetson Nano that default to being pulled or driven high. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer/shifter should be disabled until the device power is enabled.

Table 58. Jetson Nano Pins Pulled/Driven High by Tegra Prior to SYS_RESET* Inactive

Jetson Nano Pin	Power-ON reset Default	Pull-up Strength (kΩ)		Jetson Nano Pin	Power-ON reset Default	Pull-up Strength (kΩ)
SYS_RESET*	Driven high	na		SPI0_CS0*	Internal pull-up	~15
SLEEP/WAKE*	Internal pull-up	~100		SPI0_CS1*	Internal pull-up	~15
FORCE_RECOVERY*	Internal pull-up	~100		SPI1_CS0*	Internal pull-up	~18
UART1_RXD	Internal pull-up	~100		SPI1_CS1*	Internal pull-up	~18

Table 59. Jetson Nano Pins Pulled High on the Module with External Resistors to Supply that is on Prior to SYS_RESET_IN* Inactive

Jetson Nano Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)		Jetson Nano Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)
I2C0_SCL/SDA	3.3	2.2		SPI1_CS0*	1.8	100
I2C1_SCL/SDA	3.3	2.2		SPI1_CS1*	1.8	100
I2C2_SCL/SDA	1.8	2.2		PCIE0_CLKREQ*	3.3	47
CAM_I2C_SCL/SDA	3.3	2.2		PCIE0_RST*	3.3	4.7
				PCIE_WAKE*	3.3	100

11.0 UNUSED INTERFACE TERMINATIONS

11.1 Unused MPIO (Multi-purpose Standard CMOS Pad) Interfaces

The following Jetson Nano pins (and groups of pins) are Tegra MPIO pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed below that are not used can be left unconnected.

Table 60. Unused MPIO pins / Pin Groups

Jetson Nano Pins / Pin Groups		Jetson Nano Pins / Pin Groups
FORCE_RECOVERY*		SDMMC
GPIO00		I2S
PCIE0_CLK/RST/CLKREQ/WAKE		UART
GPIO07, GPIO13, GPIO14		I2C
DP0_HPD, DP1_HPD, HDMI_CEC		SPI
CAM Control, Clock		

12.0 DESIGN CHECKLIST

The checklist below is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

Table 61. Checklist

Check Item Description						Same/Diff/NA
Carrier Board Signal Terminations (To be implemented on the carrier board for interfaces that are used)						
	Parallel Termination			**Series Termination**		
USB/PCIe						
USBSS_TX_N/P (USB 3.0)	–			0.1uF capacitors		
USBSS_RX_N/P (USB 3.0)	–			0.1uF capacitors if directly connected to device		
PCIE0_TX[3:0]_N/P	–			0.1uF capacitors		
PCIE0_RX[3:0]_N/P	–			0.1uF capacitors if directly connected to device		
Ethernet						
GBE_MDI0_N/P	–			Magnetics near or in RJ45 connector		
GBE_MDI1_N/P	–			Magnetics near or in RJ45 connector		
GBE_MDI2_N/P	–			Magnetics near or in RJ45 connector		
GBE_MDI3_N/P	–			Magnetics near or in RJ45 connector		
GBE_ACT	0.1uF capacitor to **GND**			series resistor – value depends on LED used. Max current limit must be met.		
GBE_LINK	0.1uF capacitor to **GND**					
DP0 for eDP/DP						
DP0_TXD3_N/P	ESD to **GND**			0.1uF capacitors		
DP0_TXD2_N/P	ESD to **GND**			0.1uF capacitors		
DP0_TXD1_N/P	ESD to **GND**			0.1uF capacitors		
DP0_TXD0_N/P	ESD to **GND**			0.1uF capacitors		
DP0_AUX_P	100kΩ pull-down to GND near connector and ESD to **GND**			0.1uF capacitor		
DP0_AUX_N	100kΩ pull-up to 3.3V near connector and ESD to **GND**			0.1uF capacitor		
DP0_HPD	10kΩ pull-up to 1.8V near module and 100kΩ pull-down to **GND** on DP side of level shifter. ESD to **GND**			Level Shifter (w/output toward module) and 100kΩ resistor to DP connector. Level shifter must be non-inverting.		
DP1 for HDMI (See above if implementing DP on DP1 pins)						
DP1_TXD3_N/P	499Ω, 1% resistor to 600Ω bead to **GND.** ESD to **GND** just before series resistors.			0.1uF capacitors then series resistors (see HDMI section about value)		
DP1_TX[2:0]_N/P	499Ω, 1% resistor to 600Ω bead to **GND**			0.1uF capacitors then series resistors (see HDMI section about value)		
DP1_AUX_N/P	10kΩ pull-up to 3.3V near module and 1.8kΩ pull-up to 5V near HDMI conn.			Bidirectional level shifter between Pull-ups in Parallel Termination column		
DP1_HPD	10kΩ pull-up to 1.8V near module and 100kΩ pull-down to **GND** near HDMI conn. ESD to **GND**.			Level shifter (w/output toward module) between Pull-up and Pull-down in Parallel Termination column. Level shifter can be inverting or non-inverting. 100kΩ series resistor between pull-down and HDMI connector.		
Power						
Module Power Supplies						
Supply (Carrier Board)	Usage	(V)	Supply Type	Source	Enable	
VDD_IN	Main Supply from Adapter	5V	Adapter	na	na	
PMIC_BBAT	Real-time clock supply	1.65-5.5	PMIC is supply when charging cap or coin-cell	Super-cap or coin-cell is source when system power removed	na	

Carrier Board Supplies						
Main Input	Main power input from DC Adapter	5		Main Input	Connect power source	
Main 3.3V Supply	Main 3.3V supply	3.3		Main Input	**SYS_RESET***	
Main 1.8V Supply	Main 1.8V supply	1.8		Main Input	**SYS_RESET***	
Power Control						
SYS_RESET* is used as enable for carrier board supplies (can also be driven low to force module reset)						
SHUTDOWN_REQ* - when active, causes the carrier board to power off						
MOD_SLEEP* is connected to supplies/devices to be disabled during module deep sleep (LP0)						
SLEEP/WAKE* is optional signal to wake system from sleep mode.						
USB/PCIe/SATA Connections						
USB 2.0						
USB0_D_N/P available to be used as device for USB recovery at a minimum						
VBUS from connector connects to load switch (if host supported) and through level shifter to **GPIO00 (USB0_VBUS_EN0)** on the module.						
USB[2:0]_D_N/P connected to **D-/D+** pins on USB 2.0 connector/device.						
Any EMI/ESD devices used are suitable for USB High-speed						
USB 3.0						
USBSS_RX_N/P connected to **RX-/+** pins on USB 3.0 connector. (See Signal Terminations section)						
USBSS_TX_N/P connected to **TX-/+** pins on USB 3.0 conn., device, hub, etc. (See Signal Terminations section)						
AC caps are provided for device **TX** pins (those connected to the module **RX_N/P**) if device is on the carrier board (See Signal Terminations section)						
If external ESD protection needed, Texas Instruments TPD4E05U06 device is recommended						
PCIe						
PCIe Controller #0 (supports up to x4)						
PCIE0_TX0/RX0 used for 3.3V single-lane device/connector						
PCIE0_TX[1:0]/RX[1:0] used for 3.3V 2-lane device/connector						
PCIE0_TX[3:0]/RX[3:0] used for 3.3V 4-lane device/connector						
TX_N/P connected to corresponding pins on connector, or **RX_N/P** on device on the carrier board (See Signal Terminations section)						
RX_N/P connected to corresponding pins on connector, or **TX_N/P** on device on the carrier board (See Signal Terminations section)						
AC caps are provided for device **TX_N/P** pins (those connected to the module **RX_N/P**) if device is on the carrier board (See Signal Terminations section)						
Reference clock used for PCIe is **PCIE0_CLK1_N/P**						
Clock Request and Reset for PCIe **PCIE0_CLKREQ* and PCIE0_RST***. Pull-ups are provided on the module						
PCIE_WAKE* connected to **WAKE** pins on devices/connectors. Pull-up is provided on the module.						
Ethernet						
GBE_MDI[3:0]_N/P connected to equivalent pins on magnetics device (See Signal Terminations)						
GBE_LED_LINK connected to Link LED (green) pins on connector (See Signal Terminations)						
GBE_LED_ACT connected to Activity LED (yellow) pins on connector (See Signal Terminations)						
SDMMC Connections						
SDMMC_CLK connected to **CLK** pin of device/socket						
SDMMC_CMD connected to **CMD** pin of device/socket. (See Signal Terminations)						
SDMMC_D[3:0] connected to **DATA[3:0]** pins of device/socket. (See Signal Terminations)						
GPIO08 connected to SD Card card-detect pin if implemented.						
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended).						
Display Connections						
DSI						
DSI Dual Link Configurations						
DSI_CLK_N/P connected to **CLKn/p** pins of the DSI interface of display						
DSI_D[1:0]_N/P connected to data lanes of x2 DSI interface of display						
Any EMI/ESD devices used on DSI signals are suitable for highest frequencies supported (low capacitive load: <1pf recommended)						

DP0 for eDP / DP	
DP0_TXD[3:0]_N/P connected to **D[3:0]-/+** pins on eDP/DP connector (See DP/HDMI Pin Mapping table and Signal Terminations)	
DP0_AUX_N/P connected to Aux Lane of panel/connector (See Signal Terminations)	
DP0_HPD connected to **HPD** pin of panel/connector (See Signal Terminations)	
Any EMI/ESD devices used are suitable for highest frequencies supported (Texas Instruments TPD4E05U06 recommended)	
DP1 for HDMI	
DP1_TXD3_N/P connected to **C-/C+** pins on HDMI connector (See Signal Terminations)	
DP1_TXD[2:0]_N/P connected to **D[0:2]_-/+** pins (See DP/HDMI Pin Mapping table) (See Signal Terminations)	
DP1_HPD connected to **HPD** pin on HDMI connector (See Signal Terminations)	
HDMI_CEC connected to **CEC** on HDMI connector through gating circuitry (see HDMI connection figure for details).	
DP1_AUX_P connected to **SCL** and **DP1_AUX_N** to **SDA** on HDMI connector (See Signal Terminations)	
HDMI 5V Supply connected to **+5V** on HDMI connector.	
See Common High-Speed Interface Requirements section for common-mode choke requirements if this is needed (not recommended unless EMI issues seen)	
See HDMI section for ESD requirements. Texas Instruments TPD4E02B04 recommended	
Video Input	
Camera (CSI)	
CSI[4:2,0]_CLK_N/P connected to clock pins of camera. See CSI Configurations table for details	
CSI[3:0]_D[1:0]_N/P & CSI4_D[3:0]_N/P connected to data pins of camera. See CSI Configurations table for details	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Control	
CAM_I2C_SCL/SDA connected to I2C **SCL** and **SDA** pins of imager (See Signal Terminations).	
CAM[1:0]_MCLK connected to Camera reference clock inputs.	
CAM[1:0]_PWDN connected to power-down pins on camera(s) or used as GPIO for other purposes.	
Audio	
Codec/I2S/DMIC/DSPK	
Either **I2S0** or **I2S1** are used for audio codec if present in design	
Either **I2S0** or **I2S1** are used for Bluetooth if present in design	
I2Sx_SCLK Connect to I2S/PCM **CLK** pin of audio device.	
I2Sx_FS Connect to left/right clock pin of audio device.	
I2Sx_DOUT Connect to data input pin of audio device.	
I2Sx_DIN Connect to data output pin of audio device.	
GPIO09 Connect to clock pin of audio codec.	
Available GPIO connected to interrupt pin of audio codec (wake capable GPIO used if this is required).	
I2C/SPI/UART	
I2C	
I2C devices on same I2C interface do not have address conflicts (comparisons are done 7-bit to 7-bit format or 8-bit to 8-bit format)	
I2C0_SCL/SDA, I2C1_SCL/SDA and CAM_I2C_SCL/SDA are used for 3.3V devices (or level shifters employed) and do not have pull-ups on the carrier board since the devices are pulled to 3.3V on the module with 2.2kΩ resistors.	
I2C2_SCL/SDA is used for 1.8V devices (or level shifters employed) and does not have pull-ups on the carrier board since the devices are pulled to 1.8V on the module with 2.2kΩ resistors.	
Pull-up resistors are provided on the non-module side of any level shifters.	
Pull-up resistor values after any level shifters are based on frequency/load (check I2C Spec)	
I2C[2:0]_SCL/SDA and CAM_I2C_SCL/SDA pins connect to SCL/SDA pins of devices	
SPI	
SPI[1:0]_CLK connected to peripheral **CLK** pin(s)	
SPI[1:0]_MOSI connected to slave peripheral **MOSI** pin(s)	
SPI[1:0]_MISO connected to slave peripheral **MISO** pin(s)	
SPI[1:0]_CS[1:0]* connected one **CS** pin per SPI IF to each slave peripheral **CS** pin on the interface	
UART	
UARTx_TX connects to peripheral **RX** pin of device	
UARTx_RX connects to peripheral **TX** pin of device	
UARTx_CTS* connects to peripheral **RTS#** pin of device	

UARTx_RTS* connects to peripheral **CTS#** pin of device		
Strapping		
FORCE_RECOVERY*: To enter Forced Recovery mode, pin is connected to **GND** when system is powered on.		
Unused Dedicated Special Function Interface Pins		
Ball Name	Termination	
USB 2.0		
USB[2:1]_D_N/P	Leave NC any unused pins	
USB 3.0 / PCIe		
PCIE0_TXx_N/P, USBSS_TX_N/P	Leave NC any unused TX lines	
PCIE0_RXx_N/P, USBSS_RX_N/P	Leave NC any unused RX lanes	
PCIE0_CLKx_N/P	Leave NC if not used	
Ethernet		
GBE_MDIx	Leave NC if not used	
GBE_LED_LINK, GBE_LED_ACT	Leave NC any not used	
DSI		
DSI_CLK_N/P	Leave NC any clock lane not used.	
DSI_Dx_N/P	Leave NC any unused DSI data lanes	
CSI		
CSIx_CLK_N/P	Leave NC any unused CSI clock lanes	
CSIx_Dx_N/P	Leave NC any unused CSI data lanes	
eDP		
DP0_TXDx_N/P	Leave NC any unused lanes	
DP0_AUX_N/P	Leave NC if not used	
DP0_HPD	Leave NC if not used	
HDMI/DP		
DP1_TXDx_N/P	Leave NC if lanes not used for HDMI or DP	
DP1_AUX_N/P	Leave NC if not used	
DP1_HPD	Leave NC if not used	
HDMI_CEC	Leave NC if not used	

13.0 JETSON NANO PIN DESCRIPTIONS

Table 62. Jetson Nano Connector (260-Pin SO-DIMM) Pin Descriptions (Odd Side)

Pin #	Jetson Nano Signal Name	Tegra X1 Pin Name	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
1	GND	–	GND	GND	–	GND
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0	Not assigned	Input	MIPI D-PHY
5	CSI1_D0_P	CSI_B_D0_P				
7	GND	–	GND	GND	–	GND
9	RSVD	–	Not used	-	-	-
11	RSVD					
13	GND	–	GND	GND	–	GND
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1	Not assigned	Input	MIPI D-PHY
17	CSI1_D1_P	CSI_B_D1_P				
19	GND	–	GND	GND	–	GND
21	CSI3_D0_N	CSI_F_D0_N	Camera, CSI 3 Data 0	Not assigned	Input	MIPI D-PHY
23	CSI3_D0_P	CSI_F_D0_P				
25	GND	–	GND	GND	–	GND
27	CSI3_CLK_N	CSI_F_CLK_N	Camera, CSI 3 Clock	Not assigned	Input	MIPI D-PHY
29	CSI3_CLK_P	CSI_F_CLK_P				
31	GND	–	GND	GND	–	GND
33	CSI3_D1_N	CSI_F_D1_N	Camera, CSI 3 Data 1	Not assigned	Input	MIPI D-PHY
35	CSI3_D1_P	CSI_F_D1_P				
37	GND	–	GND	GND	–	GND
39	DP0_TXD0_N	EDP_TXDN0	Display Port 0 Data Lane 0	DP connector	Output	AC-Coupled on carrier board
41	DP0_TXD0_P	EDP_TXDP0				
43	GND	–	GND	GND	–	GND
45	DP0_TXD1_N	EDP_TXDN1	Display Port 0 Data Lane 1	DP connector	Output	AC-Coupled on carrier board
47	DP0_TXD1_P	EDP_TXDP1				
49	GND	–	GND	GND	–	GND
51	DP0_TXD2_N	EDP_TXDN2	Display Port 0 Data Lane 2	DP connector	Output	AC-Coupled on carrier board
53	DP0_TXD2_P	EDP_TXDP2				
55	GND	–	GND	GND	–	GND
57	DP0_TXD3_N	EDP_TXDN3	Display Port 0 Data Lane 3	DP connector	Output	AC-Coupled on carrier board
59	DP0_TXD3_P	EDP_TXDP3				
61	GND	–	GND	GND	–	GND
63	DP1_TXD0_N	HDMI_DP_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2	HDMI connector	Output	AC-Coupled on carrier board
65	DP1_TXD0_P	HDMI_DP_TXDP0				
67	GND	–	GND	GND	–	GND
69	DP1_TXD1_N	HDMI_DP_TXDN1	DisplayPort or HDMI Lane 1	HDMI connector	Output	AC-Coupled on carrier board
71	DP1_TXD1_P	HDMI_DP_TXDP1				
73	GND	–	GND	GND	–	GND
75	DP1_TXD2_N	HDMI_DP_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0	HDMI connector	Output	AC-Coupled on carrier board
77	DP1_TXD2_P	HDMI_DP_TXDP2				
79	GND	–	GND	GND	–	GND
81	DP1_TXD3_N	HDMI_DP_TXDN3	DisplayPort 1 Lane 3 or HDMI Clk Lane	HDMI connector	Output	AC-Coupled on carrier board
83	DP1_TXD3_P	HDMI_DP_TXDP3				
85	GND	–	GND	GND	–	GND
87	GPIO00	USB_VBUS_EN0	GPIO #0 or USB 0 VBUS Detect	USB 2.0 Micro AB	Input	USB VBUS, 5V
89	SPI0_MOSI	SPI1_MOSI	SPI 0 Master Out / Slave In	Expansion Header	Bidir	CMOS – 1.8V
91	SPI0_SCK	SPI1_SCK	SPI 0 Clock			
93	SPI0_MISO	SPI1_MISO	SPI 0 Master In / Slave Out			
95	SPI0_CS0*	SPI1_CS0	SPI 0 Chip Select 0			
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1			
99	UART0_TXD	UART3_TXD	UART #0 Transmit	M.2 Key E	Output	CMOS – 1.8V
101	UART0_RXD	UART3_RXD	UART #0 Receive		Output	
103	UART0_RTS*	UART3_RTS	UART #0 Request to Send		Input	
105	UART0_CTS*	UART3_CTS	UART #0 Clear to Send		Input	
107	GND	–	GND	GND	–	GND
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB 2.0 Micro AB	Bidir	USB PHY
111	USB0_D_P	USB0_DP				
113	GND	–	GND	GND	–	GND
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB 3.0 Type A	Bidir	USB PHY
117	USB1_D_P	USB1_DP				
119	GND	–	GND	GND	–	GND
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	M.2 Key E	Bidir	USB PHY
123	USB2_D_P	USB2_DP				

Pin #	Jetson Nano Signal Name	Tegra X1 Pin Name	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
125	GND	–	GND	GND	–	GND
127	GPIO04	NFC_INT	GPIO #04	M.2 Key E	Input	CMOS – 1.8V
129	GND	–	GND	GND	–	GND
131	PCIE0_RX0_N	PEX_RX4N	PCIe #0 Receive 1 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Input	PCIe PHY, AC-Coupled on carrier board
133	PCIE0_RX0_P	PEX_RX4P				
135	GND	–	GND	GND	–	GND
137	PCIE0_RX1_N	PEX_RX3N	PCIe #0 Receive 1 (PCIe Ctrl #0 Lane 1)	Not assigned	Input	PCIe PHY, AC-Coupled on carrier board
139	PCIE0_RX1_P	PEX_RX3P				
141	GND	–	GND	GND	–	GND
143	RSVD	–	Not used	–	–	–
145	RSVD					
147	GND	–	GND	GND	–	GND
149	PCIE0_RX2_N	PEX_RX2N	PCIe #0 Receive 2 (PCIe Ctrl #0 Lane 2)	Not assigned	Input	PCIe PHY, AC-Coupled on carrier board
151	PCIE0_RX2_P	PEX_RX2P				
153	GND	–	GND	GND	–	GND
155	PCIE0_RX3_N	PEX_RX1N	PCIe #0 Receive 3 (PCIe Ctrl #0 Lane 3)	Not assigned	Input	PCIe PHY, AC-Coupled on carrier board
157	PCIE0_RX3_P	PEX_RX1P				
159	GND	–	GND	GND	–	GND
161	USBSS_RX_N	PEX_RX6N	USB SS Receive (USB 3.0 Ctrl #0)	USB 3.0 Type A	Input	USB SS PHY, AC-Coupled (off the module)
163	USBSS_RX_P	PEX_RX6P				
165	GND	–	GND	GND	–	GND
167	RSVD	–	Not used	–	–	–
169	RSVD					
171	GND	–	GND	GND	–	GND
173	RSVD	–	Not used	–	–	–
175	RSVD					
177	GND	–	GND	GND	–	GND
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	M.2 Key E	Input	Open Drain 3.3V, Pull-up on the module
181	PCIE0_RST*	PEX_L0_RST_N	PCIe #0 Reset (PCIe Ctrl #0). 4.7kΩ pull-up to 3.3V on the module.		Output	Open Drain 3.3V, Pull-up on the module
183	RSVD	–	Not used	–	–	–
185	I2C0_SCL	GEN1_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (General)	Bidir	Open Drain – 3.3V
187	I2C0_SDA	GEN1_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.		Bidir	Open Drain – 3.3V
189	I2C1_SCL	GEN2_I2C_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.		Bidir	Open Drain – 3.3V
191	I2C1_SDA	GEN2_I2C_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.		Bidir	Open Drain – 3.3V
193	I2S0_DOUT	DAP4_DOUT	I2S Audio Port 0 Data Out	Expansion Header	Input	CMOS – 1.8V
195	I2S0_DIN	DAP4_DIN	I2S Audio Port 0 Data In		Bidir	CMOS – 1.8V
197	I2S0_FS	DAP4_FS	I2S Audio Port 0 Left/Right Clock		Output	CMOS – 1.8V
199	I2S0_SCLK	DAP4_SCLK	I2S Audio Port 0 Clock		Bidir	CMOS – 1.8V
201	GND	–	GND	GND	–	GND
203	UART1_TXD	UART2_TXD	UART #1 Transmit	Expansion Header	Output	CMOS – 1.8V
205	UART1_RXD	UART2_RXD	UART #1 Receive		Input	CMOS – 1.8V
207	UART1_RTS*	UART2_RTS	UART #1 Request to Send		Output	CMOS – 1.8V
209	UART1_CTS*	UART2_CTS	UART #1 Clear to Send		Input	CMOS – 1.8V
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock		Output	CMOS – 1.8V
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Camera connector	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.		Bidir	Open Drain – 3.3V
217	GND	–	GND	GND	–	GND
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0	Not assigned	Bidir	CMOS – 1.8V
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1		Bidir	CMOS – 1.8V
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2		Bidir	CMOS – 1.8V
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3		Bidir	CMOS – 1.8V
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command		Bidir	CMOS – 1.8V
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock		Output	CMOS – 1.8V
231	GND	–	GND	GND	–	GND
233	SHUTDOWN_REQ*	–	Used by the module to request a shutdown from the carrier board. ~5kΩ pull-up to VDD_IN (5V) on the module.	System	Output	Analog 5.0V
235	PMIC_BBAT	(PMIC BBATT)	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). Connects to Lithium Cell or	Battery Back-up using Super-capacitor	Bidir	1.65V-5.5V

Pin #	Jetson Nano Signal Name	Tegra X1 Pin Name	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
			super capacitor on Carrier Board. PMIC is source when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.			
237	POWER_EN	(PMIC EN0 through converter logic)	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. 100kΩ pulldown on the module.	System	Input	CMOS- 5.0V
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 4.7kΩ pull-up to 1.8V on the module.	System	Bidir	Open Drain, 1.8V
241	GND	–	GND	GND	–	GND
243	GND					
245	GND					
247	GND					
249	GND					
251	VDD_IN	–	Main power – Supplies PMIC & other regs	Main DC input	Input	5.0V
253	VDD_IN					
255	VDD_IN					
257	VDD_IN					
259	VDD_IN					

Table 63. Jetson Nano Connector (260-Pin SO-DIMM) Pin Descriptions (Even Side)

Pin #	Jetson Nano Signal Name	Tegra X1 Pin Name	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
2	GND	–	GND	GND	–	GND
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0	Camera connector	Input	MIPI D-PHY
6	CSI0_D0_P	CSI_A_D0_P				
8	GND	–	GND	GND	–	GND
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	Camera connector	Input	MIPI D-PHY
12	CSI0_CLK_P	CSI_A_CLK_P				
14	GND	–	GND	GND	–	GND
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1	Camera connector	Input	MIPI D-PHY
18	CSI0_D1_P	CSI_A_D1_P				
20	GND	–	GND	GND	–	GND
22	CSI2_D0_N	CSI_E_D0_N	Camera, CSI 2 Data 0		Input	MIPI D-PHY
24	CSI2_D0_P	CSI_E_D0_P				
26	GND	–	GND	GND	–	GND
28	CSI2_CLK_N	CSI_E_CLK_N	Camera, CSI 2 Clock		Input	MIPI D-PHY
30	CSI2_CLK_P	CSI_E_CLK_P				
32	GND	–	GND	GND	–	GND
34	CSI2_D1_N	CSI_E_D1_N	Camera, CSI 2 Data 1		Input	MIPI D-PHY
36	CSI2_D1_P	CSI_E_D1_P				
38	GND	–	GND	GND	–	GND
40	CSI4_D2_N	CSI_D_D0_N	Camera, CSI 4 Data 0	Not assigned	Output	MIPI D-PHY
42	CSI4_D2_P	CSI_D_D0_P				
44	GND	–	GND	GND	–	GND
46	CSI4_D0_N	CSI_C_D0_N	Camera, CSI 4 Data 0	Not assigned	Output	MIPI D-PHY
48	CSI4_D0_P	CSI_C_D0_P				
50	GND	–	GND	GND	–	GND
52	CSI4_CLK_N	CSI_C_CLK_N	Camera, CSI 4 Clock	Not assigned	Output	MIPI D-PHY
54	CSI4_CLK_P	CSI_C_CLK_P				
56	GND	–	GND	GND	–	GND
58	CSI4_D1_N	CSI_C_D1_N	Camera, CSI 4 Data 1	Not assigned	Output	MIPI D-PHY
60	CSI4_D1_P	CSI_C_D1_P				
62	GND	–	GND	GND	–	GND
64	CSI4_D3_N	CSI_D_D1_N	Camera, CSI 4 Data 1	Not assigned	Input	MIPI D-PHY
66	CSI4_D3_P	CSI_D_D1_P				
68	GND	–	GND	GND	–	GND
70	DSI_D0_N	DSI_A_D0_N	Display, DSI Data 0	Not assigned	Bidir	MIPI D-PHY
72	DSI_D0_P	DSI_A_D0_P				
74	GND	–	GND	GND	–	GND

76	DSI_CLK_N	DSI_A_CLK_N	Display, DSI Clock 0	Not assigned	Output	MIPI D-PHY
78	DSI_CLK_P	DSI_A_CLK_P				
80	GND	–	GND	GND	–	GND
82	DSI_D1_N	DSI_A_D1_N	Display, DSI Data 1	Not assigned	Output	MIPI D-PHY
84	DSI_D1_P	DSI_A_D1_P				
86	GND	–	GND	GND	–	GND
88	DP0_HPD	DP_HPD0	Display Port 0 Hot Plug Detect	DP connector	Input	CMOS – 1.8V
90	DP0_AUX_N	DP_AUX_CH0_N	Display Port 0 Auxiliary Channel		Bidir	Open Drain, 1.8V
92	DP0_AUX_P	DP_AUX_CH0_P			Input	CMOS – 1.8V
94	HDMI_CEC	HDMI_CEC	HDMI CEC	HDMI connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - I2C)
96	DP1_HPD	HDMI_INT_DP_HPD	Display Port 1 or HDMI Hot Plug Detect			
98	DP1_AUX_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
100	DP1_AUX_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL			
102	GND	–	GND	GND	–	GND
104	SPI1_MOSI	SPI2_MOSI	SPI 1 Master Out / Slave In	Expansion header	Bidir	CMOS – 1.8V
106	SPI1_SCK	SPI2_SCK	SPI 1 Clock			
108	SPI1_MISO	SPI2_MISO	SPI 1 Master In / Slave Out			
110	SPI1_CS0*	SPI2_CS0	SPI 1 Chip Select 0			
112	SPI1_CS1*	SPI2_CS1	SPI 1 Chip Select 1			
114	CAM0_PWDN	CAM1_PWDN	Camera 0 Powerdown or GPIO	Camera connector	Output	CMOS – 1.8V
116	CAM0_MCLK	CAM1_MCLK	Camera 0 Reference Clock			
118	GPIO01	CAM_AF_EN	GPIO #1 or Camera MCLK #2	Not assigned		
120	CAM1_PWDN	CAM2_PWDN	Camera 1 Powerdown or GPIO		Output	CMOS – 1.8V
122	CAM1_MCLK	CAM2_MCLK	Camera 1 Reference Clock			
124	GPIO02	GPIO_PH6	GPIO #2	M.2 Key E	Input	CMOS – 1.8V
126	GPIO03	GPS_EN	GPIO #3			
128	GPIO05	AP_WAKE_NFC	GPIO #5		Output	CMOS – 1.8V
130	GPIO06	NFC_EN	GPIO #6			
132	GND	–	GND	GND	–	GND
134	PCIE0_TX0_N	PEX_TX4N	PCIe #0 Transmit 0 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Output	PCIe PHY, AC-Coupled on carrier board
136	PCIE0_TX0_P	PEX_TX4P				
138	GND	–	GND	GND	–	GND
140	PCIE0_TX1_N	PEX_TX3N	PCIe #0 Transmit 1PCIe Ctrl #0 Lane 1)	Not assigned	Output	PCIe PHY, AC-Coupled on carrier board
142	PCIE0_TX1_P	PEX_TX3P				
144	GND	–	GND	GND	–	GND
146	GND					
148	PCIE0_TX2_N	PEX_TX2N	PCIe #0 Transmit 2 (PCIe Ctrl #0 Lane 2)	Not assigned	Output	PCIe PHY, AC-Coupled on carrier board
150	PCIE0_TX2_P	PEX_TX2P				
152	GND	–	GND	GND	–	GND
154	PCIE0_TX3_N	PEX_TX1N	PCIe #0 Transmit 3 (PCIe Ctrl #0 Lane 3)	Not assigned	Output	PCIe PHY
156	PCIE0_TX3_P	PEX_TX1P				
158	GND	–	GND	GND	–	GND
160	PCIE0_CLK_N	PEX_CLK1N	PCIe #0 Reference Clock (PCIe Ctrl #0)	M.2 Key E	Output	PCIe PHY, AC-Coupled on carrier board
162	PCIE0_CLK_P	PEX_CLK1P				
164	GND	–	GND	GND	–	GND
166	USBSS_TX_N	PEX_TX6N	USB SS Transmit (USB 3.0 Ctrl #0)	USB 3.0 Type A	Output	USB SS PHY, AC-Coupled on carrier board
168	USBSS_TX_P	PEX_TX6P				
170	GND	–	GND	GND	–	GND
172	RSVD	–	Not used	–	–	–
174	RSVD					
176	GND	–	GND	GND	–	GND
178	MOD_SLEEP*	GPIO_PA6	Module Sleep. When active (low), indicates module has gone to Deep Sleep (LP0) mode.	System control. Used to disable HDMI termination pull-down FET control.	Output	CMOS – 1.8V
180	PCIE0_CLKREQ*	PEX_L0_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module.	Not assigned	Bidir	Open Drain 3.3V, Pull-up on the module
182	RSVD	–	Not used	–	–	–
184	GBE_MDI0_N	–	GbE Transformer Data 0	LAN	Bidir	MDI
186	GBE_MDI0_P					
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output	
190	GBE_MDI1_N	–	GbE Transformer Data 1		Bidir	MDI
192	GBE_MDI1_P					
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)		Output	
196	GBE_MDI2_N	–	GbE Transformer Data 2		Bidir	MDI
198	GBE_MDI2_P					
200	GND	–	GND	GND	–	GND

202	GBE_MDI3_N	–	GbE Transformer Data 3	LAN	Bidir	MDI
204	GBE_MDI3_P					
206	GPIO07	LCD_BL_PWM	GPIO #7 or Pulse Width Modulator	Expansion Header	Output	CMOS – 1.8V
208	GPIO08	GPIO_PZ2	GPIO #8 or SD Card Detect	Fan	Input	CMOS – 1.8V
210	CLK_32K_OUT	(PMIC GPIO4 32K CLK Out)	Sleep/Suspend clock	M.2 Key E	Output	CMOS – 1.8V
212	GPIO10	LCD_BL_EN	GPIO #10	M.2 Key E	Output	CMOS – 1.8V
214	FORCE_RECOVERY*	BUTTON_VOL_UP	Force Recovery strap pin	System	Input	CMOS – 1.8V
216	GPIO11	GPIO_PZ0	GPIO #11 or Camera MCLK #3	Expansion Header	Bidir	
218	GPIO12	LCD_TE	GPIO #12		Input	CMOS – 1.8V
220	I2S1_DOUT	DMIC2_CLK	I2S Audio Port 1 Data Out	M.2 Key E	Output	CMOS – 1.8V
222	I2S1_DIN	DMIC1_DAT	I2S Audio Port 1 Data In		Input	CMOS – 1.8V
224	I2S1_FS	DMIC1_CLK	I2S Audio Port 1 Left/Right Clock		Bidir	CMOS – 1.8V
226	I2S1_SCLK	DMIC2_DAT	I2S Audio Port 1 Clock		Bidir	CMOS – 1.8V
228	GPIO13	GPIO_PE6	GPIO #13 or Pulse Width Modulator	Expansion Header	Bidir	CMOS – 1.8V
230	GPIO14	GPIO_PE7	GPIO #14 or Pulse Width Modulator	Fan	Output	CMOS – 1.8V
232	I2C2_SCL	GEN3_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	I2C (General)	Bidir	Open Drain – 1.8V
234	I2C2_SDA	GEN3_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.		Bidir	Open Drain – 1.8V
236	UART2_TXD	UART1_TXD	UART #2 Transmit.	Serial Port	Output	CMOS – 1.8V
238	UART2_RXD	UART1_RXD	UART #2 Receive		Input	CMOS – 1.8V
240	SLEEP/WAKE*	BUTTON_PWR_ON	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V
242	GND	–	GND	GND	–	GND
244	GND					
246	GND					
248	GND					
250	GND					
252	VDD_IN	–	Main power – Supplies PMIC & other regs	Main DC input	Input	5.0V
254	VDD_IN					
256	VDD_IN					
258	VDD_IN					
260	VDD_IN					

Legend

Ground	Power	Reserved

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

14.0 APPENDIX A: GENERAL ROUTING GUIDELINES

Signal Name Conventions

The following conventions are used in describing the signals for Tegra:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDMMC_CMD**, written in bold to distinguish it from other text. All active-low signals are identified by an asterisk (*) after the signal name. For example, **SYS_RESET*** indicates an active-low signal. Active-high signals do not have the underscore-N (_N) after the signal names. For example, **SDMMC_CMD** indicates an active-high signal. Differential signals are identified as a pair with the same names that end with _P and _N or for USB 2.0, DP and DN (for positive and negative, respectively). For example, **CSI_0_D0_P** and **CSI_0_D0_N** indicate a differential signal pair.
- The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The table below lists the I/O codes used in the signal description tables.

Table 64. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils (1/1000 of an inch) unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in “mm” (millimeter) or “in” (inch) or in terms of signal delay in “ps” (pico-seconds) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

Signal Routing Conventions

Throughout this document, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- SE impedance of trace (along with diff impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline. Note: 1 mil = 1/1000th of an inch.

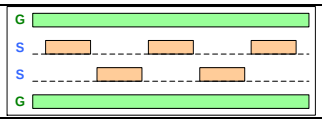
Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

General Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.0, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

- **Controlled Impedance**
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified SE and Diff impedances. Unless otherwise noted, trace impedance values are ±15%.
- **Max Trace Lengths/Delays**
  Trace lengths/delays should include the carrier board PCB routing (where the Jetson Nano mating connector resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson Nano to the actual connector (i.e. USB, HDMI, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- **Trace Delay/Flight Time Matching**
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) and inner-layer 180psi. If one signal is routed 10 inches on outer layer and second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see diagram to right)	
Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.	

Note: *The requirements detailed in the Interface Signal Routing Requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.*

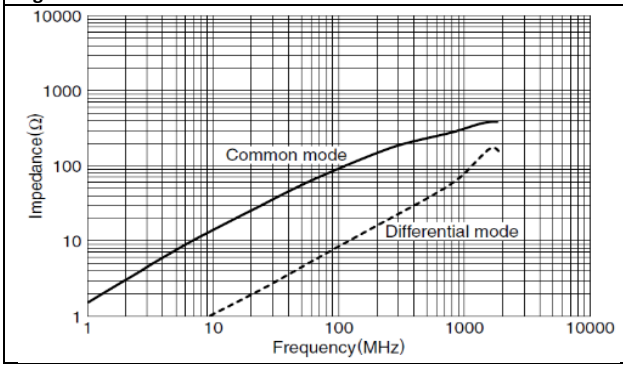
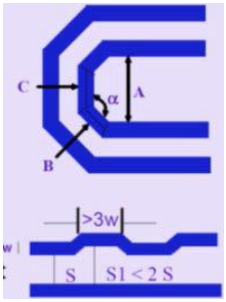
14.1 Common High-Speed Interface Requirements

Table 65. Common High-Speed Interface Requirements

Parameter	Requirement	Units	Notes
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues)			
Preferred device			Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)	8 (53)	mm (ps)	TDK ACM2012D-900-2P See USB 3.0 Guideline Figure 1
Common-mode impedance @ 100MHz Min/Max	65/90	Ω	
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω	@T_R-200ps (10%-90%)
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Serpentine			
Min bend angle	135	deg (α)	

Dimension	Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair. See USB 3.0 Guideline Figure 2
General				
Routing over Voids		Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling		Keep critical high-speed traces away from other signal traces or unrelated power traces/areas or power supply components		

Table 66. Common High-Speed Interface Signal Routing Requirements Figures

Figure 1: Common Mode Choke	Figure 2: Serpentine
	

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